Department of Physics and Astronomy
Heidelberg University

Master Thesis
in Physics

submitted by
René Hagdorn
born on
December 28$^{\text{th}}$ 1988
in
Neustadt an der Weinstraße

April 2017

Performance Optimization of the MuPix7 Sensor Prototype

This Thesis has been carried out by

René Hagdorn

at the

Physikalisches Institut Heidelberg

under the supervision of

Prof. Dr. André Schöning

Performance Optimization of the MuPix7 Sensor Prototype:

The Mu3e experiment searches for the charged lepton flavor violating decay $\mu^+ \to e^+e^-e^+$ with a target sensitivity of one in 10^{16} events. This process is suppressed to a branching level of 10^{-54} in the Standard Model. Hence, any observed signal is a clear indication for New Physics.

The muons decay at rest, limiting the maximum momentum of the decay products to $\sim$53 MeV/c. In this momentum region the vertex and momentum resolution are limited by multiple Coulomb scattering in the detector, making a low material budget crucial. Therefore, the tracking detector consists of 50 µm thin silicon pixel sensors utilizing the High Voltage Monolithic Active Pixel Sensor (HV-MAPS) concept. To validate this concept, a series of prototypes, the MuPix chips, are developed. The gaseous helium cooling system of the detector is designed for a maximal power of 400 mW/cm^2, limiting the specified sensor power consumption.

The MuPix7 is analyzed in the scope of this thesis. The bias settings influencing signal quality, power consumption, and noise are systematically optimized in lab measurements and validated during a testbeam campaign. An optimal setting was found, reaching a power consumption of $\sim$275 mW/cm^2, while simultaneously providing a wide operating region with efficiencies of >99 % and a slightly increased signal quality. A comparison of all tested settings is shown.

Furthermore, a new method was developed to determine an efficiency-like quantity in lab measurements, which facilitates the preparation and conduction of future efficiency measurements. The principle behind this method is explained and test results are presented.

Leistungsoptimierung des MuPix7 Sensorprototyps

Das Mu3e-Experiment sucht mit einer Sensitivität von einem in 10^{16} Myonzerfällen nach dem leptonfamilienzahlverletzenden Prozess $\mu^+ \to e^+e^-e^+$. Im Standardmodell ist dieser Prozess auf ein Verzweigungsverhältnis von 10^{-54} unterdrückt. Daher ist ein beobachtetes Signal ein klarer Hinweis auf Neue Physik.

Durch in Ruhe zerfallende Myonen ist der maximale Impuls der Zerfallsprodukte auf $\sim$53 MeV/c beschränkt. In diesem Impulsbereich limitiert Coulomb-Vielfachstreuung die Impuls- und Vertexauflösung, weswegen die Materialstärke des Detektors gering gehalten werden muss. Deshalb besteht der Spurdetektor aus 50 µm dünnen Siliziumpixelsensoren basierend auf dem Konzept der hochspannungsbetriebenen monolithischen aktiven Pixelsensoren (HV-MAPS).

Zum Test dieses Konzepts wird eine Reihe von Prototypen, die MuPix-Chips, entwickelt. Die Heliumgaskühlung des Detektors ist auf eine maximale Kühlleistung von 400 mW/cm^2 ausgelegt, was den erlaubten Energieverbrauch der Sensoren limitiert.

Im Rahmen dieser Arbeit wird der MuPix7 untersucht. Die Betriebseinstellungen, welche die Signalqualität, den Energieverbrauch und das elektronische Rauschen beinflussen, wurden in Labormessungen systematisch optimiert und während einer Teststrahlkampagne validiert. Es wurde eine optimale Einstellung mit einem Energieverbrauch von $\sim$275 mW/cm^2 gefunden, die gleichzeitig einen breiten Arbeitsbereich mit Effizienzen von >99 % und eine leicht verbesserte Signalqualität bietet. Ein vergleich zwischen allen untersuchten Einstellungen wird gezeigt.

Desweiteren wurde ein Verfahren entwickelt, mit dem effizienzähnliche Werte in einer Labormessung bestimmt werden können, was die Planung und den Ablauf künftiger Effizienzmessungen vereinfacht. Das Prinzip dieses Verfahrens wird erklärt und Testergebnisse werden vorgestellt.

Contents

Part I.

INTRODUCTION

1. Introduction

The current knowledge about the elementary particles and their interactions is summed up in the Standard Model of Particle Physics (SM). It has been shown to be very precise in its experimental predictions, but there are still some open questions, such as the quantum nature of gravity, the existence of neutrino masses, and the matter/anti-matter asymmetry in the universe. These unexplained phenomena motivate the search for New Physics processes predicted by theories beyond the Standard Model.

There are several methods of searching for New Physics. The direct approach is to explicitly look for new particles created at high energy scales in collider experiments, as it is done at the LHC. Indirect search methods make use of the fact that new processes can also enter in particle decays and reactions via quantum loops. These effects can for instance be determined by measuring branching ratios with high precision and comparing them to the Standard Model predictions. This makes New Physics searches also accessible at low energy scales.

One such process is the charged lepton flavor violating decay $\mu^+ \to e^+e^-e^+$. The Mu3e experiment aims to search for this decay with a sensitivity of one in 10^{16} events. Since this decay is highly suppressed in the Standard Model, any observed signal is an indication for New Physics. In the case that such a signal is not found, the goal is to set an upper limit on the branching ratio of $BR(\mu^+ \to e^+e^-e^+) < 10^{-16}$ at 90 % CL [1]. In order to achieve this limit in a reasonable amount of time, rates in the order of 10^9 decaying muons per second need to be observed.

For the first phase of the experiment, 10^8 muons per second can be stopped using a high intensity continuous muon beam, provided by the High Intensity Proton Accelerator (HIPA) at the Paul Scherrer Institute (PSI) in Switzerland. The muons will be stopped on a target in the detector and decay at rest. Therefore, the maximum momentum of the decay electrons is 53 MeV/c. In this energy range multiple Coulomb scattering is one of the dominant processes for particle interactions in detectors, affecting the precise track reconstruction of the decay particles and therefore constrains momentum and vertex resolution. In order to minimize the effect of these scattering processes, a very low material budget is required. This is achieved by using thinned silicon pixel sensors based on the High Voltage Monolithic Active Pixel Sensor (HV-MAPS) technology [2] as tracking components. The HV-MAPS concept combines the principle of Monolithic Active Pixel Sensors, which integrate sensor and readout on the same chip, with a fast charge collection and signal generation by applying high voltage to a diode, creating a thin active depletion zone for charge collection. The thin detector volume, given by a depletion zone thickness of approximately $10-15\,\mu$m, makes it possible to thin the entire sensor down to 50 µm. In the central detector region, the sensors are arranged in four cylindrical layers around the beam axis, placed in a 1 T magnetic field.

In addition to the silicon pixel layers, a scintillating fiber tracker and tile detector are used for precise timing, which is required to reduce combinatorial background by ensuring the time coincidence between the decay products, and to identify the charge of recurling particles by determining their direction of propagation in the magnetic field.

The HV-MAPS prototypes developed in the Mu3e context are called MuPix chips. This thesis focuses on the newest prototype, the MuPix7. Different bias current settings for its on-chip amplification and comparator stages have been tested in terms of power consumption and signal quality. The goal is to optimize the chip performance by improving its power consumption properties to szay below $400\,\mathrm{mW/cm^2}$, which is the upper limit at which the proposed gaseous helium cooling system can still sufficiently cool the detector. Simultaneously a high signal-to-background separation has to be achieved.

The settings obtained in the lab are tested during a dedicated testbeam campaign at PSI in order to determine their efficiencies.

Additionally, a method to determine preliminary efficiencies in the lab was developed to get a higher prediction power on the behavior of the sensors at future testbeam campaigns. In this thesis, the concept and first results of these lab-determined 'relative efficiencies' are presented.

2. Theory

2.1. The Standard Model of Particle Physics

The Standard Model of Particle Physics (SM) is a quantum field theory that describes the known fundamental particles and interactions. It comprises twelve fermionic particles and their anti-particles, part of which form the constituents of matter, and the gauge bosons, which mediate the three fundamental interactions, the electromagnetic, the weak, and the strong interaction (see Figure 2.1). Gravity is not described by this theory, but its effects in particle interactions are negligible compared to the other three forces.

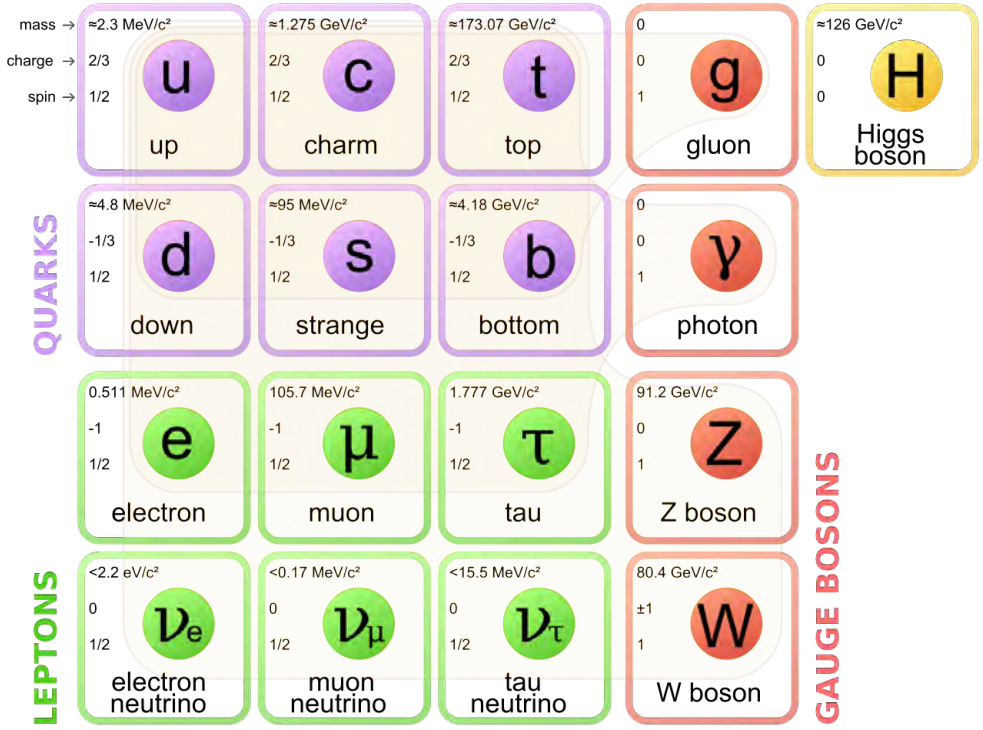


Figure 2.1.: The fundamental particles of the Standard Model [3].

The fundamental particles are grouped together according to their quantum numbers: spin, electric charge, weak hypercharge, color charge, and flavor. All fermions have a spin of $\frac{1}{2}$ and are divided into two groups. There are six quarks that carry color charge and can therefore interact via the strong force and six leptons, which do not take part in this interaction. Quarks and leptons are arranged in three families with rising masses.

Besides the strong interaction, quarks also interact electromagnetically and weakly. Each quark family consists of an up-type quark, up (u), charm (c), and top (t), that carries an electric charge of $+\frac{2}{3}$ elementary charges and a down-type quark, down (d), strange (s), and bottom (b), with $-\frac{1}{3}$ elementary charges.

The lepton families each contain a massive particle, electron (e), muon (μ), and tau (τ) that carries a charge of -1. They interact only via the weak and electromagnetic force. The other members of the lepton families are the corresponding neutrinos, labeled as ν_e, ν_μ, and ν_τ,

respectively. Since they are not electrically charged, neutrinos only interact weakly and are, in the theory of the Standard Model, treated as massless.

The three interactions of the Standard Model are mediated by so-called gauge bosons, which all have spin 1. The gluon (g) is the mediator of the strong interaction. It is massless and couples to the color charge. Since it carries a color charge itself, it does not only interact with quarks but also with other gluons. These self-interactions limit the range on which the strong force can act, and are also the reason that there are no free quarks or other color-charged objects observed in nature. They are all confined into color-neutral states, called hadrons. The photon (γ) mediates the electromagnetic force by coupling to the electric charge. Photons are also massless, but do not couple directly to each other, which makes their range infinite. The weak force is mediated by two charged bosons, W^+ and W^-, and a neutral boson, Z. They have masses of $m_{W^\pm} \approx 80.4\,\text{GeV}$ and $m_Z \approx 90.2\,\text{GeV}$, which gives them a finite lifetime and therefore a limited interaction range [4].

In the Standard Model the weak and electromagnetic interactions can be unified to the electroweak force with four massless gauge bosons, W^1, W^2, W^3, and B. The fact that the observable weak bosons are massive means that the underlying gauge symmetry of the electroweak interaction is broken. This symmetry breaking occurs by the so-called Higgs mechanism, which gives all the fundamental particles their masses. A spin 0 particle, the Higgs boson, was predicted by this mechanism and finally observed at LHC in 2012 with a mass of $m_H \sim 126\,\text{GeV}$ [5, 6].

2.2. Lepton Flavor Violation

The flavor, which denotes the species or family of a particle, is not always a conserved quantity. In weak interactions it is possible for quarks to change flavor. This is due to the fact, that the flavor or mass eigenstate of a quark is not equal to its weak eigenstate, which takes part in the weak interaction, but is rather a superposition of weak eigenstates. This means that quarks can transition from one family to another in weak interactions. The mixing between the different eigenstates is described by the Cabibbo-Kobayashi-Maskawa (CKM) matrix [7].

In leptonic SM interactions flavor violation does not occur. The total lepton number, as well as the lepton number of each family are supposed to be conserved. However, there have been observations of neutrino mixing by different experiments [8, 9, 10], showing lepton flavor violation (LFV) in the neutrino sector. This implies the existence of non-zero neutrino masses. An extension to the Standard Model can be given by the Pontecorvo-Maki-Nakagawa-Sakata (PMNS) matrix that describes neutrino mixing analogously to the CKM matrix in the quark sector. An explicit violation of lepton flavor in charged interactions (cLFV) has not been observed yet.

2.3. Muon Decay

2.3.1. Muon Decay in the Standard Model

Since lepton family number is conserved, the decay $\mu^+ \to e^+e^-e^+$ is forbidden. The leading order decay for muons in the SM is the so-called Michel decay $\mu^+ \to e^+\nu_e\bar{\nu}_\mu$, depicted in Figure 2.2. There are two more possible decay modes: Next to leading order, there is the radiative decay $\mu^+ \to e^+\nu_e\bar{\nu}_\mu\gamma$, in which the final state positron additionally radiates a photon, and next to next to leading order, the internal conversion decay $\mu^+ \to e^+e^-e^+\nu_e\bar{\nu}_\mu$ (see Figure 3.2a), in which the radiated photon creates an electron-positron-pair [4].

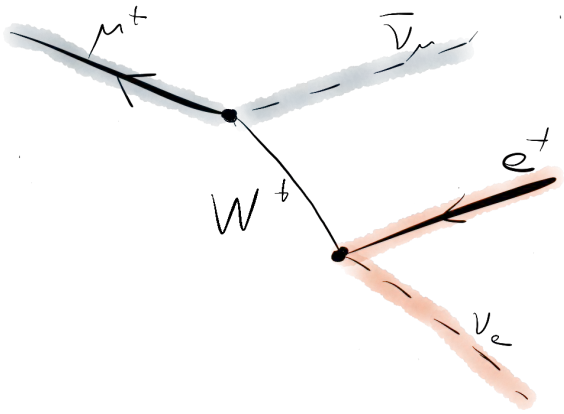


Figure 2.2.: Michel decay $\mu^+ \to e^+ \nu_e \bar{\nu}_\mu$.

If the Standard Model is extended to account for lepton flavor violating processes via neutrino mixing as described above, the decay $\mu^+ \to e^+e^-e^+$ is possible as a higher order decay, in which neutrino mixing occurs in a loop. Figure 2.3 shows the corresponding Feynman diagram. Due to the high mass of the intermediate W^+ boson as compared to the mass difference of the neutrinos, this process is suppressed by a factor of $\frac{(\Delta m_\nu^2)^2}{m_W^4}$. This suppression yields a branching ratio of $BR(\mu \to eee) < 10^{-54}$, which is too small to be observed.

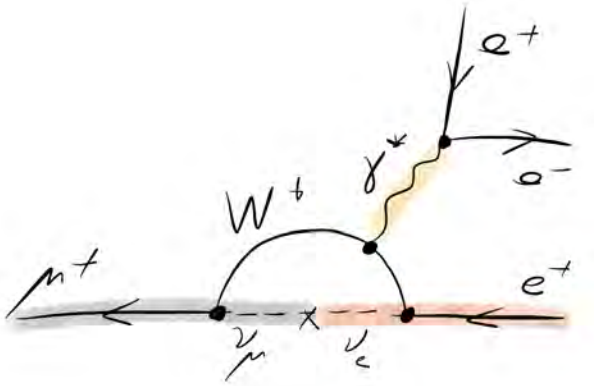


Figure 2.3.: $\mu^+ \to e^+e^-e^+$ decay via neutrino mixing.

The related radiative decay $\mu^+ \to e^+\gamma$, in which the photon is not converted to an electron-positron pair is slightly less suppressed, because of the missing electromagnetic vertex factor of $\alpha_{em}(\mathcal{O}(10^{-2}))$ for the $\gamma \to e^+e^-$ process. However, it is still unobservable.

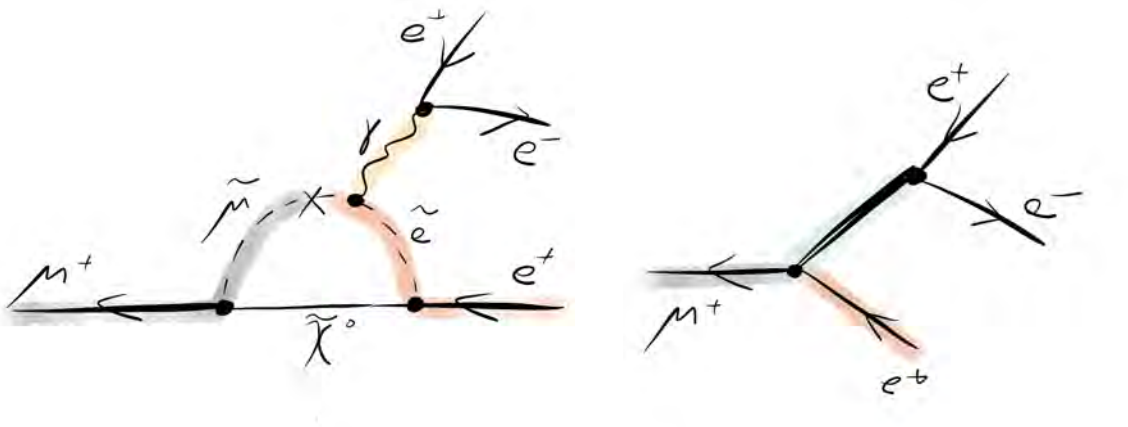
Any measured signal coming from either of these decays would therefore be an indication for the existence of physical processes beyond the Standard Model description.

2.3.2. Muon Decay Beyond the Standard Model

New theories beyond the Standard Model include the possibility of cLFV, which could enhance the branching ratio of processes like $\mu \to eee$.

One way to describe such a process is the inclusion of supersymmetric (SUSY) theories. SUSY particles could enter via loops as depicted in Figure 2.4a and cause cLFV via slepton mixing.

Another possibility is a process mediated by a heavy particle that couples to muons and electrons, leading to cLFV directly at tree-level (Figure 2.4b).



(a) Loop diagram including SUSY.

(b) Tree level process via heavy mediator.

Figure 2.4.: $\mu \to eee$ processes beyond the Standard Model.

The heavy masses of the new particles would still suppress the branching ratios of these processes. Neither of the particles necessary for these decays have been observed yet, so their masses and therefore the resulting branching ratio suppressions, are still unknown.

However, previous experiments have set upper limits on the branching ratios for the processes $\mu^+ \to e^+\gamma$ and $\mu^+ \to e^+e^-e^+$ (see Section 3.1).

3. The Mu3e Experiment

The Mu3e experiment searches for the lepton flavor violating decay $\mu^+ \to e^+e^-e^+$ with a sensitivity of one in 10^{16} decays. To achieve this goal on a reasonable time scale, 2×10^9 muon decays per second will have to be observed.

The following section describes the current status of cLFV searches. Afterwards, the experimental challenges and requirements, as well as the planned detector design for the Mu3e experiment are depicted.

3.1. Current Experimental Status of cLFV Decay Searches

Figure 3.1 shows the experimental limits for the branching ratios of different charged lepton flavor violating decays. The current limits are set by the SINDRUM and MEG experiments, which are explained in detail below.

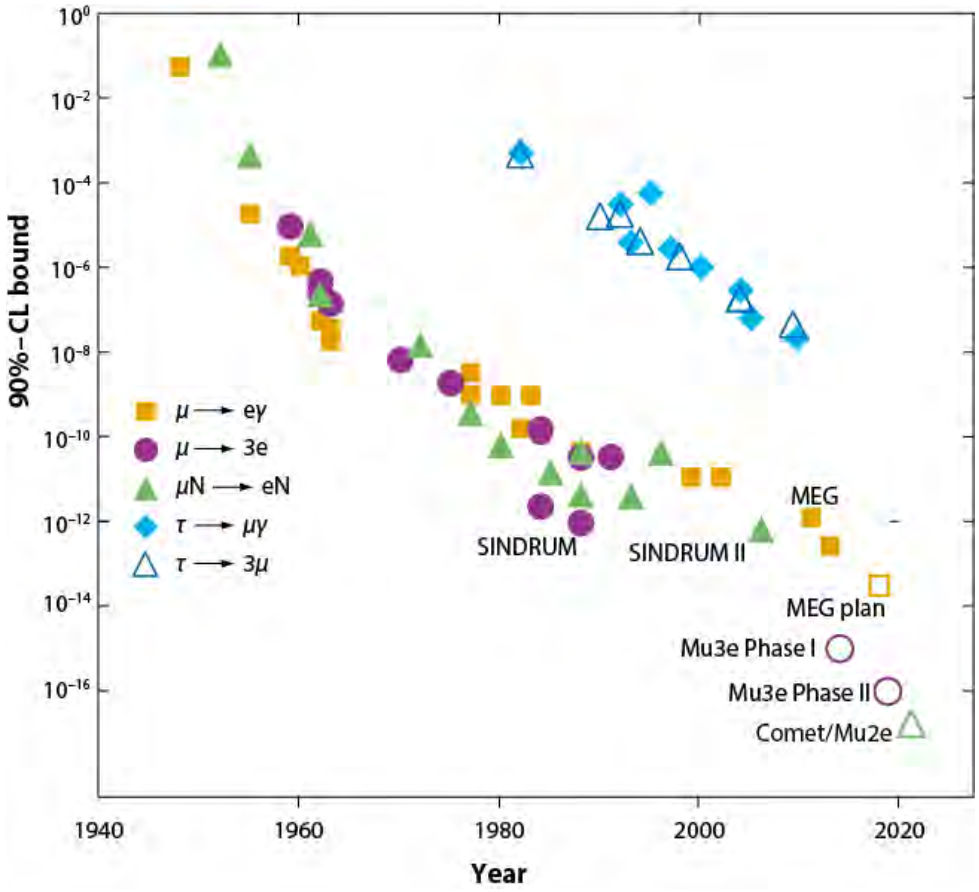


Figure 3.1.: Measured and planned limits on searches for cLFV processes. Adapted from [11].

3.1.1. SINDRUM

The SINDRUM experiment was conducted at PSI from 1983 to 1986. It searched for the decay $\mu^+ \to e^+e^-e^+$. In absence of a signal, an upper limit for the branching ratio of $BR < 10^{-12}$ was determined at 90 % CL [12].

For this experiment, 28 MeV/c surface muons were stopped on a double cone target inside a 0.33 T magnetic field. A five-layer Multi Wire Proportional Chamber (MWPC) tracker and a hodoscope trigger were positioned around the target. The main background, coming from the internal conversion decay $\mu^+ \to e^+e^-e^+\nu_e\bar{\nu}_\mu$, was used to estimate the sensitivity of the experiment to 5×10^{-14} [13]. The experimental results of SINDRUM were limited by the number of observed muon decays.

3.1.2. MEG

The MEG experiment is running at PSI since 2008 and searches for the LFV radiative decay $\mu^+ \to e^+\gamma$. The main detector consists of a liquid Xenon calorimeter for photon detection and a drift chamber for positron reconstruction [14].

With the analysis of the full data set collected between 2009 and 2013 an upper limit of $BR < 4.2 \times 10^{-13}$ at 90 % CL was reached [15]. An upgrade of the experiment is aiming to reach a sensitivity of better than one in 10^{13} for $\mu \to e\gamma$ decays, which corresponds to a sensitivity of at least one in 10^{15} for $\mu \to eee$ events, due to the additional suppression of the latter process by $\alpha_{em} \approx \frac{1}{137}$ (see previous chapter). Unlike Mu3e, however, MEG is insensitive to tree level processes, such as the one depicted in Figure 2.4b.

3.1.3. Conversion Experiments

Another cLFV process is the conversion $\mu N \to eN$ in the vicinity of an atomic nucleus N. The advantage of this process is a signature of monoenergetic electrons outside the energy range of the normal Michel decay. The current experimental limit for the branching ratio was set by SINDRUM II ($BR < 7 \times 10^{-13}$ at 90 % CL) in $\mu\text{Au} \to e\text{Au}$ processes using a gold target [16]. New muon conversion experiments like Mu2e at Fermilab or DeeMe, PRISM, and COMET at J-PARC, are aiming for branching ratios between 10^{-14} and 10^{-17} [17, 18, 19].

3.2. The Signal Decay

In the $\mu^+ \to e^+e^-e^+$ decay the electrons originate from the same vertex, as depicted in Figure 3.3a. Considering momentum conservation, the sum of the momenta of the decay products vanishes since the muon decays at rest.

$$|\vec{p}_{\text{tot}}| = \left|\sum_{i=1}^{3} \vec{p}_i\right| = 0 \tag{3.1}$$

Furthermore, the total energy of the decay products must add up to the muon rest mass[1]:

$$E_{\text{tot}} = \sum_{i=1}^{3} E_i = m_\mu \cdot c^2 = 105.658\,\text{MeV} \tag{3.2}$$

Equations 3.1 and 3.2 restrict the energy of a daughter particle to, at most, half the muon mass ($\sim$53 MeV).

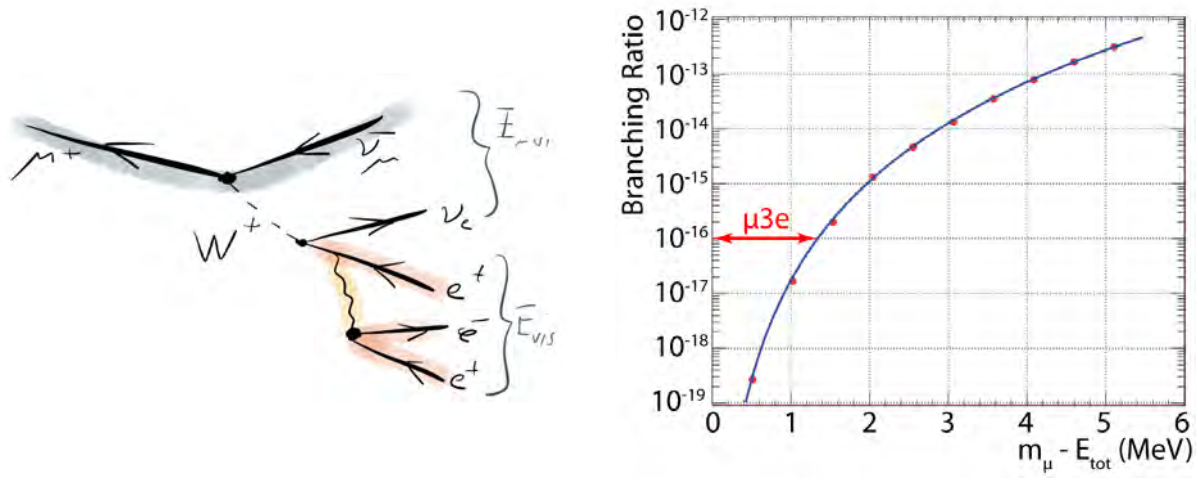
These relations are used to separate the signal decay from the occurring background effects.

3.3. Backgrounds

The background events of $\mu^+ \to e^+e^-e^+$ can be separated into two categories: Accidental background and irreducible background given by physics processes, mainly the internal conversion decay $\mu^+ \to e^+e^-e^+\nu_e\bar{\nu}_\mu$.

3.3.1. Internal Conversion

The Feynman diagram for the internal conversion decay is shown in Figure 3.2a. The decay products originate from the same vertex but due to the creation of neutrinos, which leave the experiment undetected, the relations given by Equations 3.1 and 3.2 do not hold any longer.



(a) $\mu^+ \to e^+e^-e^+\nu_e\bar{\nu}_\mu$ decay.

(b) Branching ratio of the internal conversion decay as a function of missing energy [20].

Figure 3.2.: Internal conversion.

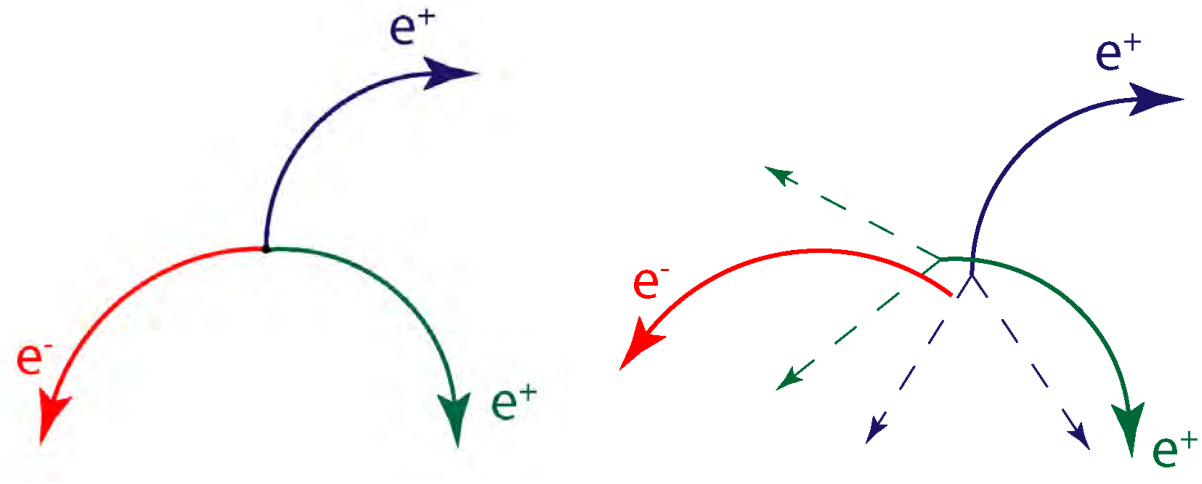
[1]The muon mass in Eq. 3.2 is taken from [4]

To discriminate against this background, a very high momentum resolution is necessary. Figure 3.2b shows the branching ratio contribution of the internal conversion decay as a function of missing energy. To achieve a sensitivity of at least one in 10^{16}, a total momentum resolution of better than 1 MeV is required [1].

3.3.2. Accidental Background

Accidental backgrounds can arise from topologies that look like two positrons and an electron originating from the same vertex despite being completely separate from one another in space and time. A common accidental background may come from an event, as depicted in Figure 3.3b, where two positrons are created by Michel decays ($\mu^+ \to e^+\nu_e\bar{\nu}_\mu$). The additional electron can come, for example, from Bhabha scattering of a decay positron with an electron in the target material. Because of the high rate of incoming muons, events like this give a significant contribution to the overall background.

In order to suppress accidental backgrounds a very good spatial resolution and precise timing are necessary.



(a) Signal event topology.

(b) Accidental background topology coming from two Michel decays and an additional electron.

Figure 3.3.: $\mu \to eee$ topologies.

3.4. Detector Requirements

The above mentioned experimental conditions impose high requirements on the detector design. It must be able to handle the high rate of 2×10^9 muon stops per second. The geometrical acceptance and detection efficiency must be high in order to keep the measurements on a reasonable time scale. The detector needs excellent momentum and vertex resolution as well as precise timing to sufficiently discriminate against the above mentioned background sources.

The fact that the momenta of the decay products are at most 53 MeV/c puts an additional constraint on the detector. In this low momentum region, multiple Coulomb scattering in the detector becomes the limiting factor for the spatial and momentum resolution. To keep this effect as low as possible, a very low material budget is required.

3.5. The Mu3e Detector

The goal of the Mu3e experiment is to stop more than 10^{16} muons on a target and observe the decay $\mu^+ \to e^+e^-e^+$ of a muon into three charged particles. To track the decay products, a highly granular silicon pixel detector is used. It consists of several barrel shaped layers surrounding the target and facing along the beam axis. A scintillating fiber tracker and a scintillating tile detector are used for precise timing measurements (see Figure 3.4).

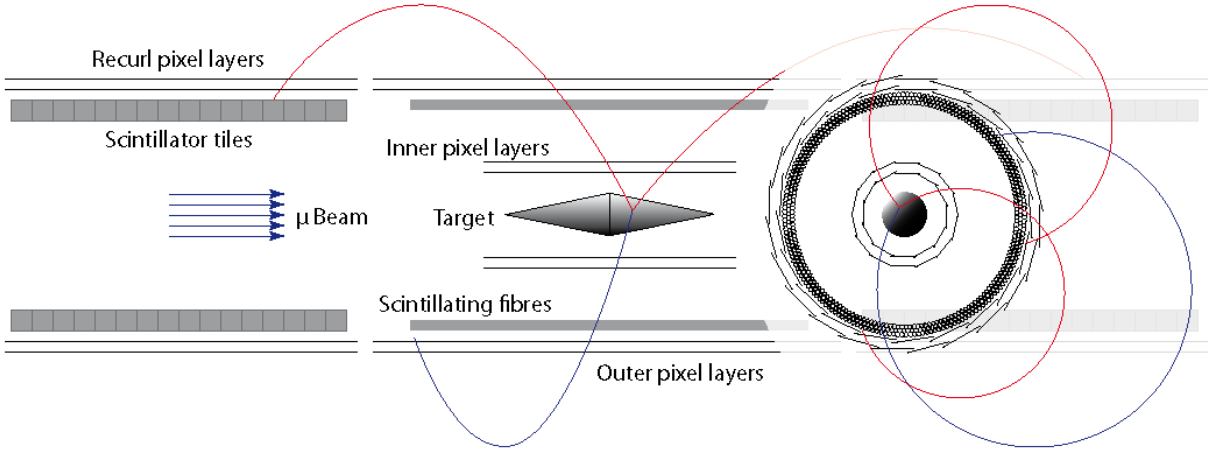


Figure 3.4.: Schematic side view (left) of the Mu3e detector showing a $\mu^+ \to e^+e^-e^+$ event and a view along the beam axis (right).

The experimental setup is placed in a 1 T magnetic field to determine the momenta of the decay products by measuring the curvature of their trajectories. The setup is cooled using a flow of gaseous helium.

3.5.1. Muon-Beam & Target

At the moment, there is no facility that can provide the rate of 2×10^9 muon stops per second needed for the final sensitivity of the Mu3e experiment. Therefore, the experiment is planned to run in two phases.

In phase I, the setup uses the πE5 beamline of the High Intensity Proton Accelerator (HIPA) at PSI. A layout of the accelerator facility and the beamlines can be seen in Figure 3.5.

The 590 MeV/c protons provided by the HIPA cyclotron are directed towards two rotating carbon targets, Target M and Target E. From Target E 28 MeV/c surface muons are extracted and directed along the πE5 beamline. The muons are created by pions decaying at rest on the surface of the target, hence the name. The muon rate is in the order of 10^8 Hz, currently making this beam the highest intensity continuous muon beam worldwide.

To reach the goal muon rate in phase II, a new beamline has to be constructed. A possibility to increase the muon intensity is currently studied at PSI and will most likely involve upgrading the target [21].

The muon beam is stopped in the Mu3e detector using a hollow double cone shaped Mylar® target, so that the muons can decay at rest.

Figure 3.5.: PSI Experiment Hall with πE5 beam line.

3.5.2. The Tracking Detector

In its entirety, the tracking detector is separated in five barrel shaped units of thinned silicon pixel detectors along the beam axis. The central barrel surrounding the target consists of four layers. The two innermost layers very close to the target are used for vertex reconstruction. The outer layers at a further distance are used to determine the momenta of the decay products by measuring the curvature of the trajectories in the 1 T magnetic field.

The central barrel is the first unit to be operated with the beginning of the first phase (phase Ia). Additional units are added upstream and downstream during the other phases (phase Ib and phase II) to increase the acceptance for decay particles that are bent back into the detector region by the magnetic field. Measuring these recurling particles will improve the momentum resolution. The recurl units consist of two pixel detector layers each, positioned at the same radii as the outer layers of the central barrel.

(a) Support structure prototype for inner layers.

(b) Support structure prototype for an outer layer module.

Figure 3.6.: Polyimide support structure prototypes.

The layers are built of 50 µm thin detectors mounted on a 25 µm self-supporting polyimide structure (see Figure 3.6). Additionally, the sensors are bonded to a polyimide/aluminum circuit flexprint providing power, slow control, and sensor readout via 1.25 Gbit/s Low Voltage Differential Signal (LVDS) links. With this design the material budget can be reduced to $\sim$1 ‰ of radiation length per layer.

The active area of one sensor is about $2 \times 2\,\mathrm{cm}^2$, with a pixel size of $80 \times 80\,\mu\mathrm{m}^2$. The overall active area for the detector is $>1\,\mathrm{m}^2$ consisting of 275 million pixels.

3.5.3. The Timing Detector

The precise timing measurements for coincidence determination will be achieved by two parts: A scintillating fiber detector in the central part of the setup and a scintillating tile detector in the recurl stations.

Fiber Detector

The fiber detector consists of ribbons of three layers of tightly stacked 250 µm thick and 36 cm long scintillating fibers, located between the inner and outer pixel detector layers of the central barrel. It is designed to have a time resolution of <1 ns [1] while keeping the additional material budget in the central detector region as low as possible. The fibers are read out by Silicon Photomultipliers (SiPM) at each end. SiPMs are used because of their compact size, their high gain at relatively low operating voltages, and their insensitivity towards magnetic fields. Figure 3.7 shows a cross section through a fiber ribbon.

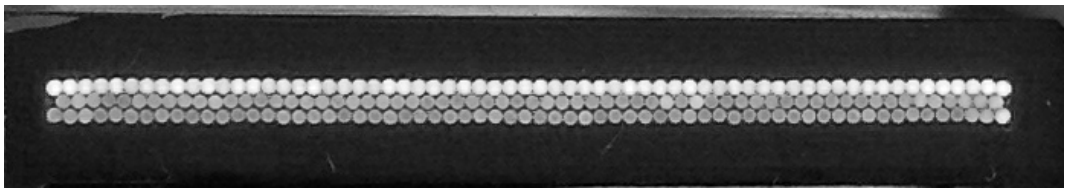


Figure 3.7.: Cross section of a three-layer scintillating fiber ribbon [22].

Tile Detector

The four modules of the scintillating tile detector are located in the recurl stations, directly below the pixel detector layers. Since they form the last detection station for the decay products they can be optimized for time resolution even at the cost of a higher material budget. They are composed of $6.5 \times 6.5 \times 5\,\mathrm{mm}^3$ tiles, which are individually read out by SiPMs. The tile detector is aiming for precise timing with a resolution of <100 ps [1].

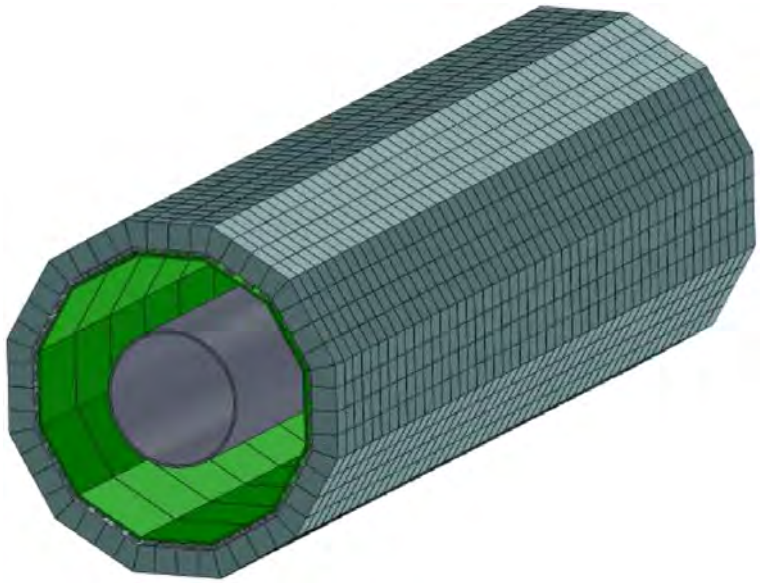


Figure 3.8.: Drawing of a tile detector module [1].

3.5.4. Readout Concept

Figure 3.9 shows the readout scheme for the complete detector. The Mu3e experiment does not use a hardware trigger, which means the detector is continuously read out, resulting in a total data rate of >100 GB/s. The steering and readout of the detector components occurs via Field Programmable Gate Arrays (FPGA). From the FPGAs the data stream is sent to readout

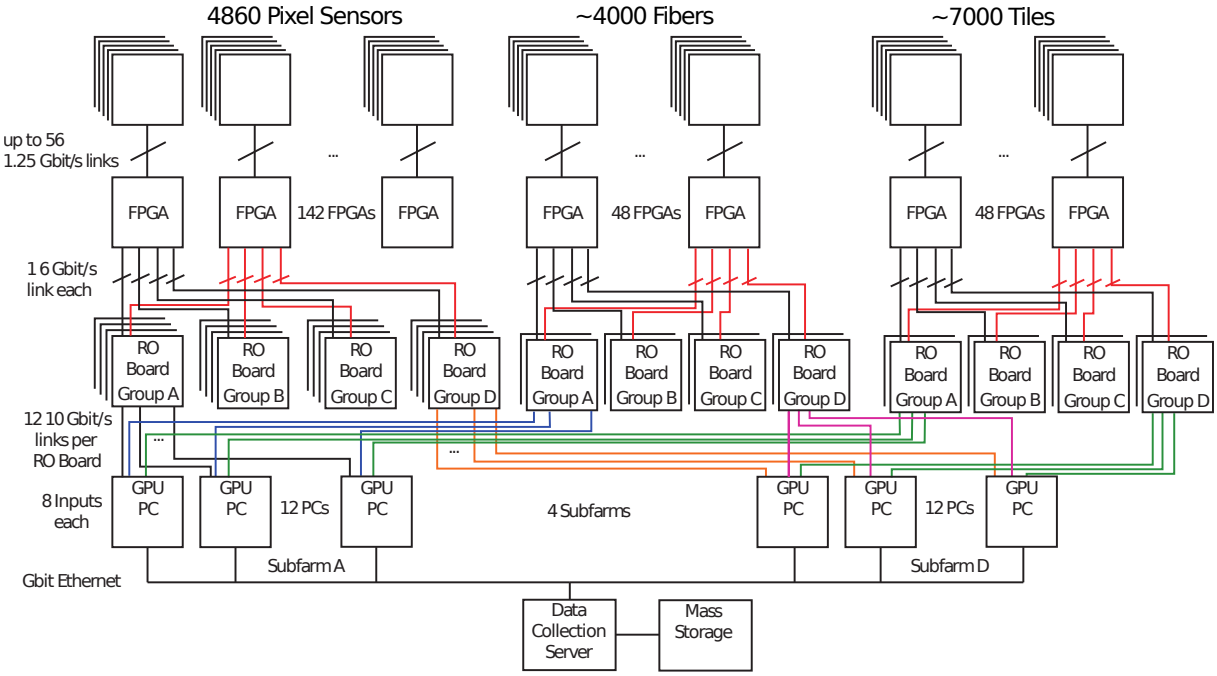


Figure 3.9.: Mu3e readout scheme.

boards, which transmit time ordered slices of the complete data to filter farm PCs. The Graphic Processing Units (GPUs) are used for online track reconstruction and filtering. At the end ~100 MB/s of data remain, which are sent to a mass storage system.

3.5.5. Cooling

When in use, all electrical components of the detector produce heat, with the pixel sensors being the main heat source. A cooling system using a flow of gaseous helium along the beam axis is used to cool the detector to <70 °C. Helium was chosen to reduce the contribution to the multiple scattering processes in the detector. Besides that, it has good heat conduction properties, which make it more efficient than, for example, using air.

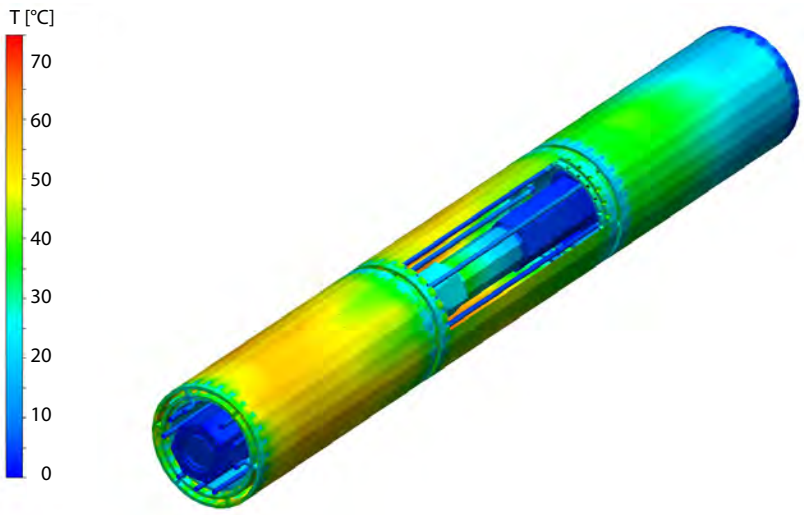


Figure 3.10.: Cooling simulation for a 3-stage detector geometry using 0 °C helium with a maximum pixel layer power consumption of 400 mW/cm^2 [56].

During the course of several master's theses [23, 24] a cooling concept for the Mu3e detector was developed and tested. Simulations showed that a total heating power of $400\,\mathrm{mW/cm^2}$ can be sufficiently cooled by using a combination of a global helium flow through the whole detector and a local flow directly at the pixel sensors (see Figure 3.10). The local flow at the sensors is realized by using prism shaped folds in the polyimide support structures, as shown in Figure 3.11.

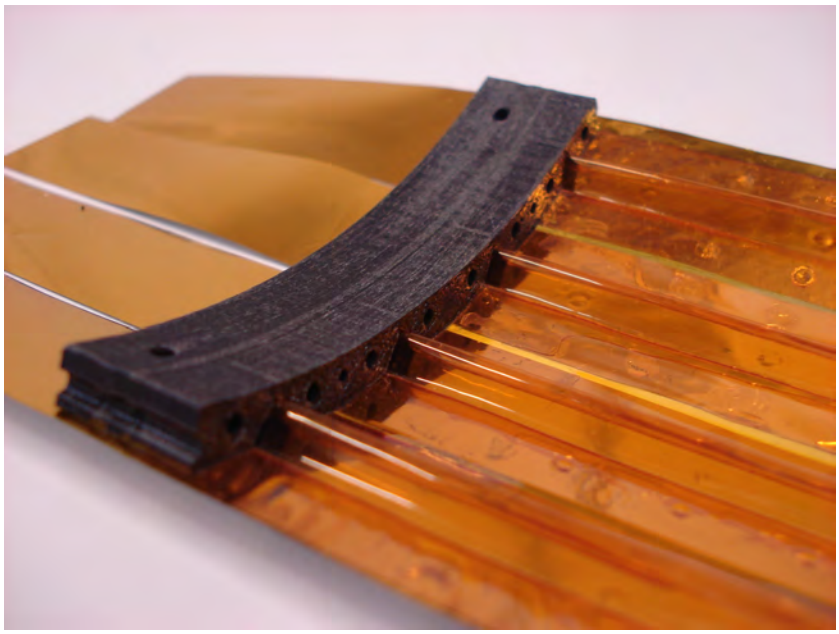


Figure 3.11.: Close-up of an outer layer support structure prototype with prism shaped folds [24].

4. Charged Particles: Interactions with Matter and Detection

Particles are detected via their interactions with matter. Their properties are determined by the types of interactions they partake in. This however influences the particles and gives rise to effects like scattering processes, which are a dominant error source for the determination of particle properties in the Mu3e experiment. This chapter elucidates the interactions of charged particles with matter and how their properties are used for particle detection.

4.1. Interactions with Matter

The interaction properties of charged particles with matter depend primarily on their charge and mass. A distinction between electrons or positrons and heavier particles is important since the occurrence of kinematic effects like bremsstrahlung scales with the mass of the particle. For hadronic particles also strong interactions come into play, but they can be neglected for Mu3e.

4.1.1. Heavy Particles

For charged particles with masses of $m_0 \geq 100\,\mathrm{MeV}$ the dominant process for energy loss in a medium is ionization. The mean energy loss per traveled distance $-\left\langle \frac{\mathrm{d}E}{\mathrm{d}x} \right\rangle$ is given by the Bethe-Bloch formula [25]:

$$-\left\langle \frac{\mathrm{d}E}{\mathrm{d}x} \right\rangle = \frac{4\pi n z^2}{m_e c^2 \beta^2} \cdot \left(\frac{e^2}{4\pi\epsilon_0} \right)^2 \cdot \left[\log\left(\frac{2 m_e c^2 \beta^2}{I \cdot (1-\beta^2)} \right) - \beta^2 \right] \tag{4.1}$$

where n denotes the electron density of the material, z the charge of the particle (in units of the elementary charge e), m_e the rest mass of the electron, c the vacuum speed of light, β the relative velocity $\frac{v}{c}$ of the particle, ϵ_0 the vacuum permittivity, and I the mean excitation energy of the material.

The Bethe-Bloch formula is plotted in Figure 4.1 for different materials. It shows a minimum at $\beta\gamma = \frac{p}{m_0 \cdot c} \approx 3$. Particles traversing a material with corresponding momentum experience minimal energy loss via ionization and are therefore called Minimum Ionizing Particles (MIP). For slower particles the mean energy loss rises with $\frac{1}{\beta^2}$ due to longer interaction time with the material. At high momenta the relativistic squeezing of the transverse electric field gives rise to a logarithmic increase in energy loss.

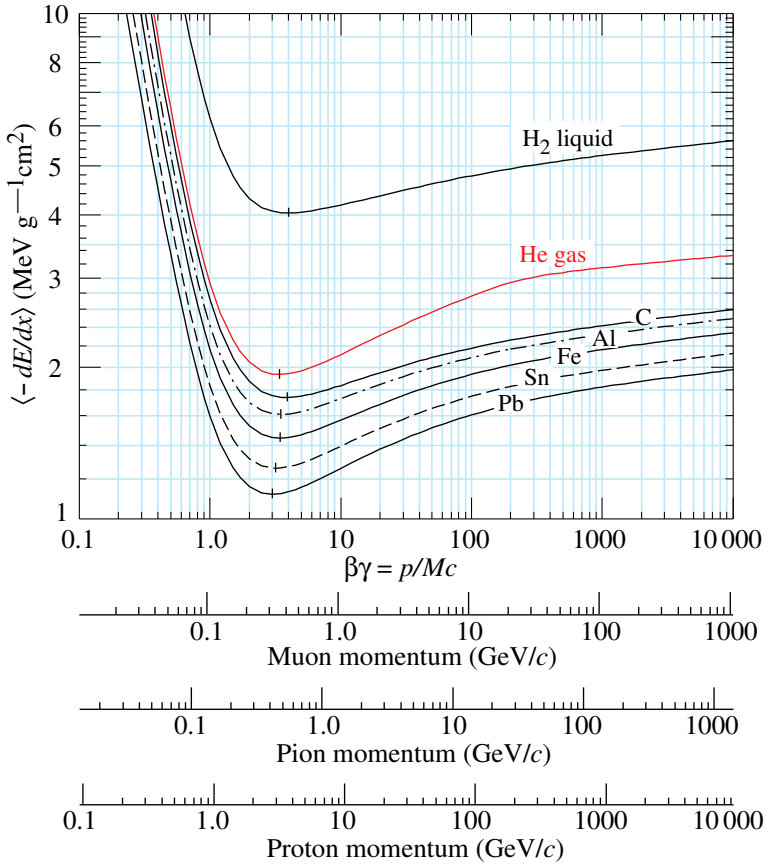


Figure 4.1.: Mean energy loss of charged particles in different materials described by the Bethe-Bloch formula [4].

4.1.2. Electrons and Positrons

Electrons and Positrons are very light particles. Their two main sources of energy loss in material are ionization and bremsstrahlung.

The energy loss via ionization in this case is given by the Berger-Seltzer formula [26]:

$$-\left\langle \frac{\mathrm{d}E}{\mathrm{d}x} \right\rangle = \rho \cdot \frac{0.153536}{\beta^2} \frac{Z}{A} \cdot \left[B_0(T) - 2\log\left(\frac{I}{m_e c^2}\right) - \delta \right] \tag{4.2}$$

which depends on the density ρ, atomic number Z, and mass number A of the material, as well as a density correction term δ, the mean excitation energy I of the material, and the stopping power $B_0(T)$, which depends on the material and the kinetic energy T of the electron or positron.

The energy loss for electrons and positrons traversing silicon with momentum P is plotted in Figure 4.2. The difference between the electron and positron is due to the indistinguishability between incident and material electrons, which is not given for positrons.

For highly relativistic particles ($\beta \approx 1$) also bremsstrahlung effects play an important role. The energy loss is proportional to the total energy E of the particle and depends on the radiation length X_0 of the material [27]:

$$-\frac{\mathrm{d}E}{\mathrm{d}x} = -\frac{E}{X_0} \tag{4.3}$$

The radiation length of a material is dependent on its atomic number Z and nucleon number A and can be approximated by [28]:

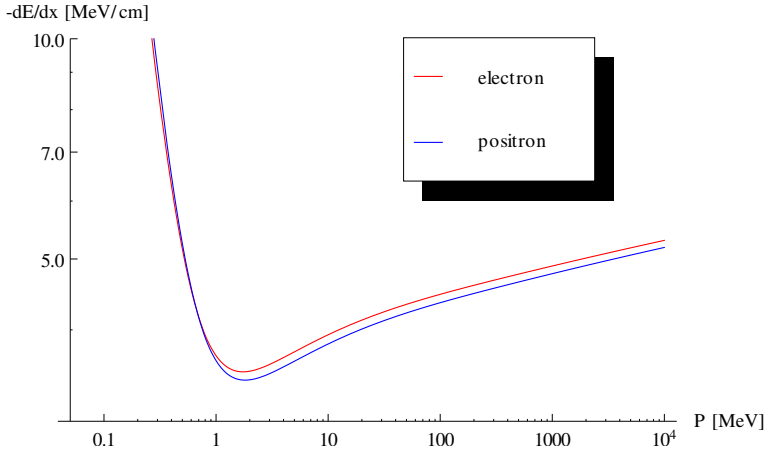


Figure 4.2.: Energy loss of electrons and positrons in silicon with momenta from 50 keV/c to 10 GeV/c [21], using data from [26].

$$\rho \cdot X_0 = \frac{716.4\,\mathrm{g/cm^2} \cdot A}{Z(Z+1) \cdot \log\left(287/\sqrt{Z}\right)} \tag{4.4}$$

4.2. Multiple Coulomb Scattering

A particle that traverses a material will undergo several interactions, each causing the particle to slightly change its path by a small angle, resulting in a visible deflection angle, as seen in Figure 4.3. Most of these scattering processes are due to interactions with the Coulomb field of the nuclei in the material. Using a Gaussian approximation results in Eq. 4.5 for the RMS of the central 98 % of the angular distribution [4].

$$\Theta_{\mathrm{RMS}} = \frac{13.6\,\mathrm{MeV}}{\beta cp} z \sqrt{\frac{x}{X_0}} \cdot \left[1 + 0.038 \log\left(\frac{x}{X_0}\right)\right] \tag{4.5}$$

For the small momenta ($\lesssim 53\,\mathrm{MeV/c}$) of the final state electrons and positrons of the $\mu \to eee$ decay, this leads to large scattering angles in the material of the Mu3e detector. This can be counteracted, however, by reducing the material thickness in units of radiation length, the so-called effective radiation length $\frac{x}{X_0}$.

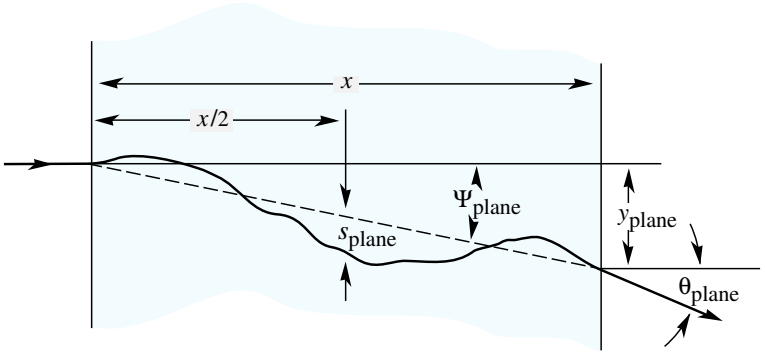


Figure 4.3.: Illustration of a particle undergoing several scattering processes while traversing a material [4].

4.3. Particle Detectors

In particle detectors different approaches are used, depending on the particle property that one wants to measure. The two main ideas are either complete absorption of a particle in high Z material to measure the total energy, as it is done in calorimetry, or minimal disturbance in low material budget trackers for momentum and vertex determination.

For the Mu3e experiment a very precise momentum measurement is essential, which gives two options for detectors using the minimal disturbance approach, either thin layers of solid state detectors or a Time Projection Chamber (TPC).

TPCs are large gas filled vessels with sensors at opposing ends between which a high voltage is applied. A charged particle traversing the gas volume creates a trail of ionized gas and electrons along its trajectory. In the electric field ions and electrons drift with rather constant velocities to the ends of the volume where they create a measurable electrical signal. Using the drift time information the particles path can be reconstructed. Due to the long drift times, TPCs are quite slow and since the gas has to be completely discharged before a new particle can be detected, they are limited in rate, which makes them unsuitable for a high rate experiment like Mu3e.

Solid state detectors made of semi-conducting material have a fast charge collection and are capable of handling high rates. Their disadvantages, however, are high material budget and expensive production. While passing through the material, a charged particle creates electron-hole pairs that can be detected at an electrode. Lately, an increase in demand and development of new procedures have lead to a decrease in production costs, making thinned semiconductors much more affordable.

5. Semiconductor Physics

The most commonly used materials for the fabrication of semiconductor sensors are silicon and germanium. For the Mu3e experiment the sensors are made of silicon. The relevant properties of semiconductors are explained in this chapter.

5.1. Silicon

In its condensed state silicon forms diamond like crystals. Its four valence electrons form covalent bonds with neighboring atoms as depicted in Figure 5.1. Important properties of silicon are summed up in Table 5.1.

Property		Value	Unit
Atomic number	Z	14	
Atomic mass		28.09	u
Density	ρ	2.33	g/cm^3
Crystal structure		Diamond	
Atom density		5.0×10^{22}	$1/cm^3$
Intrinsic charge density	n_i	1.5×10^{10}	$1/cm^3$
Dielectric constant	ϵ	11.9	
	at 300 K		
Band gap	indirect	1.12	eV
	direct	3.4	eV
Average creation energy for an electron-hole-pair	ω	3.66	eV
Fano Factor	F	0.115	
Mobility	μ_n	1450	$cm^2/(Vs)$
	μ_p	500	$cm^2/(Vs)$

Table 5.1.: Properties of silicon [29, 30, 31, 32, 33, 34].

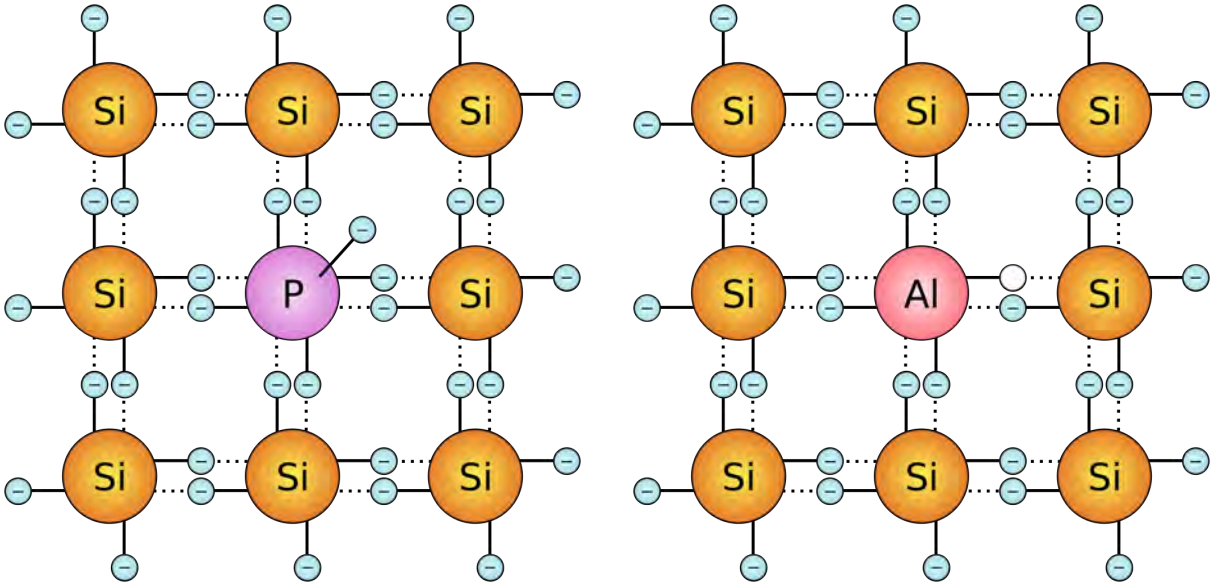
In semiconductors, the energy gap between the covalent bound electron state (valence band) and the state of electrons moving as free charge carriers through the crystal (conduction band) is small enough for electrons to be thermally excited to the latter state at room temperature. Electrons that are excited to the conduction band leave a so-called hole in the valence band, which can be filled by another electron in the covalent structure, so that the hole effectively changes its position. Therefore, the hole can be treated as a freely moving positive charge in the valence band. In a process called recombination, an electron in the conduction band can de-excite again to the valence band and fill up a hole. Both processes, excitation and recombination, underly Fermi-Dirac statistics.

5.2. Doping

As seen in Table 5.1, the number of free charge carriers in pure silicon (intrinsic charge density) at room temperature is more than ten orders of magnitude smaller than the atomic density, which leads to low conductivity compared to metal.

In order to increase conductivity, artificial impurities can be added in a process known as doping. These impurities can be elements with either three or five valence electrons. Using atoms with five valence electrons, e.g. phosphorous or arsenic, leads to four of them forming covalent bounds with the silicon atoms and one weakly bound electron at an energy level close to the conduction band (see Figure 5.1a). This electron can easily be thermally excited to the conduction band. Implants that bring additional electrons to the conduction band are called donators, the process of doping silicon with donators is called n-doping.

Conversely, in a process called p-doping the silicon is implanted with atoms, which are called acceptors, that have only three valence electrons, like boron or aluminum. In this case, only three covalent bounds with the silicon atoms can be formed, which creates an effective hole in the valence band that can be filled with de-excited electrons from the conduction band (see Figure 5.1b).



(a) N-doping (b) P-doping

Figure 5.1.: Schematic silicon crystal lattice with phosphorous and aluminum dopants. Images from [35].

5.3. The p–n Junction

When p- and n-doped semiconductors are in contact, their shared boundary is called a p–n junction, which can be used as a diode. The difference in concentrations of free charge carriers at this boundary gives rise to a diffusion of electrons into the p-doped and holes into the n-doped region. The charge carriers recombine in the junction region and leave behind their respective donator and acceptor ions. This gives rise to an electric field, which in turn creates a drift of charge carriers opposite to the diffusion movement. The field region no longer contains free charge carriers and is called depletion zone or space charge region (see Figure 5.2).

Assuming an equilibrium between diffusion movement and drift current, the diffusion voltage in the junction region is given by [37]:

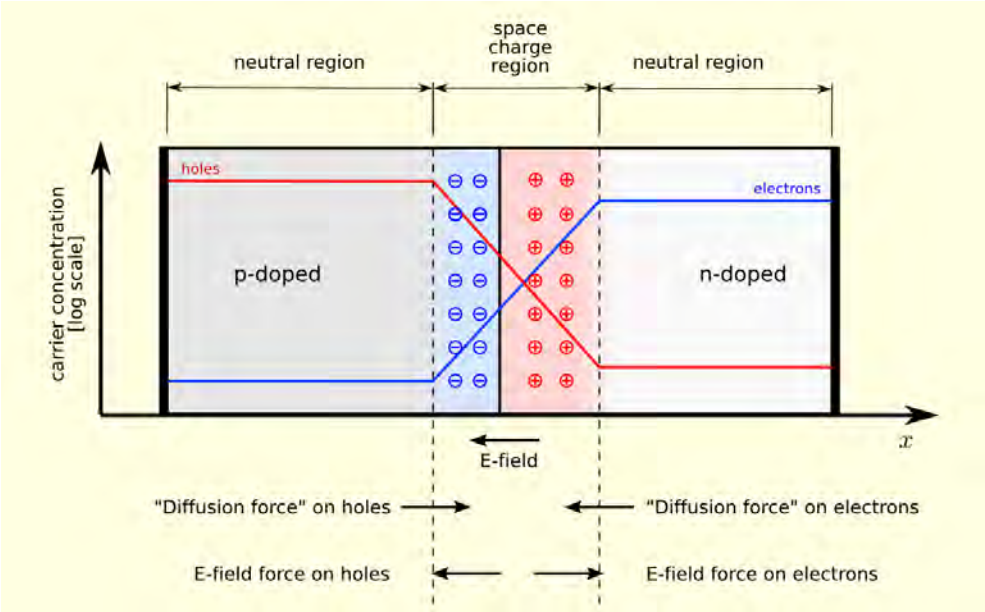


Figure 5.2.: p–n junction equilibrium schematic. Image from [36].

$$V_D = V_T \cdot \log\left(\frac{N_A N_D}{n_i^2}\right) \tag{5.1}$$

where $V_T = \frac{k_B T}{e}$, with Boltzmann's constant k_B, is the thermal voltage equivalent (25.9 mV at 300 K), n_i is the intrinsic charge density of the semiconductor (see Table 5.1), N_A and N_D are the acceptor and donator concentrations, respectively.

The dynamics of this system are given by Poisson's equation (Eq. 5.3). Starting with Gauss's law for the one-dimensional case

$$\boldsymbol{\nabla} \cdot \vec{E} = \frac{\rho(\vec{x})}{\epsilon_0 \epsilon} \quad \xrightarrow{1\text{ dim.}} \quad \frac{\mathrm{d}E_x}{\mathrm{d}x} = \frac{\rho(x)}{\epsilon_0 \epsilon} \tag{5.2}$$

where ϵ denotes the dielectric constant (Table 5.1) and $\rho(x)$ the charge density distribution, one can substitute $E_x = -\frac{\mathrm{d}V}{\mathrm{d}x}$, to arrive at Poisson's equation:

$$\frac{\mathrm{d}^2 V}{\mathrm{d}x^2} = -\frac{\rho(x)}{\epsilon_0 \epsilon} \tag{5.3}$$

This makes it possible to calculate the thickness w of the depletion zone, as described in detail in [37]:

$$w = \sqrt{\frac{2\epsilon_0 \epsilon V_D}{e} \frac{N_A + N_D}{N_A N_D}} \tag{5.4}$$

5.4. The p–n Junction with External Voltage

The equilibrium between diffusion and drift can be disturbed by externally applying a voltage V_{ext} to the p–n junction, which influences the thickness of the depletion zone. The polarity of

V_{ext} is defined opposite to V_D. In case of positive V_{ext} (forward bias) the electrostatic potential in the depletion region decreases in strength. This results in a smaller drift current compared to diffusion. More electrons now diffuse into the p-doped region and more holes diffuse into the n-doped region, which causes the depletion zone to narrow. Negative V_{ext} (reverse bias) leads to a higher potential, which counteracts diffusion. As a result the depletion zone widens [37].

The thickness of the depletion zone can be calculated by including a term for the external voltage in Equation 5.4:

$$w = \sqrt{\frac{2\epsilon_0\epsilon(V_D - V_{ext})}{e}\frac{N_A + N_D}{N_A N_D}} \tag{5.5}$$

5.5. Charge Collection and Signal Generation

As described in Chapter 4, charged particles traversing the semiconductor lose energy by exciting electrons in the material to the conduction band, creating electron-hole pairs. Soft X-ray photons in the energy region of a few keV are absorbed via the photoelectric effect, creating a free electron. The energy of this electron is high enough to create secondary electron-hole pairs, forming a charge cloud. The mean excitation energy necessary to create an electron-hole pair in silicon is 3.66 eV (see Table 5.1).

The charge collection depends on two components, drift and diffusion. Electron-hole pairs that are created in the depletion zone rapidly drift in the electric field toward the opposite electrode. This creates the fast component of the signal. Electron-hole pairs that are created outside the depletion zone and diffuse into the material and recombine in the most cases. Some of them can eventually diffuse into the depletion zone, where they are again collected via drift, giving rise to a slow signal component. Their contribution to the overall signal, however, can be neglected. The drift movement induces an influence signal in the detection electrode, according to the Shockley-Ramo theorem [38, 39]. The total charge measured at the electrode depends on the drift time of the electrons and holes which is given by the drift velocity $\vec{v}_{\text{drift}}$. The drift velocity is dependent on the electric field and the mobility μ:

$$\vec{v}_{\text{drift}} = \vec{E} \cdot \mu \tag{5.6}$$

In Table 5.1 it can be seen that the mobility for holes is about three times lower than for electrons. For a fast signal generation in the case of the MuPix sensors only the signal component coming from electrons is used.

6. Pixel Detectors and HV-MAPS Concept

6.1. Pixel Detectors

Semiconductor pixel detectors are commonly used as trackers in particle physics experiments like ATLAS, CMS, and ALICE at LHC. Their advantage is a high granularity leading to an excellent two-dimensional spatial resolution. Usually, they are produced from silicon or germanium wafers in a lithographic process resulting in doped structures that can be used as fully depleted detection diodes. The detectors used in these experiments are so-called hybrid detector systems, realizing the readout electronics on a separate chip that is bump bonded to the sensor chip. This leads to the disadvantage of having a lot of material in the detector, which contributes to multiple scattering and also increases production costs. A pixel detector using this approach is therefore not suitable for the Mu3e experiment. Instead, the HV-MAPS concept is used, which combines fast charge collection and signal generation with a readout scheme that is implemented on the same substrate as the sensors to keep the material budget as low as possible.

6.2. MAPS: Monolithic Active Pixel Sensors

The first Active Pixel Sensors (APS) were developed by and used in the photo industry. The pixels are divided into an active detection surface area and a digital readout cell. These structures have relatively small fill factors of $\sim$30 %. The fill factor denotes the size active area relative to the total area of the sensor. The concept can be enhanced for particle detectors by not only using the surface but the complete substrate material below the pixel. These so-called Monolithic Active Pixel Sensors (MAPS) have fill factors of $\sim$100 % and have been developed for particle detectors since the 1990s. They can be fabricated in commercial Very Large Scale Integrated (VLSI) CMOS processes, which makes it possible to produce large numbers of sensors at low costs.

MAPS are used for example in the MIMOSA chip, which is the basis for the STAR vertex detector [40] and the EUDET beam telescopes [41]. These chips are operated with a non-depleted substrate, which means charge is not collected via drift as it is the case in depleted detection diodes, but via diffusion, meaning charge collection is slower and the produced signals are smaller.

6.3. High Voltage MAPS

The High Voltage MAPS (HV-MAPS) approach combines the MAPS concept with the fast charge collection of depleted detection diodes. It was first proposed by Ivan Perić [2] in 2007 and is the basis for the MuPix family of chips.

The pixels are implemented as deep n-doped wells in a p-doped substrate. The n-well contains the pixel logic, as depicted in Figure 6.1. By applying a high reverse bias voltage, usually 85 V in the case of the MuPix, the junction between n-well and p-substrate is used as depleted detection diode. A traversing particle creates electron-hole pairs of which the electrons are collected via drift, which gives a fast signal.

This design allows for the use of commercially available High Voltage CMOS (HV-CMOS) production processes, as they are used in the automotive and power industry, keeping the production costs low.

Since the width of the depletion zone is small (10 – 15 µm), it is possible to thin the entire chip down to 50 µm without losing performance. This helps to reduce the material budget and thus decreases the amount of multiple scattering processes in the final detector.

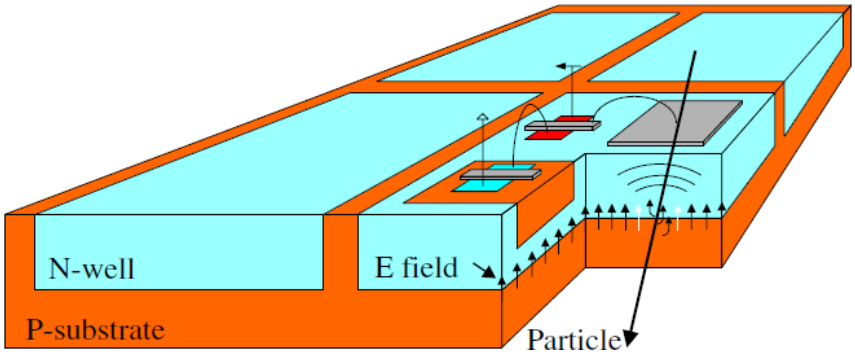


Figure 6.1.: Simplified HV-MAPS concept [2].

Part II.

SETUP

7. The MuPix Chip

7.1. The MuPix Prototypes

The MuPix chips are a series of prototypes of HV-MAPS for the Mu3e experiment. They a produced using the AMS 180 nm process. Table 7.1 shows a list of all MuPix iterations so far. The basic layout is very similar for all chips. They consist of an active pixel matrix with built-in preamplifiers and a peripheral strip in which signals are discriminated and digitized.

Prototype	Pixel Matrix	Pixel Size	Novelty	Year
MuPix1 & MuPix2	36×42	$39 \times 30\,\mu m^2$	proof-of-principle	2011, 2012
MuPix3 & MuPix4	32×40	$92 \times 80\,\mu m^2$	digital readout	2013
MuPix6	32×40	$103 \times 80\,\mu m^2$	2^{nd} amplifier stage	2014
MuPix7	32×40	$103 \times 80\,\mu m^2$	full integration	2014
MuPix8	*128 × 200*	*81 × 80 µm²*	*large scale test*	*2017*

Table 7.1.: MuPix Prototypes.

The first versions, MuPix1 and MuPix2, served as a test of the HV-MAPS concept and the chip design. In later iterations the digital processing of the analog pixel signal was improved and a zero-suppressed readout was implemented. MuPix6 introduced a second amplification stage in the periphery. The current version is the MuPix7 chip, which is described in detail in the next section.

A new prototype, the MuPix8, has been designed and submitted for production at the time of writing. With a physical size of about $1 \times 2\,cm^2$, a size similar to the sensors planned for the final experiment, it will be the first large scale test of the HV-MAPS chip concept.

7.2. MuPix7

7.2.1. Layout

The MuPix7 is the first prototype in the MuPix family to have a fully integrated state machine, its own timestamp generator, a zero-suppressed fast serial readout, and data transmission at 1.25 Gbit/s.

The analog part is identical to that of the previous generation. Figure 7.1 shows the layout of the MuPix7. The physical size of the chip is $3.5 \times 4.16\,mm^2$. The pixel matrix covers an area of $3.296 \times 3.2\,mm^2$, consisting of 32×40 pixels, with a size of $103 \times 80\,\mu m^2$ each. Each pixel houses a charge sensitive amplifier (CSA) and a source follower (SF), which drives the signals to the corresponding digital cell in the periphery.

The periphery containing the digital cells is located below the pixel matrix. Most cells contain a second amplifier and a comparator. However, the digital parts corresponding to the first four pixel columns do not contain an additional amplifier, which means these pixels operate in the one-stage amplification scheme that was used up to MuPix4. The digital cells are arranged in a 64×20 matrix. Therefore, one pixel column corresponds to two columns in the digital part (see Figure 7.2). As, in case of a hit, only the digital cell position is transmitted in the readout, it is

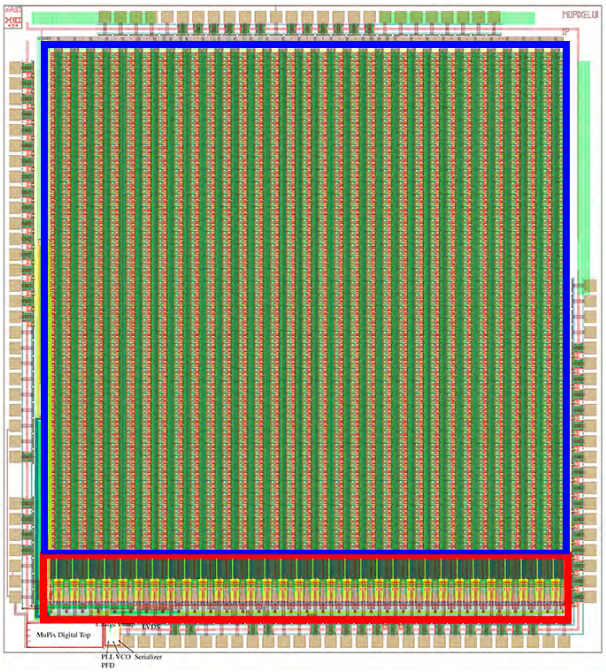


Figure 7.1.: MuPix7 Layout. **Blue:** Pixel Matrix, **Red:** Periphery.

necessary to convert the digital position back to the corresponding position in the pixel matrix to determine where a particle passed through the sensor. The decoding procedure in case of MuPix6, which has the same layout as MuPix7, can be found in [42].

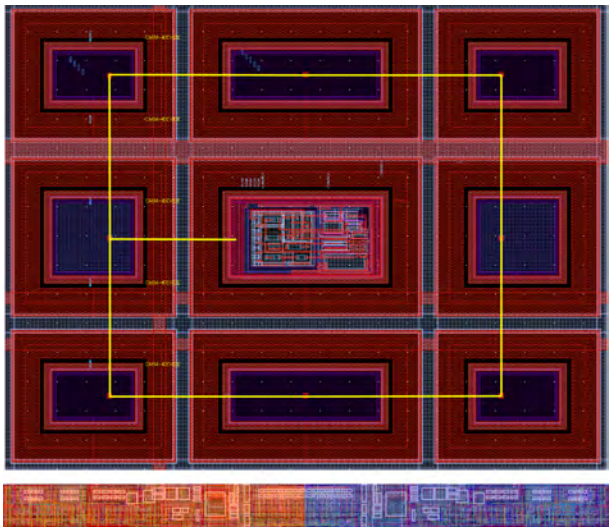


Figure 7.2.: MuPix7 pixel in the active matrix (top) and two digital cells in the periphery (bottom).

The chip also contains two shift registers for the steering of the performance. The first one is used to control the on-chip digital-to-analog converters (chip DACs). The DACs set the bias voltages for the different electronic components of the chip, which are explained in the following. The second register is used for the so-called tune DACs and to select the hitbus readout of a dedicated pixel, i.e. the comparator output signal of this pixel.

7.2.2. Pixel

A single pixel is realized as a 3×3 diode structure (see Figure 7.2) consisting of deep n-wells in a p-substrate. The charge collection electrodes the nine diodes are shorted to create a single electrode for the entire pixel.

The central diode houses the CSA and the SF. The CSA is capacitively coupled to the electrode, as shown in Figure 7.3. When a particle hits the pixel, an influence charge is created at the electrode, charging a connected capacity. This leads to a voltage drop at the CSA input. The resulting output signal charges a feedback capacity, which is linearly discharged via a transistor acting as a resistor (VNFB).

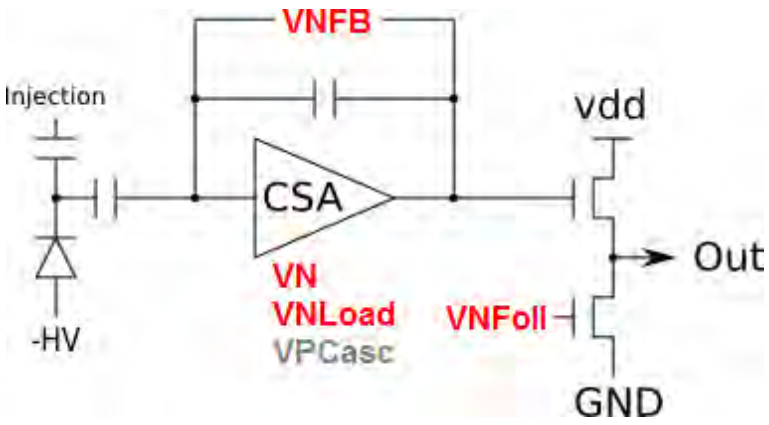


Figure 7.3.: Schematic of the in-pixel CSA and SF [21].

For test purposes the chip also provides the possibility of using so-called injection pulses as signal sources instead of traversing particles. These tunable pulses are generated using a capacity built of a metal layer and the n-well at the central diode. Applying a voltage to the capacity leads to a collection of electrons on the n-well side. When the voltage is turned off, the electrons are released and collected by the electrode.

Since the CSA itself is not designed to drive signals through a high capacity line, the SF is needed, which is built of two transistors working as resistors in a voltage divider.

The CSA and SF are steered by five bias voltages. Four of them are provided via chip DACs and one is set externally (VPCasc). VN steers the current provided for the amplifier, VNLoad and VPCasc adjust the amplification, VNFB steers the linear feedback and VNFoll controls the SF. The bias voltages and their effects are also listed in Table 7.2 as an overview.

7.2.3. Digital Part

In the periphery, the SF driven transmission line is capacitively coupled to the input of a second amplifier (see Figure 7.4), which operates in the same manner as the CSA in the analog pixel, albeit with a smaller amplification factor (about a factor of 3, as compared to the first amplifier with ~ 100). The bias voltages, as listed in Table 7.2, fulfill the same functions as in the first case, but can be set separately.

The amplifier output couples capacitively to the so-called baseline (BL), which is set externally, usually to 0.8 V, and is modulated by a signal coming from the amplifier. It directly connects to a comparator that compares the modulated baseline with an externally set threshold voltage (THR). When the modulated BL voltage drops below the set threshold value, the comparator puts out a standardized digital signal. The signal lasts for the duration of the modulated BL

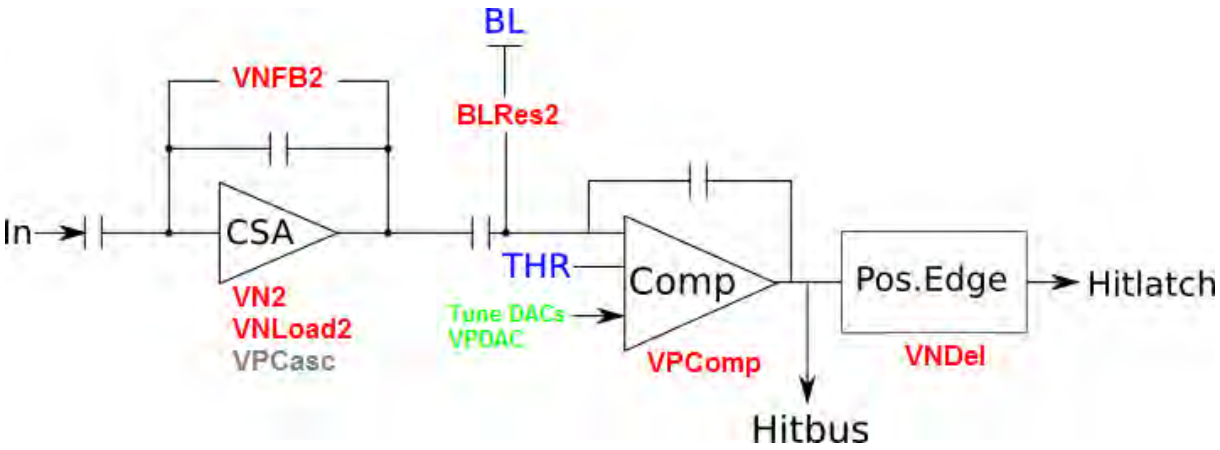


Figure 7.4.: Schematic of the second amplifier and the comparator in the digital part [21].

being below THR. This defines the so-called Time-over-Threshold (ToT)[2]. The THR value can be slightly adjusted for each pixel individually by using a 4 bit tune DAC, which steers an additional current fed into the comparator. This method is used to compensate for pixel-to-pixel variations in the signals coming from inhomogeneities in the production process. The maximum current provided for the tuning is determined by VPDAC.

The comparator performance is controlled by one bias voltage (VPComp) steering the provided current. The restoration of the BL to its original value is steered by a transistor in resistor mode. It is controlled by a further bias voltage called either BLRes in the case of the first four pixel columns with one amplification stage or BLRes2 for the pixels with two amplifiers. Together with the feedback capacitance of the comparator it forms a high pass, which is the main shaping component of the pixel.

For further digital processing of the signal it is only relevant whether Comparator signals were created or not. An edge detector creates a short digital pulse on detecting the rising edges of the direct comparator output and a time delayed duplicate. The delay between the two sets the width of the digital pulse and is controlled by VNDel. Upon detecting these edges, a hit flag is stored in the connected so-called hitlatch. The corresponding timestamp is also stored until the latch is read out. The on-chip state machine controls the readout of all hitlatches, it only needs an externally provided clock signal [43]. Mupix7 is the first iteration to have the state machine integrated on the chip itself. Previous versions required an external state machine provided by an FPGA. A detailed explanation of the state machine and the digital readout can be found in [21] and [44].

For measurements of the comparator signal properties, e.g. pulse shape determination, there is also the possibility of a direct comparator readout via the so-called hitbus (see Figure 7.4).

The following table sums up all bias voltages for the analog and digital pixel electronics, including their sources and properties. Bold typed DACs are the ones that are further analyzed in this thesis, since their variations determine the changes in chip performance in terms of signal quality and power consumption.

[2]In case of the two-stage amplification, the modulated signal is negative with respect to the BL, actually defining a Time-under-Threshold. For historical reasons, however, the term ToT is used.

Bias Voltage	Origin	Component	Function	Effect
VN	DAC	CSA	Current Source	steers current
VNLoad	DAC	CSA	Voltage Divider	adjusts amplification
VPCasc	External			
VNFB	DAC	CSA	Resistor	linear CSA feedback
VNFoll	DAC	SF	Current Source	SF output voltage control
VN2	DAC	2nd Amp	Current Source	steers current
VNLoad2	DAC	2nd Amp	Voltage Divider	adjusts amplification
VPCasc	External			
VNFB2	DAC	2nd Amp	Resistor	linear CSA feedback
VPComp	DAC	Comparator	Current Source	current and speed control
BL	External	Comparator	Baseline	voltage offset for signal at comparator input
THR	External	Comparator	Threshold	comparator reference
BLRes/**BLRes2**	DAC	Comparator	Resistor	Baseline restoration, shaping
VPDAC	DAC	Comparator	Current Source	tuning
VNDel	DAC	Edge Detector		delay

Table 7.2.: MuPix7 bias voltages in the analog and digital pixel parts [21].

7.2.4. Signal Shaping

Signal shaping describes the controlled deformation of an incoming signal using the bandwidth properties of the pixel electronics. Descriptions of the pulse shaping mechanisms of the different MuPix sensors can be found in [21, 43, 45, 46, 47].

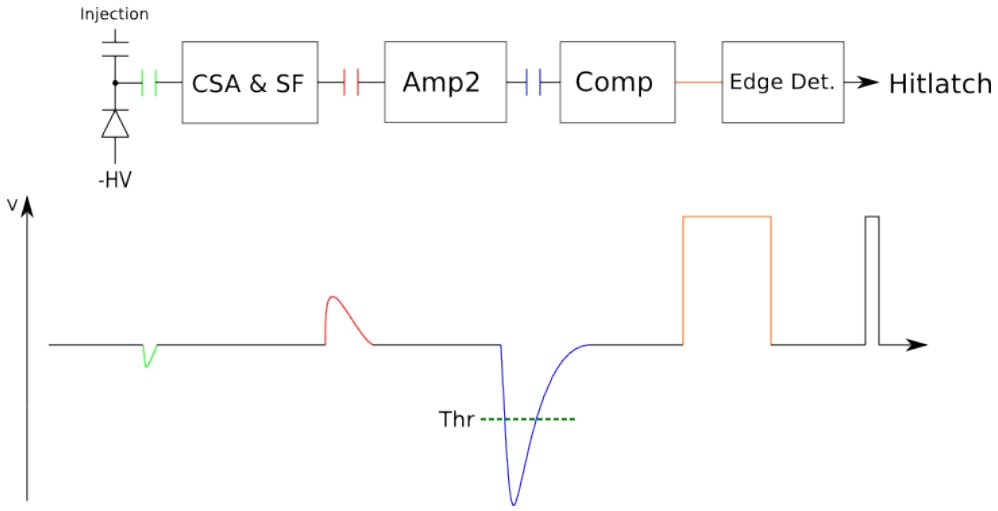


Figure 7.5.: Signal propagation from diode to hitlatch [21].

The MuPix chip only uses high-pass filters as active shaping components [21]. However, due to the intrinsic bandwidths of the filters, the first edge of a signal pulse is not infinitely sharp, as it would be the case for an ideal high-pass filter. The effective shaping can instead be described as a combination of high-pass and low-pass filters acting on the rectangular signal pulse coming from the collection diode in the pixel. Figure 7.5 shows the development of the signal shape from the detection diode to the hitlatch.

Mathematically, the signal shape can be approximated by the convolution of the rectangular pulse with the signal functions for a high-pass filter or differentiator (V_{CR}) and a low-pass filter or integrator (V_{RC}):

$$V_{\text{pulse}}(t) = V_{\text{rect}}(t) * V_{CR}(t) * V_{RC}(t) \tag{7.1}$$

where the solutions for the high-pass and low-pass filters are given by:

$$V_{CR}(t) = V_0 \cdot e^{-t/\tau_{\text{diff}}} \tag{7.2}$$

$$V_{RC}(t) = V_0 \cdot (1 - e^{-t/\tau_{\text{int}}}) \tag{7.3}$$

This gives two solutions for the final signal shape, depending on the time constants τ_i [31]:

$$V_{\text{pulse}}(t) = \begin{cases} V_0 \cdot \frac{\tau_{\text{diff}}}{\tau_{\text{diff}} - \tau_{\text{int}}} \cdot (e^{-t/\tau_{\text{diff}}} - e^{-t/\tau_{\text{int}}}) & \text{if } \tau_{\text{diff}} > \tau_{\text{int}} \\ V_0 \cdot \frac{t}{\tau} \cdot e^{-t/\tau} & \text{if } \tau_{\text{diff}} = \tau_{\text{int}} = \tau \end{cases} \tag{7.4}$$

In Figure 7.6 different pulse shapes for different time constants are depicted.

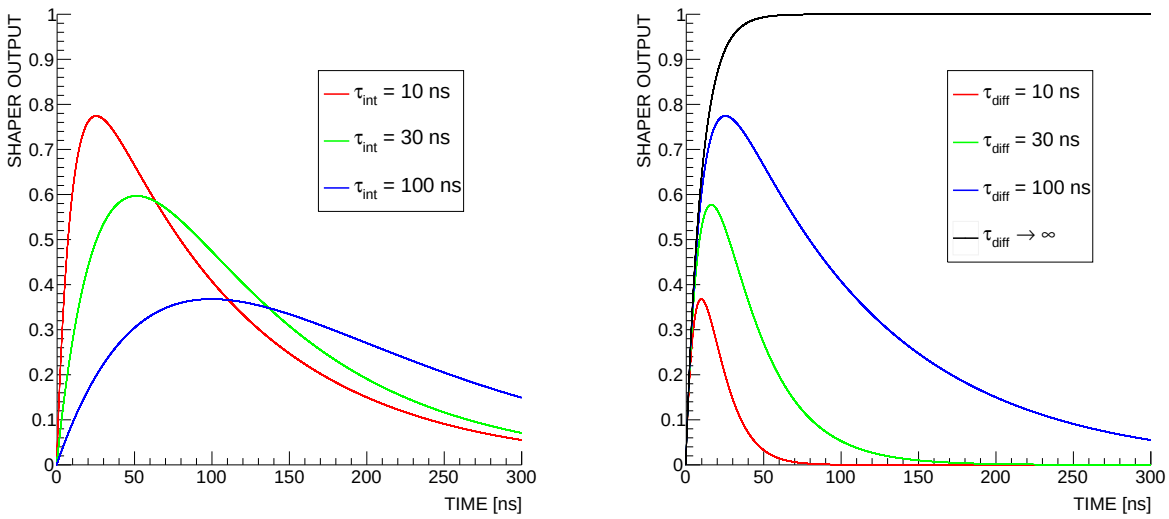


Figure 7.6.: Dependence of the pulse shape on the time constants. Reworked from [31]
Left: $\tau_{\text{diff}} = 100\,\text{ns}$. **Right**: $\tau_{\text{int}} = 10\,\text{ns}$.

The pulse shape described by Equation 7.4, however, is only an approximation that does not take the linear feedback of the amplifiers into account, nor the fact that, in case of the two-stage amplification, the resulting pulse gets shaped a second time, but it can still be used to estimate the effects of the shaping.

8. Single Setup

The Single Setup was developed as a tool to characterize the MuPix chips and test their functions and signal properties. In this thesis it is used to perform variation measurements for the bias voltages of the amplification and comparator stages of the chip. The used setup can be seen in Figure 8.1. In the following, the different hardware components of the setup are described. Furthermore, the software used to control the MuPix sensor is explained.

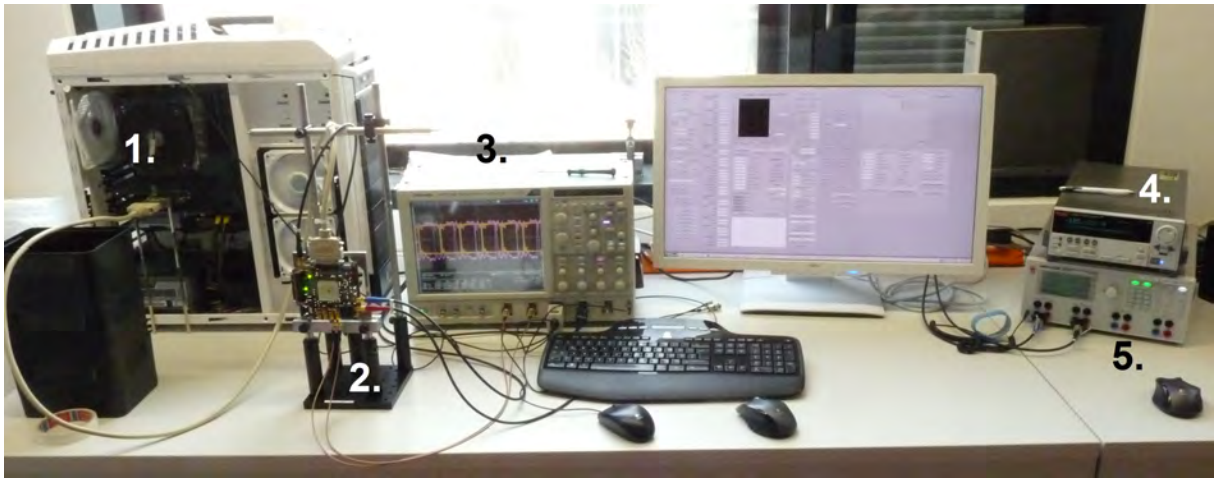


Figure 8.1.: Picture of the Single Setup [43]. From left to right: 1. PC housing an FPGA, 2. MuPix7 on PCB, 3. oscilloscope, 4. Keithley® HV power supply, 5. HAMEG® LV power supply.

8.1. Hardware

A printed circuit board (PCB) houses the chip and provides input and output contacts for the chip. The board is connected to an FPGA that steers the chip control and readout and is in turn connected to a PC.

8.1.1. The PCB

There are two ways to connect the chip to the PCB. It can either be glued and wire bonded directly onto the PCB (see Figure 8.2) or onto a special ceramic carrier that is then plugged and soldered to corresponding sockets in the center of the PCB.

SubMiniature version A (SMA) connectors are used for power supply. The high voltage (HV) of $-85\,\mathrm{V}$ is used to widen the depletion zone to $\sim 15\,\mathrm{nm}$ and provide a fast charge collection. The LVDS supply of $5\,\mathrm{V}$ is converted to $3.3\,\mathrm{V}$ on the PCB and used to generate the differential output signals, which enable a fast and stable long range transmission. The $5\,\mathrm{V}$ low voltage (LV) is again converted to $3.3\,\mathrm{V}$, as well as $1.8\,\mathrm{V}$ and $1.5\,\mathrm{V}$. The latter two are used as bias

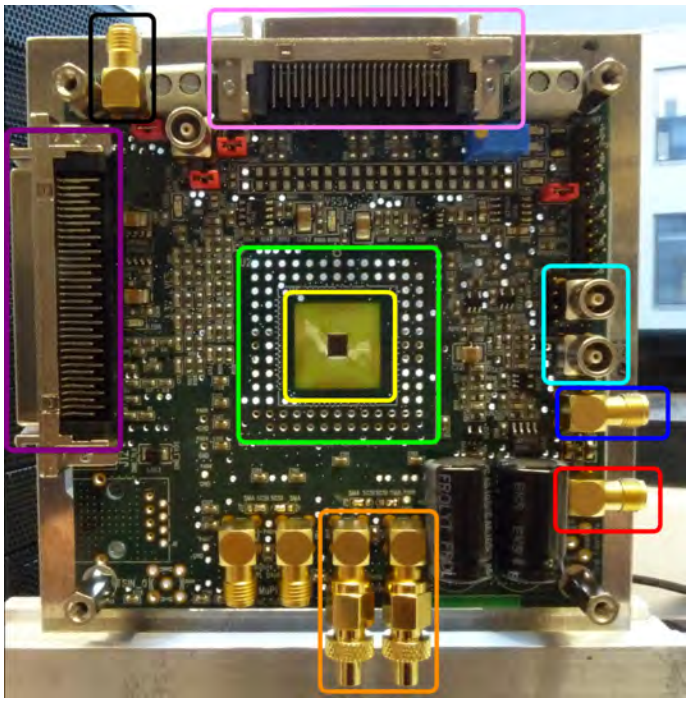


Figure 8.2.: MuPix7 PCB [43]. **Red**: HV SMA. **Blue**: LV SMA. **Black**: LVDS SMA. **Yellow**: Wire bonded MuPix7. **Green**: Carrier sockets. **Cyan**: Injection tap connections (LEMO®). **Pink**: Chip control and digital readout (connection to FPGA). **Purple**: Hitbus readout (connection to FPGA). **Orange**: Clock output.

voltages for the chip components while 3.3 V power DACs on the board, which are used to set the comparator threshold for the chip and to generate injection pulses to simulate hits on the chip. The PCB contains two LEMO® connectors where the injection signals can be tapped to analyze their properties.

For the measurements with the Single Setup, PCB 7714 is used, which carries 64 µm thin chip, glued directly to the PCB, which is itself thinned to 100 µm in this region.

8.1.2. The FPGA

Field Programmable Gate Arrays were first developed in the 1980s when the realization of more and more complex logic systems as Application Specific Integrated Circuits (ASIC) became too time consuming and cost intensive. FPGAs consist of thousands of basic logic gates that can be connected by programmable switches to perform complex operations. This gives FPGAs high application flexibility and enables time efficient programming and debugging.

The FPGA used to steer and readout the MuPix7 is implemented on a Stratix IV Development Kit [48], which is directly plugged into a computer's Peripheral Component Interconnect Express (PCI-E) slot. It provides two High Speed Mezzanine Card (HSMC) connections, one for digital data and chip control and the other one for the hitbus readout. The connection from PCB to FPGA occurs via Small Computer System Interface II (SCSI) cables and specially designed SCSI-to-HSMC adapter cards.

8.1.3. The Trigger System

The adapter cards also provide trigger inputs via LEMO® connectors for synchronization with external signal sources, which are used to measure the time behavior of the chip. The reference system for the Single Setup consists of a scintillating tile connected to a SiPM, similar to the

components of the tile detector for the Mu3e experiment setup. They are produced and provided by the Kirchhoff Institute for Physics (KIP) and ensure precise time measurements with a resolution of <1 ns.

The SiPM output signals are discriminated and the resulting uniform digital pulses are used as trigger input for the FPGA.

For the purposes of this thesis, the trigger setup is used for coincidence measurements. They are used to make efficiency predictions for MuPix chips outside of testbeam measurements (see Chapter 9).

8.2. Software

8.2.1. The FPGA Firmware

The firmware enables data configuration and readout from the FPGA via registers. A driver has been developed to ensure the communication between FPGA and computer and map the data to the computer's Random Access Memory (RAM) [49].

The firmware provides the following features:

- Setting the values for the PCB-side DACs that control the comparator threshold voltage and the injection pulses.
- Filling the chip's shift registers and loading them into RAM cells to control the chip DACs.
- Controlling the readout of the chip hit data.
- Sampling of the trigger and hitbus signals with 500 MHz. The information on the ToT from the hitbus signal is filled into histograms with 8 ns bin size.
- Providing a reference clock with an adjustable frequency of typically 125 MHz for the on-chip clock controlling the state machine.

8.2.2. The GUI

The Graphical User Interface (GUI) is used to configure the MuPix and to measure its properties. It is written in C++ and uses the Qt- and boost-libraries [50, 51]. A screenshot of the GUI main window can be found in Appendix A.

The main window provides interfaces to set the different chip and PCB components, like individual chip DACs, injection pulse properties, global comparator threshold (THR), and tune DAC values.

It also provides a continuous readout for longtime data taking with constant settings or automated scans over variable threshold regions. In additional windows different correlation plot can be shown for the purposes of online monitoring.

8.2.3. Data & Readout

With the Single Setup three types of data can be obtained: Hit data, containing hit position and time, triggers, and the hitbus signal. The data are stored in blocks in the FPGA memory. The structure and content of such blocks are described in [21].

The data blocks are pulled from the FPGA and stored in three queues via a readout thread. A second thread, the so-called framepacker, reads out the queues in small slices, called frames. Each frame consists of the hit data of one readout cycle of the chip and all triggers and hitbus information seen up to the hit data timestamp. Depending on the amount of hit data that needs

to be read out, the length of such a frame varies, but is usually in the order of 200 ns. The frames are then stored on the computer in raw data files of sizes up to 500 MB for later evaluation.

Additionally, the frames are also sent to a further thread, which evaluates them in real time and visualizes important data correlations for the purpose of online monitoring.

9. Setup for Lab-Determined Efficiencies

9.1. Motivation

The efficiencies of the MuPix sensors are usually determined at testbeam campaigns. Since these campaigns are conducted infrequently and access time is very limited, a method was developed to measure quantities comparable to actual efficiencies in a small lab setup. So, predictions about the efficiency behavior of the chip can be made without testbeam access. This method might be used to give immediate feedback of how, for example, certain changes in the basic chip settings may influence its efficiency and therefore could facilitate the planning and conducting of future testbeam campaigns, especially for new pixel chips.

9.2. Working Principle

The efficiency, as determined at testbeams, is a measure of how many particle hits are registered by the MuPix chip, compared to the total number of particles passing through it, which is determined by using several planes of sensors to reconstruct tracks (see Chapter 12).

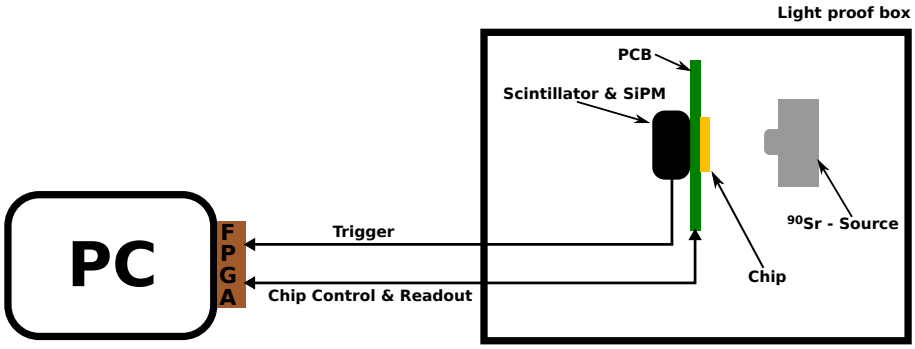


Figure 9.1.: Schematic setup to measure lab-efficiencies.

In the lab setup (Figure 9.1), only one sensor plane is used. In order to calculate an efficiency-like quantity, coincidences between the sensor and a trigger system are measured. A scintillating tile is positioned at the backside of the PCB and fixed using adhesive tape. The signal source available in the lab setup is a strontium-90 (^{90}Sr) source.

Strontium-90 decays to yttrium-90 via β-decay, which in turn decays to zirconium-90. The maximum energies of the emitted electrons are 0.55 MeV and 2.28 MeV, respectively [52]. Because the source is sealed with a metal layer, the electrons from the strontium decay are absorbed. Only the latter leave the container and can be observed. Due to their low energies, the electrons are subject to very strong multiple Coulomb scattering, which makes the use of several MuPix layers for the lab-efficiency setup impossible.

The ^{90}Sr is placed as close as possible to the chip such that the entire chip is illuminated. The alignment of chip, scintillator, and source can be tested using the online monitoring function of the GUI with a window showing the pixel matrix and the number of hits per pixel that correlate to a seen trigger. Ideally, this map should show a uniform distribution of hits. Correlation plots for the two chips used in this setup can be found in Appendix F.

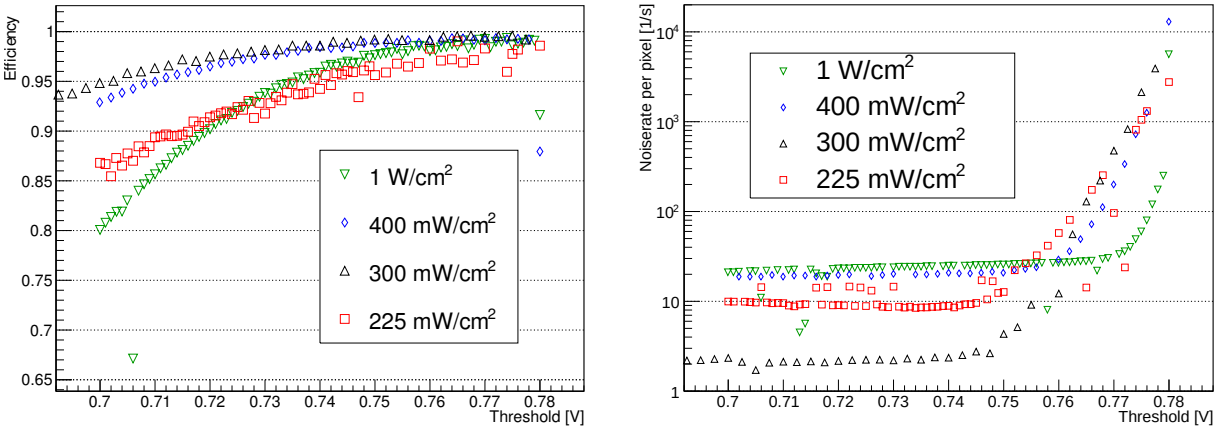
For the measurement, an automatic scan over a certain threshold range is performed in which hit and trigger data are taken and stored in raw data files, as described in Section 8.2.3. The analysis of the data and the determination of the lab-efficiencies can be found in Chapter 13.

Part III.

MEASUREMENTS

10. Power Consumption and Dependence on DAC Settings

Previous measurements showed a strong dependence of the efficiency of the MuPix chips on the chosen DAC settings [53]. Figure 10.1 shows the efficiencies for four settings with different power consumptions. The names of the different DAC settings reference their power consumption properties. The High Power (HP) settings are the standard DAC settings with which the MuPix7 and its predecessor, the MuPix6, were first operated. In [21] their power consumption was estimated to be $\sim$1000 mW/cm^2. In a first approach of optimizing the power consumption the Low Power (LP) settings with a power consumption of $\sim$225 mW/cm^2 were determined. The two intermediate DAC settings labeled as Medium Power (MP) settings and Low-Medium Power (LMP) settings were determined making extrapolations from the HP and LP settings. For the MP settings, the three main power DACs of the amplifiers and comparator (VN, VN2, VPComp) were reduced to one half of their HP value, while all other DACs were kept the same. The LMP settings decreased these three DAC values even further. The remaining DACs were set to values between the HP and LP settings. The different power settings are summed up in Table 10.1 for comparison.



(a) Efficiencies.

(b) Noise rates.

Figure 10.1.: Efficiency and noise curves for different DAC settings and power consumptions (measured with tuned sensors at PSI, 2015) [53].

As a 2015 PSI testbeam campaign showed, the MP and LMP settings give the highest efficiencies with more than 95 % over a threshold region twice as wide as the HP and LP settings (Figure 10.1a). Furthermore, the measured pixel noise rate for the LMP settings is the lowest for all the settings up to a threshold voltage of 0.76 V(Figure 10.1b). The power consumptions of the MP and LMP settings were determined to $\sim$400 mW/cm^2 and $\sim$300 mW/cm^2, respectively, which means they are directly at or slightly below the power limit of the helium cooling system for the Mu3e experiment.

Therefore, this thesis aims to find improved DAC settings, which reduce the power consumption in order to have a larger safety margin for the cooling, while simultaneously keeping the good performance of the LMP settings.

DAC [dec]	Setting			
	HP	MP	LMP	LP
VN	60	30	20	5
VNLoad	5	5	4	2
VNFB	10	10	8	3
VNFoll	10	10	10	10
VN2	60	30	20	5
VNLoad2	5	5	4	2
VNFB2	10	10	8	3
BLRes2	10	10	10	10
VPComp	60	30	20	10
approx. power consumption [mW/cm^2]:	1000	400	300	225

Table 10.1.: DAC values for the four power settings of the MuPix7.

11. DAC Optimization

11.1. Measured Quantities

In order to determine the sensor performance and the change in power consumption four basic quantities are measured for all variations of the DAC bias voltages: time-over-threshold (ToT), latency, signal-to-noise ratio, and the change in current drawn by the chip. As a signal source injections with a rate of 500 Hz per pixel and an amplitude of 0.5 V are used. This amplitude is chosen, because in previous measurements [46] comparisons between the ToT spectra of an iron-55 (^{55}Fe) X-ray source, which is commonly used as a signal source for lab measurements, and the injection pulses have shown a match at an injection voltage of 0.4 V to 0.5 V. However, an exact calibration is not possible, due to pixel-to-pixel variations. The advantage of using injections for the following measurements is the much higher rate compared to ^{55}Fe, which allows for detailed measurements in a feasible time frame.

11.1.1. Time-over-Threshold (ToT)

The ToT is the time interval during which the pulse height exceeds the threshold voltage for the comparator (see Figure 11.1), which has been set to 0.65 V for these measurements. Since a pixel is insensitive to further hits during that time, large ToTs should be avoided, in order to keep the dead time of the sensor as low as possible. The ToT is measured using an oscilloscope. A probe is used to tap the hitbus signal at the corresponding chip carrier socket connection on the PCB. The mean value and standard deviation for the ToT are calculated automatically by averaging over 5000 measurements.

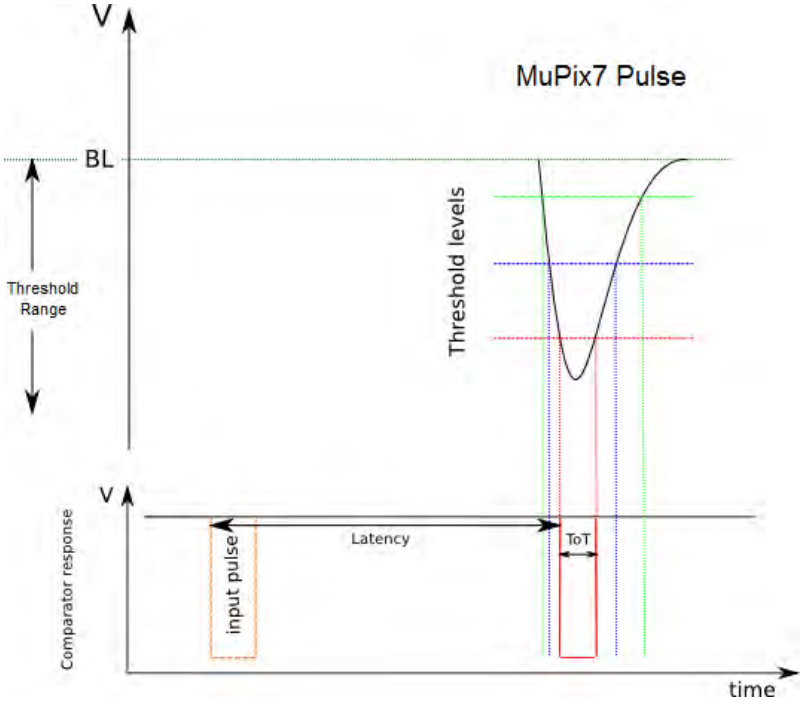


Figure 11.1.: MuPix7 pulse shape and definition of ToT and latency.

Due to variations in the injection charge, as well as signal smearing due to noise, the measured ToTs vary greatly, with uncertainties in the order of ∼10 %. Measuring the ToT, together with the latency, can be used to describe the pulse shape and width but can also give indirect information about the pulse height, since the ToT increases with the pulse height. The pules shape, as explained in Section 7.2.4, can be approximately described by a high-pass and a low-pass contribution, with the former dominating the ToT. For the exponential signal decline ($V_0 \propto e^{-t/\tau_{\text{diff}}}$) this gives a logarithmic dependence of the ToT on the pulse height. Because the ToT information of the MuPix7 is received from the hitbus, it is only possible to determine it for one pixel at a time. The standard pixel for the hitbus readout is positioned in the center of the pixel matrix.

11.1.2. Latency

The latency is defined as the time difference between an initial signal and the comparator response, so it describes the time a pixel needs to react to an input signal, depending on the threshold. Using LEMO® connectors on the PCB, the injection pulses can be tapped and viewed on an oscilloscope. As seen in Figure 7.5 the injection signal is negative. Since the amplified pulse at the comparator input is negative in relation to the baseline (see Figure 11.1), the latency is determined by measuring the delay between the falling edges of the injection signal and the hitbus signal with the oscilloscope. In order to have a fast chip response, the goal is to keep the latency as small as possible.

11.1.3. Signal-to-Noise Ratio

The signal-to-noise ratio (SNR) is a measure how well a signal pulse can be separated from the background noise of the electronics. It is determined by performing a threshold scan, which measures the number of registered hits compared to the number of injections in a given time window at different threshold voltages. For this scan the digital hit information is used, which makes it possible to perform it for all pixels at once.

The measurement can be interpreted as a Bernoulli experiment, which then gives a binomial description of the measurement, where a hit was either registered or not. For a large number of injection pulses n the number of registered hits k approaches the expectation value given by $\mu_{bin} = n \cdot p$. This yields the hit probability $p \approx \frac{k}{n}$ and therefore, the standard deviation for each measurement point is[3]:

$$\sigma_{bin} = \sqrt{n \cdot p \cdot (1-p)} \approx \sqrt{k \cdot (1 - k/n)} \tag{11.1}$$

In an ideal pixel the comparator response is always the same for an invariant input signal. Therefore, the comparator response would be given by a step function with its step at the threshold value corresponding to the input pulse maximum. However, in a real pixel the step function is smeared out due to noise, giving it the form of an S-curve (Figure 11.2).

The S-curve is described by a Gaussian error function of the form:

$$f(x) = \frac{A}{2}\left(1 + \text{erf}\left(\frac{x-\mu}{\sqrt{2}\cdot\sigma}\right)\right) \tag{11.2}$$

where the expectation value μ gives the threshold voltage at which 50 % of the hits are recognized. The absolute value of the difference between this parameter μ and the fix baseline voltage b of 0.8 V can be interpreted as the average signal pulse height. The standard deviation σ

[3]Note that μ_{bin} and σ_{bin} describe the expectation value and standard deviation of a binomial distribution. They are not to be confused with the similarly labeled fit parameters μ and σ of Equation 11.2

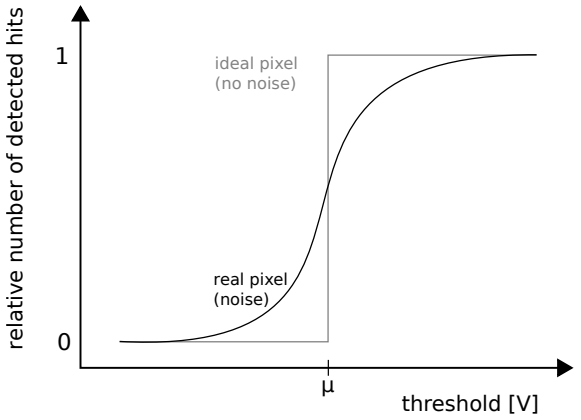


Figure 11.2.: Comparator output of a threshold scan for an ideal and a real pixel. Adapted from [43]

is a measure for the noise, and A is the total number of injections in the time interval. If the number of injections is fixed, the number of registered events can be normalized and A is set to 1. The SNR is determined from the pulse height and the noise:

$$SNR = \frac{|\mu - b|}{\sigma} \tag{11.3}$$

In order to be consistent with the latency and ToT measurements, the SNR is calculated for the same pixel (hitbus pixel). Using the hit information of all pixels together, there is also the possibility to calculate a global SNR for the entire chip. Due to pixel-to-pixel variations that broaden the S-curve, this SNR is usually much smaller than for a single pixel. Additionally, an average SNR can be calculated from all single pixel SNRs. This gives the possibility to determine how the SNR of the chosen hitbus pixel behaves compared to the average (see Section 11.2.1).

11.1.4. Change in Power Consumption

The low voltage power supply displays the current drawn by chip and PCB and varies for different DAC settings. The difference in power consumption per area for each DAC setting can be estimated by the change in drawn LV-current and the supply voltage.

$$\Delta P_{\text{per area}} = \frac{V_{\text{supply}} \cdot \Delta I_{\text{LV}}}{A_{\text{active}}} \tag{11.4}$$

The active area A_{active} for the MuPix7 contains all power consuming parts in the analog pixel and the periphery. It is similar to that of the MuPix6, which has been measured to be $13\,\text{mm}^2$ in [21]. For the MuPix7 there is additional power consumed by the on-chip state machine and the LVDS drivers, but their power consumption is not affected by changing the DACs for the electronics in the pixel and the periphery. Measurements of the power consumption done in [21], as well as the circuit schematics (e.g. Figure 11.3 for the first amplifier) show that the supply voltage for all DACs except VN is given by 1.8 V, and 1.5 V for VN. The uncertainties on the power consumption are calculated from the uncertainty of the measured current, given by the accuracy of the low voltage supply, which is typically 0.5 mA for low currents (<500 mA) according to the manual [54]. The change in power consumption shown in the following measurement plots always denotes a change relative to the power consumption of the LMP settings.

11.2. First Variations of DAC Values for the CSA

The two amplification stages and the comparator are all coupled capacitively. Therefore, one can expect that changing the DAC settings in one stage has no significant effect on the settings of the other stages. This makes it possible to analyze the stages separately. However, the components within each stage form a highly interconnected system where variations of one component easily influence the performance and shift the working point of the other parts. Figure 11.3 shows the circuit layout of the first amplifier stage, including the source follower. The response from each component is non-linear, making it very difficult to predict the behavior of the system for changing a DAC value. To find an optimum, it would make sense to go through all DAC settings step by step and analyze the effects of the changes. However, every DAC can take 64 values (6 bits), resulting in a total number of $64^9 = \mathcal{O}\left(10^{16}\right)$ of possible DAC settings for the nine analyzed DACs of the two amplifiers and the comparator. Checking all possible settings is therefore an unfeasible task.

As mentioned before, the LMP settings already provide a reasonable starting point due to their excellent performance. In the following measurements the effects of small variations of the DAC values around the LMP settings were analyzed.

In a first approach only the DACs of the first amplifier are varied, in order to test the setup and find possible error sources.

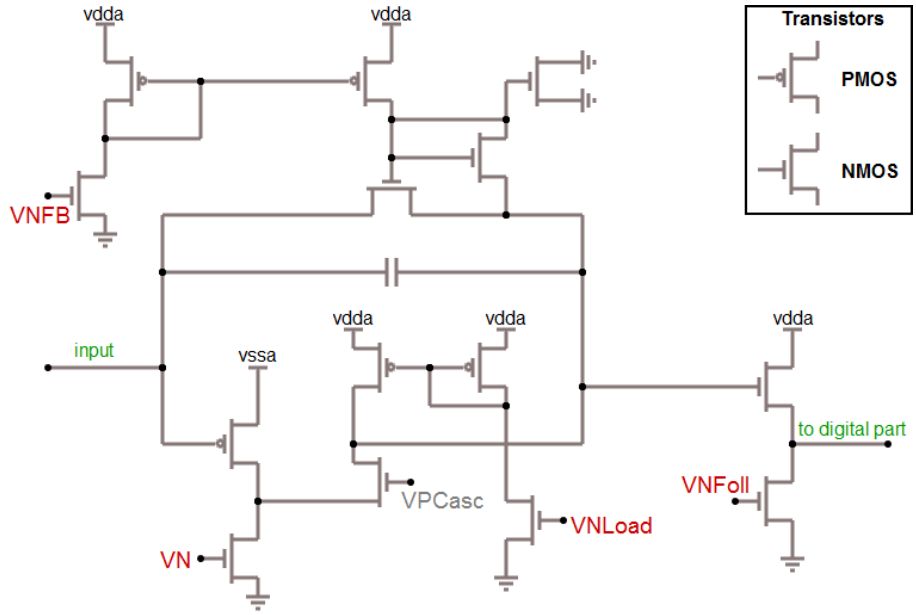


Figure 11.3.: Circuit schematic of CSA and Source Follower. The adjustable DACs are shown in red. VSSA and VDDA denote the supply voltages of 1.5 V and 1.8 V, respectively.

11.2.1. Measurement Approach

Starting from the LMP settings, the DAC values are varied in a ±3 region. This number is chosen a priori to keep the time consumption of the measurements in an acceptable range. The most important quantities analyzed in these measurements are the signal-to-noise ratio and the power consumption. As primary measure for the signal quality, the SNR should not decrease or if possible even be improved. The main goal is to decrease power consumption as far as possible. However, in some cases this means finding a compromise between the lower power consumption and an acceptable SNR. Also the latency and ToT should be considered concerning the performance of the pixel in terms of speed and pulse shape.

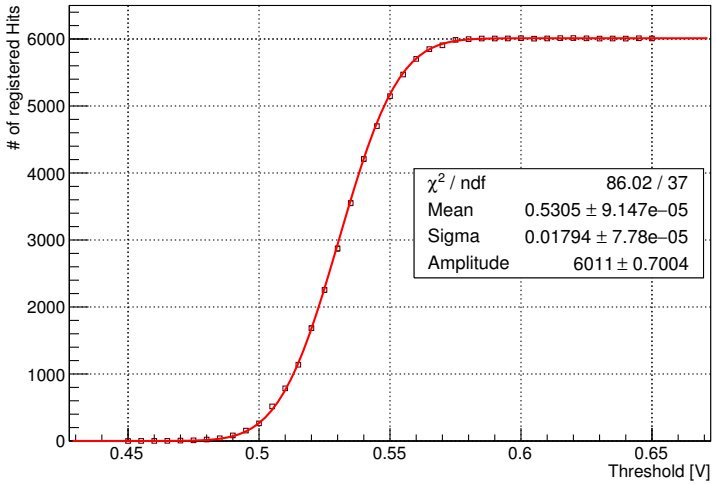


Figure 11.4.: S-curve fit of a threshold scan for a single pixel using LMP settings.

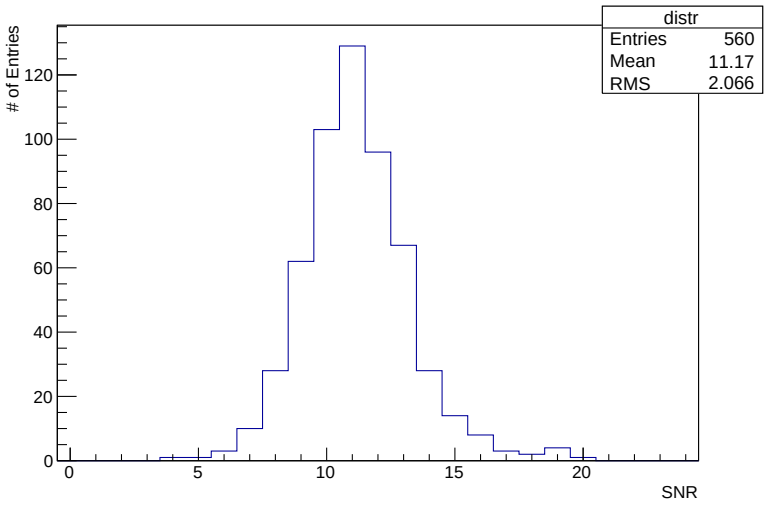


Figure 11.5.: Distribution of SNRs for the used chip.[4]

The variations are performed for one DAC at a time, while keeping the other three DACs fixed. For each new DAC value the ToT and latency are measured for the standard hitbus pixel as described above, simultaneously the change in the current drawn by the chip is taken from the LV-source display and used to calculate the change in power consumption as described in Equation 11.4. After that a threshold scan is performed and evaluated to determine the position of the pulse maximum and the noise of the pixel. The time intervals of the scan are 12 seconds, resulting in ∼6000 injections per voltage step. Figure 11.4 shows an example of an S-curve resulting from a threshold scan and an error function fit that determines the values for μ and σ, giving an SNR of 15.02 ± 0.06 for this single pixel on the untuned sensor with LMP settings at room temperature. In the distribution of all pixel SNRs (see Figure 11.5) it can be seen that the average pixel SNR for the chip is around a value of 11, meaning that the chosen pixel has a slightly higher performance. Once all variation measurements for one DAC have been performed, the results are compared. All optimization measurements are conducted with PCB 7714, which is also used for the testbeam measurements in the next chapter.

[4]For these measurements the injections were only set for half the pixel matrix, hence there are only ∼500 entries.

11.2.2. First Results

The first results of the DAC variations showed the non-linearity of the system. The effects of the variation of the individual DAC values on the chip performance can be seen in Figure 11.6 using the example of VNLoad. Plots for the other DACs of the first amplifier can be found in Appendix C. The center value on the x-axes in the following plots denotes the LMP value for the respective DAC.

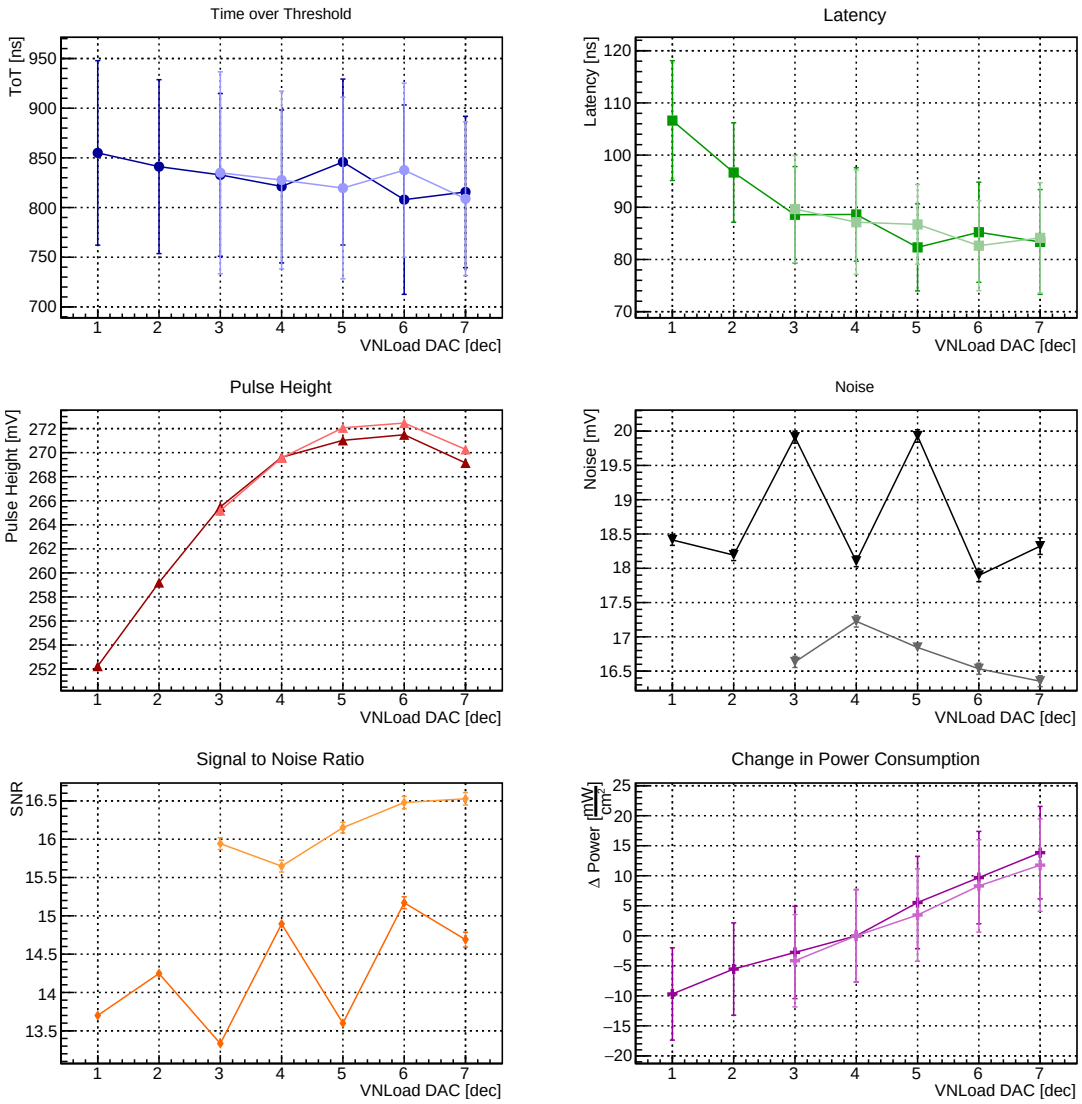


Figure 11.6.: Variation of VNLoad and its effect on ToT, latency, pulse height, SNR, and power consumption. Lighter colors indicate remeasured points in the darkened lab.

A decrease in ToT and especially latency can be observed with higher VNLoad values, as well as a local maximum in pulse height for VNLoad = 6, indicating that the chosen DAC variation region of ±3 is already sufficient to observe important changes and find maxima or minima in the signal and performance behaviors for the individual DACs.

It can be seen that the change in SNR is significantly more influenced by the change in noise than in the pulse height. The noise variations from point to point are very large, resulting in a series of dips and peaks. This may very well be due to the fact that the points have been measured at different times of day, resulting in different light conditions in the lab.

Observations of the current drawn from the HV source have shown that it is very sensitive to changes in ambient light. With increased light levels, the chip draws more current from the HV source, at some point reaching the current limit of 50 µA, resulting in a drop of the high voltage. This effect coincides with the sun shining through the window, illuminating the chip directly through the thinned backside of the PCB, making the chip essentially act like a photodiode.

New measurements with the lab window blinds closed result in a reduction in the point-to-point variations, as well as the overall noise level as seen in the case of VNLoad and VNFB in Figures 11.6 and C.2, respectively. This indicates that, for further detailed measurements, an improvement of the setup is needed to shield the chip from the influences of the ambient light level.

11.3. Setup Improvement

11.3.1. Light Protection

In order to reduce the noise fluctuations created by the ambient light, the setup is placed inside a cardboard box wrapped in light-tight fabric. This already reduces the noise level, resulting in an SNR of 16.43 ± 0.07 for the same settings as before.

In addition, the chip is tuned to the new environment. Tuning provides the possibility to individually adjust the threshold of each pixel to compensate for pixel-to-pixel variations.

11.3.2. Tuning Method

As described in Section 7.2.3 and illustrated in Figure 7.4, the TDACs steer a small current that flows into the comparator to achieve a shift in the threshold. That way, the response of all pixels can be made more uniform. The current provided for the TDACs is limited by the value of VPDAC. The value for VPDAC should be low, because it significantly contributes to the overall power consumption of the chip. For optimal tuning the distribution of the individual TDAC values shows a Gaussian form. Several methods to find the optimal tuning setting are implemented in the setup software. The one used for the tuning of this chip is the MuPix7 Tuning. The method works as follows:

First, the maximum acceptable noise rate for each pixel (usually 1 Hz, i.e. one registered hit per second in absence of an input signal) is chosen, all TDACs are set to zero, and VPDAC is set to a starting value (usually 10). Then, the threshold is increased step by step until a pixel exceeds the noise limit. The TDAC for this pixel is then set to the maximum value (15). If the noise rate is still higher than the goal noise rate VPDAC gets increased by one until the noise level is again below the limit. The threshold increase continues and the method of setting TDACs and VPDAC is repeated until all TDACs are set to 15. The threshold voltage and VPDAC value at the end of the procedure are stored, setting the maximum current (i.e. the current necessary to ensure a noise rate below the set limit for all pixel) for the TDACS.

After that, all TDACs are set to zero again and VPDAC is set to the stored goal value. Then a second scan is performed where the threshold is again increased until a pixel exceeds the noise limit. In this case the TDAC value is increased by one until the noise is below the limit again. This is repeated until the saved goal threshold voltage is reached. At this threshold all pixels should have a noise rate equal to or less than the set goal noise rate.

Additionally, a fine adjustment (FA) to the tuning can be performed, where overtuned pixels are recovered. The number of noise hits in each pixel is measured for a longer time and if the resulting noise rate is smaller than 10 % of the allowed noise rate the TDAC gets reduced by one. This adjustment ensures the pixels to be more sensitive to hits, but comes at the cost of a higher noise rate for the pixel.

Further explanations to the tuning methods and the linearity between VPDAC and TDAC values can be found in [21] and [46].

11.3.3. Effects of the Tuning on the Setup

Noise Reduction

By tuning the chip, an improvement of the SNR is achieved. As seen in Figure 11.7 (blue curve) the noise determined after the tuning is lower than before. A possible explanation for this reduction in noise may be that the tuning leads to a more stable working point for the comparator. This hypothesis is, however, still under investigation.

The SNR measured with this reduced noise level is estimated to be 19.20 ± 0.09 according to the measured mean and sigma values shown in Figure 11.7. This estimation, however, does not take the shift of the threshold level during the tuning into account.

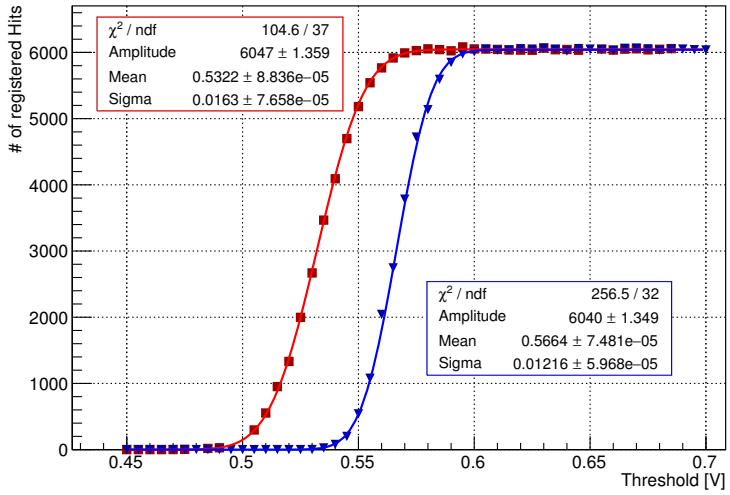


Figure 11.7.: Threshold scan and S-curves for a single pixel in darkened setup for untuned (red) and tuned (blue) chip, both with LMP settings.

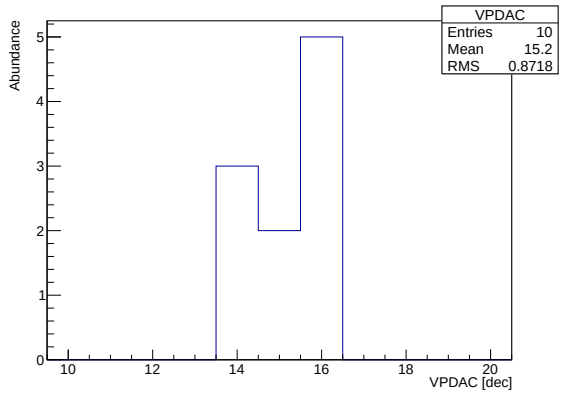
Baseline Shift

The threshold scans before and after the tuning show that because of the readjustment of the comparator threshold the mean value has shifted towards a higher voltage. However, in the software the threshold value is still set globally for all pixels via the Board DAC settings (see Figure A.1). In order to account for the shift in the calculation of pulse heights and SNRs, one can instead assume an effective baseline shift by the same amount. Assuming that the tuning only shifts the baseline but keeps the absolute pulse height h, one can equate the pulse heights before and after the tuning:

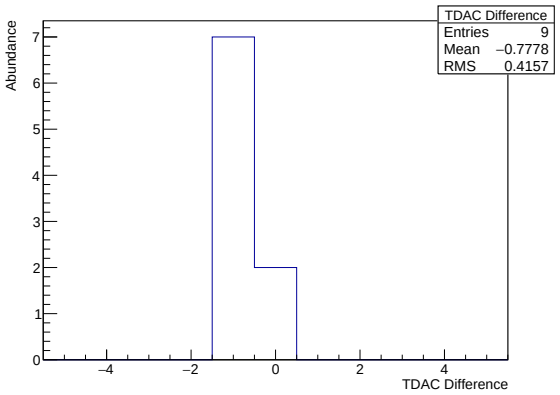
$$h_{\text{before}} = b_{\text{before}} - \mu_{\text{before}} = b_{\text{after}} - \mu_{\text{after}} = h_{\text{after}} \tag{11.5}$$

with the baseline voltage denoted by b and the pulse maximum by μ.

By performing two threshold scans for the same DAC settings, one before and one after the tuning, and fitting them with error functions, the effective baseline shift can be calculated from the shift in the determined mean value. The new baseline then is:



(a) VPDAC values for the tunings at LMP settings and nine new DAC settings.



(b) TDAC differences between LMP settings and new settings for the analyzed hitbus pixel.

Figure 11.8.: VPDAC and TDAC differences for the tested settings.

$$b_{\text{after}} = b_{\text{before}} - \mu_{\text{before}} + \mu_{\text{after}} \tag{11.6}$$

For the two threshold scans in Figure 11.7, this results in $b_{\text{after}} = 834.29\,\text{mV}$ for this pixel. The SNR for the adjusted baseline is then 22.02 ± 0.10.

All following measurements are performed with a tuned sensor. The SNR is always estimated using the standard baseline of 0.8 V. This will give a lower limit for the SNR, understanding that, when accounting for a tuning shift, the actual SNR will be higher. In order for the SNRs of the different new settings to be comparable, this shift should be the same for all settings. Different DAC settings may have an effect on the tuning and therefore the shift in baseline voltage. However, comparing the tune DAC distributions for the new settings show that the TDAC values of the observed hitbus pixel vary at most by one step (see Figure 11.8b). Most tunings result in a VPDAC value of 16 (Figure 11.8a), enabling an effective baseline shift of up to 70 mV. The voltage shift per TDAC step for this VPDAC value is about 4 mV [21]. For VPDAC values below 16 the resulting voltage shift per TDAC step is even lower. This means that any variation in the baseline shift due to different settings is smaller than the voltage resolution of the performed threshold scans, which is 5 mV. Therefore, the resulting offset in the baseline voltage can be viewed as independent of the settings and the standard baseline voltage can be used for all SNR estimates. In Appendix B an examples of TDAC differences between the LMP settings and two of the new settings can be found, illustrating the entire pixel map.

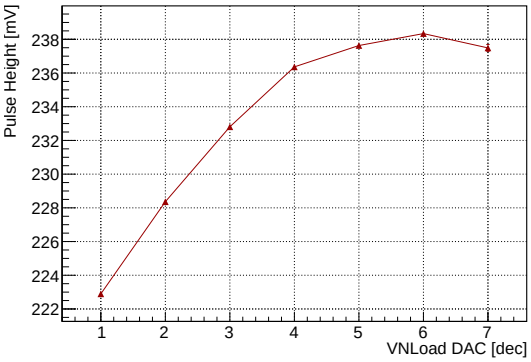
11.4. Determination of New DAC Settings

Once the setup has been put inside the light tight box and the chip has been tuned, new variation measurements are performed to optimize the DAC settings for the MuPix7 chip. This time the behavior of all three stages is analyzed and new DAC settings are derived from these results. The optimization aims to reduce the power consumption of the chip without influencing the signal quality too much. Additionally, settings are analyzed that allow for slight increases in energy consumption, but are useful to increase the performance of the chip. In the end nine new settings are identified that are then further characterized at the PSI testbeam. In the following, the optimization procedure for the DACs is described and the results are briefly discussed. The most notable changes in signal behavior and power consumption for the DAC values are shown below. An overview of all changes can be found in Appendix D.

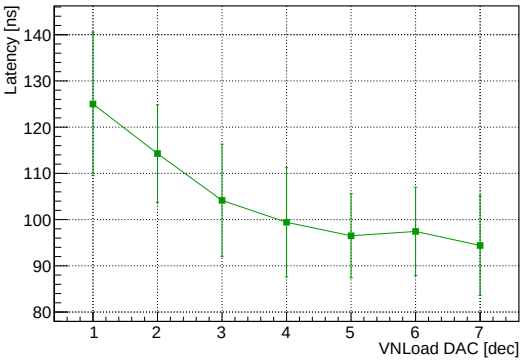
11.4.1. DAC Optimization and Signal Behavior

The measurements start with the first amplifier. VN acts as the amplifiers main current source. Therefore, changing VN leads to a change in power consumption. This change correlates linearly to the DAC value with a ΔP of 5 mW/cm^2 per DAC step (Fig. D.1). For higher VN the noise decreases, leading to an improved SNR. Conversely, for lower VN the SNR decreases due to a rise in noise. The changes in pulse height occur in the same directions but the change in SNR is dominated by the change in noise. The range of the pulse height variation is in the order of ± 0.5 %, whereas the noise variation range is ± 3 %.

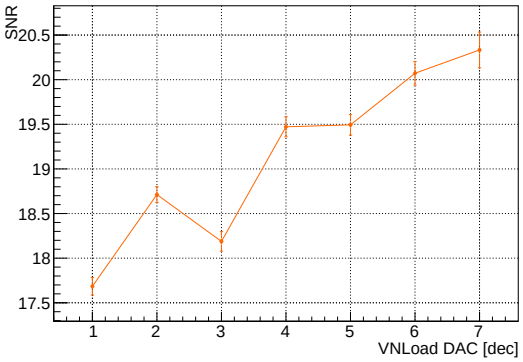
VNLoad shows a maximum in pulse height for an increased value of VNLoad = 6, as seen in Figure 11.9a. The decrease in noise leads to an improvement in SNR of >20 for this setting, which makes it a candidate for signal quality improvement (Fig 11.9c). Also, increasing VNLoad gives a slightly smaller latency, while decreasing VNLoad leads to strong rise (Fig. 11.9b). The power consumption again correlates linearly to VNLoad by approximately 4 mW/cm^2 per DAC value (Fig. D.2).



(a) Pulse height.



(b) Latency.

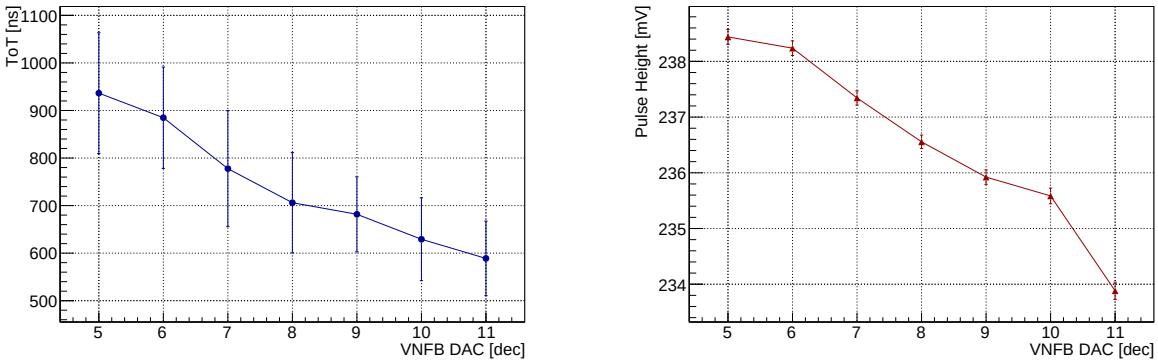


(c) Signal-to-noise ratio.

Figure 11.9.: Variation of VNLoad.

A decrease of VNFB improves pulse height and SNR while not drawing any more current, making this DAC the ideal candidate for signal improvements without increasing power consumption (Figure D.3). The cost of the improved the SNR, however, is a strong increase in ToT (Fig. 11.10a). This illustrates the shaping properties of VNFB.

Higher values for VNFoll do not show significant improvements of the SNR. However, at a value of VNFoll = 7 there is a very steep drop in the noise level leading to an increase in SNR (Figure D.4). Combined with the reduction of power consumption by 7 mW/cm^2, this value is



(a) Time over threshold.

(b) Pulse height.

Figure 11.10.: Variation of VNFB.

also considered for new power settings. There is the tendency of a slight increase in latency of <5 ns.

One would expect a similar behavior when changing the DACs in the second stage, VN2, VNLoad2, VNFB2, since they fulfill the same functions for this amplifier as their counterparts do for the first one.

The variation of VNLoad2, however, leads to a very different behavior. Lower VNLoad2 values cause an increase in pulse height, as opposed to a decrease seen in the first amplifier. A tendency towards lower pulse heights for larger DAC values can be seen. There is almost no change in latency observed. The power consumption has a maximum at the standard value of VNLoad = 4 and decreases slightly for changes in both directions (see Figure D.6). A later remeasurement of the VNLoad2 values showed no change in power consumption towards lower, and a slight decrease ($0.7\,\mathrm{mW/cm^2}$) towards higher values.

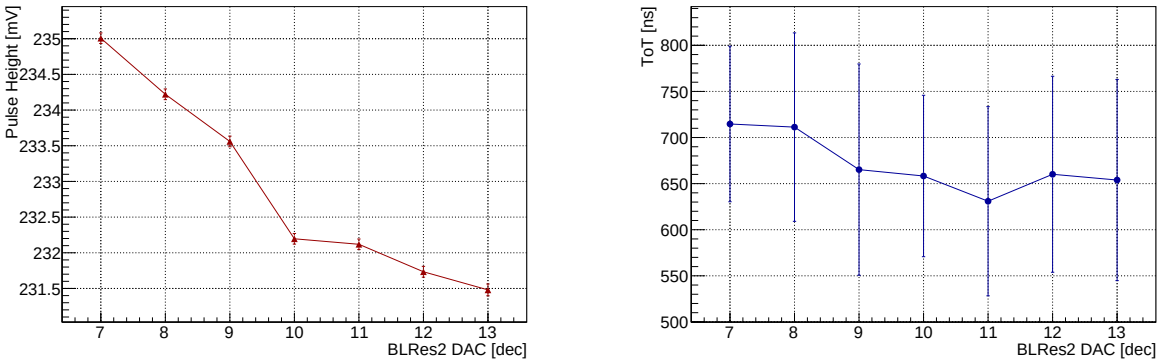
For VN2, the pulse height and noise variations occur on a smaller scale than for VN, leading to a smaller range of variation for the SNR, while the change in power consumption is almost the same as for the first amplifier (Figure D.5). The reason of the smaller variations is the lower gain of the second amplifier as compared to the first one. This means that in terms of saving power, it makes more sense to go to lower VN2 values instead of VN, since the loss in signal quality is not as severe.

VNFB2 (Figure D.7) variations show a decrease in pulse height for higher DAC values. In a first measurement, the pulse height reaches a maximum for VNFB2 = 7, however, since there is a large drop in noise for a DAC value of 5, the SNR is best there. The power consumption seems to show a slight increase in both directions. In a remeasurement of the VNFB2 values below the standard setting, 5 and 6 show almost the same pulse height and noise level. Therefore, as with the first amplifier, VNFB = 6 is chosen as new working point. Additionally, the power consumption is now constant for all three points.

The comparator has two components that are analyzed. VPComp acts as the main power regulator for the comparator, similar to VN and VN2 in the amplifiers, while BLRes2, together with the comparator capacitance, forms a feedback component similar to VNFB and VNFB2.

As seen in Figure 11.11a, the pulse height continuously decreases with increasing BLRes2 values. The power consumption stays practically constant, as it does for the feedback components in the amplifiers. The ToT slightly increases for lower BLRes2 (Fig. 11.11b), which is due to the shaping influence of this DAC, as mentioned in section 7.2. A local minimum in noise occurs at

BLRes2 = 8, resulting in a maximum for the SNR. Therefore, this point can again be chosen for optimized pixel performance at constant power consumption.



(a) Pulse height.

(b) Time over threshold.

Figure 11.11.: Variation of BLRes2.

A linear increase in power consumption is seen for higher values of VPComp, as it is the case for VN and VN2, albeit on a smaller scale of $\sim$2.5 mW/cm^2 per step. Here, the pulse height increases for higher DAC values, which is not the case for the main switches of the two amplifiers. The noise levels varies from point to point with no clear directional tendency. There is, however, a minimum at VPComp = 18, which is beneficial for power saving settings, because it leads to a higher SNR than in the standard setting (see Figure D.8).

11.4.2. New DAC Settings

From the behavior of the signal for different DAC values, possible new settings are determined. The settings are labeled with continuous numbers, starting from Setting1 up to Setting9. A summary of all DAC settings and their effects can be found in Table 11.1 at the end of this section.

At first, settings with which the signal quality could be improved while keeping power consumption constant are determined. As seen above, the feedback components are ideal candidates for this. The first three new settings keep all DACs constant except for VNFB, VNFB2, and BLRes2 for Setting1, Setting2, and Setting3, respectively. In Setting4 the three previous settings are combined in order to maximize the increase in SNR. Since the new VNFB and BLRes2 settings both lead to increased ToTs, the resulting ToT for Setting4 is quite large with $\sim$900 ns at a threshold of 0.65 V.

The next two settings, Setting5 and Setting6, are chosen such that a reduction in power consumption is possible, while not worsening the signal quality too much. As seen above, the dominant DACs in terms of power consumption are VN, VNFoll, VN2, and VPComp. Since reducing the power for the components in the first amplifier has the largest effect on the SNR, Setting5 leaves the first amplifier untouched and only decreased the power for VN2 and VPComp. VN2 is set to the lowest analyzed value (VN2 = 17) and VPComp is set to above mentioned 'sweet spot' of VPComp = 18. This setting results in a total reduction of drawn current of 1.7 mA (1.25 mA by amplifier two and 0.45 mA by the comparator), or equivalently, a ΔP of $\sim$24 mW/cm^2. In Setting6, the power for all stages (including VN and VNFoll) is changed. VN is reduced to 18, where the previous pulse height measurement showed a maximum. However, the increase in noise for the lower VN value results in a reduction of the SNR. The new VNFoll value is chosen to be 7, because of the low noise of this point. This new setting for the first stage has a slight influence on the behavior of the other stages, since a remeasurement of the SNR for

lowered VN2 and VPComp now shows the best results for VN2 = 18 and VPComp = 17, but the overall SNR for this setting is still slightly worse than for the LMP settings, due to the effect of the lower VN. This setting draws about 3 mA less, where 0.85 mA are due to VN (bias voltage of 1.5 V) and 2.15 mA are due to the other DACs (bias voltage of 1.8 V). The total reduction in power is $\sim$40 mW/cm^2.

For Setting7, the DACs are chosen to improve the signal quality, even if this means admitting a slight increase in power consumption. In order to keep this increase low, however, VN and VN2, the two main contributors in power consumption, are not changed. As described above, for VNLoad = 6 a maximum in pulse height and a slightly lower latency are observed. This leads to an increase in power consumption that can be compensated for, however, by lowering VNFoll as in Setting6, not leading to any net change in power consumption for the first stage. The new VNLoad and VNFoll both lead to an increase in SNR. A further SNR improvement is reached by lowering all feedback components. In the second stage an increase of VNLoad2 brings further improvements, as does an increase of VPComp in the comparator. This last change increases the current by 0.5 mA, so that the overall increase in power is just $\sim$7 mW/cm^2, while giving a vastly improved SNR. However, this comes at the cost of very high ToTs of >1000 ns at a threshold voltage of 0.65 V.

Setting8 and Setting9, finally, are combinations of the two power saving settings, Setting5 and Setting6, with Setting4. The idea behind this is to increase the SNR again by reducing the feedback to compensate for any potential losses in SNR due to the power reduction.

After the determination of the new DAC settings, the chip has been prepared for efficiency measurements at the PSI testbeam. For this purpose it is tuned again for each of the nine settings. Again, the tuning is done inside the light-tight box. At the following testbeam campaign (see next chapter), the reduction of light falling onto the chip is realized by covering it with plastic protection caps from both sides.

DAC [dec]	LMP-Setting	Setting1	Setting2	Setting3	Setting4	Setting5	Setting6	Setting7	Setting8	Setting9
VN	20	20	20	20	20	20	18	20	20	18
VNLoad	4	4	4	4	4	4	4	6	4	4
VNFB	8	6	8	8	6	8	8	5	6	6
VNFoll	10	10	10	10	10	10	7	7	10	7
VN2	20	20	20	20	20	17	18	20	17	18
VNLoad2	4	4	4	4	4	4	4	6	4	4
VNFB2	8	8	6	8	6	8	8	5	6	6
BLRes2	10	10	10	8	8	10	10	7	8	8
VPComp	20	20	20	20	20	18	17	23	18	17
ToT [ns]:	732 ± 85	843 ± 111	733 ± 103	769 ± 84	914 ± 106	743 ± 86	774 ± 91	1028 ± 123	938 ± 113	954 ± 119
Latency [ns]:	99 ± 10	98 ± 9	98 ± 11	99 ± 11	100 ± 10	99 ± 9	103 ± 11	97 ± 11	101 ± 12	102 ± 11
ΔP [mW/cm^2]:	—	0	0	0	0	∼ -24	∼ -40	∼ +7	∼ -24	∼ -40
SNR:	18.58 ± 0.10	19.49 ± 0.10	18.77 ± 0.11	18.55[a] ± 0.10	20.36 ± 0.12	19.36 ± 0.10	18.35 ± 0.09	22.58 ± 0.13	19.57 ± 0.11	19.91 ± 0.10

Table 11.1.: DAC values and remeasured ToTs, Latencies, ΔP, and SNRs for the new power settings. Best and worst changes are highlighted in green and red, respectively.

[a] One would expect a higher SNR here, as described previously. It is possible that the DACs were not set correctly for the threshold scan.

12. PSI June 2016 Testbeam

In June 2016, a testbeam campaign was performed at PSI. The goal was to characterize the different settings from above in terms of efficiency, noise rates, and crosstalk properties using a four-layer beam telescope consisting of MuPix7 chips [42].

The measurements were performed at the πM1 beam line of the HIPA. It provides a beam with tunable momentum ranging from 100 MeV/c to 490 MeV/c that is extracted from Target M (see Figure 3.5). The beam momentum was set to 220 MeV/c for the measurements. The beam consists mostly of π^+ with a small fraction of μ^+ and e^+, at an average rate of 20 kHz.

12.1. Setup

The telescope is set up on a Thorlabs® stage. The PCBs carrying the MuPix chips are held in place by custom mechanical frames with two micrometer screws for precise positioning in x- and y-directions (with z being the direction of the beam). The setup additionally consists of two scintillating tiles for timing measurements. However, due to the high rate of the beam, the SiPMs connected to the scintillating tiles were damaged very early in the campaign. Therefore, no timing measurements could be conducted. Figure 12.1 shows the four-layer telescope in the beam area.

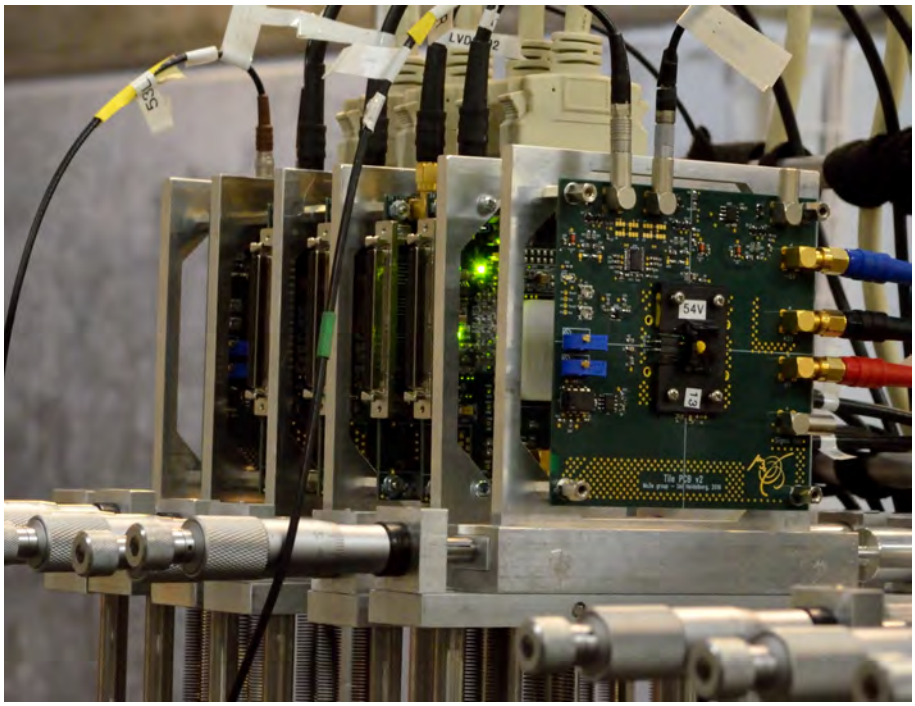


Figure 12.1.: Four-layer MuPix telescope + 2 layers of scintillating tiles in beam area.

The second telescope plane is used as device-under-test (DUT). The DUT is the same sensor that has been used in the lab setup. Due to technical difficulties at the accelerator, which resulted in a very limited beam time, only one sensor with the settings listed in the next section could be tested.

12.2. Measurements

A total of 10 efficiency measurements are performed using the following settings and tuning methods:

Scan	Setting	Tuning
1	LMP	1 Hz, FA
2	Setting1	1 Hz, FA
3	Setting2	1 Hz, FA
4	Setting3	1 Hz, FA
5	Setting5	1 Hz, FA
6	Setting6	1 Hz, FA
7	Setting7	1 Hz, FA
8	LMP	1 Hz, no FA
9	LMP	10 Hz, FA
10	LMP	30 Hz, FA

Table 12.1.: Settings tested for efficiency at PSI testbeam.

In order to analyze the efficiency behavior over a longer threshold range, a scan is performed for each of the used settings. The threshold range for the first measurement is chosen from 0.650 to 0.748 V, in order to avoid the high noise region close to the baseline. For the remaining settings, however, the upper threshold could be increased to 0.768 V.

The scans are done in automated measurements. The MuPix Telescope software provides the possibility to set start and stop threshold, step size, and measurement time per step. The chip DACs for all four layers are set automatically at the start of each scan.

12.3. Results

12.3.1. Efficiency Determination

For the measurements the hit information from all four planes is read out and stored. Using the hit information from the three tracking planes, particle trajectories can be reconstructed and extrapolated on the DUT. The exact track reconstruction method is explained in other works [42, 55]. If a hit is observed in the DUT within a time window of three timestamps ($\hat{=} \pm 48$ ns) and a search radius of 800 µm around the extrapolated hit position, the hit is marked as belonging to the reconstructed track. The efficiency is then calculated using the number of all reconstructed tracks and the number of tracks that correlate to a hit in the DUT (matched tracks):

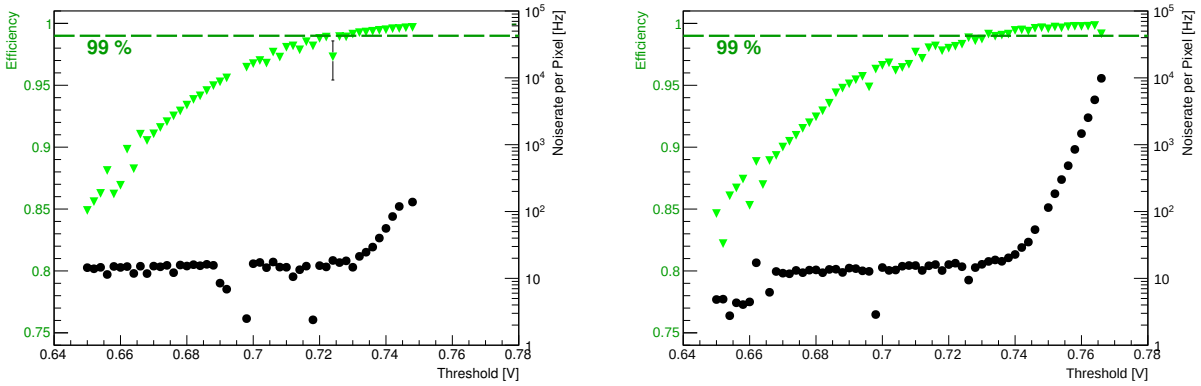
$$\text{Efficiency} = \frac{\#\text{ of matched tracks}}{\#\text{ of reconstructed tracks}} \tag{12.1}$$

An efficiency curve resulting from a threshold scan can be seen in Figure 12.2, together with the noise rate per pixel.

12.3.2. Efficiency Regions

In all efficiency scans for the different DAC settings and the different tuning methods efficiencies above 99 % could be achieved.

Most of the curves show a behavior, where the efficiencies seem to split into two distinct curves (most notably Setting2 in Figure E.3). Behaviors like these have already been observed in



(a) LMP settings.

(b) Setting1.

Figure 12.2.: Efficiency and noise rate scans for different settings.

previous efficiency scans. There is no final explanation for this effect. An assumption is that it is created by oscillations in the comparators of the pixels.

For the operational range of the chip, at least 99 % efficiency is required while simultaneously keeping the noise as low as possible. The noise rate per pixel is constant with about 15 Hz in the lower threshold voltage region. For thresholds close to the baseline, the noise rate increases rapidly. The Mu3e experiment requires a maximum pixel noise rate of 20 Hz [56]. This number corresponds to an allowed frame noise rate of 10^{-6} for a planned frame size of 50 ns (i.e. 20 million frames per second). However, higher noise rates of up to 10^{-5} might still be workable. Therefore, different operational ranges are determined for 20 Hz, 100 Hz and 200 Hz noise per pixel.

It is important to note that the depicted noise rates are not only due to pure electronic noise on the chip. For these measurements there is also an additional beam related background, consisting of hits created by particles that leave no reconstructible tracks, because they are not seen in all three tracking layers of the telescope. This can either be due to inefficiencies in one of the tracking planes or due to particles that are either scattered away from the active detection area of the chips or particles that get scattered into the detection area while passing through the PCBs. This beam related contribution affects the determination of the operational range for the chip by overestimating the amount of actual noise.

The operational regions for each setting are determined by fitting the efficiency and noise data with functions describing their behaviors. A Gaussian error function (Eq. 11.2) suits the efficiency behavior best.

For the noise rate an exponential function plus constant offset is assumed. The occasional drops in the noise rate are excluded from the fit, as are points at thresholds close to the baseline, where the noise does not follow the exponential behavior anymore, but instead shows a saturation effect, as seen, for example, with the 30 Hz tuning (Figure E.10). For these saturated noise regions, also a sudden drop in efficiency is observed. The reason for this is that, due to the readout pattern of the MuPix7, which is designed for low sensor occupancies [21], the increasing amount of hits can no longer be read out properly. This limits the readout of the MuPix7 to a pixel hit rate of a few kHz, or about 1 million hits per second for the entire chip.

Table 12.2 shows the calculated working regions for the different DAC settings and tuning methods for the three allowed maximum noise rates. The operational region is defined by an efficiency above 99 % and pixel noise rates below the above mentioned limits. The efficiency and noise rate plots for the different measurements can be found in Appendix E.

Setting (Tuning)	Operational Range [mV]		
	20 Hz	100 Hz	200 Hz
LMP (1 Hz, FA)	3.61 ± 1.23	15.46 ± 1.22	18.77 ± 1.22
Setting1 (1 Hz, FA)	6.67 ± 4.75	16.98 ± 4.77	19.82 ± 4.78
Setting2 (1 Hz, FA)	4.11 ± 0.59	14.61 ± 0.23	17.43 ± 0.23
Setting3 (1 Hz, FA)	4.53 ± 3.84	15.11 ± 3.86	18.04 ± 3.86
Setting5 (1 Hz, FA)	5.84 ± 0.35	16.08 ± 0.19	18.98 ± 0.18
Setting6 (1 Hz, FA)	—	8.39 ± 0.24	11.27 ± 0.24
Setting7 (1 Hz, FA)	3.76 ± 0.42	14.85 ± 0.26	17.68 ± 0.26
LMP (1 Hz, **no**FA)	1.17 ± 0.38	12.80 ± 0.23	15.88 ± 0.23
LMP (10 Hz, FA)	5.97 ± 3.49	16.71 ± 3.51	19.69 ± 3.52
LMP (30 Hz, FA)	*1.79 ± 0.20*	*18.69 ± 0.20*	*20.64 ± 0.21*

Table 12.2.: Efficiency regions for the different DAC settings and tuning methods.

The uncertainties for the operational ranges are calculated via error propagation from the fit parameters and are dominated by the uncertainties coming from the noise fits. Setting6 does not fulfill the above mentioned requirement for the 20 Hz limit. This setting only reaches 99 % efficiency after already passing the noise limit. For the LMP settings with 30 Hz tuning, a maximum threshold for the working region could not be calculated from the noise fit, since in this case the fit does not describe the data very well, especially in the region of low threshold voltages. Instead, the operational regions for this setting are determined by linear interpolation between the data points, again with all the drops being excluded.

Setting5, which reduces power consumption by $\sim$24 mW/cm^2, has wide operational ranges for all allowed noise limits and the lowest fit uncertainties, making it the preferred candidate for a power saving setting.

Since it is not known how to solve the problem of the occurring splits in the efficiency curves, the best one can currently do is fit the data as described above, which results in a fit function somewhere in between the two possible paths.

An interesting thing to note concerning the testbeam measurements is that for the tuning methods that allowed for higher noise rates, the split in the efficiency curves seems to be greatly reduced. However, since only one scan has been done for each of the tunings with higher noise limits, this could also have been by accident. Further measurements using these tunes could give a conclusion. It would also be interesting to see how and if the different DAC settings effect the double curve structure for these higher noise tunes.

12.3.3. Crosstalk

Crosstalk is a source of noise, where a signal from one circuit or component can create fake signals in neighboring parts. In the case of the MuPix chip, crosstalk can appear between neighboring transmission lines from the analog pixels to the digital cells. Signals in one line cause small fluctuations in neighboring lines, that can get processed by the connected digital cell as if it is coming from a real hit. There is a spatial separation between the transmission lines for even and odd numbered pixels, as illustrated in Fig 12.3. When crosstalk occurs, the resulting hit structure on the pixel map shows two or three simultaneous hits in next-to-neighboring pixels in the same column, depending on weather only one or both neighboring lines are affected. These events are called double and triple crosstalk, respectively.

Previous testbeam analyses have shown that the crosstalk probability rises with smaller values for VNFoll. Therefore, it is expected that the new settings with a lower VNFoll reflect this behavior.

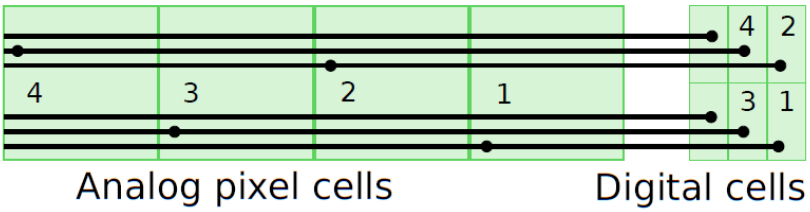


Figure 12.3.: Sketch of signal transmission lines with point-to-point connections between analog pixels and digital cells [57].

In order to check effects of the different DAC settings on the crosstalk, all power settings are analyzed for their crosstalk probability. It can be assumed that especially changes in the DACs of the first amplification stage affect the crosstalk (e.g. Setting1), since they determine the properties of the signal that is sent through the transmission lines to the digital cells.

All DUT hits showing the above described structure are stored as crosstalk events. In the case such an event can be matched with a reconstructed track, it is labeled as matched crosstalk. The probabilities for double and triple crosstalk are then calculated from the number of matched crosstalk events and the number of tracks matched to a DUT hit:

$$\text{double crosstalk} = \frac{\#\text{ of matched double events}}{\#\text{ of matched tracks}} \tag{12.2}$$

$$\text{triple crosstalk} = \frac{\#\text{ of matched triple events}}{\#\text{ of matched tracks}} \tag{12.3}$$

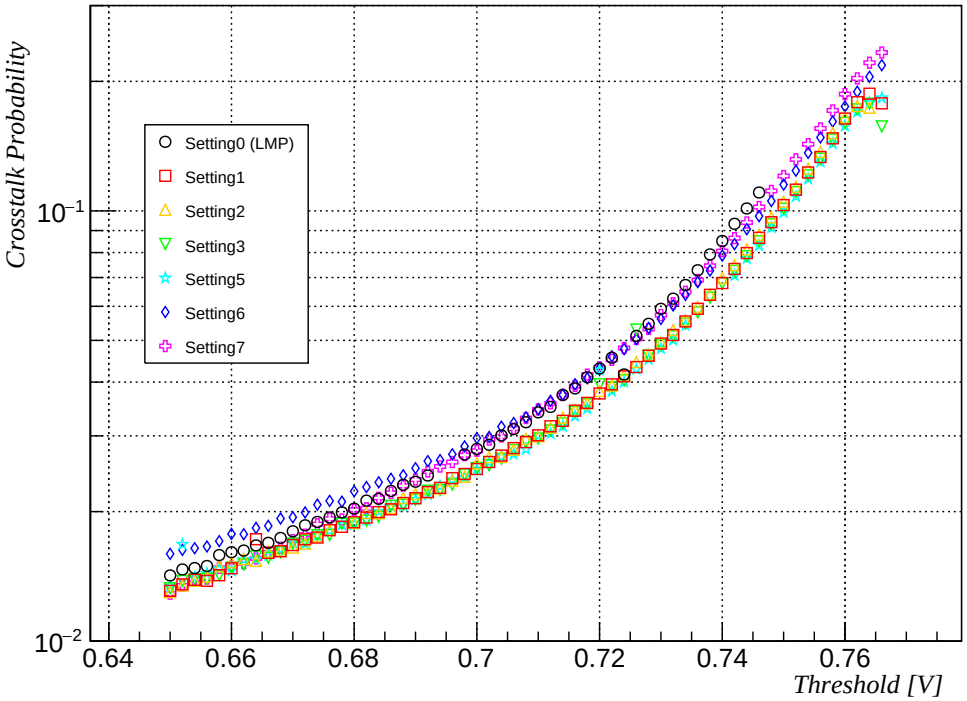
Figure 12.4 shows the behavior of double and triple crosstalk over the scanned threshold region for the different DAC settings.

The crosstalk probability increases for higher threshold voltages, because the closer the threshold is to the baseline, the more fluctuations can exceed the threshold and be counted as a hit. Due to variations between the pixels it is more likely that at higher threshold voltages crosstalk affects only one cell, which leads to faster rise of double crosstalk events. For threshold voltages very close to the baseline ($>$0.76 V) the crosstalk probability seems to decrease again. This is, however, not due to a reduction in crosstalk, but again due to the readout limits of the chip (see previous section).

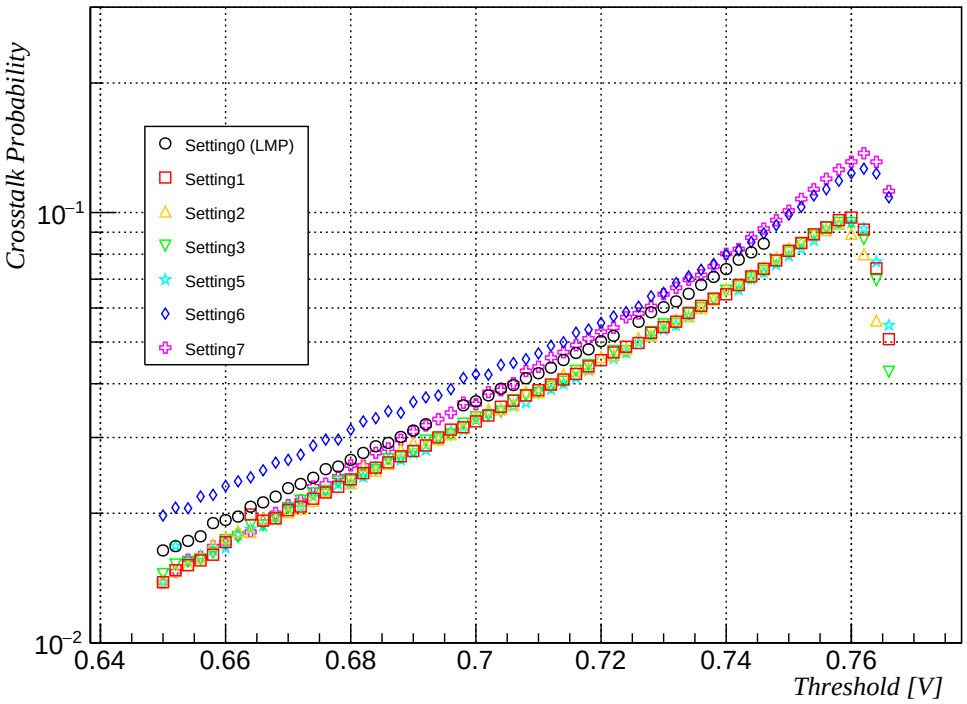
The double and triple crosstalk probabilities for Setting1 to Setting5 are comparable, which means that despite the increased pulse height for Setting1 due to the reduction of VNFB, the crosstalk probability does not increase. However, for Setting6 and Setting7, which are the settings where VNFoll has been reduced, higher crosstalk probabilities are observed.

Regarding double crosstalk events, Setting7 shows similar crosstalk probabilities to all other settings at thresholds below $\sim$0.68 V. For increasing threshold voltages, however, the crosstalk probability for Setting7 rises faster than for the other new settings. Setting6 already starts off with a higher crosstalk probability and shows more crosstalk than Settings 1 to 5 over the whole scanned threshold region.

The increased crosstalk probability for Setting6 and Setting7 can also be observed for the triple crosstalk events. In this case, Setting6 shows considerably more crosstalk from the start. So, in order to keep crosstalk as low as possible, VNFoll should not be decreased. An increase in VNFoll might lead to less crosstalk, however, as described in Section 11, this would increase the power consumption of the chip.



(a) Double crosstalk.



(b) Triple crosstalk.

Figure 12.4.: Double and triple crosstalk behavior for all tested DAC settings.

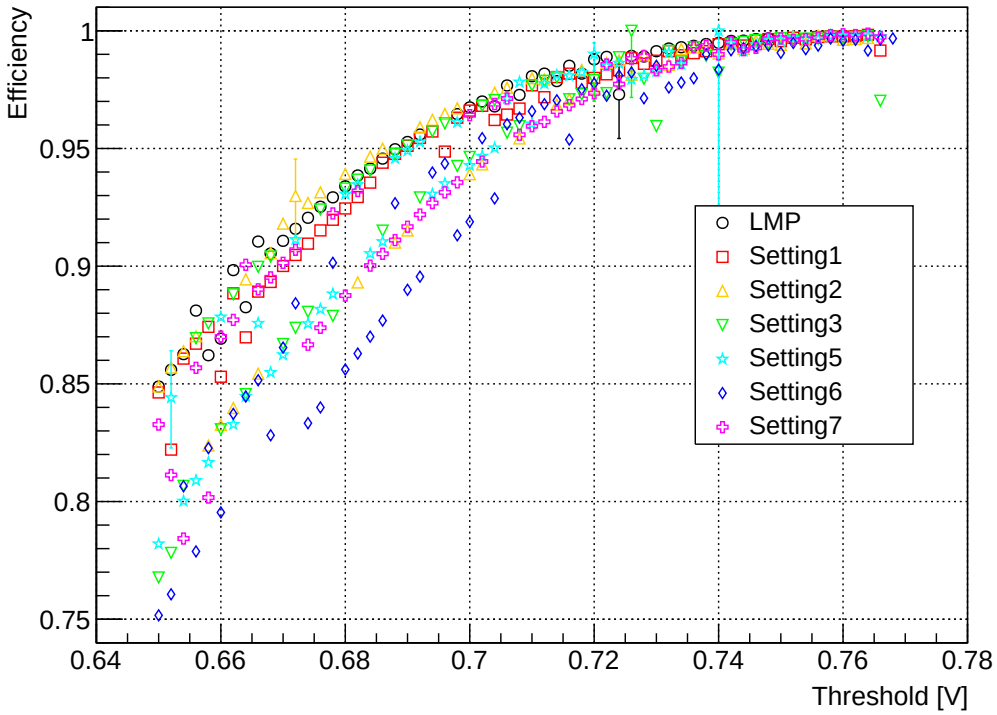
12.3.4. Summary

From the newly determined DAC settings, Setting1 to Setting3 and Setting5 to Setting7 are tested for efficiency and pixel noise rate. With all of them efficiencies of >99 % can be reached. The operational regions for noise limits of 20 Hz, 100 Hz and 200 Hz are determined for each setting and compared to that of the LMP settings. Setting5, which reduces the total power consumption by $\sim$24 mW/cm^2, reaches relatively wide working regions with the lowest uncertainties of all settings. Setting6 shows a lower efficiency than all other settings resulting in the smallest operational regions, which is due to the fact that this setting reduces VN, leading to a loss in performance. Figure 12.5 shows a direct comparison between all efficiencies and noise rates for the different DAC settings.

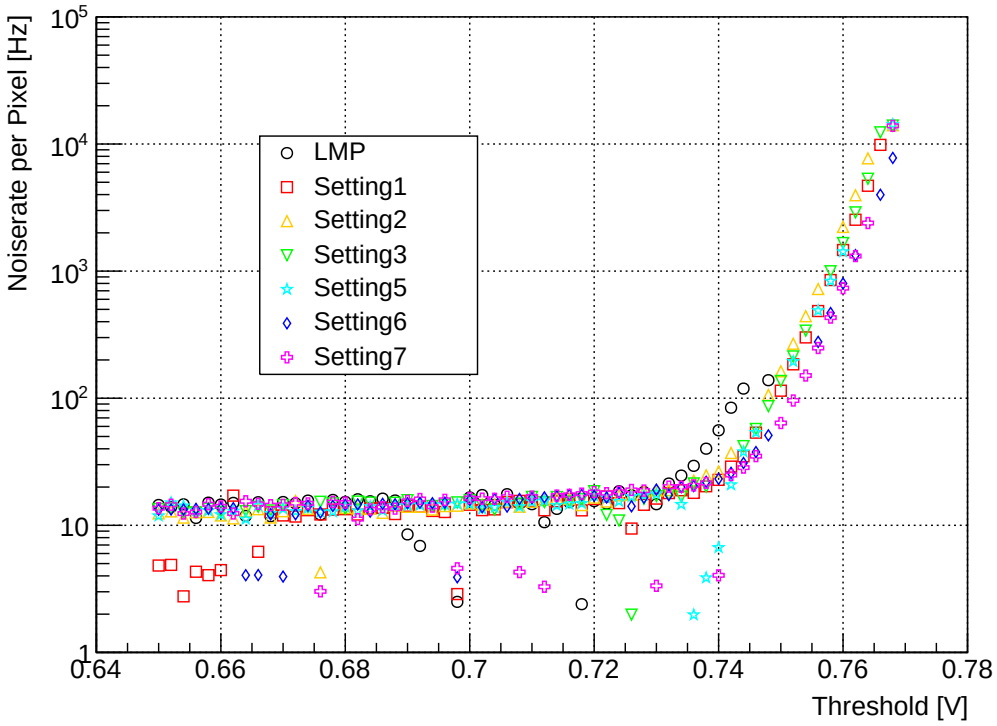
The observed split for efficiency behaviors seems to vanish when allowing for higher noise rates in the tuning.

An analysis of the crosstalk behavior of the new DAC settings show an increased crosstalk probability for Setting6 and Setting7, which is due to the changes in VNFoll. All other DAC settings show a very similar crosstalk behavior.

The wide efficiency region and the results of the crosstalk analysis make Setting5 an ideal candidate for achieving the main goal of this work, the reduction of power consumption in the chip.



(a) Efficiencies.



(b) Noise rates per pixel.

Figure 12.5.: Efficiency and noise behavior for all tested DAC settings.

13. Lab-Efficiency Measurements

In the scope of this thesis, a lab measurement has been set up to determine efficiency like quantities for the MuPix7 (see also Chapter 9) and compare them to actual efficiencies measured at testbeams. In this chapter the method of determining these lab-efficiencies is described and the first results of the measurements are presented.

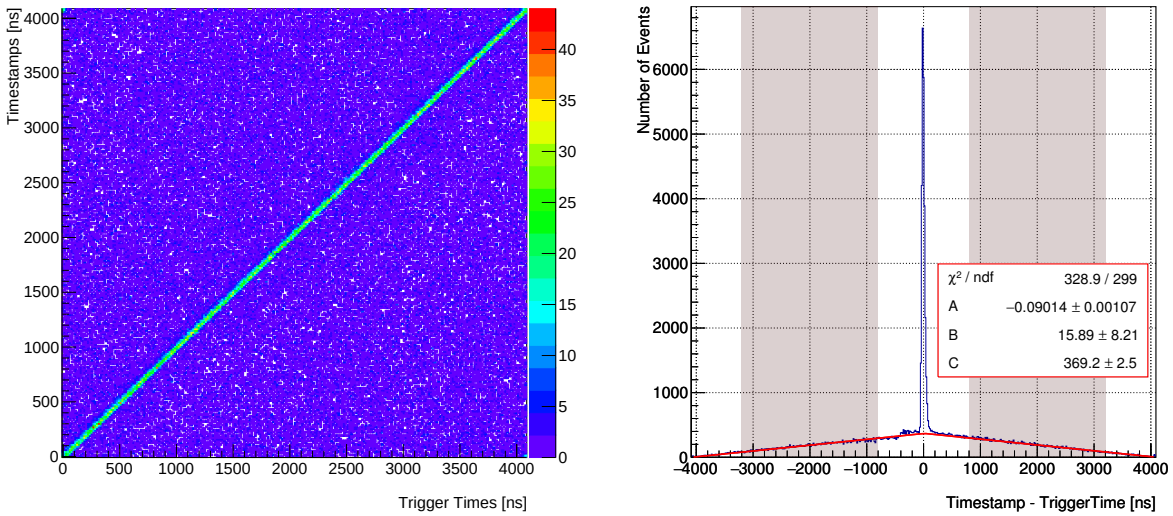
13.1. Setup

As described in Chapter 9, the setup for the lab-efficiency measurements uses a single MuPix7 chip and a scintillating tile as trigger system. A ^{90}Sr sample is used as particle source. To protect the setup from ambient influences, most notably light falling onto the chip, the setup is placed into a cardboard box wrapped in a light-tight fabric.

13.2. Method

To determine lab-efficiencies the data from the raw data files has to be extracted and analyzed. A program designed to check the quality of the data extracts the hit, trigger, and ToT information from the files and writes their correlations into histograms, which are then saved in ROOT-files.

For the lab-efficiencies, the correlation between the hit timestamps and the trigger times is important. A correlation plot for single events, i.e. events with only one registered on-chip hit and one trigger per frame is shown in Figure 13.1a.



(a) Correlation between hit timestamps and trigger times for single events.

(b) Difference between hit timestamps and trigger times for single events with absolute value background fit (conducted in marked regions).

Figure 13.1.: Trigger – timestamp correlations for lab-efficiency determination (binning size: 16 ns).

Single events are used to get a cleaner data sample, since having more than one hit or trigger in a frame leads to ambiguities in the assignment, which gives rise to random background.

There are still background events seen in the distribution, which occur due to noise on the chip or particles that are only seen by either the chip or trigger system due to scattering.

In order to remove this background, and only have the true coincidences, the trigger timestamp correlation is projected in a 1-dimensional histogram by calculating the difference between timestamps and trigger times (see Figure 13.1b). Here the correlated times form a central peak. The background is a triangular distribution, given by the difference of two uniformly distributed random variables (timestamps and trigger times) [58]. It can be fitted with an absolute value function of the form:

$$f(x) = A \cdot |x - B| + C \tag{13.1}$$

The lab-efficiency is then calculated from the number of true coincidences and the total number of measured triggers:

$$\frac{\#\text{ of coincidences}}{\#\text{ of triggers}} = \frac{\#\text{ of single events} - \text{background } (f(x))}{\#\text{ of triggers}} \tag{13.2}$$

Using this method, the lab-efficiency for one threshold setting is determined. To analyze the behavior of this quantity over a larger threshold range, a scan can be performed, as it is done in actual efficiency measurements.

13.3. Limitations and Error Sources

The lab-efficiencies measured with this setup are considerably smaller than actual efficiencies measured at testbeams. This is, for one, due to the fact that the surface of the tile facing the source is larger than the active chip area, therefore triggers from particles are seen that do not pass through the chip. The measured efficiency scales with the ratio of the areas of chip and tile. With an area of approximately $4\,\text{mm} \times 4\,\text{mm}$ for the tile and a pixel matrix area of $3.296\,\text{mm} \times 3.2\,\text{mm}$, the maximum lab-efficiency can only be $\sim$65 %, given by the geometric acceptance of this setup. This value gets reduced even more when considering the non-uniform irradiation from the ^{90}Sr source and the large amount of multiple scattering in the setup.

Additionally, the total number of triggers that is used to calculate the lab-efficiency (Eq. 13.2) does not only contain trigger information from single events, but also from events that have more than one trigger or hit per frame.

While the cut on single events for the lab-efficiency calculation ensures a cleaner data sample at low threshold levels, it comes with additional error sources for higher thresholds and the increasing amount of noise.

For high occupancies, the number of single events reduces, because it is less likely for a frame to contain only a single hit.

Furthermore, the calculation of the number of coincidences also starts to fail at thresholds close to the baseline, because the high occupancy leads to a deformation of the background, as shown in Figure 13.2. A second peak at later trigger times (negative timestamp – trigger differences) starts to dominate the background.

The reason for the formation of this second peak is once again the readout structure of the MuPix chip and its limits. The problem is visualized in Figure 13.4. Since the readout occurs columnwise, the illustration is reduced to one column for easier explanation.

In the case of low chip occupancies, the association between hits and triggers occurs as depicted in Figure 13.3. Only one hit and one trigger are seen per frame. For thresholds close to the baseline, however, chip occupancy increases due to noise.

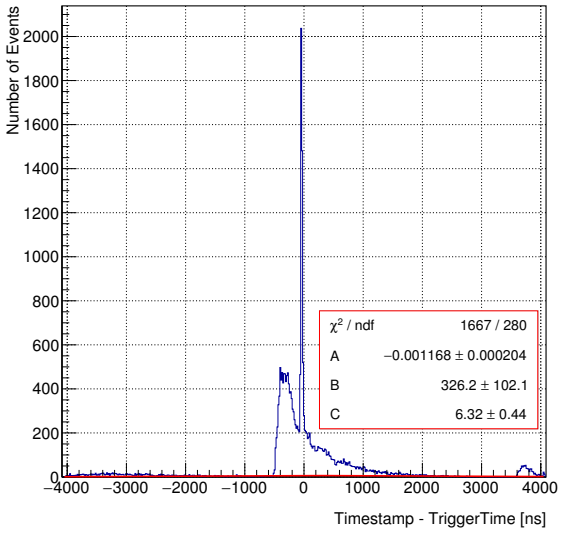


Figure 13.2.: Trigger timestamp differences at a threshold voltage of 0.76 V.

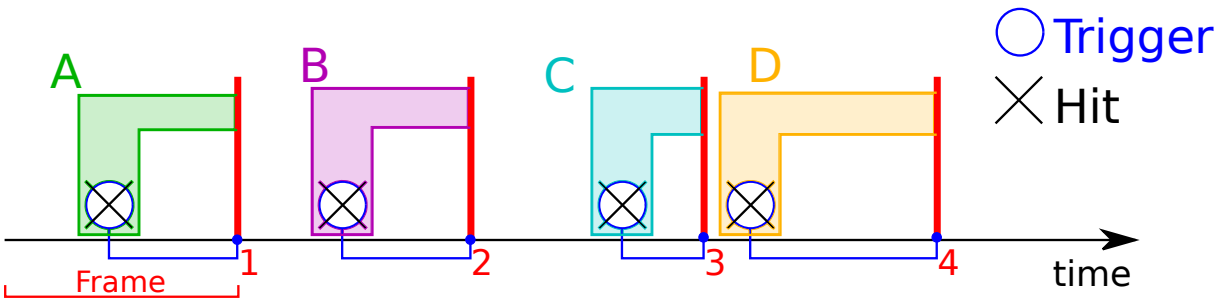


Figure 13.3.: Assignment between hits and triggers per frame at low chip occupancies.

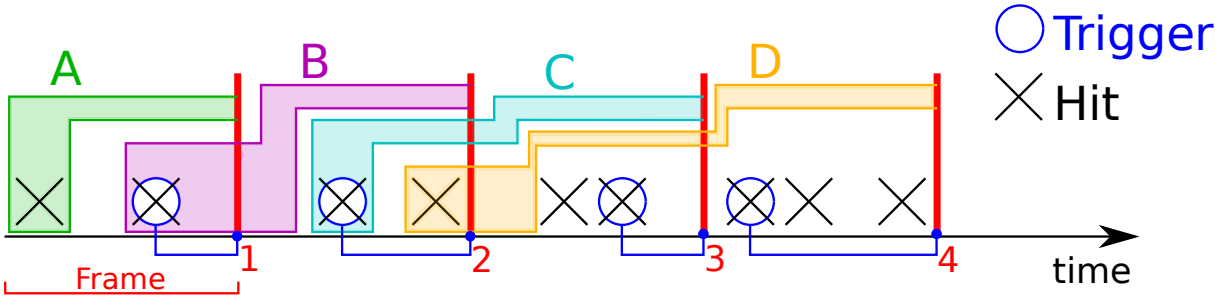


Figure 13.4.: Wrong assignment between trigger hit for high chip occupancies.

In the first frame shown in Figure 13.4 two hits occur within the same column. One of those hits also produces a trigger event which gets assigned to this frame. Only one hit is read out during this readout cycle and is assigned to the frame and, therefore, the trigger (Event A). In Frame 2, again a trigger is seen that gets assigned to this frame. During the readout cycle of the chip, the remaining hit from Frame 1 is read out but is wrongly assigned to Frame 2 and the trigger seen in this frame (Event B), but since this hit occurred in an earlier frame, its timestamp is smaller than the time assigned to the trigger in Frame 2. The result is a negative timestamp – trigger difference. This effect can even occur over more than one frame (Event D). The higher the occupancy of the chip due to noise, the more prevalent events like this become, leading to an increase of the background deformation for threshold voltages close to the baseline.

For the calculation of the number of coincidences this means that, due to the wrongly assigned events, the background distribution can no longer be described by an absolute value function. As shown in Figure 13.2, the fit, which is conducted in the same region as before (see Figure 13.1b), considerably underestimates the number of background events that are subtracted. The events in the second peak at negative timestamp – trigger differences are then wrongly counted as coincidences. As a consequence, this overestimated number of coincidences leads to a strong sudden increase in the calculated lab-efficiency, as can be seen in Figure 13.5.

13.4. First Tests of Setup

The lab setup is tested using different chips. The first measurements are done using a tuned, 50 µm thin MuPix7 chip on a PCB with a thinned backside (labeled 7728). After that, the chip and PCB are replaced by the chip used for the previous lab and testbeam measurements (7714) to have a direct comparison between lab-efficiencies and actual efficiencies.

13.4.1. First Chip

After several test runs and debugging of the measurement procedure, a first lab-efficiency curve in the threshold region from 0.655 V to 0.765 V is measured, shown in Figure 13.5. The steps size is 5 mV, measuring ∼120 s per step.

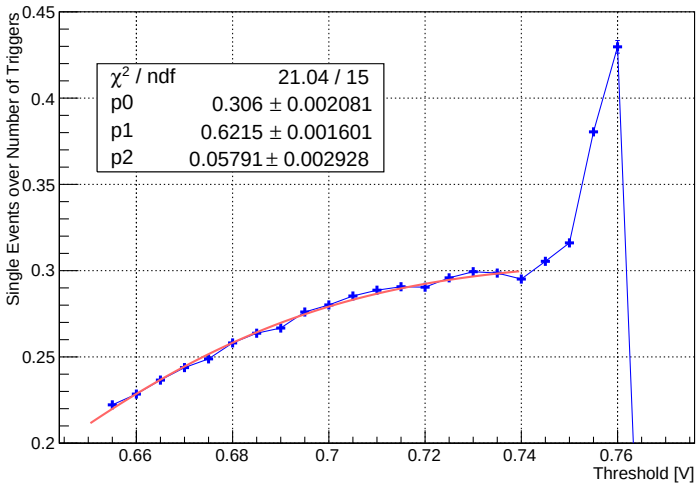


Figure 13.5.: Lab-efficiency behavior for a 50 µm chip on PCB 7728 at LMP settings.

The lab-efficiency for this chip increases with the threshold voltage up to a value of ∼30 % at 0.74 V. This behavior is very similar to the increase in efficiency seen in testbeam scans. At higher thresholds, however, there is a sudden strong increase in measured lab-efficiency, followed by a steep drop for the last measured point.

The reason for this behavior is a wrong number calculated for the coincidences due to the aforementioned deformation of the background distribution.

To illustrate the efficiency-like behavior, the curve in Figure 13.5 is fitted with a Gaussian error function, as it has been done with the actual efficiencies in Chapter 12. The function includes an additional free parameter for scaling (p_0). The resulting parameters for mean (p_1) and sigma (p_2) are similar to the corresponding parameters for the efficiency fit of the LMP settings (Figure F.2), but since the fits are performed for different chips they are not directly comparable.

13.4.2. Second Chip

As before, the step size is 5 mV and the measurement time per step is 120 s. The lab-efficiency curve for this chip is shown in Figure 13.6 in a region form 0.65 V to 0.77 V, which corresponds to the threshold range used in the testbeam measurements.

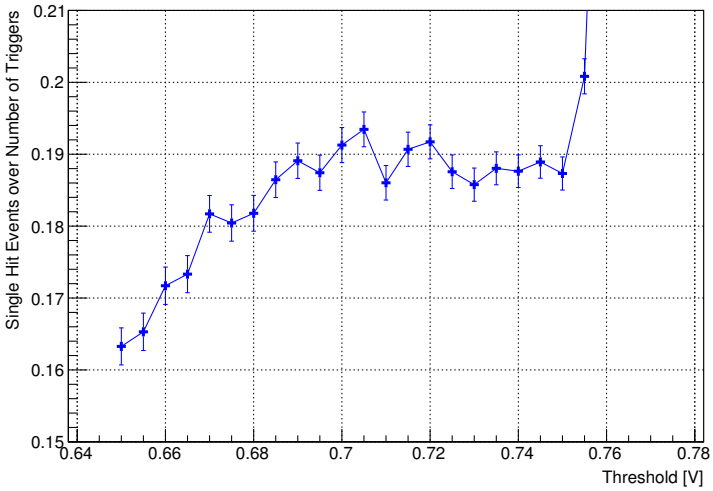


Figure 13.6.: Lab-efficiency for 64 µm chip on PCB 7714, LMP settings.

The lab-efficiency shows a reasonable behavior up to 0.75 V, although there seems to be a tendency for a slight decrease in lab-efficiency values in the region from 0.7 V to 0.75 V. This is likely due to the decrease of single events for higher chip occupancy, as described in Sectionsec:error. After that, the steep rise due to the deformed background can be seen again. It is also clearly seen that the overall measured lab-efficiency is lower than for the previous chip. This might have a multitude of reasons:

For one, the two chips have different thicknesses. The low momenta of the β electrons lead to an increased amount of multiple scattering in the thicker chip resulting in less seen triggers. The alignment between chip, scintillating tile and ^{90}Sr source also differs greatly for the two setups, due to the complete rebuilding of the setup with the new chip. During the rebuilding of the setup, some settings of components, especially the threshold of the discriminator between the scintillator/SiPM output and trigger system input, were slightly changed, which alters the detection efficiency of the trigger system.

The difference in alignment can be seen by comparing the trigger hitmaps, which show the distribution of single events over the to chips (see Figure F.1 in Appendix F).

13.5. Comparison between Efficiency and Lab-Efficiency

The ultimate goal of these measurements is to find a relation between lab-efficiencies and actual efficiencies measured at testbeams for the same chip. For this, the measured lab-efficiencies have to be scaled to match the actual efficiencies.

This can be achieved in several ways. One way is to calculate the ratio between efficiencies and lab-efficiencies for the same threshold and to determine a scale factor by averaging over these ratios. Another way is to perform a fit to the efficiency and lab-efficiency curves and calculate a scale factor between the two fit functions.

Since the lab-efficiency measurements are performed with a threshold step size of 5 mV, whereas the testbeam measurements are done at steps of 2 mV, the ratio between an efficiency and a

lab-efficiency point can only be calculated in 10 mV intervals. The calculated ratios between the lab-efficiency measurement shown in Figure 13.6 and the testbeam efficiency for the same settings (LMP settings) are depicted in Figure 13.7.

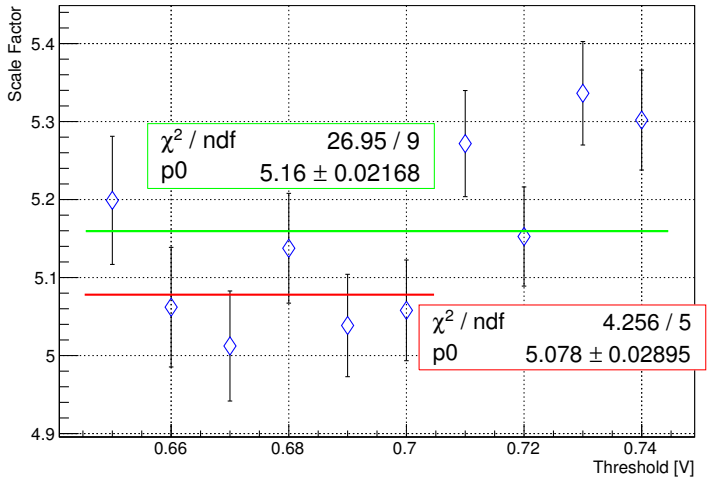


Figure 13.7.: Scale factor between efficiencies and lab-efficiencies for the chip on PCB 7714 at LMP settings.

The uncertainties on each ratio are calculated via error propagation from the efficiencies and lab-efficiencies, where the higher relative uncertainty of the lab-efficiency dominates.

The scale factor between efficiency and lab-efficiency is calculated by averaging over all ratios in a certain region. The green line in Figure 13.7 shows the average over all calculated ratios. However, since the lab-efficiencies show a slightly decreasing behavior for thresholds above 0.7 V, that is not seen in for the actual efficiencies, a second scale factor is calculated by only comparing the ratios of efficiencies in the threshold region where they are both behaving comparably. This scale factor is indicated by the red line in Figure 13.7.

The comparison between the scaled lab-efficiencies for both scale factors and the testbeam efficiency measurement for LMP settings can be seen in Figure 13.8.

There is a deviation of the lab-efficiencies from the expected behavior for large threshold voltages. In the lower threshold region, however, the lab-efficiencies can be scaled such that they match the efficiency behavior reasonably using the smaller scale factor determined above (see red graphs in Figure 13.7 and 13.8).

The disadvantage of the scale factor determination using the ratio of measured (lab-)efficiencies is that the accuracy depends on the number of points used for the averaging. This method is only really useful if the efficiency and lab-efficiency scans are performed in the same regions with the same step size, and therefore have the same number of points.

The fit approach, however, is independent of the step size and number of points. Here, the efficiencies are fitted with a normalized Gaussian error function (as described in Chapter 12). Assuming the behavior of the lab-efficiencies is similar to the efficiency behavior for the same settings, the fit parameters for the mean and width determined by the efficiency fit are taken and fixed for a second error function with a constant prefactor as additional free parameter. This second function is used as a fit for the lab-efficiencies. The fit value for the prefactor then gives the scaling between efficiencies and lab-efficiencies.

Figure 13.9 shows the testbeam determined efficiencies again with the scaled lab-efficiencies using the error function fit method as well as the ones using the ratio averaging method described above for comparison.

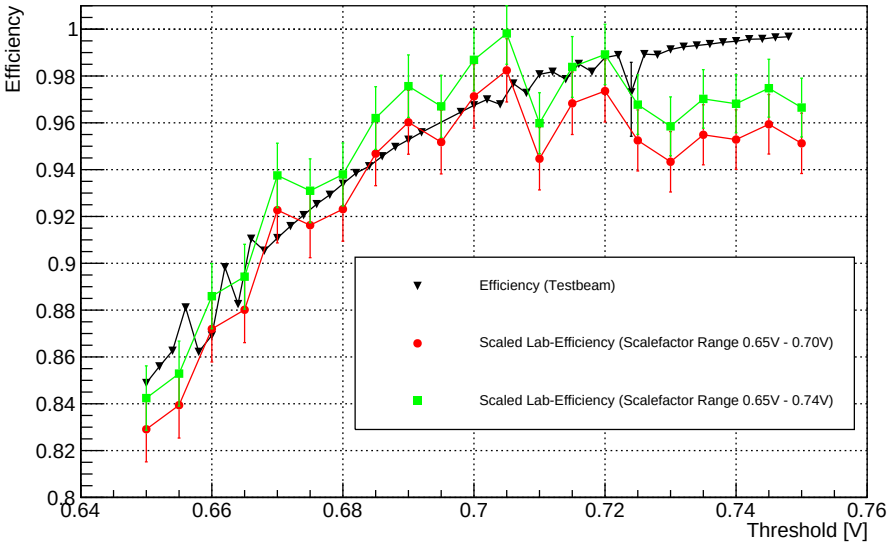


Figure 13.8.: Comparison between efficiencies and scaled lab-efficiencies for the chip on PCB 7714 at LMP settings.

The fit to the lab efficiencies is performed only in the threshold region below 0.7 V, where the two quantities show a comparable behavior. It can be seen that the scale factor determined with this method is slightly larger than for the other method, but gives a comparable result. In order to be independent of the chosen step size for the efficiency and lab-efficiency measurements, the fit method should be used for the scaling of future lab measurements. Table 13.1 shows the two scale factors. The fitted efficiency and lab-efficiency curves can be found in Figure F.2 in the Appendix.

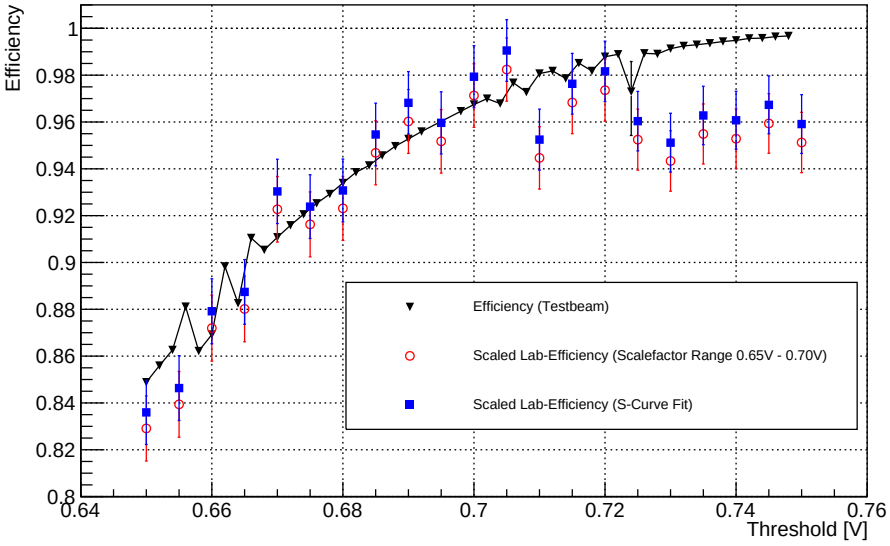


Figure 13.9.: Comparison between the different scaling methods (average of ratios and S-curve fit) for lab-efficiencies of the chip on PCB 7714 at LMP settings.

Method	Scale Factor
averaged ratios	5.08 ± 0.03
error function fit	5.12 ± 0.02

Table 13.1.: Scale factors for lab-efficiencies at LMP settings for two different scaling methods.

It should be noted that, while the two measurements (efficiency and lab-efficiency) were done for the same chip and the same DAC settings, the tuning was different. The tuning for the lab measurement was done after the chip was returned from the testbeam facility to quickly check the functionality of the chip and to test if it works in the lab setup. For this new tuning a different integration time and a different threshold step size were chosen. As a result there is a notable difference in the TDAC distribution (see Figure F.3). The scale factors calculated above are therefore not necessarily suitable to find a gauging for the two quantities, but are rather intentioned to proof the overall concept and functionality of the setup.

So far no measurement using the exact testbeam tune settings for the lab setup has been performed. This will be the next step in the conditioning of this setup.

13.6. Setup Improvements

As described before, the lab-efficiency determination is limited to low threshold voltage regions. The wrong assignment between hits and triggers at thresholds closer to the baseline occurs due to the way the data is interpreted (see Section 13.3). A possible improvement is to use additional time sorting of the hit and trigger times in the analysis in order to ensure that the hit timestamps are correlated with their corresponding trigger times. Such a time sorting method is not yet implemented in the analysis program.

Additionally the problem with the high occupancy could be solved by reducing the measurement to a smaller sub-matrix of the chip, which would result in less data that needs to be read out. In Section 14.2 it is explained how this could be realized in future lab-efficiency measurements.

Part IV.

CONCLUSIONS

14. Discussion

14.1. Summary & Conclusion

The Mu3e experiment is designed to search for the lepton flavor violating decay $\mu^+ \to e^+e^-e^+$ with a sensitivity of one in 10^{16} decays [1], which is about four orders of magnitude more precise than the current limit, set by SINDRUM [12]. In the Standard Model, this decay channel is highly suppressed with a branching fraction of $BR < 10^{-54}$. Any observed signal would therefore be a clear indicator for New Physics.

To achieve this sensitivity, a detector is needed that can handle the high rates of decay particles. Simultaneously, the material budget must be kept at a minimum to avoid multiple Coulomb scattering in the detector, which has a strong effect on the vertex and momentum resolution. Therefore, the Mu3e detector uses a tracker consisting of four layers of silicon pixel detectors that make use of the High Voltage Monolithic Active Pixel Sensor (HV-MAPS) concept that provides a fast charge collection and signal generation while making it possible to thin down the sensors to 50 µm.

The current sensor prototype, the MuPix7 chip, was the object of this thesis. With its currently used bias settings, it consumes $\sim$300 mW/cm^2 of power, which get dissipated into heat that has to be cooled in the final experimental setup. In a series of lab measurements, new bias settings for the on-chip DACs were investigated in order to reduce the power consumption of the chip, while not worsening the signal quality too much.

For this, each DAC was scanned individually in a small region around its standard setting in order to find an optimum, while the other DACs were kept at their standard value. New settings were chosen based on the observed improvements.

This procedure of determining new DAC values can be improved by performing several iterations of these scans, such that first one DAC is optimized and fixed and then the remaining parameter space is scanned again in relation to this new setting. This procedure would the be repeated until all DACs are improved. However, this task will be much more time consuming than the procedure presented here.

A total of nine possible new settings were investigated. Settings 1 through 4 aimed at improving the signal quality without changing power consumption. This was achieved by reducing the feedback of the on-chip amplifiers and comparator. With a tuned sensor in a darkened environment and the new settings, an SNR of up to 20 could be reached using injection test pulses as signal source.

Another setting (Setting7) with the goal to improve signal quality reached even higher SNR values, but also lead to a small increase in power consumption of $\sim$7 mW/cm^2.

Two settings, Setting5 and Setting6, were chosen to specifically reduce the power consumption by $\sim$24 mW/cm^2 and $\sim$40 mW/cm^2, respectively. In the latter case this lead to a slight increase in latency and a very small, although not significant, decrease in SNR compared to the standard settings. There is, however, the possibility to increase signal quality again by combining the two power saving settings with the reduced feedback settings (Setting8 and Setting9).

The most promising of these new settings were analyzed for their efficiency at a testbeam campaign at PSI. Three operational threshold ranges were determined for each setting in which efficiencies of at least 99 % could be reached while not exceeding maximum pixel noise rates of 20 Hz, 100 Hz and 200 Hz. In all three cases Setting5 showed a wide operational range and the lowest uncertainties on the width of said range for all settings.

Additionally the effect of the different DAC settings on the crosstalk of the signal transmission lines between analog and digital part of the chip was tested. Settings 1 through 5 showed a very similar behavior with crosstalk probabilities comparable to the probability for the standard settings. Setting6 and Setting7, which changed the settings for the source follower bias voltage, showed a higher crosstalk probability. This confirms previous observations of the influence of the source follower settings on the crosstalk. Alternatives for the signal transmission from the pixels to the digital cells that might reduce the crosstalk will be investigated with the new MuPix8 prototype.

The efficiency and crosstalk studies marked Setting5 as a possible candidate for new settings with less power consumption and a slightly improved SNR.

In addition to the optimization of the chip settings, this thesis also focused on the development and testing of a new lab setup that would make it possible to estimate efficiency behaviors of MuPix chips without testbeam access. This system is still in development but first test measurements have been performed.

The principle behind the setup is to determine an efficiency-like quantity by using a radioactive source. These lab-efficiencies are calculated from the number of coincidences between a single MuPix chip and a scintillating reference tile, compared to the total number of particles observed by the tile.

Test measurements done for two different chips, one of which being the same one that was used at the testbeam campaign, proved the overall functionality of the setup. An efficiency-like behavior was observed for both chips up to thresholds of $\sim$0.74 mV. For threshold voltages closer to the 0.8 V baseline, the high chip occupancy, due to rising noise, causes a deformation of the background distribution. The applied background subtraction fit can no longer accurately describe the distribution which causes a severe overestimation of the number of coincidences, and therefore the calculated lab-efficiencies.

The new setup is principally functional for measurements in the region of low threshold voltages. However, an improvement of the setup is needed for measurements at thresholds close to the baseline (see Outlook).

The lab-efficiency measurements for the same chip that was used at the testbeam were done with a different tuning and with different step sizes. An actual comparable measurement using the same tuning and step size is the next goal for the new setup. Along the same line, the measurement could be done with longer time windows in order to gain more statistics.

After that, lab-efficiencies with different DAC settings can be measured and analyzed to see if the observed changes in actual efficiencies can be reproduced.

14.2. Outlook

While the power settings presented in this thesis already meet the requirements for the final use in the Mu3e experiment, there is the motivation to go to even lower power consumptions to make the concept of the MuPix chip attractive for applications outside Mu3e with tighter power requirements. The desired goal for the power consumption is in the order of $100\,\mathrm{mW/cm^2}$, which, however, cannot be reached with the current design. Future generations of the MuPix family are aiming to reach this requirement.

Concerning the DAC settings, an overall picture of how the different DACs effect the signal quality and power consumption could be made in this thesis. The general strategy presented for the optimization of the individual DACs can be used for the configuration of the new MuPix8 chip, although the electronic components of the new chip will show some considerable changes. For example, the MuPix8 will once again contain only one amplification stage.

Additionally, the concept for the transmission line driver will be reconsidered and use an alternative to the source follower, which is planned to reduce the amount of crosstalk between transmission lines.

In order to improve the lab-efficiency measurements and to be able to go to higher threshold voltages, the problem with the high chip occupancies and the limited readout need to be solved. A possible solution would be to limit the lab-efficiency measurements to a smaller pixel sub matrix which reduces the amount of hits that needs to be read out. For the MuPix7 this could in principle be achieved by using the tuning properties of the chip to intentionally overtune larger parts of the pixel matrix so that the pixels become less sensitive to hits. The MuPix8 will provide the feature to completely turn off parts of its pixel matrix, which will be useful for future lab-efficiency measurements.

Part V.

APPENDIX

A. Graphical User Interface

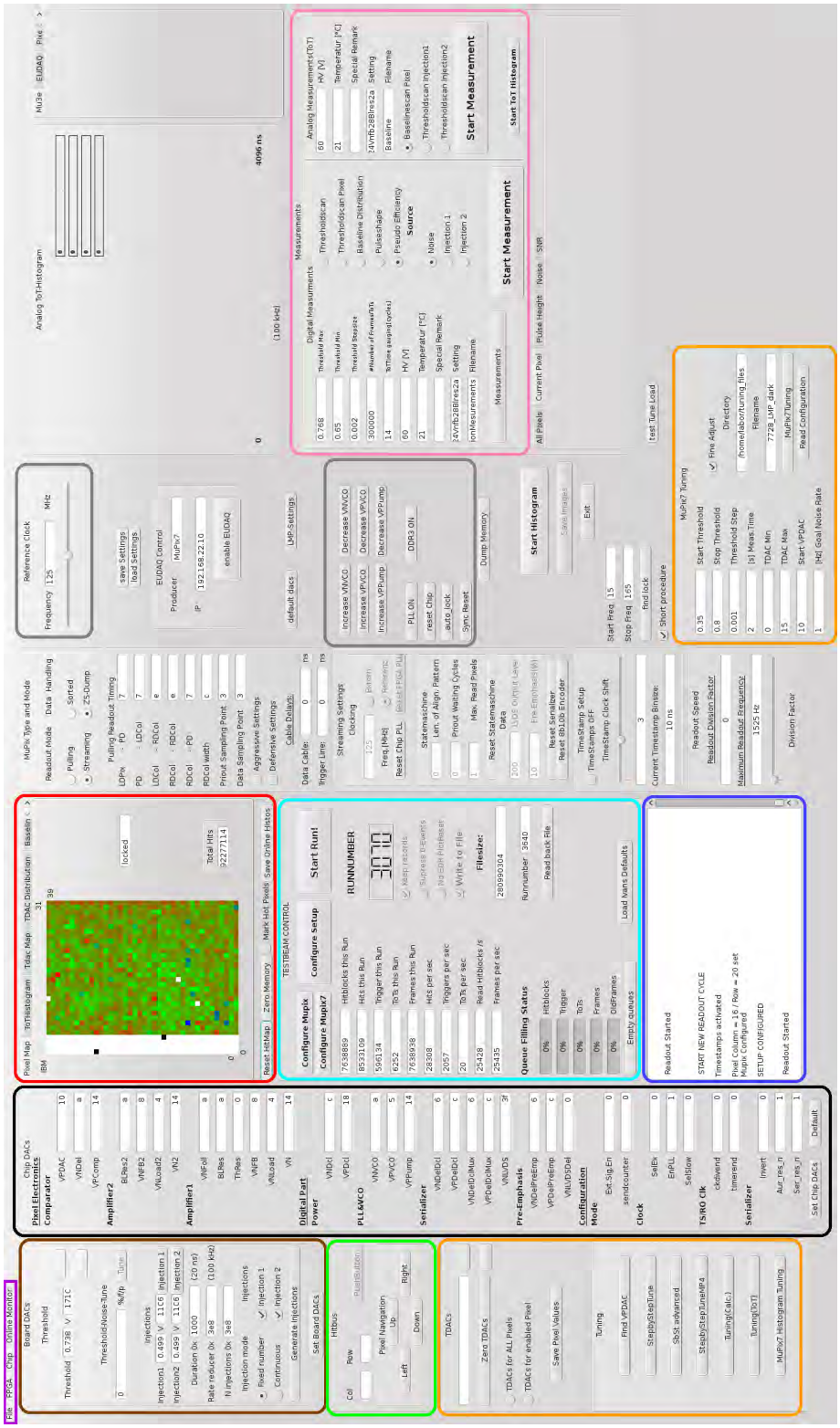


Figure A.1.: Single Setup GUI. **Brown**: Threshold and injection settings, **Green**: Hitbus selection, **Orange**: Tuning, **Black**: Chip DAC interface, **Red**: Pixel hitmap, **Cyan**: Readout control, **Blue**: Status information, **Gray**: Clock control & synchronization, **Pink**: Automated measurements, **Purple**: Additional windows for online monitoring.

B. TDAC Difference Maps

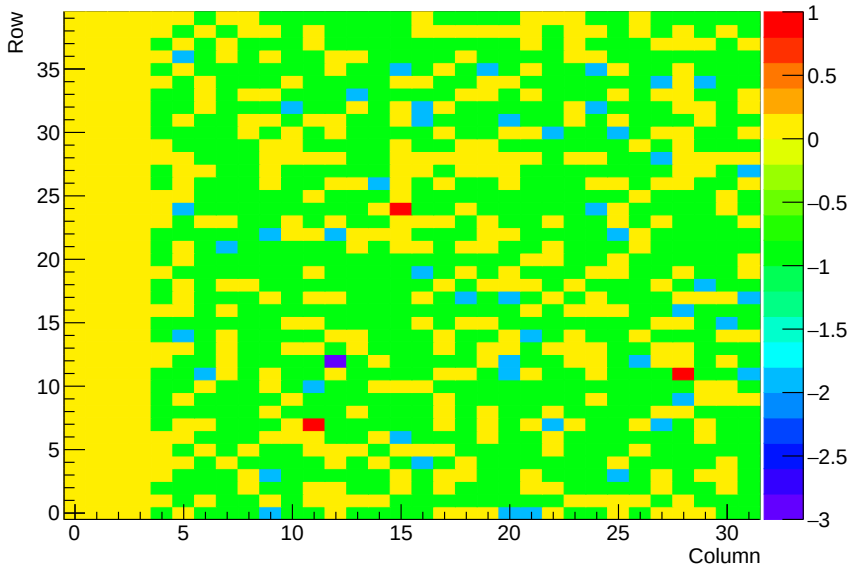


Figure B.1.: TDAC differences between LMP settings and Setting1.

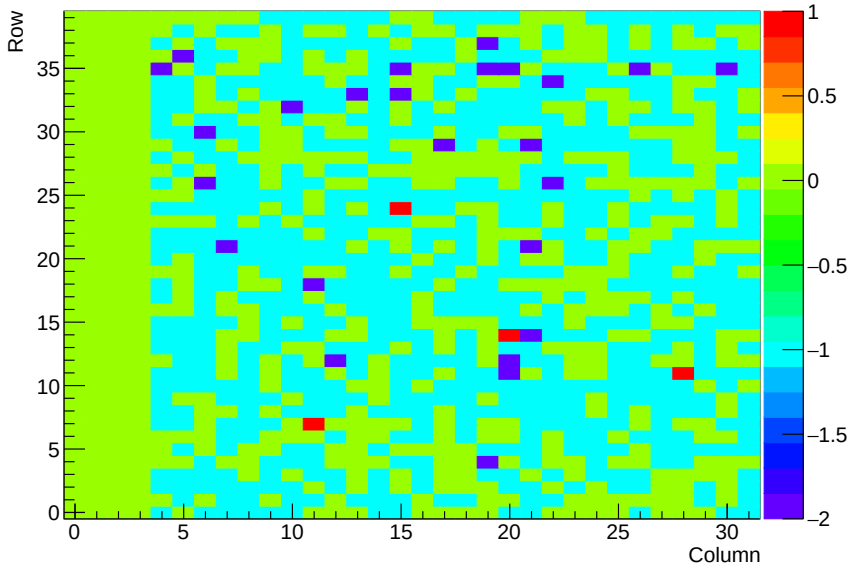


Figure B.2.: TDAC differences between LMP settings and Setting2.

C. First Measurements of VN, VNLoad, VNFB, and VNFoll

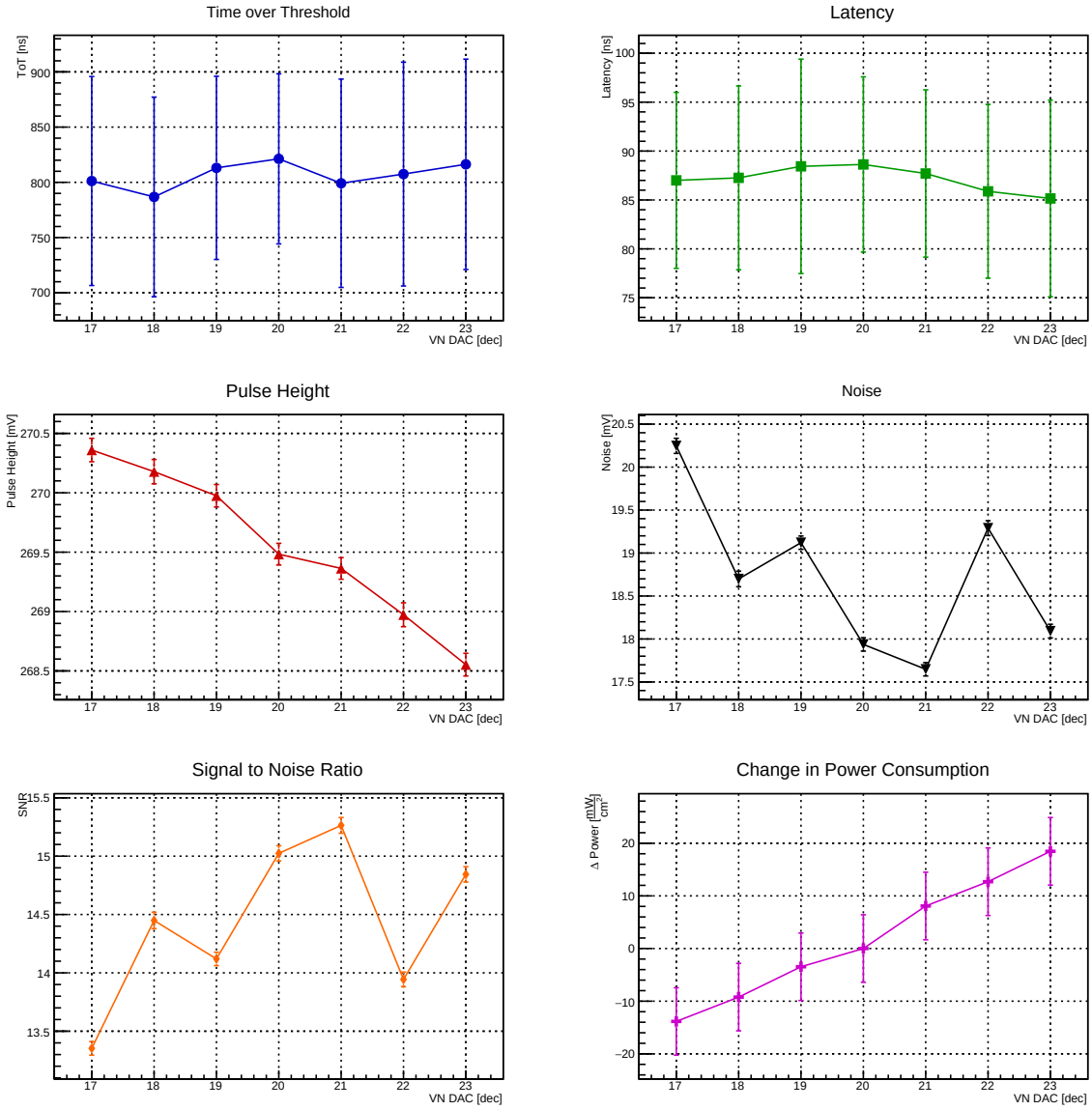


Figure C.1.: Variation of VN and its effect on ToT, latency, pulse height, SNR, and power consumption.

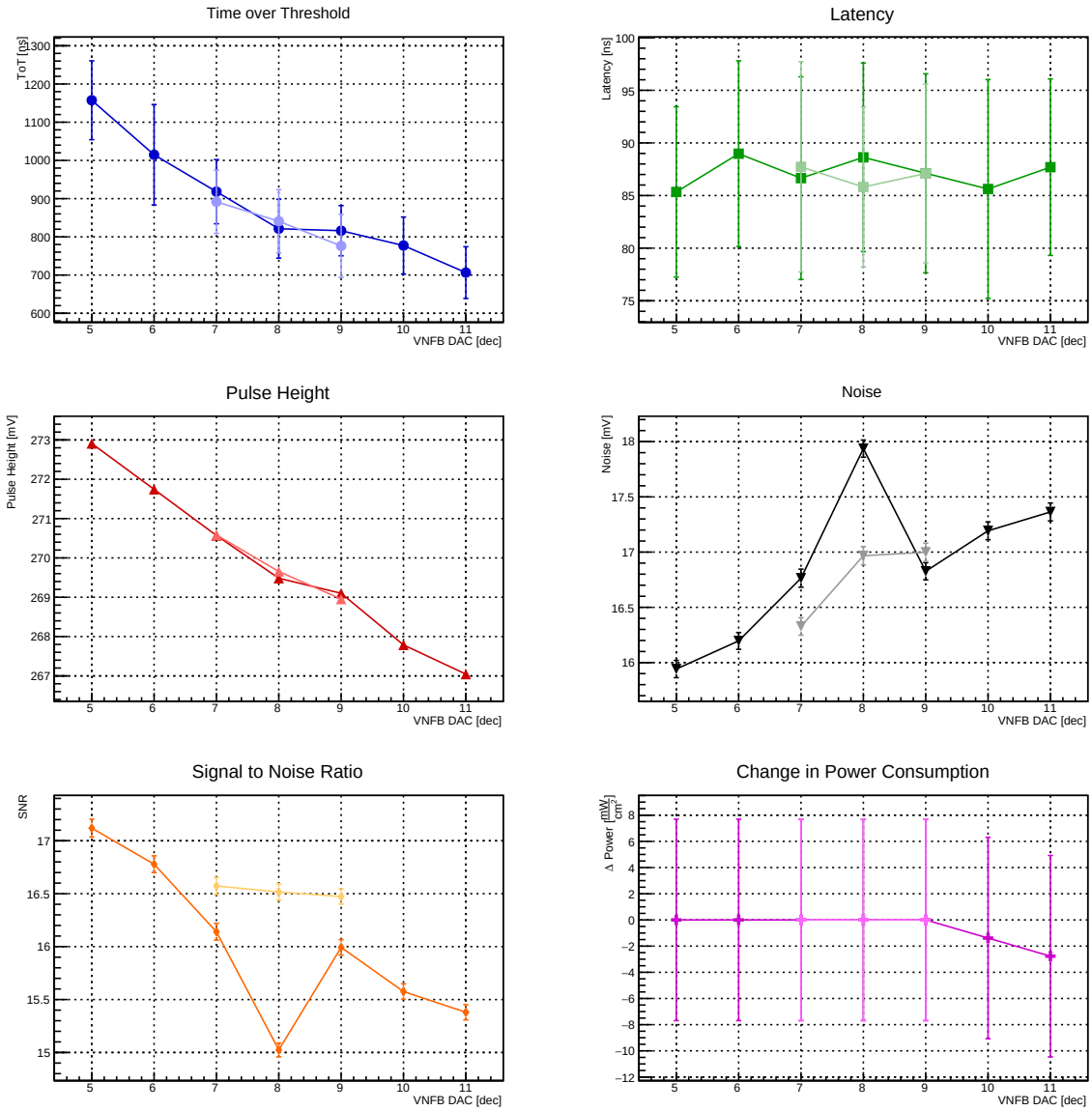


Figure C.2.: Variation of VNFB and its effect on ToT, latency, pulse height, SNR, and power consumption. Lighter colors indicate remeasured points in darkened lab.

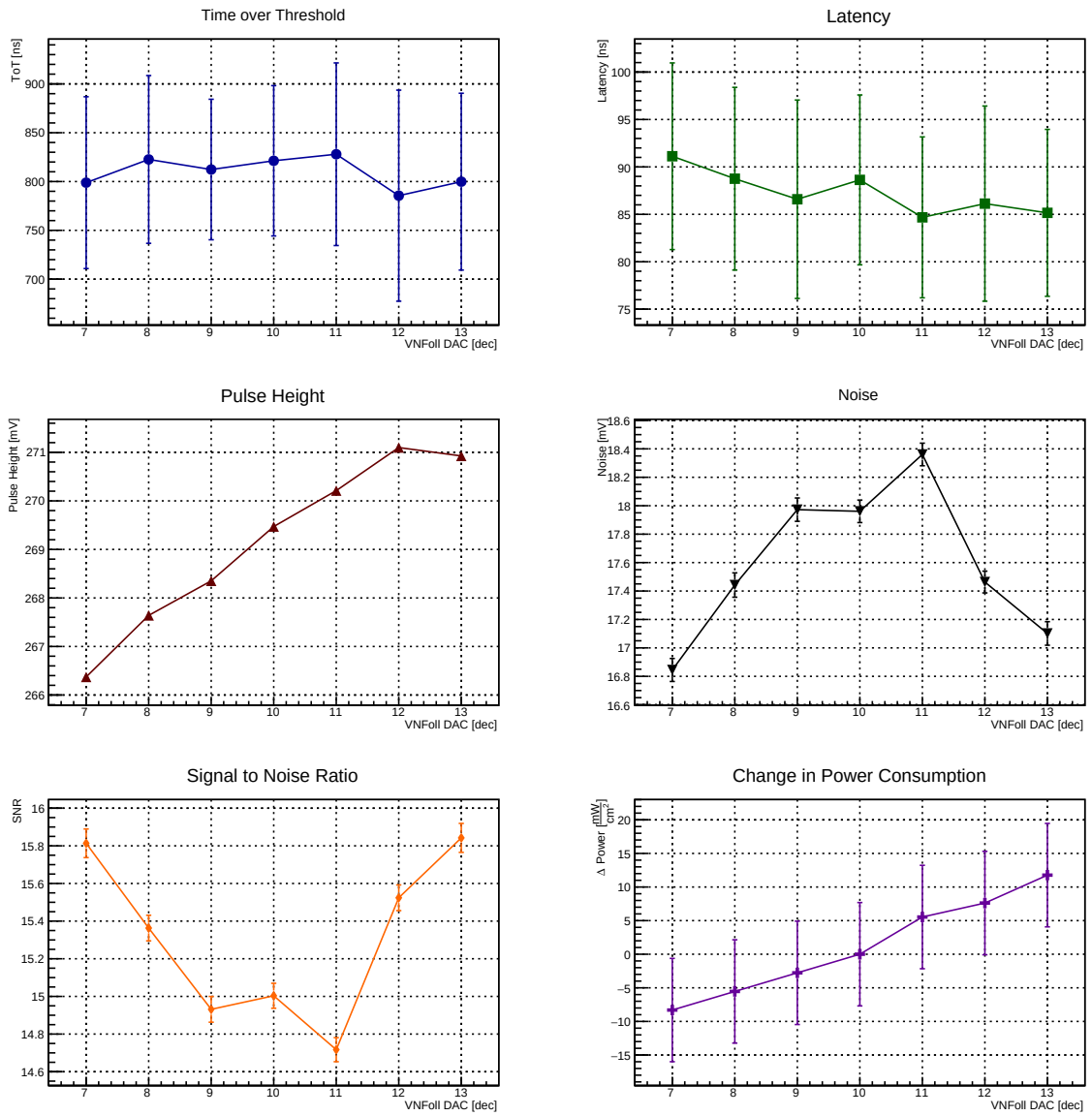


Figure C.3.: Variation of VNFoll and its effect on ToT, latency, pulse height, SNR, and power consumption.

D. Determination of New DAC Settings

D.1. First Amplifier

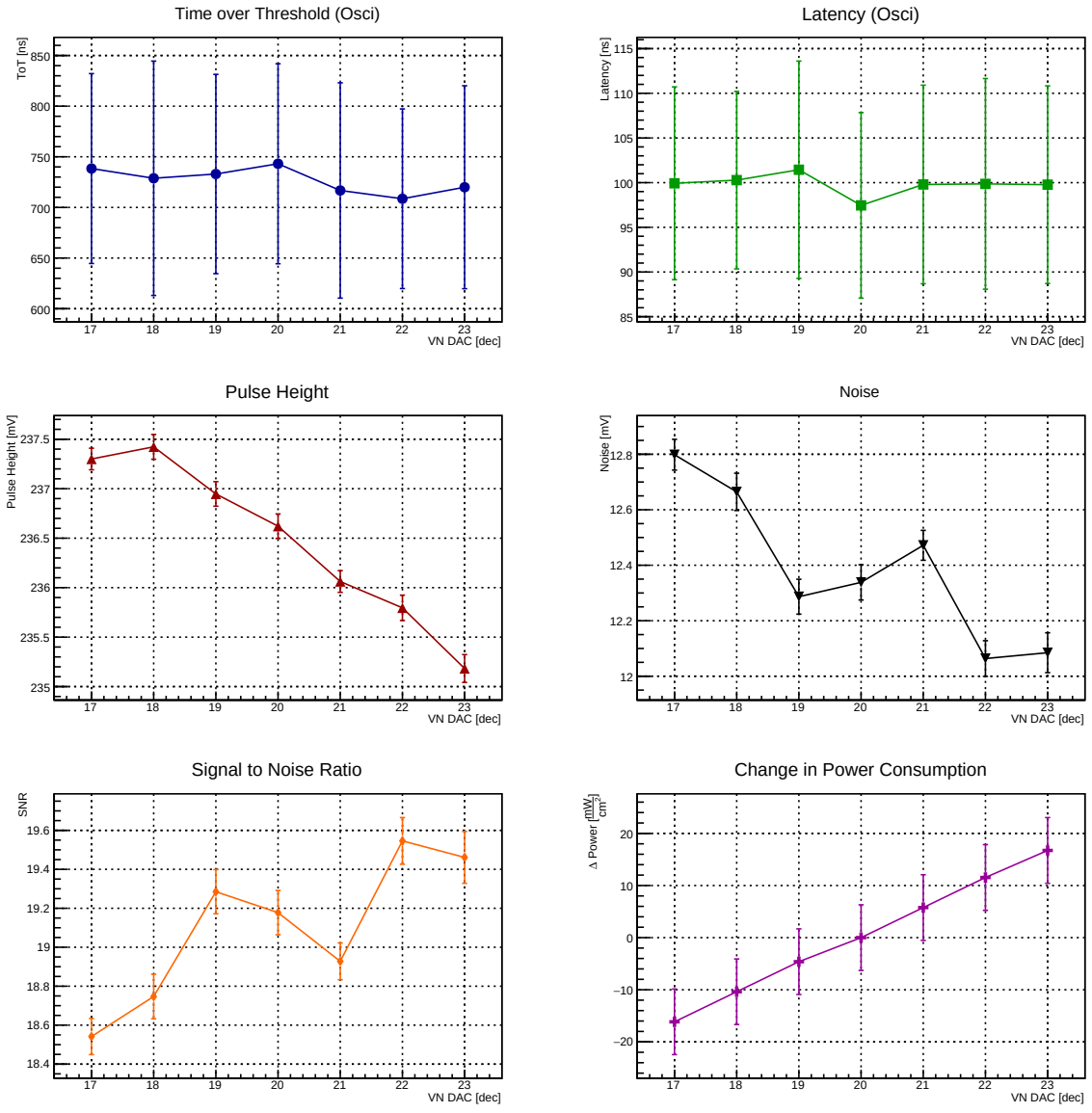


Figure D.1.: Variation of VN.

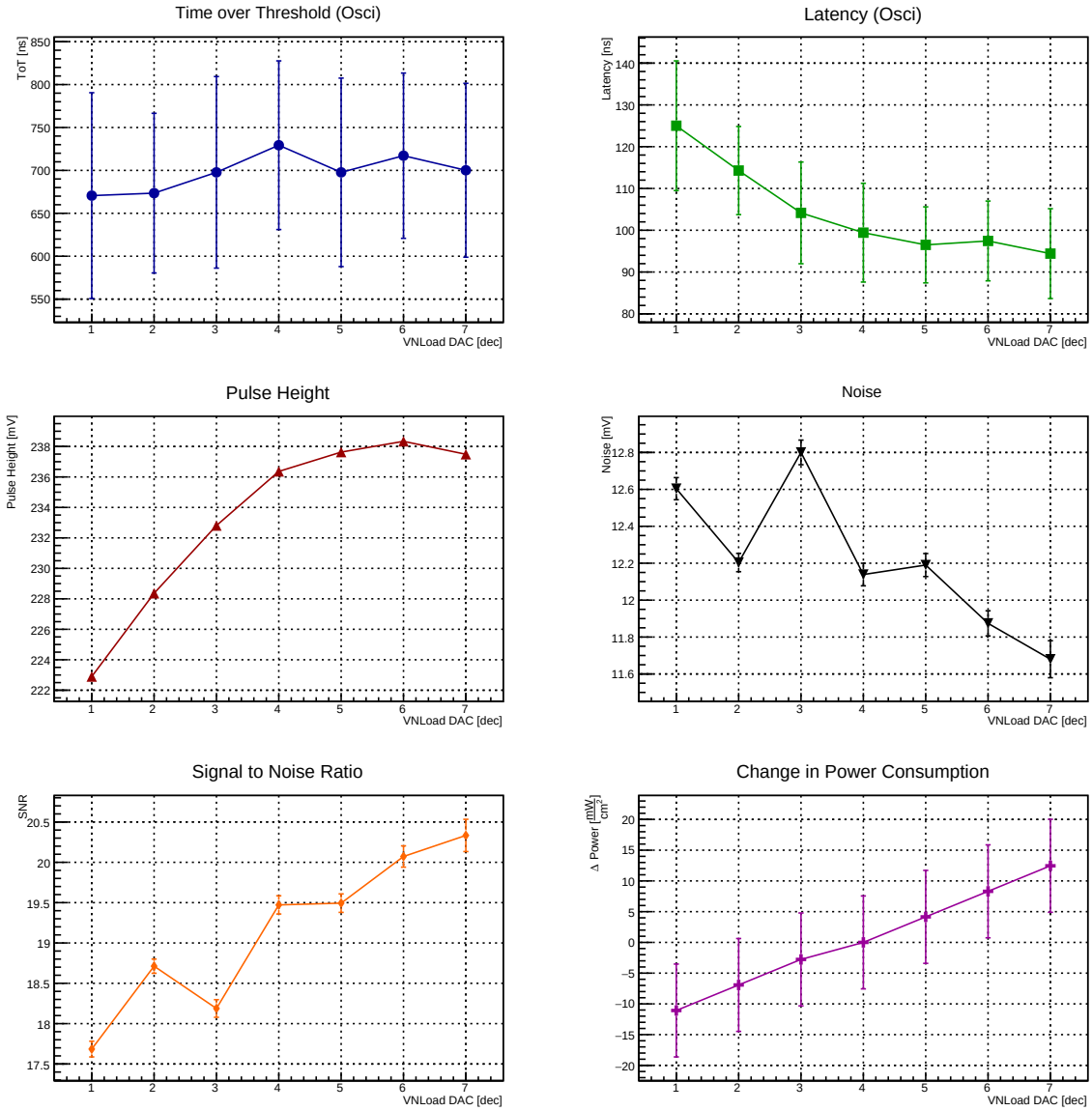


Figure D.2.: Variation of VNLoad.

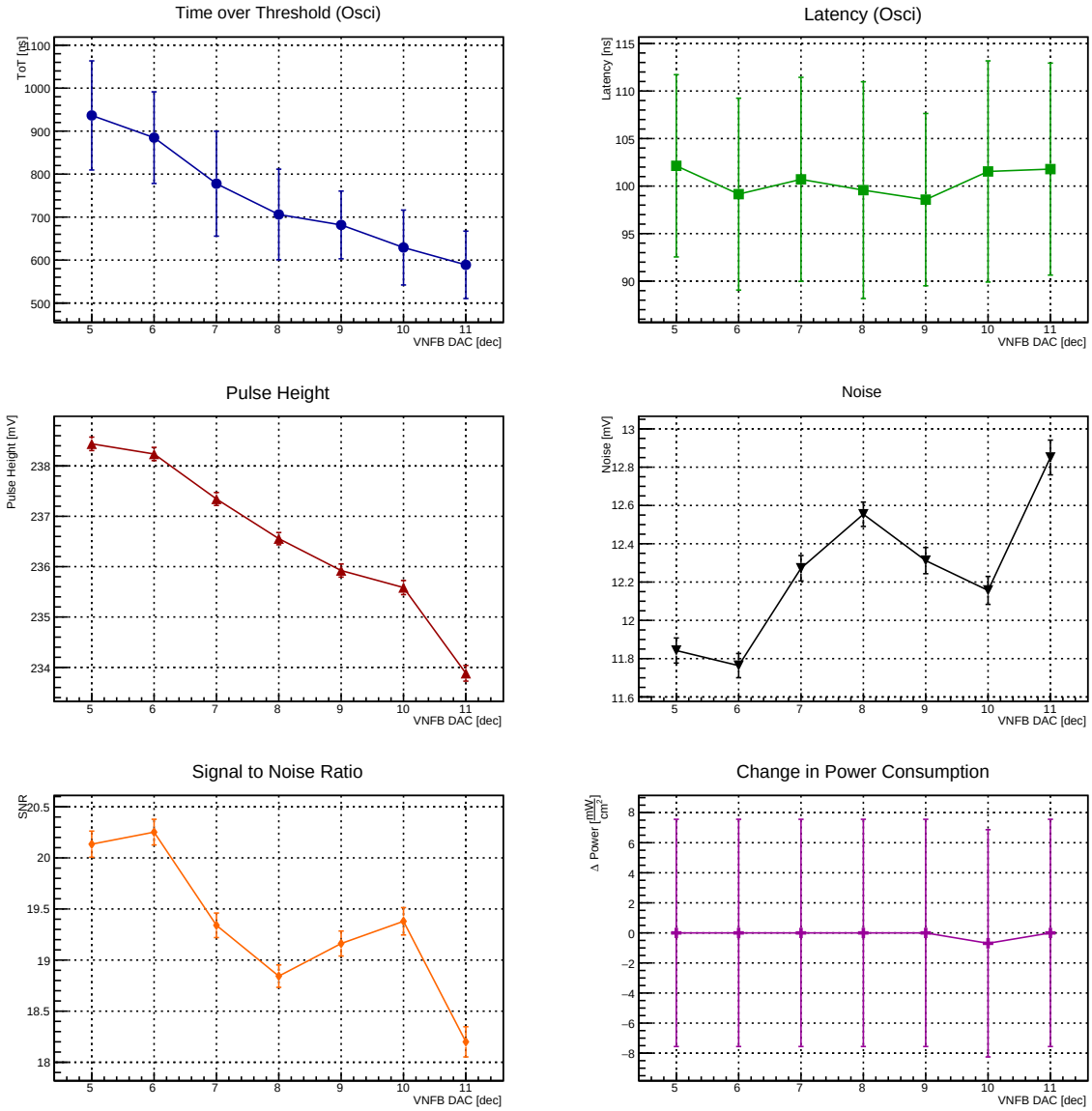


Figure D.3.: Variation of VNFB.

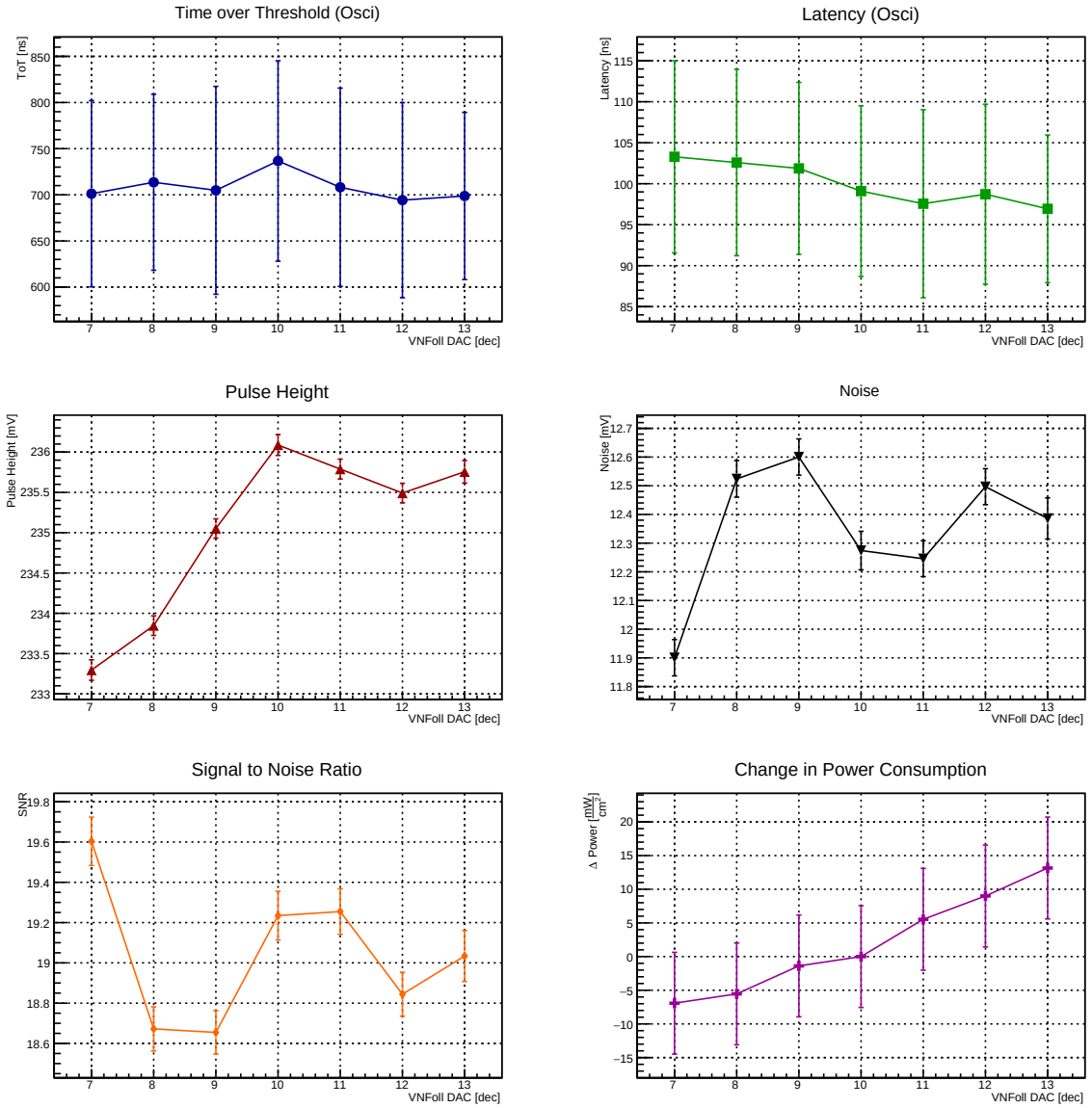


Figure D.4.: Variation of VNFoll.

D.2. Second Amplifier

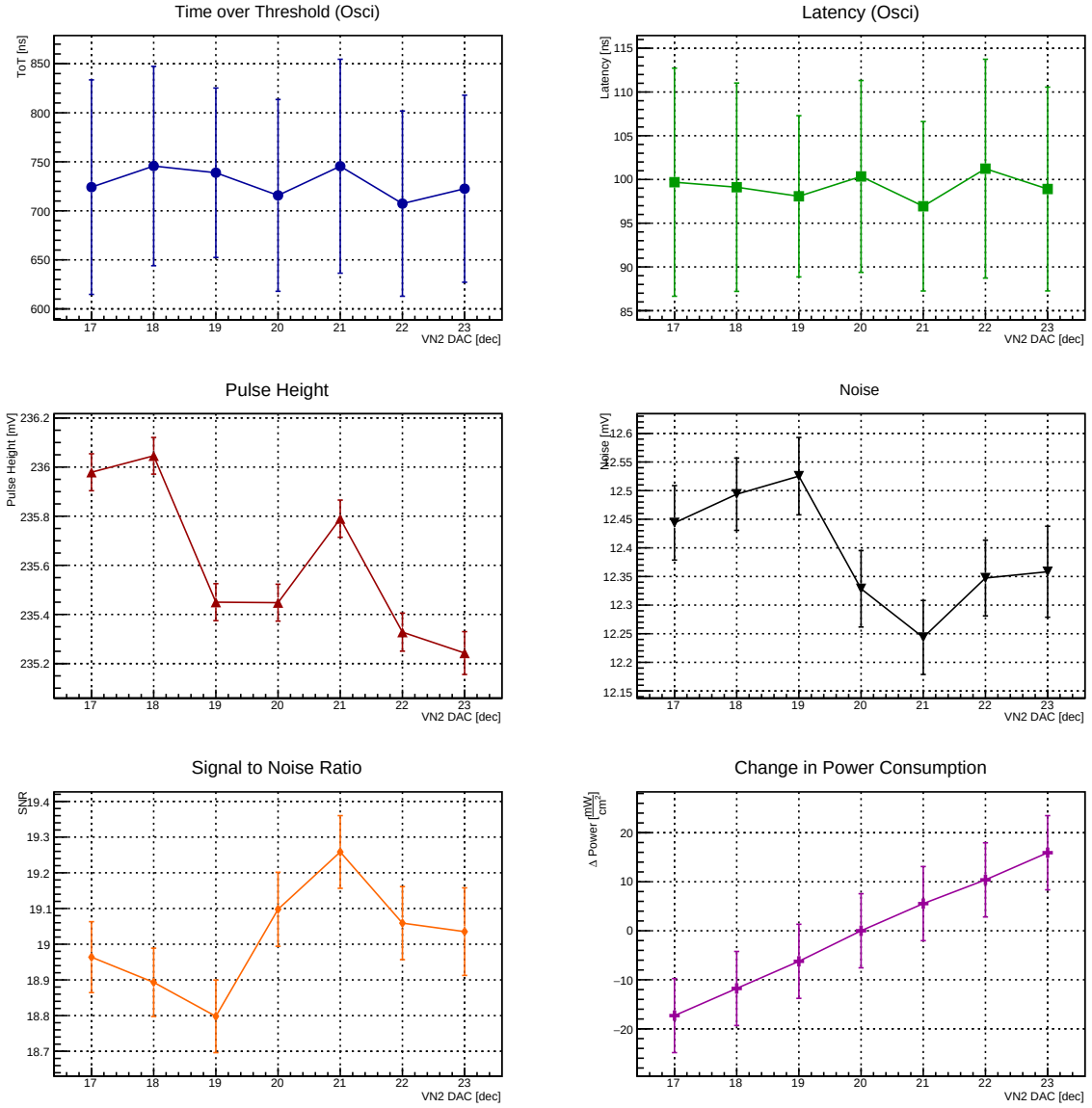


Figure D.5.: Variation of VN2.

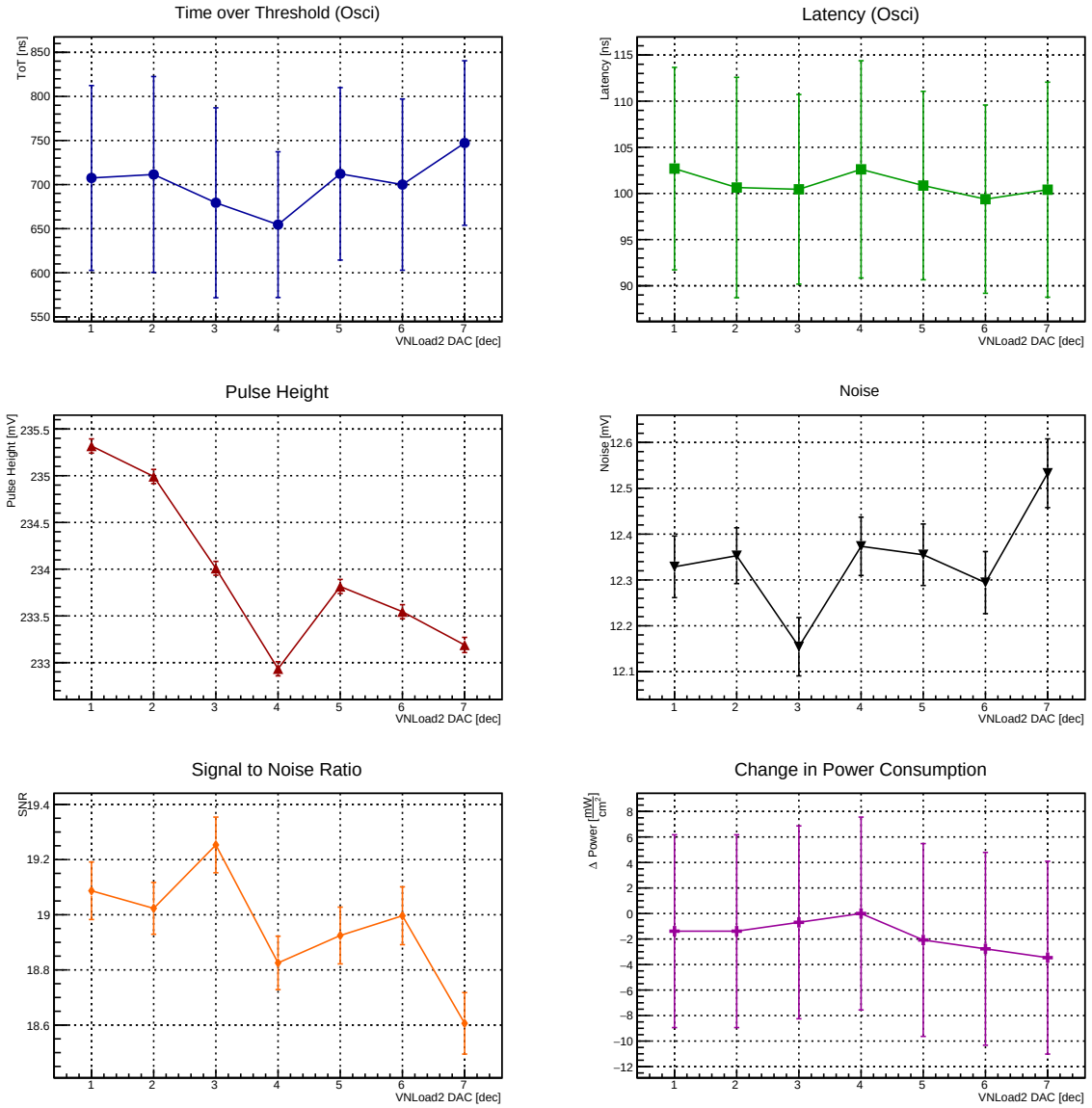


Figure D.6.: Variation of VNLoad2.

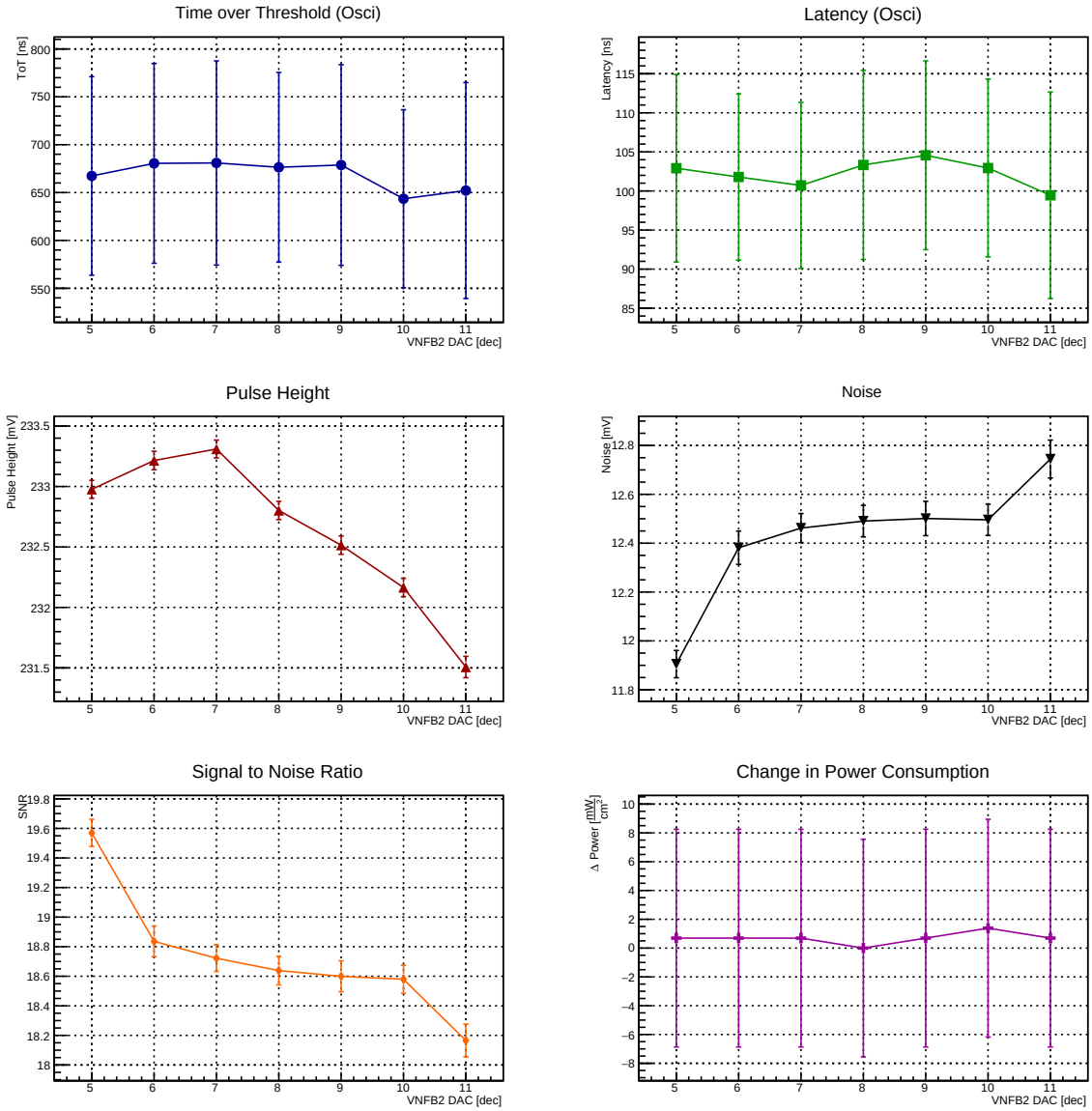


Figure D.7.: Variation of VNFB2.

D.3. Comparator

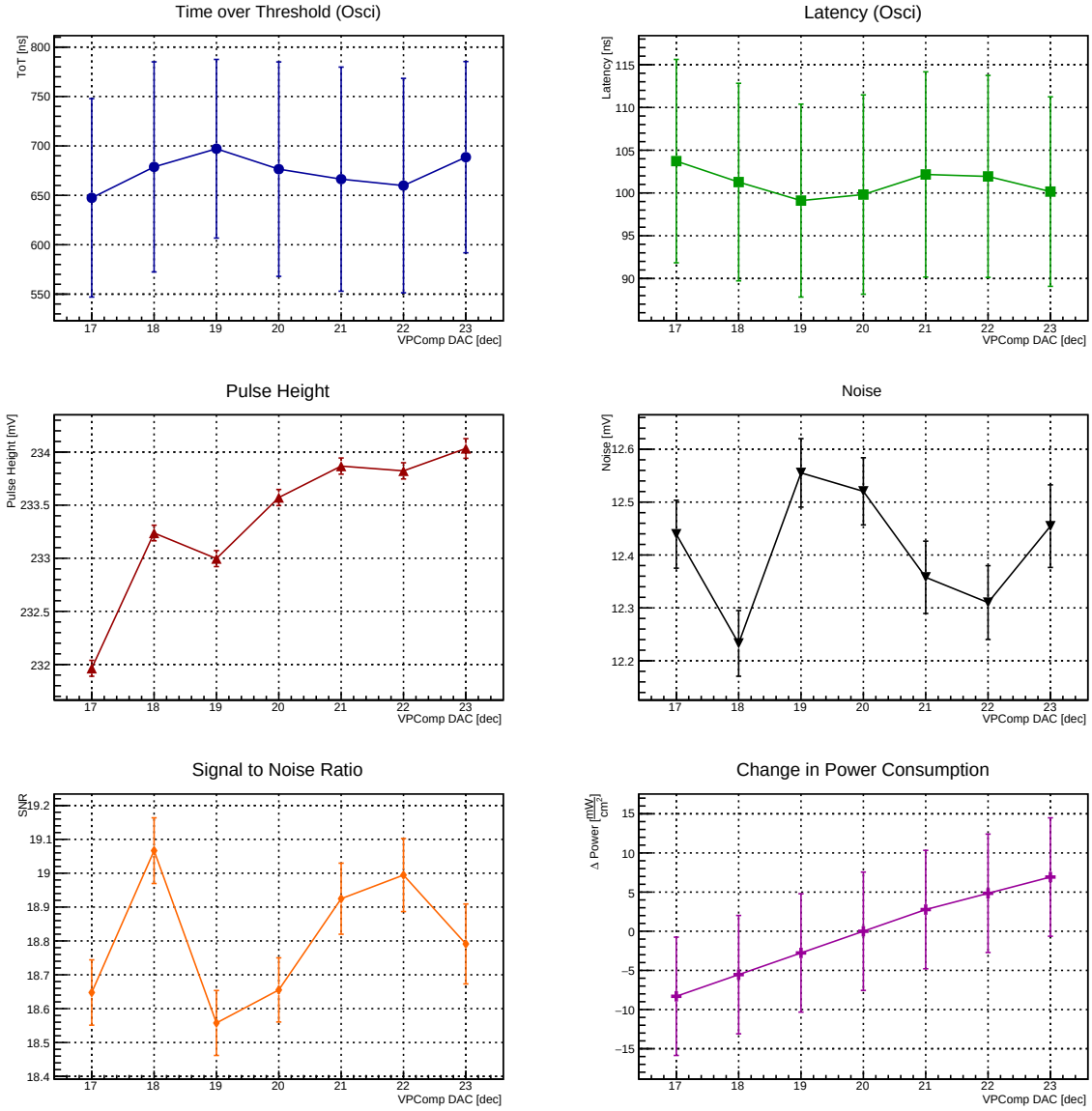


Figure D.8.: Variation of VPComp.

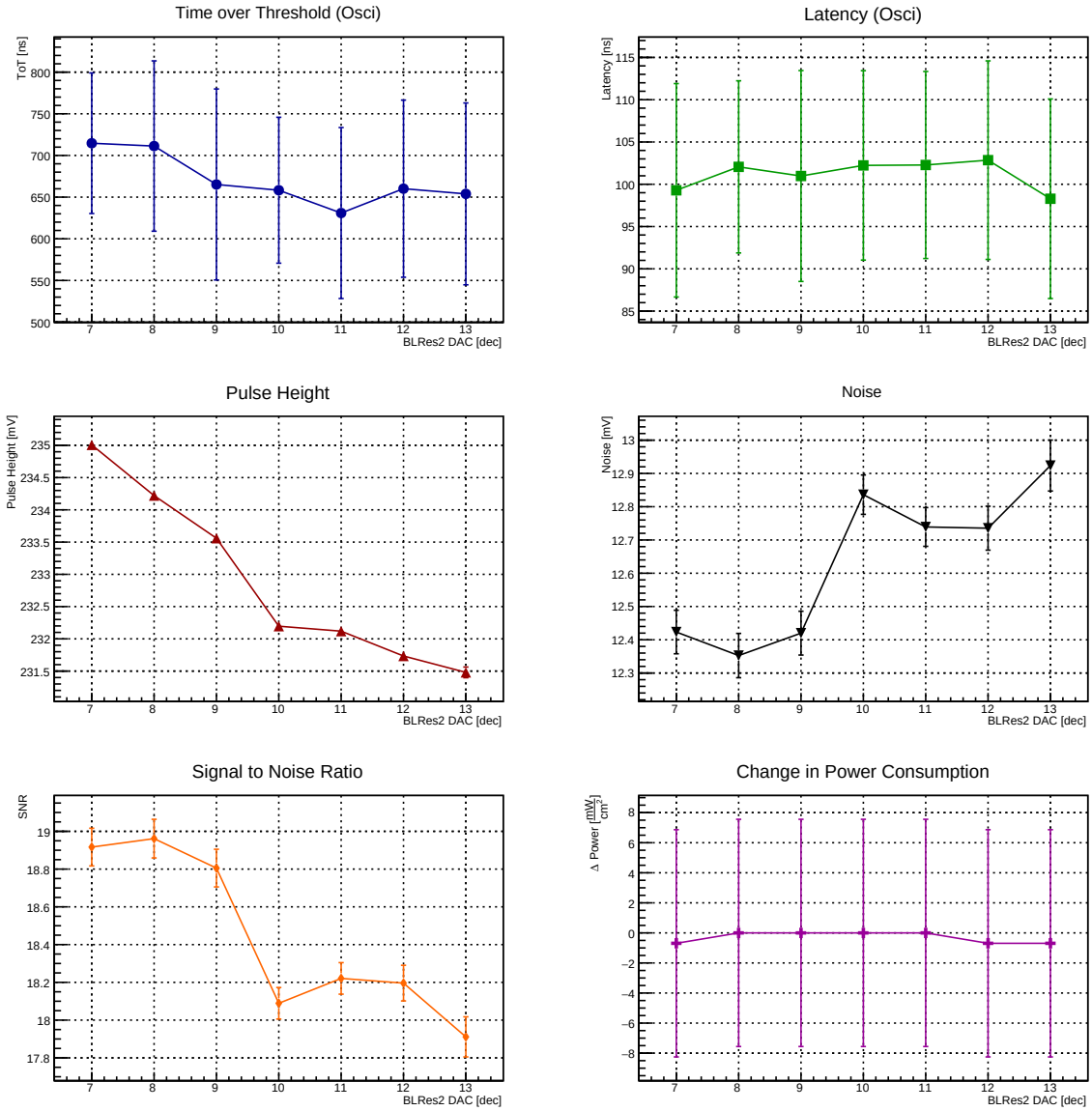


Figure D.9.: Variation of BLRes2.

E. PSI June 2016 Testbeam

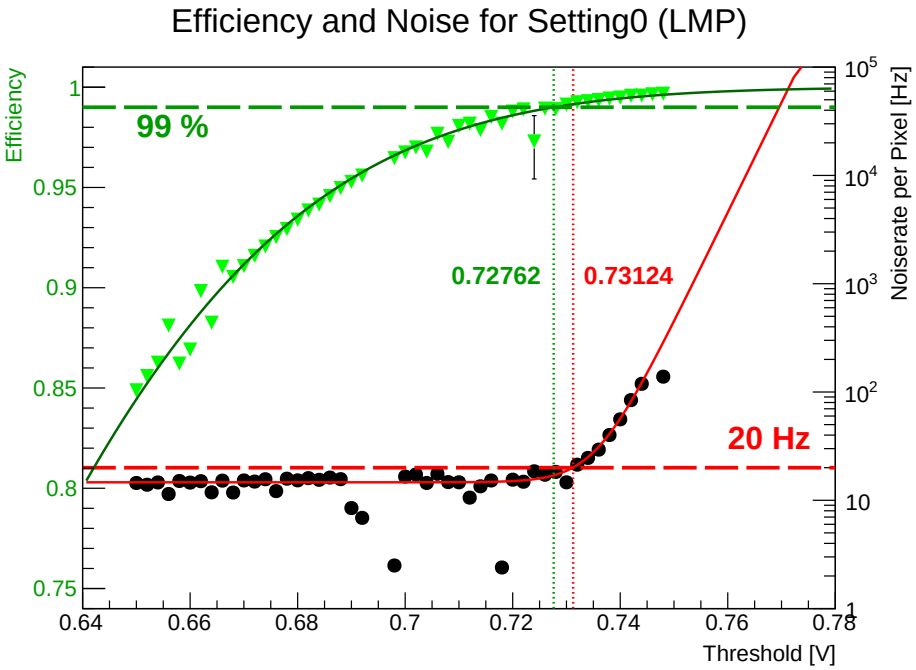


Figure E.1.: Efficiency and pixel noise rate fits for the LMP settings with standard tuning.

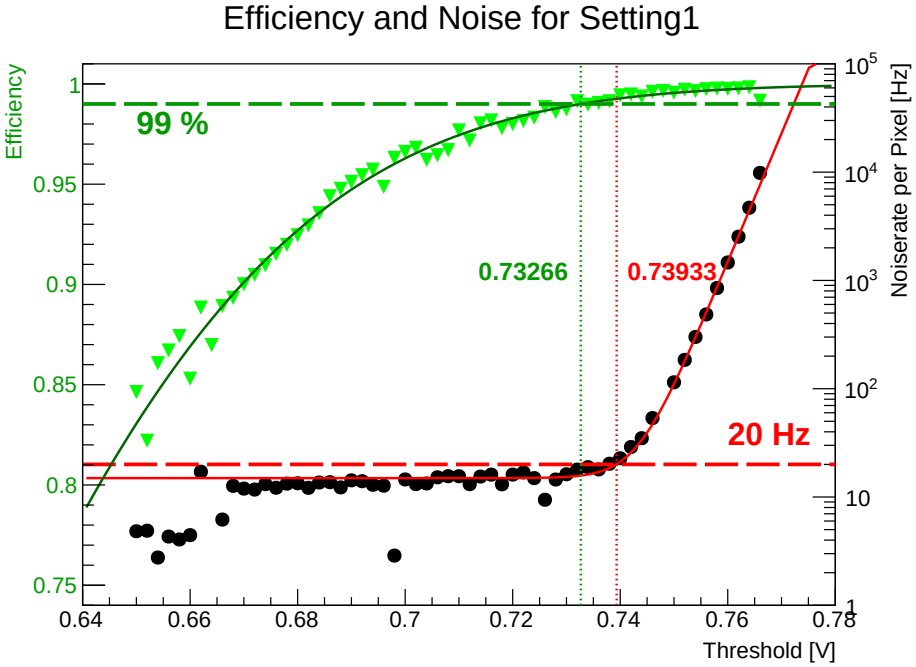


Figure E.2.: Efficiency and pixel noise rate fits for Setting1 with standard tuning.

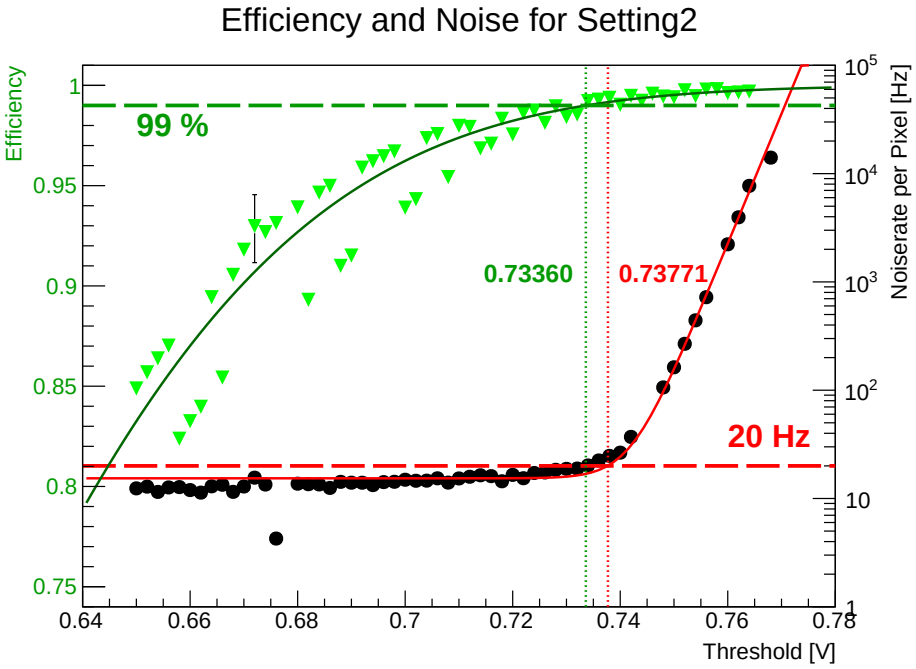


Figure E.3.: Efficiency and pixel noise rate fits for Setting2 with standard tuning.

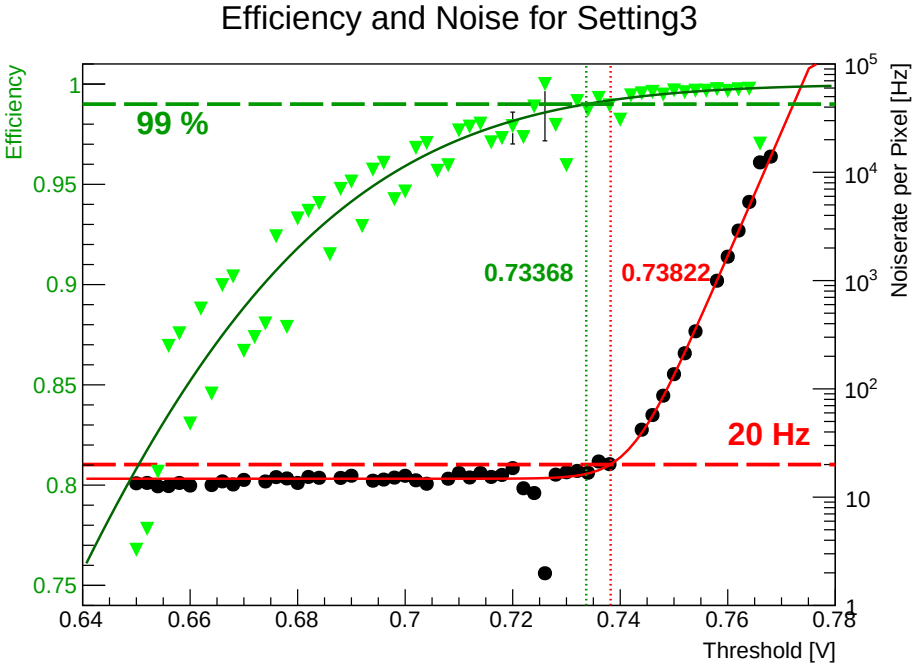


Figure E.4.: Efficiency and pixel noise rate fits for Setting3 with standard tuning.

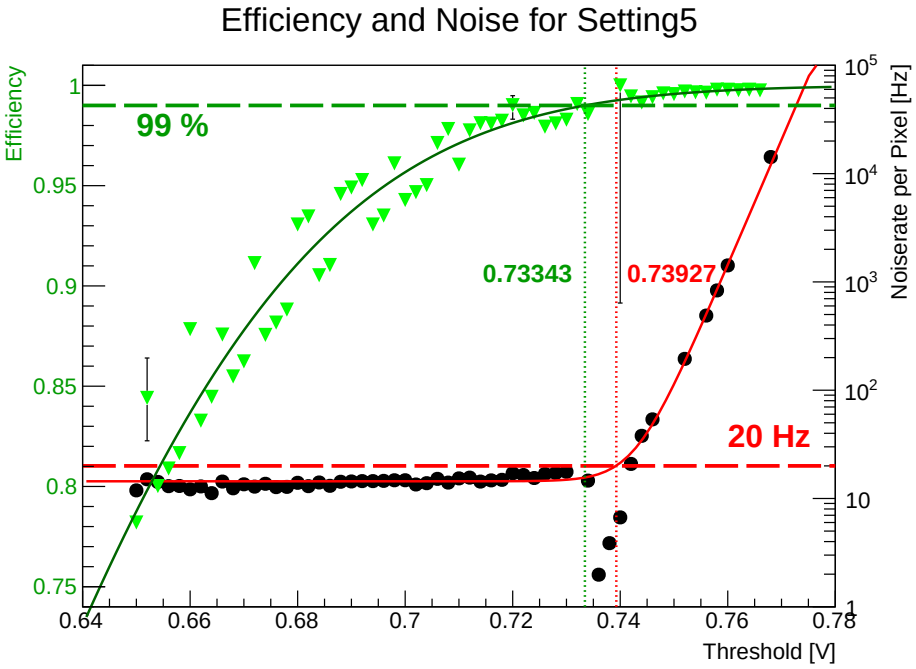


Figure E.5.: Efficiency and pixel noise rate fits for Setting5 with standard tuning.

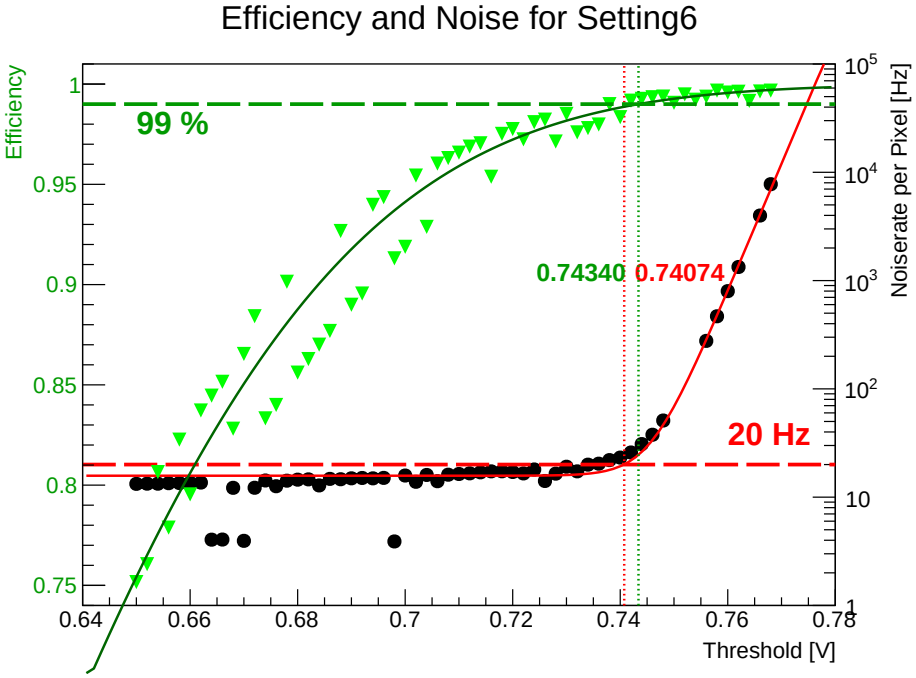


Figure E.6.: Efficiency and pixel noise rate fits for Setting6 with standard tuning.

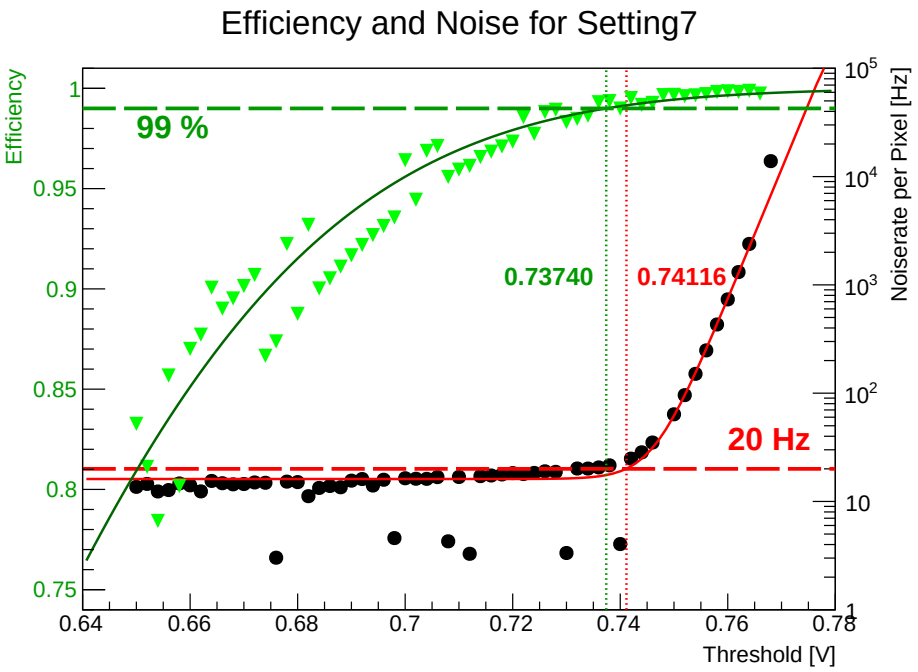


Figure E.7.: Efficiency and pixel noise rate fits for Setting7 with standard tuning.

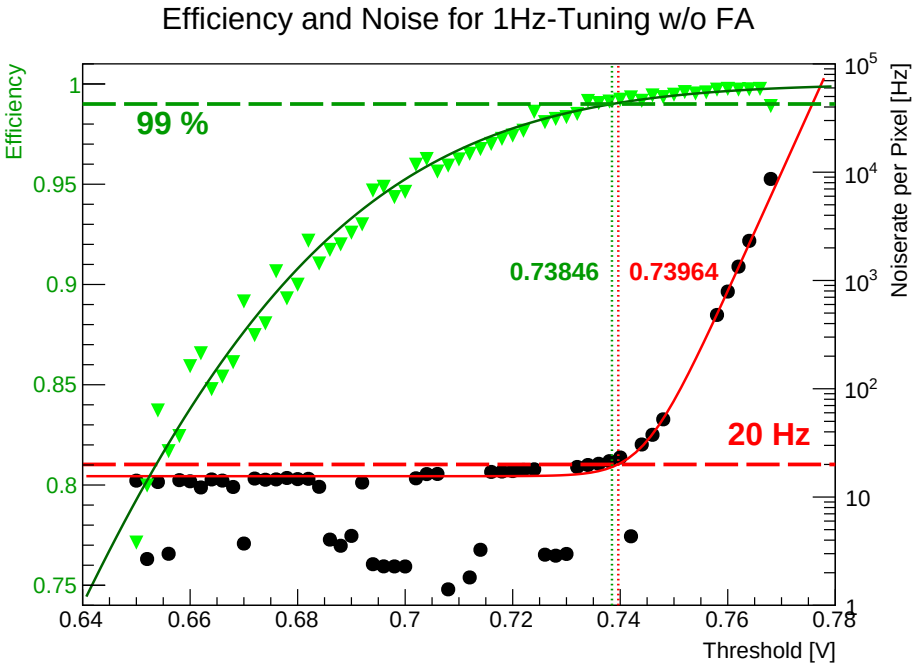


Figure E.8.: Efficiency and pixel noise rate fits for the LMP settings without fine adjustment after tuning.

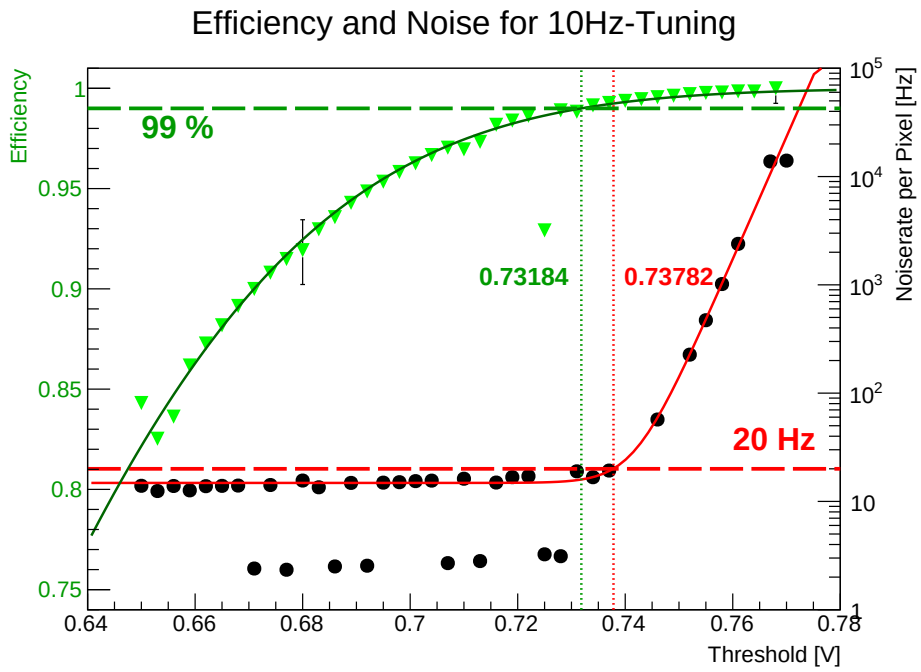


Figure E.9.: Efficiency and pixel noise rate fits for the LMP settings with 10 Hz tuning.

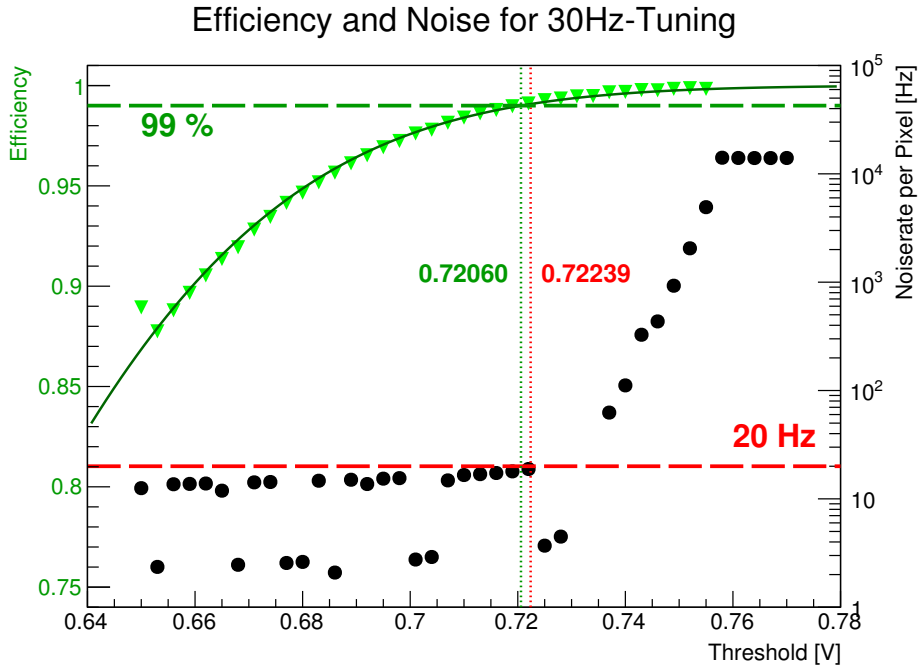
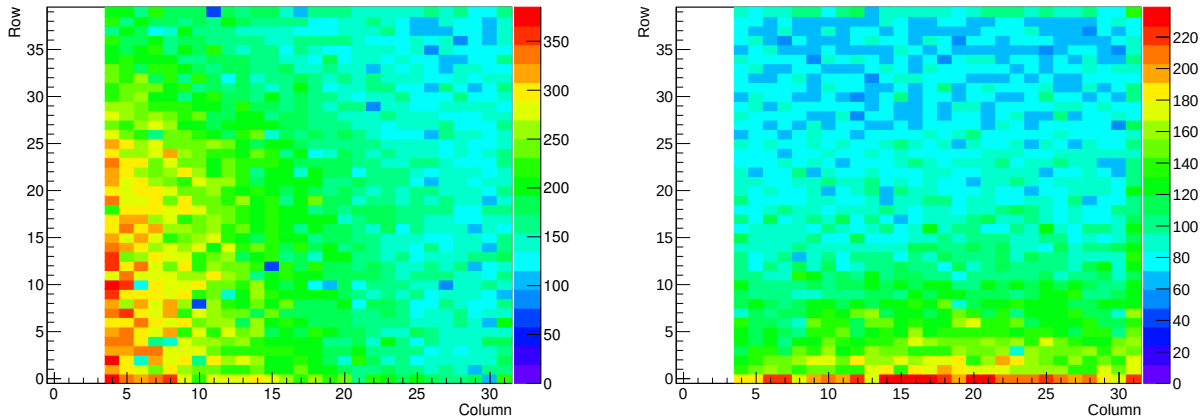


Figure E.10.: Efficiency fit for the LMP settings with 30 Hz tuning. The noise rate fit did not converge properly, the upper threshold limit was determined via linear interpolation of the noise rate points instead, excluding values of <10 Hz.

F. Lab-Efficiencies

F.1. Setup Alignment

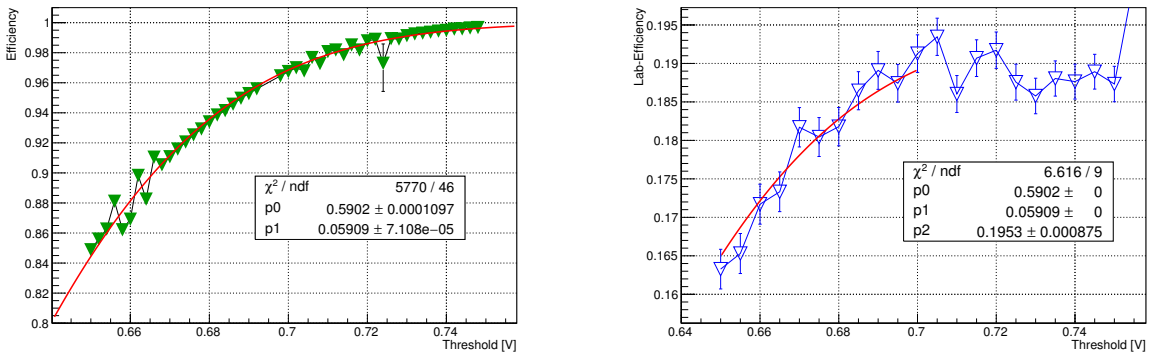


(a) Chip on PCB 7728.

(b) Chip on PCB 7714

Figure F.1.: Differences in single event distributions on the two chips due to different alignment.

F.2. Scaling Factor from Error Function Fit

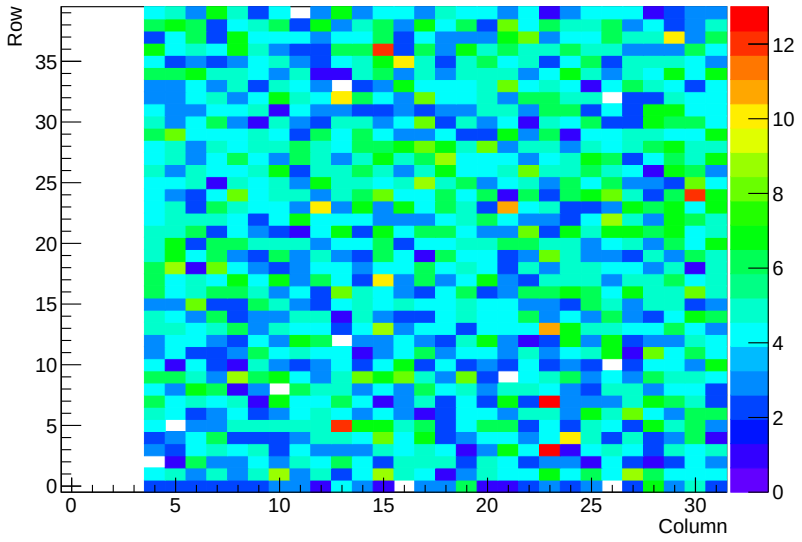


(a) Efficiency for chip on PCB 7714, LMP settings.

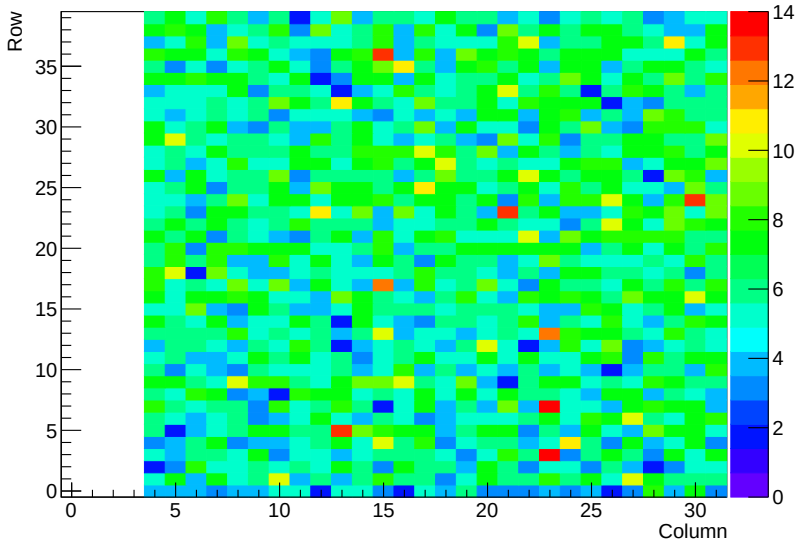
(b) Lab-efficiency for chip on PCB 7714, LMP settings. The scale factor calculates to $\frac{1}{p2} = 5.12 \pm 0.02$

Figure F.2.: Efficiencies and lab-efficiencies with error function fits. Mean and width for (b) taken from (a) and fixed.

F.3. Difference in Tuning before and after Testbeam



(a) Tuning used for testbeam measurements.



(b) Tuning used for lab-efficiency measurements.

Figure F.3.: TDAC maps of chip on PCB 7714 with LMP settings.

List of Figures

List of Tables

Bibliography

[1] A. Blondel et al. **Research Proposal for an Experiment to Search for the Decay $\mu \to$ eee**. *ArXiv 1301.6113*, 2013.

[2] I. Perić. **A novel monolithic pixelated particle detector implemented in high-voltage CMOS technology**. *Nuclear Instruments and Methods in Physics Research, A582 876-885*, 2007.

[3] Wikimedia Commons. **Standard Model of Elementary Particles**. *https://en.wikipedia.org/wiki/File:Standard_Model_of_Elementary_Particles.svg*, *accessed October 2016*.

[4] Particle Data Group. **Review of Particle Physics**. *Chin. Phys. C, Vol. 40, No. 10, accessed November 2016*, 2016.

[5] ATLAS Collaboration. **Observation of a New Particle in the Search for the Standard Model Higgs Boson with the ATLAS Detector at the LHC**. *ArXiv 1207.7214*, 2012.

[6] CMS Collaboration. **Observation of a new boson at a mass of 125 GeV with the CMS experiment at the LHC**. *ArXiv 1207.7235*, 2012.

[7] M. Kobayashi and T. Maskawa. **CP-Violation in the Renormalizable Theory of Weak Interaction**. *Progress of Theoretical Physics, Vol. 49, No. 2*, 1973.

[8] F. P. An et al. **Observation of electron-antineutrino disappearance at Daya Bay**. *ArXiv 1203.1669*, 2012.

[9] Q. R. Ahmad et al. **Measurement of the rate of $\nu_e + d \to p + p + e^-$ interactions produced by ^{8}B solar neutrinos at the Sudbury Neutrino Observatory**. *ArXiv nucl-ex/0106015*, 2001.

[10] Super-Kamiokande Collaboration. **Evidence for oscillation of atmospheric neutrinos**. *ArXiv hep-ex/9807003*, 1998.

[11] W. J. Marciano, T. Mori and J. M. Roney. **Charged Lepton Flavor Violation Experiments**. *Ann.Rev.Nucl.Part.Sci., 58: pp. 315–341, doi:10.1146/annurev.nucl.58.110707.171126*, 2008.

[12] SINDRUM Collaboration. **Search for the Decay $\mu^+ \to e^+e^-e^+$**. *Nucl.Phys., B299: p. 1, doi:10.1016/0550-3213(88)90462-2*, 1988.

[13] W. Bertl. **SINDRUM I**. *Presentation at PSI*, 2008.

[14] L. M. Barakov et al. **Search for $\mu^+ \to e^+\gamma$ down to 10^{-14} branching ratio**. *Research Proposal to PSI*, 1999.

[15] MEG Collaboration. **Search for the Lepton Flavor Violating Decay $\mu^+ \to e^+\gamma$ with the Full Dataset of the MEG Experiment**. *arXiv:1605.05081v3*, 2016.

[16] SINDRUM II Collaboration. **A search for $\mu - e$ conversion in muonic gold**. *Phys. J., C 47: 337, doi:10.1140/epjc/s2006-02582-x*, 2006.

[17] L. Morescalchi. **The Mu2e Experiment at Fermilab**. *ArXiv 1609.02021*, 2016.

[18] H. Natori. **DeeMe experiment – An experimental search for a mu-e conversion reaction at J-PARC MLF**. *Nuclear Physics B – Proceedings Supplements, Vol. 248-250, pp. 52-57, doi:10.1016/j.nuclphysbps.2014.02.010*, 2014.

[19] E. V. Hungerford. **COMET/PRISM – Muon to Electron Conversion at JPARC**. *AIP Conference Proceedings 1182, 694, doi:10.1063/1.3293903*, 2009.

[20] R. M. Djilkibaev, R. V. Konoplich. **Rare Muon Decay $\mu^+ \to e^+e^-e^+\nu_e\bar{\nu}_\mu$**. *arXiv:0812.1355*, 2008.

[21] H. Augustin. **Characterization of a novel HV-MAPS Sensor with two Amplication Stages and first examination of thinned MuPix Sensors**. *Master's Thesis, Physikalisches Institut, Heidelberg*, 2014.

[22] A. Damyanova. **Development of a Scintillating Fibre Tracker/Time-of-Flight Detector with SiPM Readout for the Mu3e Experiment at PSI**. *Master's Thesis, University of Geneva*, 2013.

[23] Y. Ng. **Finite Element Analysis of the Cooling System for the Mu3e Experiment**. *Master's Thesis, University of Applied Science, Jena / Physikalishes Institut, Heidelberg*, 2015.

[24] A. Herkert. **Gaseous Helium Cooling of a Thin Silicon Pixel Detector for the Mu3e Experiment**. *Master's Thesis, Physikalisches Institut, Heidelberg*, 2015.

[25] P. Sigmund. **Particle Penetration and Radiation Effects**. *Springer Series in Solid State Sciences, 151, Springer-Verlag*, 2006.

[26] S. Seltzer, M. Berger. **Improved Procedure for Calculating the Collision Stopping Power of Elements and Compounds for Electrons and Positrons** . *International Journal of Applied Radiation and Isotopes, Vol. 35, No. 7, doi:10.1016/0020-708X(84)90113-3*, 1984.

[27] W. R. Leo. **Techniques for Nuclear and Particle Physics Experiments**. *Springer-Verlag, ISBN: 3-540-17386-2, 0-387-17386-2*, 1987.

[28] Particle Data Group. **Review of Particle Physics**. *Physics Letters B, Vol. 592, No. 1–4,* `http://pdg.lbl.gov/2004/reviews/passagerpp.pdf`, 2004.

[29] J. C. Ashley. **Energy loss rate and inelastic mean free path of low-energy electrons and positrons in condensed matter**. *Journal of Electron Spectroscopy and Related Phenomena, Vol. 50, No. 2, doi:10.1016/0368-2048(90)87075-Y*, 1990.

[30] M. A. Green. **Intrinsic concentration, effective densities of states, and effective mass in silicon**. *Journal of Applied Physics, Vol. 67, No. 6, doi:10.1063/1.345414*, 1990.

[31] H. Spieler. **Semiconductor detector systems**. *Series on semiconductor science and technology; 12; Oxford science publications; Series on semiconductor science and technology. Oxford Univ. Press, Oxford [u.a.], repr. edition. ISBN:978-0-19-852784-8*, 2008.

[32] H. Philipp, E. Taft. **Optical Constants of Silicon in the Region 1 to 10 eV.** *Phys. Rev., Vol. 130, No. 37, doi:10.1103/PhysRev.120.37*, 1960.

[33] B. G. Lowe, R. A. Sareen. **A measurement of the electron-hole pair creation energy and the Fano factor in silicon for 5.9keV X-rays and their temperature dependence in the range 80-270K**. *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment, Vol. 576, No. 2-3, http://www.sciencedirect.com/science/article/pii/S016890020700527X*, 2007.

[34] F. Scholze, H. Henneken et al. **Determination of the electron-hole pair creation energy for semiconductors from the spectral responsivity of photodiodes**. *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment, Vol. 439, No. 2-3, http://www.sciencedirect.com/science/article/pii/S0168900299009377*, 2000.

[35] Wikimedia Commons. **Dotierung**. *https://de.wikipedia.org/wiki/Datei:Schema_-_n-dotiertes_Silicium.svg*, *https://de.wikipedia.org/wiki/Datei:Schema_-_p-dotiertes_Silicium.svg*, *accessed December 2016*, 2006.

[36] Wikimedia Commons. **P–N Junction**. *https://en.wikipedia.org/wiki/File:Pn-junction-equilibrium.png*, *accessed December 2016*, 2007.

[37] H. Kolanoski, N. Wermes. **Teilchendetektoren**. *Springer-Verlag, ISBN:978-3-662-45349-0, ISBN:978-3-662-45350-6 (eBook), doi:10.1007/978-3-662-45350-6*, 2016.

[38] W. Shockley. **Currents to Conductors Induced by a Moving Point Charge**. *Journal of Applied Physics 9, 635, doi:10.1063/1.1710367*, 1938.

[39] S. Ramo. **Currents Induced by Electron Motion**. *Proceedings of the IRE, Vol. 27, No. 9, doi:10.1109/JRPROC.1939.228757*, 1939.

[40] J. Baudot et al. **First Test Results of MIMOSA-26, a Fast CMOS Sensor with Integrated Zero Suppression and Digitized Output**. *IEEE Nuclear Science Symposium Conference Record (NSS/MIC), pp. 1169 – 1173, doi:10.1109/NSSMIC.2009.5402399*, 2009.

[41] I. Rubinskiy. **An EUDET/AIDA pixel beam telescope for detector development**. *Physics Procedia, Vol. 37, Proceedings of the 2nd International Conference on Technology and Instrumentation in Particle Physics (TIPP 2011), doi:10.1016/j.phpro.2012.02.434*, 2012.

[42] L. Huth. **Development of a Tracking Telescope for Low Momentum Particles and High Rates consisting of HV-MAPS**. *Master's Thesis, Physikalisches Institut, Heidelberg*, 2014.

[43] D. Immig. **Charakterisierung des VCO, der PLL und der Pulsform des MuPix7 in Abhängigkeit der Umgebungstemperatur**. *Bachelor's Thesis, Physikalisches Institut, Heidelberg*, 2016.

[44] I. Perić & N. Berger. **MuPix7 Data Format**. *http://www.physi.uni-heidelberg.de/Forschung/he/mu3e/wiki/images/0/09/Mupix7DataFormat.pdf*,*accessed December 2016*, 2015.

[45] A.-K. Perrevoort. **Characterisation of High Voltage Monolithic Active Pixel Sensors for the Mu3e Experiment**. *Master's Thesis, Physikalisches Institut, Heidelberg*, 2012.

[46] J. Hammerich. **Studies of HV-MAPS Analog Performance**. *Bachelor's Thesis, Physikalisches Institut, Heidelberg*, 2015.

[47] F. Förster. **HV-MAPS Readout and Direct Memory Access for the Mu3e Experiment**. *Master's Thesis, Physikalisches Institut, Heidelberg*, 2014.

[48] Altera Corporation. **Stratix IV Device Handbook Vol. 1**. *https://www.altera.com/content/dam/altera-www/global/en_US/pdfs/literature/hb/stratix-iv/stratix4_handbook.pdf, accessed January 2017*, 2016.

[49] M. Kiehn. **FPGA driver**. *Private Communication.*

[50] The Qt Company. **Qt | Cross-platform software development for embedded & desktop**. *https://www.qt.io/, accessed February 2017.*

[51] B. Dawes, D. Abrahams, R. Rivera. **Boost C++ Libraries**. *http://www.boost.org/, accessed February 2017.*

[52] S. Bachmann. **Experimental techniques in nuclear and particle physics in the Advanced Students Laboratory of the Universität Heidelberg**. *Lab course instructions, http://www.physi.uni-heidelberg.de/~bachmann/Lehre/F80_Anleitung.pdf, accessed January 2017.*

[53] H. Augustin et al. **MuPix7 – A fast monolithic HV-CMOS pixel chip for Mu3e**. *JINST 11 C11029, ArXiv 1610.02210*, 2016.

[54] HAMEG® Instruments. **Power Supply HMP4030 HMP4040 Manual**. *http://www.testequipmentdepot.com/hameg/pdf/hmp4030_4040-manual.pdf, accessed October 2016*, 2009.

[55] J. Philipp. **Effizienzanalyse von HV-MAPS anhand des MuPix-Teleskops**. *Bachelor's Thesis, Physikalisches Institut, Heidelberg*, 2015.

[56] A. Blondel et al. **Technical Design of the Phase I Mu3e Experiment**. *TDR in preparation (internal)*, 2016.

[57] F. Meier Aeschbacher. **MuPix7 – A fast monolithic HV-CMOS pixel chip for Mu3e**. *8th International Workshop on Semiconductor Pixel Detectors for Particles and Imaging – Presentation, https://agenda.infn.it/contributionDisplay.py?contribId=128&sessionId=10&confId=10190, accessed December 2016*, 2016.

[58] C. M. Grinstead & J. L. Snell. **Introduction to Probability**. *Dartmouth College, https://www.dartmouth.edu/~chance/teaching_aids/books_articles/probability_book/amsbook.mac.pdf, accessed March 2017.*

Acknowledgments

At this point, I want to express my gratitude to everyone who supported me throughout my work on this thesis.

First and foremost, I would like to thank my supervisor Prof. André Schöning for giving me the opportunity to work on this interesting project. I would also like to thank Prof. Norbert Herrmann, who agreed to be the second examiner for my thesis.

My thanks also go to all my colleagues in the Mu3e group for their help an support, as well as the fun time I had with them. Especially I want to thank:

- Heiko Augustin for his support and the great time we had ever since we started our studies together.
- David Immig, Sebastian Dittmeier, Jan Hammerich, and Jens Kröger for the enjoyable working environment and, in case of the latter three, for the much appreciated review(s) of my thesis.
- Lennart Huth for his reviews and the much appreciated support during testbeam campaigns and the help with the analysis of the acquired data.
- Dirk Wiedner for his support, his insightful comments on my work, and the fun time in this group.

Finally, I want to thank my family, who gave me the opportunity to study physics in Heidelberg and for their support throughout this time.

Thanks, everybody!

Erklärung

Hiermit versichere ich, dass ich diese Arbeit selbstständig verfasst habe und keine anderen als die angegebenen Quellen und Hilfsmittel verwendet habe.

Heidelberg, den 12. April 2017 .....