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Characterization of a novel HV-MAPS Sensor with two Amplification Stages and first examination of thinned MuPix Sensors

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Abstract The Mu3e experiment searches for the lepton flavor violating decay $\mu^+ \to e^+e^-e^+$ which is heavily suppressed in the Standard Model (SM) with a branching ratio below 10^{-54}. The observation of a signal would be a clear sign for new physics. To achieve the projected sensitivity of 1 in 10^{16} muon decays, background processes have to be suppressed below this level. Thus the experiment has to provide a good momentum, time and vertex resolution in an environment with muon decay rates up to $\mathcal{O}(10^9\ s^{-1})$.
Due to the low energetic decay particles of maximal 53 MeV, multiple scattering in the detector components is limiting the momentum and vertex resolution. As a result the material budget of the detector has to be minimized. Therefore, the tracking detector consists of novel silicon detectors, fabricated in High-Voltage Monolithic Active Pixel (HV-MAPS) technology, which can be thinned down to $50\mu m$. This allows to reduce the material budget to $\sim 1‰$ radiation length per tracking layer. The HV-MAPS technology incorporates active pixel sensors and readout electronics on a single chip and uses a depleted diode for fast charge collection.
In this thesis a framework was developed to test and characterize the MuPix6 HV-MAPS prototype which introduces a new two staged amplification scheme, aiming to amplify the signal pulses by a factor of 3 compared to previous prototypes. Besides, for the first time ever industrially thinned $50\mu m$ MuPix4 sensors have been available for testing.
First characterization results from measurements in the laboratory and from testbeam campaigns with a 250 MeV pion beam are presented. A pixel signal-to-noise ratio (SNR) of 15 was determined for a Fe-55 equivalent signal and the chip time resolution was measured to be 16 ns. The MuPix6 performance is consistent with the performance of the previous MuPix4 prototype and provides a safety margin against digital cross talk through the enhanced signal. Further, thinned MuPix4 sensors have been tested and no significant performance impairment has been observed.

Zusammenfassung Das Mu3e Experiment sucht nach dem Leptonflavorzahl-verletzenden Zerfall $\mu \to eee$, welcher im Standard Model der Teilchenphysik mit einem Verzweigungverhältnis von weniger als 10^{-54} sehr stark unterdrückt ist. Jedes beobachtete Signalereignis ist somit ein klares Zeichen für neue Physik. Um die angestrebte Sensitivität von einem in 10^{16} Zerfällen erreichen zu können, müssen Beiträge von Hintergrundprozessen unter diese Schwelle reduziert werden. Somit muss der Detector eine sehr gute Zeit-, Impuls- und Vertexauflösung bereitstellen, bei bis zu 10^9 Myonzerfällen pro Sekunde.
Aufgrund der niedrigen Energie der Zerfallsteilchen werden diese im Detektor Material stark gestreut, wodurch die Impuls- und Vertexauflösung begrenzt ist. Somit müssen die Detektorlagen möglichst dünn sein. Der Spurdetektor wird daher aus dünnen, neuartigen Siliziumsensoren gebaut, die sogenannten hochspannungsgetriebenen monolitischen aktiven Pixelsensoren (HV-MAPS), welche auf $50\mu m$ Dicke gedünnt werden können. Somit reduziert sich die Materialmenge auf $\sim 1‰$ Strahlungslänge. Die HV-MAPS Technologie kombiniert aktive Pixelsensoren und Ausleseelektronik auf einem Chip und benutzt eine in Sperrrichtung betriebene Diode zur Detektion ionisierende Strahlung, die eine schnelle Ladungssammlung garantiert.
In Rahmen dieser Arbeit wurde ein Testsetup entwickelt, um die MuPix6 Chips zu testen und zu charakterisieren. Im MuPix6 Prototyp wird eine neue zwei-stufige Signalverstärkung getestet, die das Signal um einen Faktor 3 zusätzlich verstärken soll. Außerdem können erstmals industriell gedünnte $50\mu m$ MuPix4 Sensoren untersucht werden. Erste Charakterisierungsergebnisse aus Labor und Teststrahl Messungen werden vorgestellt. Ein Pixel-Signal-zu-Rausch-Verhältnis (SNR) von 15 wurde für ein auf Fe-55 geeichtes Signal gemessen und die Zeitauflösung des Chips zu 16 ns bestimmt. Der MuPix6 stellt ein mit den MuPix4 Prototypen vergleichbares SNR bereit und bietet zusätzlich eine Sicherheit gegen digitales Übersprechen auf Grund des erhöhten Signals. Desweiteren wurden gedünnten Chips untersucht und kein Einfluss des Dünnens auf das Chipverhalten festgestellt.

Contents

Part I

Introduction

1 Introduction

Today's knowledge about particle physics is summed up in the Standard Model, which describes all known elementary particles and their interactions. In spite of its precise experimental predictions, it leaves many phenomena unexplained, e.g. the nature of gravity or the mass hierarchy. The lag of prediction for these open questions triggers the development of new theories giving rise to new phenomena not described by the Standard Model. Since non of these effects has been observed so far, the mass scale at which new physics comes into play is currently beyond our reach.

However, there are two approaches to search for new physics phenomena. One is the direct search for new physics in the form of new particles or processes at the high energy frontier by increasing the energy of colliders further, e.g. at the Large Hadron Collider (LHC). Although the direct observation of those new phenomena could only be performed at high energies, due to the quantum nature of particle physics their presence also manifests as small deviations from standard model predicted values for well known quantities, since they can enter in loops and enhance the branching ratios for rare standard model decays. As those measurements often require sub-parts-per-billion precision, they also necessitate large data samples.

The MU3E experiment is a proposed precision experiment searching for the lepton flavor violating decay $\mu \to eee$ with a branching fraction sensitivity of 1×10^{-16} at 90% confidence level [1].

To reach this goal in a reasonable amount of time the experiment needs to observe 2×10^9 muon decays per second, which are provided by stopping a muon beam on a target produced at the High Intensity Proton Accelerator (HIPA) at the Paul Scherrer Institut(PSI) in Switzerland. The detector is made up of cylindrical layers of pixel, fiber and tile detectors along the beam axis, which forms a spectrometer with a very good vertex, momentum and time resolution.

As the maximum momentum of the decay particles is fixed to 53 MeV, half the muon mass, multiple coulomb scattering is a very dominant effect and constrains the material budget of the detector to achieve a good momentum resolution.

To meet this constrain, very thin layers of silicon pixel detectors are necessary without impairments on their performance. The technology which was proven in the past to have a very high potential and suitability for this experiment are pixel sensors called HV-MAPS produced in commercial high voltage CMOS processes. This technology combines the advantages of producing detector and readout on the same chip (MAPS) with a depleted diode as active detector volume. As for this process the thickness of the depletion layer is around 10 µm the bigger part of the wafers depth is unused and allows to thin the sensors down to 50 µm thickness including metal layers.

In the following the characterization results obtained for the MuPix6 prototype as well as for the first industrially thinned MuPix4 sensors are presented. The setup and the prototypes have been tested as well in the lab as on testbeam campaigns at PSI with a 250 MeV pion beam which allows precise timing measurements and also efficiency determination with the recently developed MuPix telescope.

The MuPix6 prototype introduces a new amplification scheme consisting of two amplification stages instead of one as for previous prototypes. The pulses created by the pixel electronics are investigated with respect to their dependencies of the high voltage and the bias voltages. The power consumption of the chip is measured and an optimisation of the bias voltage settings to reduce the power consumption is performed. The signal-to-noise ratio (SNR) of the new pixel architecture is determined and scattering of pixel properties is discussed. Further the time resolution of the chip is measured from testbeam data for the chip as whole and for a single pixel.

Good SNR values and pixel behaviors have been found for the MuPix6 amplification scheme, which can be compared to the values obtained for MuPix4. This comparison reveals a amplification factor of $\sim$ 3 for the second amplification stage as expected, creating a safety margin against digital cross talk for high frequency signals.

Furthermore the first industrial thinned chips have been investigated in parallel, showing no influence of the thinning process on the chips performance.

2 Theory

2.1 The Standard Model of Particle Physics

The Standard Model of Particle Physics (SM) is a quantum field theory describing the fundamental constituents of matter and their interactions. It consists of twelve fermionic elementary particles, their anti-particles and six bosons. Three fundamental interactions are described by the electro-magnetic, weak and strong interaction. Gravitation can not be included in the SM, but can be ignored as its effect is negligible compared to the other interactions.

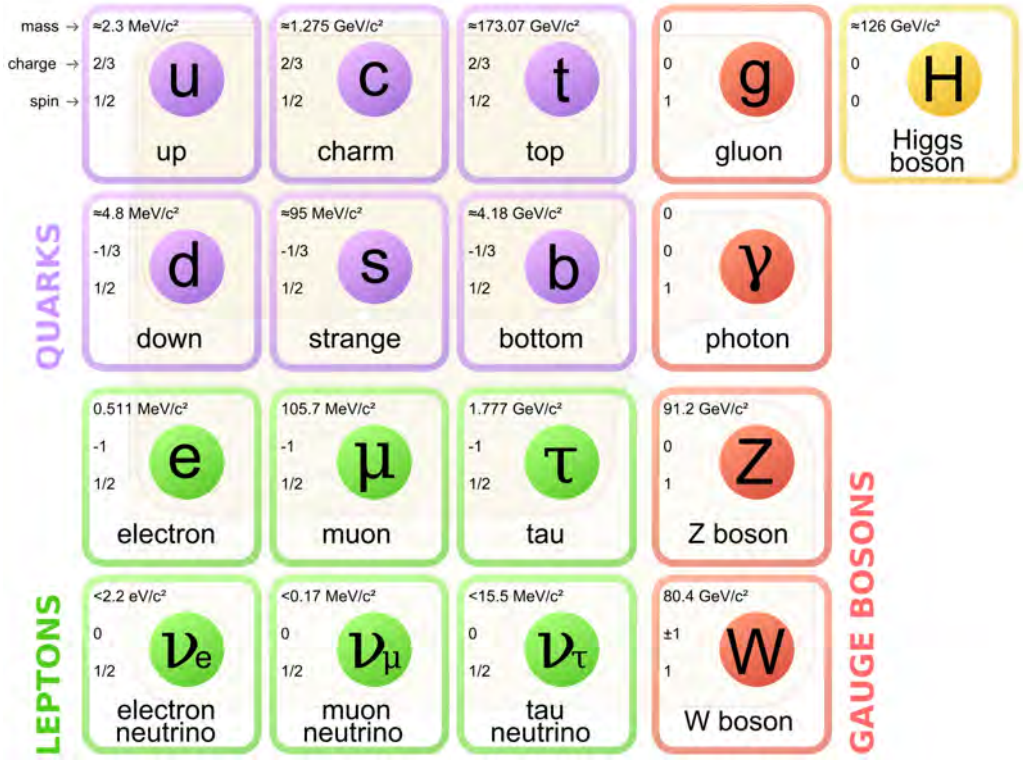


Figure 2.1: The elementary particles in the Standard Model of Particle Physics [2].

The elementary particles are described and ordered by their mass and quantum numbers: spin, electric charge, weak hyper charge, color charge and flavour quantum numbers. This splits the twelve fermions into six particles carrying color charge, the quarks and 6 leptons without color charge. Quarks and leptons are arranged in three families or generations ordered by their mass.

Each generation of quarks contains an up-type and a down-type quark in rising mass order. The up-type quarks up (u), charm (c) and top (t) carry +2/3 electrical charge (in

elementary charges e), the down-type quarks down (d), strange (s) and bottom (b) carry -1/3 e. They also interact weakly and electro-magnetic.

There are three charged leptons: the electron (e), the muon (μ) and the tau (τ). They carry charge -1 but no color charge and can interact weakly and electro-magnetic. A lepton family is build from a charged lepton and its corresponding neutral lepton, the so-called neutrino (ν). E.g. the first family consists of the electron, the lightest charged lepton and the electron-neutrino (ν_e). The neutrinos are massless in the SM and only interact weakly.

In the SM the forces are mediated by five gauge bosons. The photon (γ) is the mediator for the electro-magnetic interaction (EM), which couples to electric charge and is massless. The weak interaction is mediated by three massive gauge bosons, two charged (± 1) W-bosons with 80.4 GeV mass and the neutral Z-boson with 91.2 GeV mass. The strong interaction is described by the theory of quantum chromo dynamics (QCD), with its force carrier the massless gluon which couples to color charge and also carries color charge itself. In the SM the electro-magnetic and weak interaction can be unified and treated as a single interaction the electro-weak interaction with 4 massless gauge bosons. As the weak gauge bosons are massive there must be a process causing electro-weak symmetry breaking, which breaks this single interaction into two and gives mass to the weak gauge bosons. This process is the higgs-mechanism for the SM, which comes along with the prediction of an additional neutral scalar particle called the higgs-boson.

Whereas the range of the EM is infinite due to the zero mass of the photon, the strong force is very short ranged due to the color charge of the gluon which enables self-interaction. A further consequence is the absence of free color charged objects in nature, the so-called confinement, binding multiple quarks and gluons in color-free states (hadrons). The range of the weak force is even shorter due to the high mass of the gauge bosons and renders it the weakest force in the SM at energy scales below their masses.

Not all particle quantum numbers are good quantum numbers and conserved for all interactions. E.g. the weak force does not conserve the quark flavor, due to the fact that weak-eigenstates are superpositions of strong-eigenstates. The mixing between strong and weak quark-eigenstates is formulated in the Cabibbo-Kobayashi-Maskawa-Matrix (CKM-Matrix). In the SM a lepton flavor number is assigned to each lepton family and was assumed to be conserved, until recent observations of neutrino-oscillation showed a lepton flavor violation (LFV) in the neutrino-sector [3–5]. This required an extension of the SM including neutrino-oscillation effects, implying a none-zero mass for neutrinos. The neutrino mixing is summed in the Pontecorvo-Maki-Nakagawa-Sakata matrix (PMNS) describing the mixing of weak and mass eigenstates of the neutrinos. So far for charged leptons no flavor violation (cLFV) has been observed.

Although the SM is one of the most successful theories of modern physics and its predictions have been tested and confirmed in many measurements at last with the discovery of a higgs boson at LHC [6][7], it still leaves many open questions. Neither does it include a dark matter candidate, nor does it include a quantum theory of gravity, nor does it give an explanation for the matter-antimatter asymmetry observed in the universe. Neutrino masses as measured in neutrino-oscillation can be integrated in extended SMs, but does not explain how the neutrino masses are generated.

This triggers the development of new theories beyond the SM, predicting new particles and interactions not observed at the currently available energy regime.

2.2 The Muon Decay

2.2.1 In the Standard Model

In the original SM the lepton number is a conserved quantity and lepton flavor violating decays as e.g. $\mu \to eee$ are forbidden. Although the extended SM still does not describe charged lepton flavor violation on tree-level, lepton mixing can be induced here by neutrino oscillation in higher order loop diagrams. However, for the most dominant loop-diagram (fig. 2.2) for $\mu \to eee$ the branching ratio (BR) is heavily suppressed to $BR < 10^{-50}$ by the mass ratio $(\frac{(\Delta m^2_\nu)^2}{m^4_W})$.

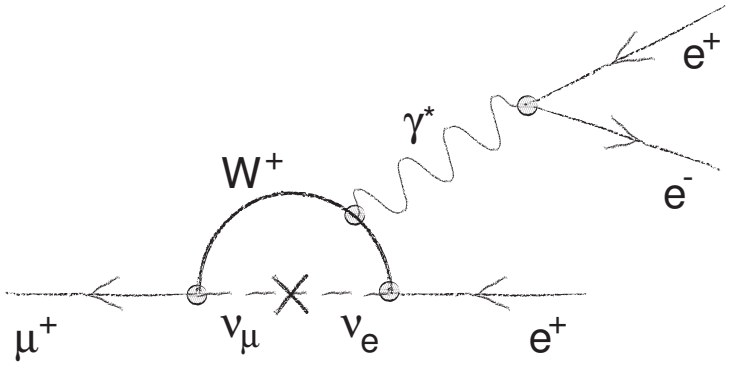


Figure 2.2: $\mu \to eee$ SM-neutrino oscillation diagram.

A further related decay, possible through the same loop, is the neutrinoless radiative decay $\mu \to e\gamma$, which only differs from $\mu \to eee$ by the missing photo conversion and so renders a slightly less suppressed BR mainly driven by the missing EM-vertex entering with a factor $\alpha_{em}(\mathcal{O}(10^{-2}))$.

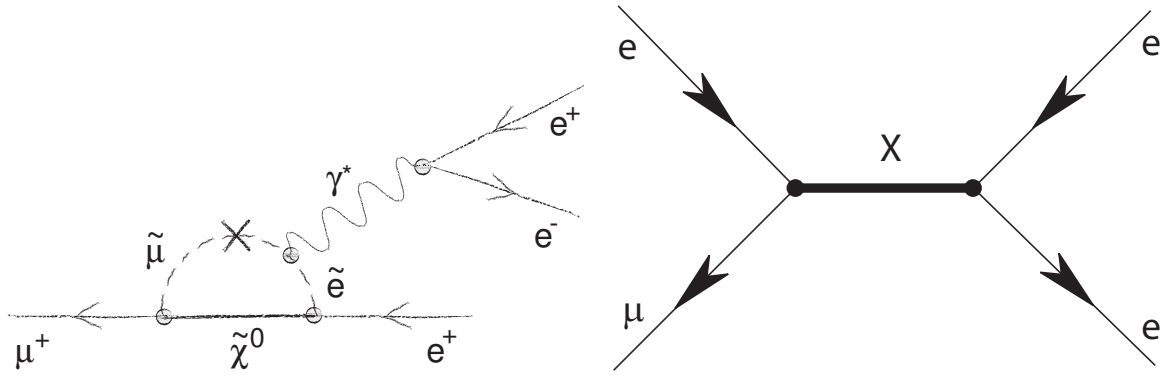
These extremely low BR predictions render these decays experimentally immeasurable and make them a perfect test ground for the SM, as any observed signal is a clear sign for physics beyond the SM.

2.2.2 Beyond the Standard Model

Although the charged lepton flavor is practically conserved in the SM, many models of beyond the SM theories include cLFV and therefore give an enhanced BR for processes as e.g. $\mu \to eee$. Those models are constraint by the limits obtained experimentally $BR < 10^{-12}$ $(\mu \to eee)$ [8] and related processes, e.g. $\mu \to e\gamma$ covering cLFV processes.

Beyond the SM theories with more dimension or an extended higgs-sector predict heavy particles which can couple to both electrons and muons, leading to LVF already at tree level as shown in figure 2.3(b). The large mass of the mediating new particle leads to a suppression of this process.

One possibility to induce enhancements on the loop-level is given by supersymmetric theories which predict loops containing supersymmetric particles as in figure 2.3(a) and create LFV via slepton mixing. As no supersymmetric particle has been observed so far they must come into play at higher mass scales. These loop diagrams are usually suppressed if the mass of the supersymmetric particles, determined by the SUSY scale parameters are large.



(a) Beyond SM $\mu \to eee$ process with loop slepton mixing (SUSY).

(b) Tree diagram for heavy mediator particle.

Figure 2.3: Beyond the SM diagrams.

3 The Mu3e Experiment

The Mu3e experiment searches for the lepton flavor violating decay $\mu^+ \to e^+e^-e^+$ with a precision of better than one in 10^{16} muon decays. To achieve this goal on a suitable time scale the experiment is designed to observe 2×10^9 muon decays per second.

In the following the challenges of the Mu3e experiment, the detector solution, as well as the current experimental situation of searches for lepton flavor violation are depicted.

3.1 The Experimental Situation - Searches for lepton flavor violating muon decays

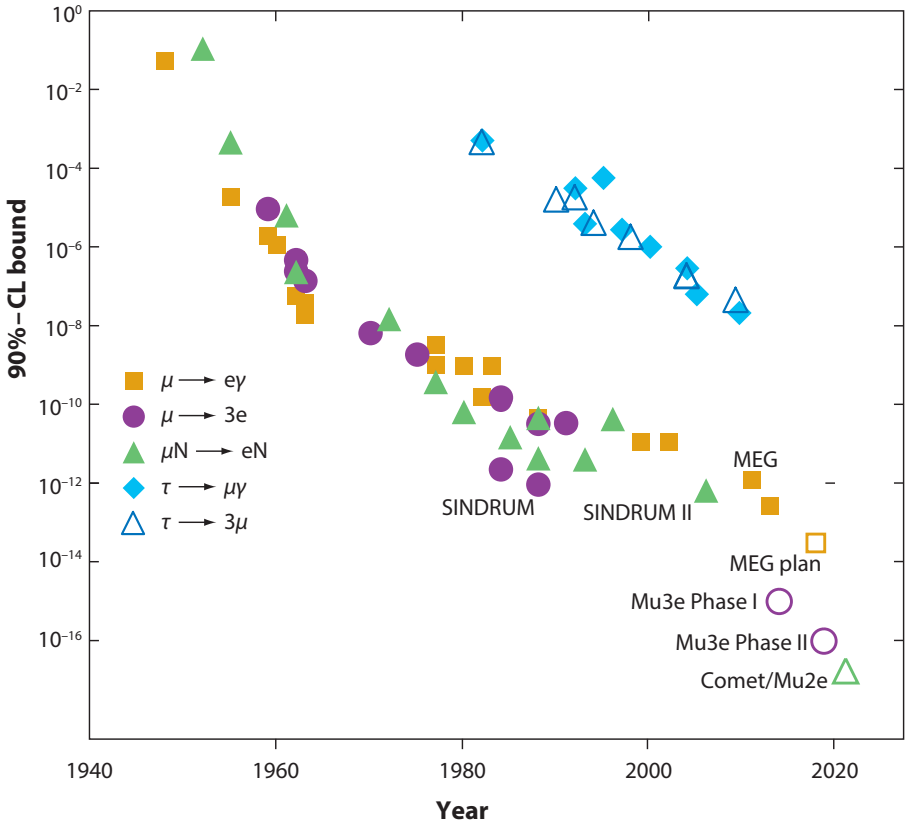


Figure 3.1: Present and aimed limits of past, present and future searches for LFV decays. Adapted from [9].

3.1.1 SINDRUM

The SINDRUM experiment searched for the decay $\mu^+ \to e^+e^-e^+$ from 1983-1986. In the absence of a detected signal an upper limit of $BR < 10^{-12}$ at 90% confidence level (CL) could be derived [8].

The SINDRUM experiment was operated at PSI, stopping 28 MeV/c surface muons on a double cone target, placed in a 0.33 T magnetic field. To track the decay products, the target was surrounded by 5 layers of multi wire proportional chambers and a trigger hodoscope. The main background source arose from $\mu^+ \to e^+e^-e^+\bar{\nu_\mu}\nu_e$ and was estimated to 5×10^{-14}. That shows the results limitation due to the number of observed muon decays.

3.1.2 MEG

The MEG experiment is a current experiment running at PSI since 2008 searching for the LFV process $\mu \to e\gamma$. The main detector components are a drift chamber for the positron reconstruction and a liquid xenon calorimeter for the photon detection [10].

In a first run with 10^{14} stopped muons a limit could be set to $BR < 2.8 \times 10^{-11}$ at 90% CL. After improvements this limit has been improved to $BR < 5.7 \times 10^{-13}$ at 90% CL [11]. A further upgrade is ongoing, aiming to reach a BR sensitivity of 10^{-13}. This challenges the search for $\mu \to eee$ to achieve BR sensitivities better than 10^{-15} to be competitive.

3.1.3 Conversion Experiments

An other possibility is the search for LVF in muon conversion $\mu \to e$ in the presence of nuclei. It has the advantage of a clear signature of monochromatic electrons, with an energy not occurring in normal muon decays.

The best limit is set by the SINDRUM II experiment for the conversion on a gold target $\mu Au \to eAu$ ($BR < 7 \times 10^{-13}$) [12]. New experiments on muon conversion are planed with Mu2e at Fermilab or DeeMe, COMET and PRISM at J-PARC they aim for BR sensitivities of 10^{-14} to 10^{-16}.

3.2 The Signal Decay

The $\mu^+ \to e^+e^-e^+$ decay is a prompt decay, so the decay particles originate from a common vertex. As a consequence of momentum conservation the vectorial sum of the particle momenta is vanishing for muon decays at rest:

$$|\vec{p}_{tot}| = |\sum_{i=0}^{2} \vec{p}_i| = 0 \tag{3.1}$$

Moreover the total energy has to add up to the muon mass:

$$E_{tot} = |\sum_{i=0}^{2} E_i| = m_\mu \cdot c^2 \tag{3.2}$$

The maximum energy of a decay particle is therefore given by half the muon mass $\sim$ 53 MeV.

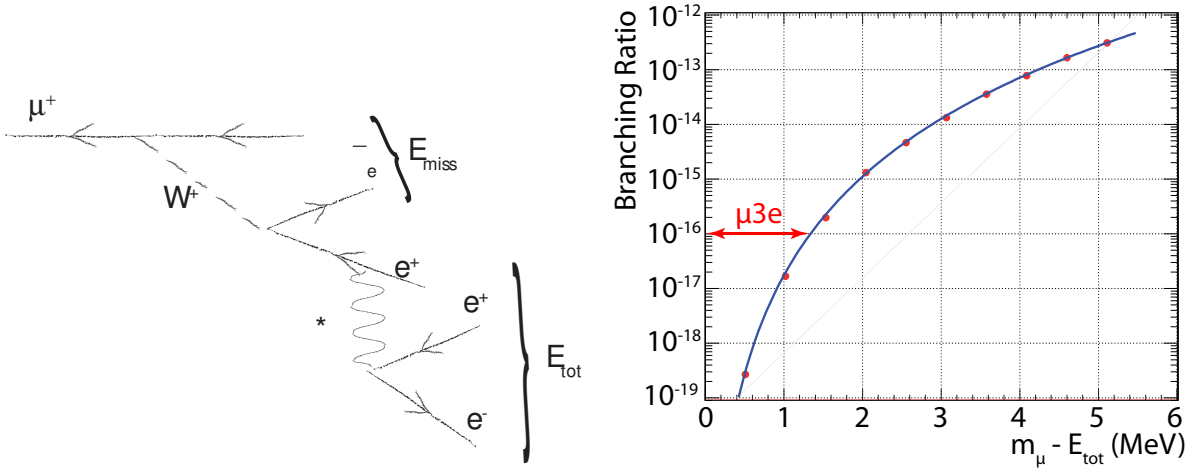
To discriminate between signal and background kinematics can be exploited by requiring momentum and energy conservation. In addition the coincidence of the particles in space and time can be used for discrimination.

3.3 The Backgrounds

The backgrounds for the signal can be divided in two categories, irreducible physics background and accidentals.

3.3.1 Internal Conversion

The physics background is mainly given by the SM internal conversion decay $\mu \to eee\bar{\nu}\nu$ (fig. 3.2(a)). Here the undetected neutrinos give rise to missing energy and momentum allowing a discrimination from the signal decay. Figure 3.2(b) shows the missing energy for a range of target sensitivities. To achieve a BR sensitivity better than 10^{-16} at 90% CL an energy resolution better than 1 MeV is required [1].



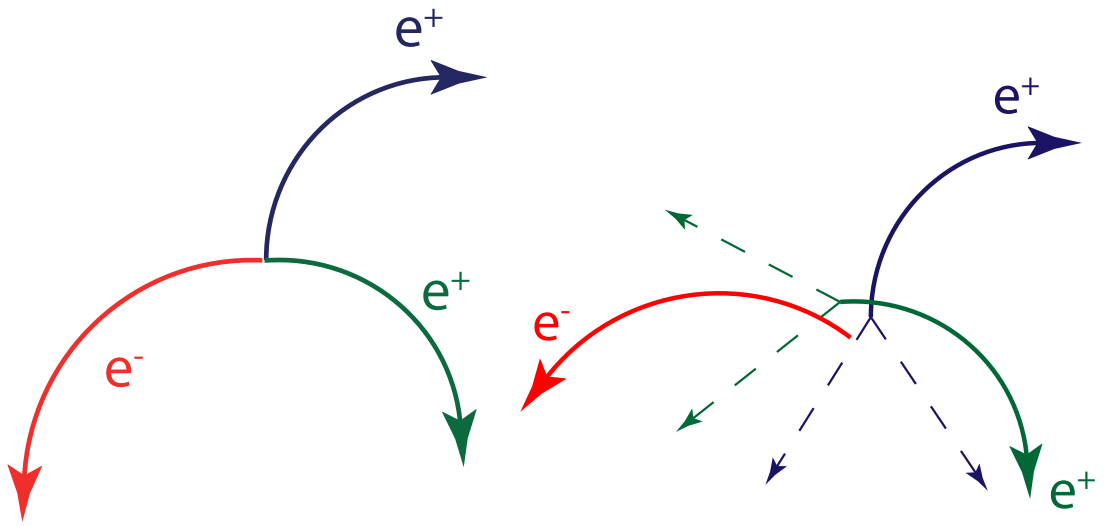
(a) SM internal conversion decay.

(b) Branching ratio contribution of internal conversion as function of missing energy. [13]

Figure 3.2: Internal Conversion.

3.3.2 Accidental Background

Accidental background can arise from event topologies as shown in 3.3(b), with e.g. two positrons from SM michel decays and an electron from a different process. The regular production of electrons in an anti-muon decay is already covered by the internal conversion background. Further origins of electrons are either caused by misreconstruction in a very crowded detector environment or by secondary interactions as photon conversion in the



(a) Signal topology: two positrons and one electron with common vertex.

(b) Fake signal closely resembling the signal topology.

Figure 3.3: Three track topologies.

target from radiative decays $\mu \to \gamma e \nu \bar{\nu}$ or bhabha-scattering of a michel positron with an electron.

For the Mu3e experiment requiring $\mathcal{O}(10^9)$ muon decays per second on the target this is a serious background source and needs to be suppressed as good as possible. Here the space and time coincidence of the signal can be used for discrimination by requiring same vertex and time origin for all decay particles (fig. 3.3(a)).

3.4 The Detector Requirements

As seen above the aim to achieve a BR sensitivity of 10^{-16} poses a lot of requirements in terms of background suppression and rate capability, which directly translate to detector requirements.

In order to accomplish the experimental goals on a suitable timescale the detectors acceptance and efficiency has to be as high as possible. The detector has to provide excellent vertex, time and momentum resolution to suppress the emerging background to a level below 10^{-16}. Further the low energy of the decay particles demands a small material budget to reduce multiple coulomb scattering which dominates the momentum resolution.

3.5 The Mu3e Detector

The basic idea of the Mu3e experiment is to stop more than 10^{16} on a target and observe their charged decay particles with a barrel detector surrounding the target. The detector is made of layers of high granular silicon detectors for tracking and scintillating fiber, and tile detectors for precise time measurements. To measure the momentum of the

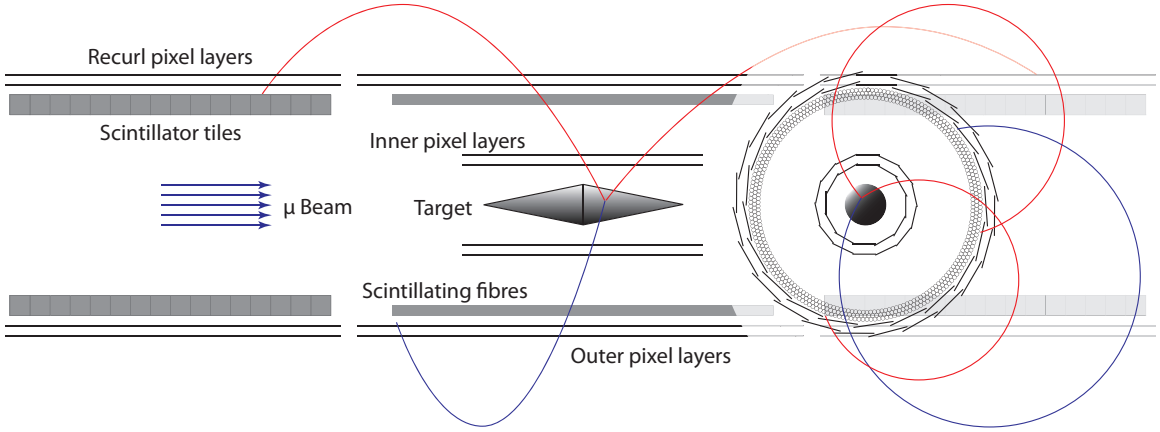


Figure 3.4: Schematic compilation of the Mu3e detector with an on-target $\mu^+ \to e^+e^-e^+$ decay. On the right a view along the beam axis [14].

charged particles the detector is placed in a 1 Tesla homogeneous magnetic field. As multiple coulomb scattering is the most severe error source the material budget has to be minimized as much as possible. The detector is cooled with a constant flow of gaseous helium, which guarantees good heat transfer and low multiple scattering.

3.5.1 The Muon Beam & Stopping Target

Since at the moment there is no muon beam existing which could provide 2×10^9 muon stops per second, the experiment is planned to run in two phases. In phase I the experiment will make use of the beam line $\pi e5$ at the High Intensity Proton Accelerator (HIPA), see figure 3.5. The HIPA cyclotron provides a 2.2 mA beam of 590 MeV protons striding two rotating targets. The $\pi e5$ beam is extracted from the carbon target E by collecting muons which originate from pions at rest on the targets surface (surface muons), generating a 28 MeV/c muon beam. For phase II a new beam line needs to be constructed. Currently a study is ongoing determining possible solutions for a high intensity muon beam (HIMB) at PSI. The possibility of a target upgrade seems most feasible at the moment. To stop the muons the beam hits a hollow double cone target made of a thin aluminum or mylar foil ($\mathcal{O}(50\mu m)$).

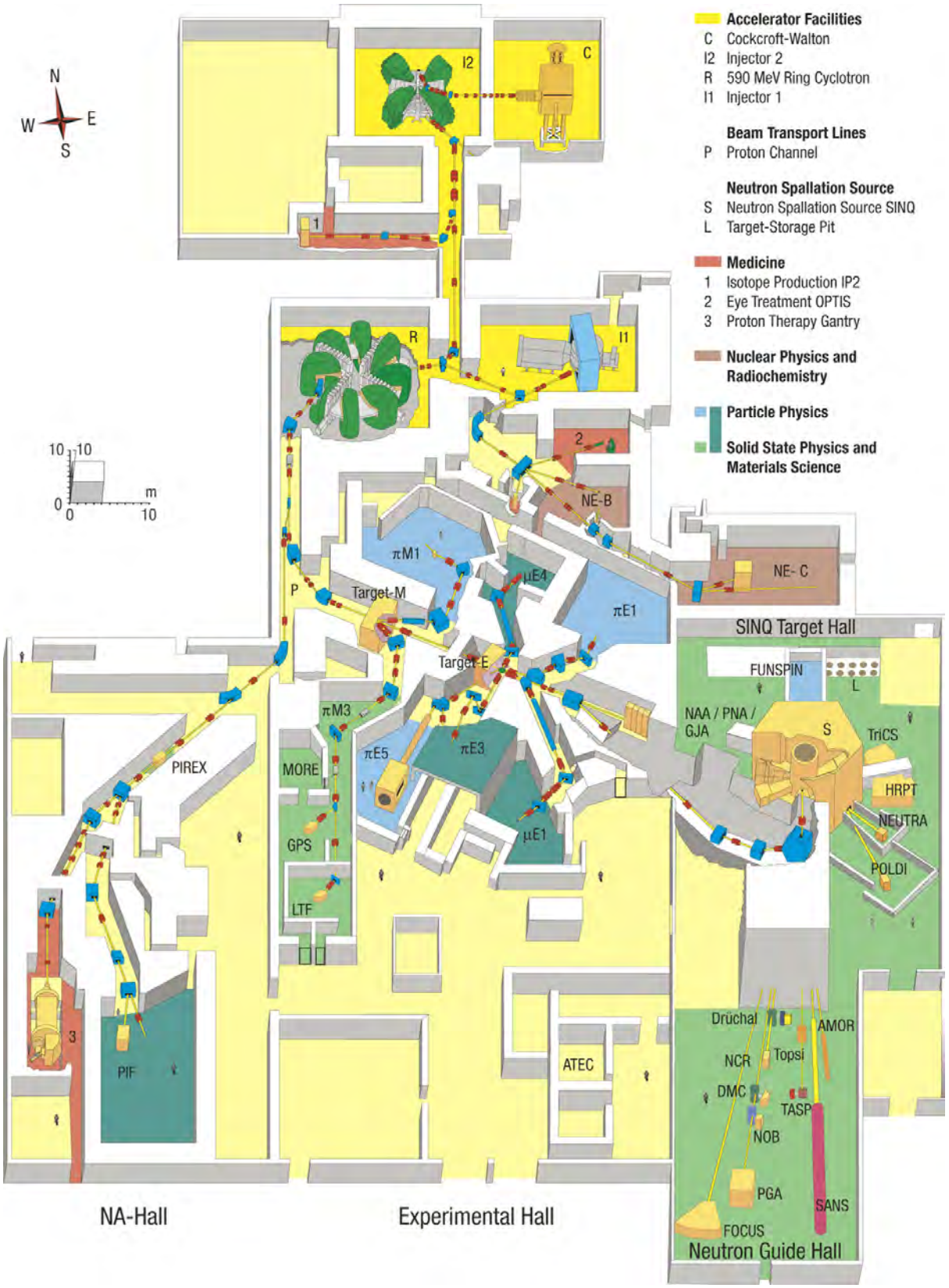


Figure 3.5: View of the PSI experimental hall with the PIE5 beam line.

3.5.2 The Tracking Detector

The tracker is subdivided in five units: the central barrel surrounding the target and two pairs of recurl stations up- and downstream respectively. In phase I at first only the central barrel will be installed (phase Ia), consisting of an inner and outer double layer of pixel sensors. The inner double layer is closest to the target and used for vertexing. The outer layers are in farther distance and allow to measure the bending of particle tracks in the magnetic field and allows for a momentum measurement. The momentum determination can be improved further by measuring the second intersection of the particles with the outer layers when recurling in the 1 Tesla magnetic field. To increase the detectors acceptance for the recurl measurement, the outer double layers are extended by adding recurl tracking layers upstream and downstream from the central station (phase Ib, II).

The detector consists of two types of sensor reticles, $2 \times 6cm^2$ sensors for the inner layers and $2 \times 18cm^2$ for the outer layers. The layers are build as regular polygons with side lengths of 1 or 2 cm housing several sensors. In the end the detector will have more than $1m^2$ of active pixelated surface and consist of about 275 million pixels with a pitch of $80 \times 80\mu m^2$.

(a) Prototype of a self supporting inner layer with 50 μm glass as silicon substitute.

(b) Outer layer prototype with V-folds for mechanical stabilization.

Figure 3.6: Prototypes of the self-supporting capton layers.

To achieve the goal of a minimal material budget, the tracking layers are build self supporting from $50\mu m$ silicon sensors glued to $25\mu m$ thick Kapton® foil. Additionally the sensors are wire bonded to a flex print manufactured from a $25/25\mu m$ Kapton®/aluminum laminate (fig. 3.6(a)&3.6(b)), which provides power, slow control steering and sensor readout via 800 MBit/s Low Voltage Differential Signals (LVDS).

3.5.3 The Fiber Detector

The fiber detector consists of ribbons made of 2-3 layers of stacked and glued $250\mu m$ scintillating fibers, placed polygon just inside the outer double pixel layer. They are read out with an array of silicon photo multipliers (SiPM) matched to the fibres. This system provides $\mathcal{O}(1ns)$ time resolution for all tracked decay particles and central barrel recurlers. This is needed to handle the high multiplicities and suppresses the accidental background.

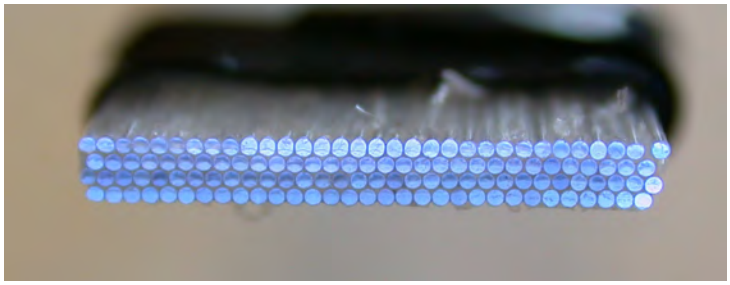


Figure 3.7: Ribbon manufactured from 4 layers of glued round scintillating fibers [1].

3.5.4 The Tile Detector

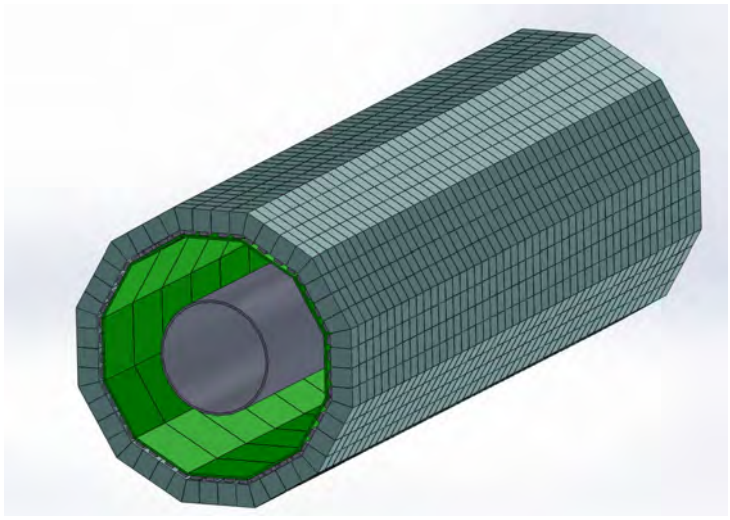


Figure 3.8: Rendering of one tile detector station consisting of many scintillating tiles [1].

To improve the matching of recurling tracks in the upstream and downstream stations and suppress background especially in phase II a very good time resolution is required. This is achieved by a tile detector consisting of a barrel of segmented scintillating tiles inside the diameter of the outer pixel layers. Each tile is connected to a SiPM and is sampled via a two threshold discriminator which allows to perform time walk corrections and through this gain $\mathcal{O}(100ps)$ resolutions.

3.6 The Readout Concept

All detector parts are steered and readout by field programmable gate arrays (FPGA). The FPGAs collect the data from the subdetectors and send the data to a front-end card sorting the data time ordered and assigning the time slices to a graphic processing unit (GPU). Each time slice contains the complete detector information used for online reconstruction. The detector produces more than 100 GB/s of raw data, after sorting, online reconstruction and filtering 100 MB/s of data remain which are stored on tape.

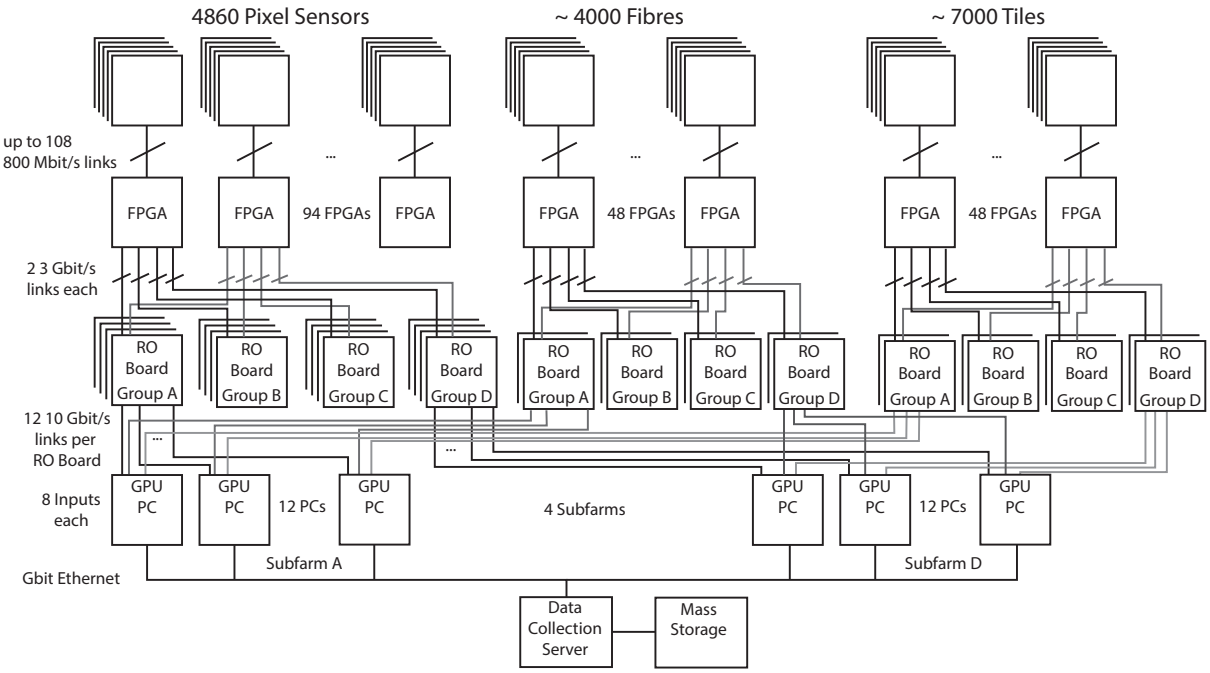


Figure 3.9: Readout concept and data flow chart of the Mu3e experiment [15].

3.7 The Cooling

All electrical components in the detector produce heat. Most heat originates from pixel sensors. To cool the detector efficiently it is placed in a gaseous helium atmosphere with a constant flow along the beam axis, making use of the good heat transfer and low multiple scattering properties of helium. The cooling capabilities of the gaseous helium constrains the power consumption for the tracking detector. The cooling is currently simulated and tested with a mock-up of the central station and the capability seems to exceed the goal set for the experiment (150 m W) giving a safety margin .

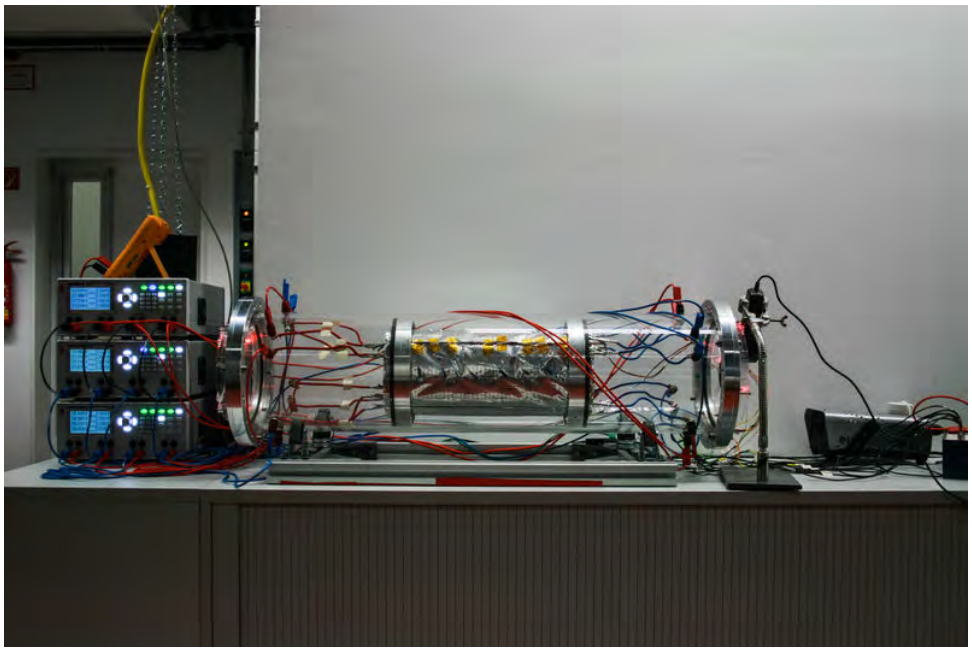


Figure 3.10: The cooling mock-up used at the Physics Institute the test the cooling capability of a global flow along the beam axis [16].

4 Interaction with Matter and Detection of charged particles

The interaction of particles with matter allows their detection in the first place, but of course it also gives rise to scattering effects, which are pre-dominantly error sources for the Mu3e experiment. In the following the interaction of charged particles with matter are discussed with emphasis to the energy deposition used for their detection and the scattering angle distribution for a particle penetrating through a layer of matter.

4.1 Interaction with Matter

The interaction of charged particles with matter depends heavily on the atomic number of the material and also on the particles charge and mass. Especially electrons and heavy particles are distinguished, as for the heavy particles bremsstrahlung only comes into play at very high energies. In the following only energy losses due to electro-magnetic interactions are considered; hadrons can also interact via the strong interaction.

4.1.1 Heavy Particles

For particle physics the most important heavy particles are muons, pions and protons. For them the most important energy loss is ionization up to GeV energies. The mean energy loss per traveled material thickness $\left\langle \frac{dE}{dx} \right\rangle$ is described by the Bethe-Bloch-formula (4.1) [17].

$$-\left\langle \frac{dE}{dx} \right\rangle = \frac{4\pi n z^2}{m_e c^2 \beta^2} \cdot \left(\frac{e^2}{4\pi\epsilon_0} \right)^2 \cdot \left[\log\left(\frac{2 m_e c^2 \beta^2}{I \cdot (1-\beta^2)} \right) - \beta^2 \right] \tag{4.1}$$

with the particle dependent parameter: the relative velocity $\beta = \frac{v}{c}$, the charge number z, the material dependent mean excitation energy I and the electron density n. Further the electron mass m_e, the speed of light c and vacuum permittivity ϵ_0.

The Bethe-Bloch-formula as plotted in figure 4.1.1 shows a minimum around $\beta\gamma = \frac{pc}{m_0 c^2} \approx 3$ for all materials, indicating a minimal energy loss for particles with the corresponding momenta. Those are referred to as Minimum Ionising Particles (MIP). For lower momenta the losses rise with β^{-2} due to the rising interaction time, for higher momenta the energy losses increase logarithmically on account of the relativistic squeezing of the transversal fields.

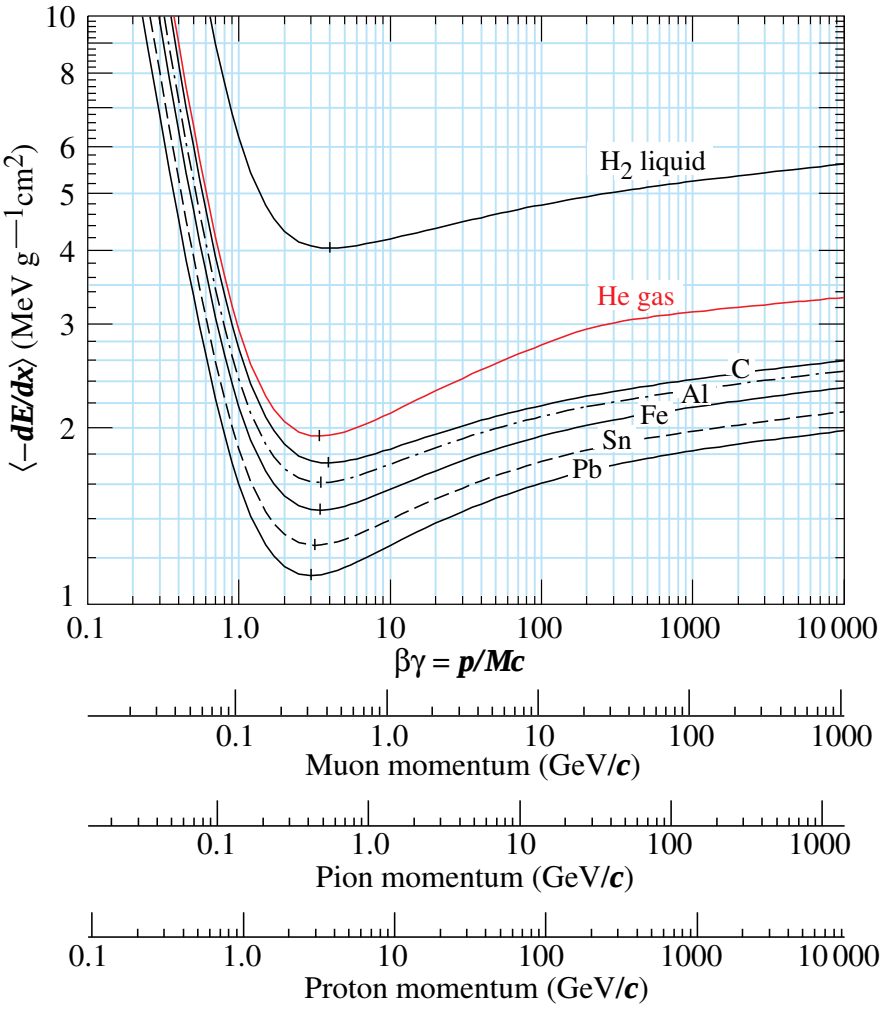


Figure 4.1: Mean energy loss of heavy particles described by the Bethe-Bloch formula for different materials [17].

4.1.2 Electrons and Positrons

The two main sources of energy loss for positrons and electrons are ionization and contrary to heavy particles bremsstrahlung. The mean energy loss via ionization is well described by Berger and Seltzer [18], the Berger-Seltzer-formula (4.2):

$$-\left\langle \frac{dE}{dx} \right\rangle = \rho \frac{0.153536}{\beta^2} \frac{Z}{A} \cdot \left(B_0(T) - 2\log(\frac{I}{m_e c^2}) - \delta \right) \tag{4.2}$$

The energy loss depends on the material and momentum dependent stopping power $B_0(T)$, the material dependent mean excitation energy I, density correction δ, atomic number Z, mass number A and material density ρ. Further it takes into account the indistinguishability of incident and scattering electrons in contrast to the positron, which leads to different energy losses. With the help of the provided data [18] one can find a description for various materials in a large energy range. The energy loss for silicon is plotted in figure 4.1.2 as function of the momentum p

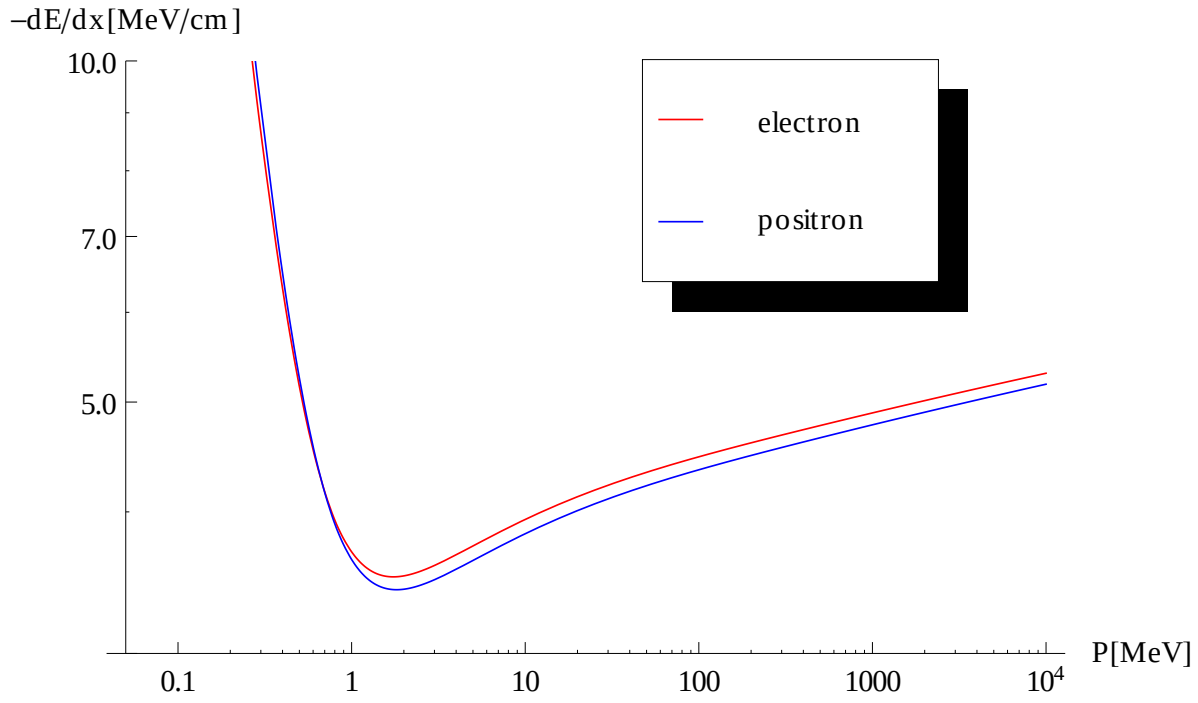


Figure 4.2: Mean energy loss of electrons and positrons in silicon for from 50 keV to 10 GeV.

Additional to the ionization loss there are also bremsstrahlung effects, which can be described by equation 4.3 for relativistic particles ($\beta^2 \approx 1$) [19]. The energy loss is proportional to the particle energy E and the material dependent radiation length X_0.

$$-\frac{dE}{dx} = -\frac{E}{X_0} \tag{4.3}$$

The radiation length is given by equation 4.4, which also takes into account coulomb screening effects of the core potential, with A the atomic mass number and Z the atomic charge number.

$$X_0 = \frac{716,4\ g/cm^2 \cdot A}{Z(Z+1) \cdot \log(287/\sqrt{Z})} \tag{4.4}$$

4.2 Multiple Coulomb Scattering

Any interaction will also cause a deflection of the penetrating particle arising from many small-angle scatters as sketched in figure 4.2. Most of those deflections are caused by coulomb scattering at the materials nuclei. For many applications it is sufficient to use a gaussian approximation which describes the rms for the central 98% of the angular distribution (Eq. 4.5) and ignores hard scatters and with this any tail contributions [17].

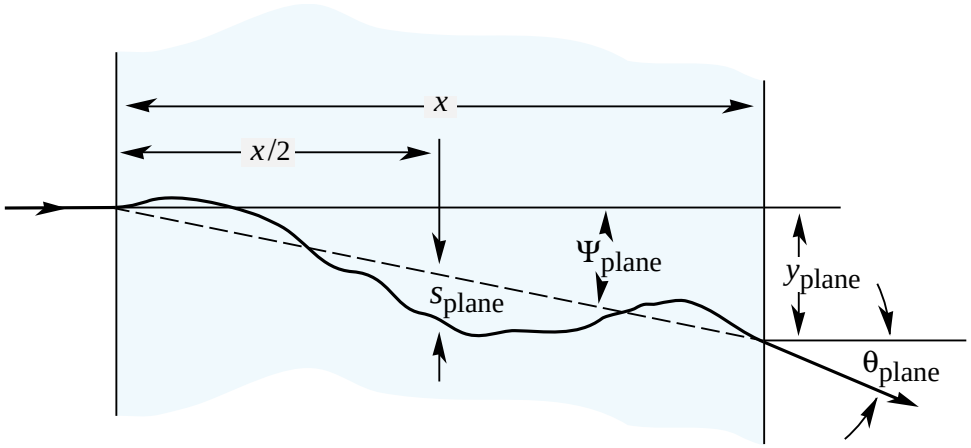


Figure 4.3: Illustration of multiple scattering in matter: many small scatters lead to one observable scattering angle [17].

$$\Theta_{rms} = \frac{13.6MeV}{\beta cp}\, z\sqrt{\frac{x}{X_0}}\left[1 + 0.038\log\left(\frac{x}{X_0}\right)\right] \tag{4.5}$$

The dependence on the particles properties charge z, velocity βc and momentum p shows already the problem for the Mu3e experiment. The multiple scattering is proportional to p^{-1}, it increases drastically for low momenta as the particles in the $\mu \to eee$ decay. But the equations also shows the possibility to balance this effect via the reduction of the material thickness in units of the radiation length x/X_0.

4.3 Particle Detectors

The above discussed effects are a potential measurement uncertainties, but the interaction of particles with matter is of course also essential for their detection.

Particle detectors allow for the measurement of particle properties e.g. the momentum, the velocity or the energy. Each of these measurements requires a different detector approach, but they can be grouped in two main detector ideas. Either the complete absorption of an incident particle with thick layers of high Z materials as for energy measurements in calorimetry or the minimal disturbance of the particle with a rather low effective thickness x/X_0 as in tracking detectors.

For the Mu3e experiment we are interested in a very precise momentum measurement, which basically offers two detector solutions, either a particle tracker based on layers of solid state detectors, or the use of a Time Projection Chamber (TPC).

A TPC makes use of a large cylindrical gas volume along the beam axis with a high voltage applied between the two ends of the cylinder. Charged particles which cross the gas will ionize atoms and the ions and the electrons will drift to opposite ends of the cylinder which are instrumented for their detection. This allows for a full reconstruction of the track, as a charged particle will leave a trace of ionized gas along its path. The disadvantage of this technology is on one hand that the drift collection is quiet slow,

which limits the rate capability of such a system and causes space charge effects. On the other hand it is hard to handle the conditions of such a large volume of gas, as already minor contamination can destroy the detectors performance. However, this is technically solved, e.g. in the ALICE detector, but lifetime limitations due to aging prevail.

The main disadvantages of a solid state detector is in general its large material budget and the expensive production, but lately commercial available process are extensively used in industry and production cost are sinking. Also thinning processes for chips are routinely used, which allow to thin down the sensors and reduce the material budget immensely. A particle striding the chips semiconductor material will loose energy by creating electrons and holes, which can be detected with an electrode. A precise discussion will follow in section 5.4. In comparison to gaseous detectors they have the advantage of fast charge collection and signal handling, with almost no dead time.

5 Semiconductor Physics

The most common materials for the fabrication of semiconductor pixel detectors are silicon and germanium. The sensors for the Mu3e experiment will be made of silicon, their properties are discussed in the following.

5.1 Silicon

Silicon atoms condense in a crystal with diamond like structure, with the four covalent electron bonds to the neighboring silicon atoms as shown in figure 5.2. The basic properties of silicon are summarized in in table 5.1.

Semiconductor properties arise from the rather small energy difference between the electron states in the covalent bonds (valence band) and the free electron states not bond to an atom and moving through the crystal as free charge carriers (conduction band) as shown in the band structure diagram (fig. 5.1). At absolute zero temperature (0 K) all electrons are bond to atoms and so in the valence band. However, at room temperature (300K) some electrons can be thermally excited to the conduction band, leaving behind a "hole" in the covalent structure. This hole can be filled with an electron of an adjacent bond, creating a new hole. This gives the impression of a moving positive charge in the valence band which are referred to as holes. Excited electrons can be caught by a hole and fall down to the valence band again. This process is called recombination. Both processes excitation and recombination are governed by fermi statistics.

5.2 Doping

At room temperature silicon has free charge carriers, but compared to metal this intrinsic given conductivity is very small as the number of charge carriers ($ni = 1.5 \times 10^{10}/cm^3$) is negligible compared to the number of atoms ($\sim 5 \times 10^{22}/cm^3$).

There is the possibility of artificially enhancing the conductivity by introducing impurities in the crystal, the so-called doping. By implanting atoms with five valence electrons, like arsenic or phosphorus, only four are involved in the covalent crystal structure while one is only weakly bound and located in a discrete energy level close to the conduction band (fig.5.2(a)). This allows a thermal excitation to the conduction band. These implants are called donators as they give additional electrons to the conduction band. But also the reverse process is possible as depicted in figure 5.2(b) by implanting atoms with 3 valence electrons like boron as a so-called acceptor. In this case one electron is missing to from the 4 covalent bonds. The missing bond can be filled by a thermally excited electron from the conduction band. Semiconductor material with donator implantations is referred to as n-doped as it creates additional negative charges, vice versa the implantation of acceptors is called p-doping.

Property		Value	Unit
Atomic number	Z	14	
Nucleon number	28.09		
Density	ρ	2.33	g/cm^3
Crystal structure		Diamond	
Atom density		5.02	cm^{-3}
Intrinsic charge density	1.5×10^{10}	$1/cm^3$	
Dielectric constant	ϵ	11.9	
	at 300K		
Band gap	indirect band gap	1.12	eV
	direct band gap	3.4	eV
Average creation energy for an electron-hole pair	ω	3.66	eV
Fano Factor	F	0.115	
Mobility	μ_n	1450	cm^2s/V
	μ_p	500	cm^2s/V

Table 5.1: Important silicon properties [20–25].

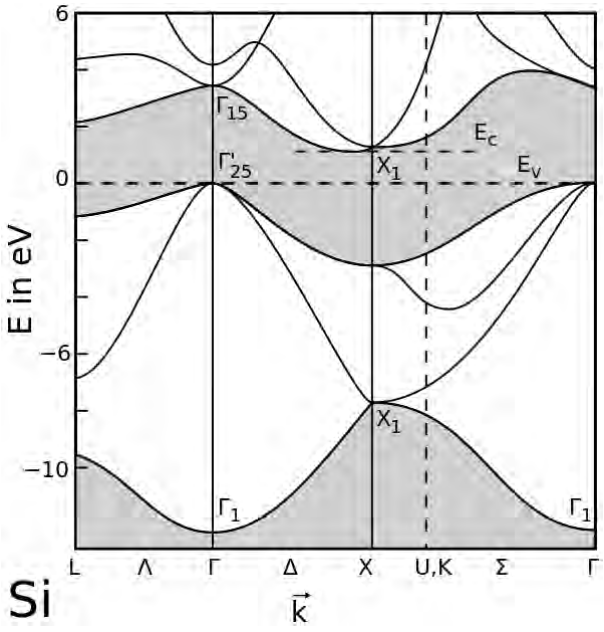
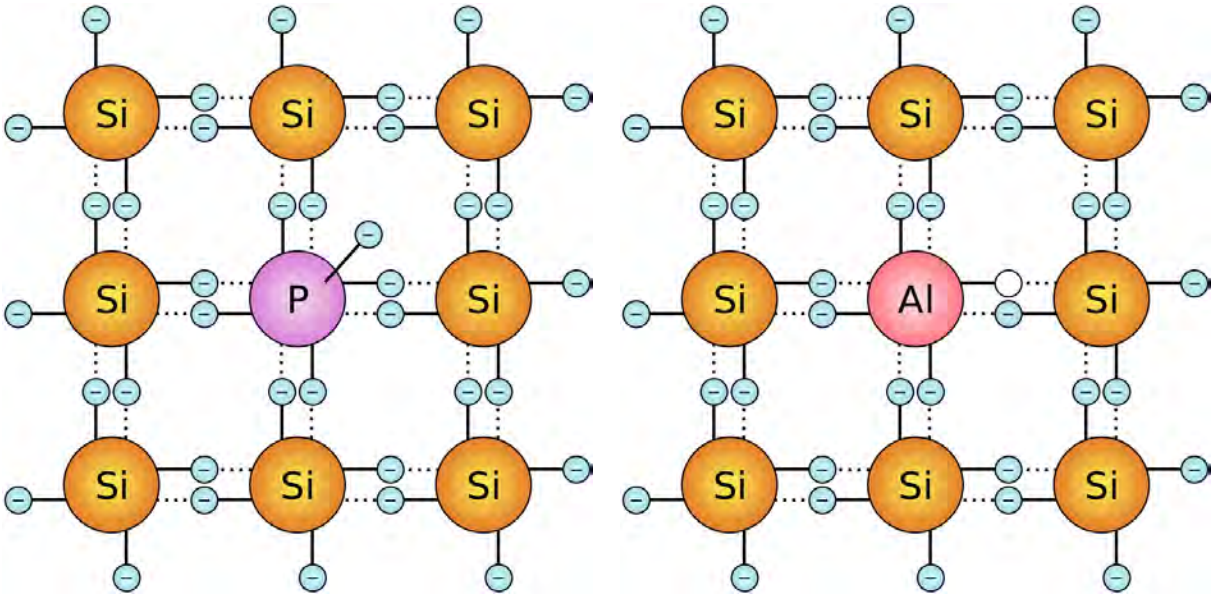


Figure 5.1: Band structure of silicon the indirect band gap of 1.12 eV is marked [26].



(a) N-Doping. (b) P-Doping.

Figure 5.2: Crystal structure with dopand atoms. Image from [27][28]

The doping's magnitude is either described by the dopants-concentration $N_{D/A}[1/cm^3]$ or by the resistivity ρ[1]

$$\rho = R \cdot \frac{A}{l} = \frac{1}{e(N_D \mu_n + N_A \mu_p)} \tag{5.1}$$

with R beeing the resistance, the length l, and cross section A of a material probe and the relation describing the resistivity for a solid state body with dopand-concentration N, the elementary charge e and the charge carrier mobility. As the mobility differs for electrons and holes they have to be distinguished, but in general the dopants concentration is dominating, which simplifies the description to $\rho = (eN\mu)^{-1}$.

5.3 PN-junction Diode

The boundary between a p-doped and n-doped volume is called pn-junction and can be used as a diode. It is the corner stone of all chip technology as it provides unique technical properties.

At the pn-contact there is a huge difference in the concentration of free charge carriers between both materials, which leads to diffusion of charge carriers into the bordering material, trying to balance this inequality. As electrons, diffusing into the p-doped material, are opposed to a majority of holes they will most likely recombine and vice versa. These recombining electrons and holes leave behind their corresponding acceptor and donator ions, giving rise to an electric field across the pn-junction. This field is opposing the diffusion movement and leads to an equilibrium of thermal diffusion and the drift movement

[1] not to be mistaken for the charge density distribution

caused by the field. In this field region no mobile charge carriers are present as they are drawn away by the field created by the ions in the crystal lattice, it is called depletion zone (fig. 5.3).

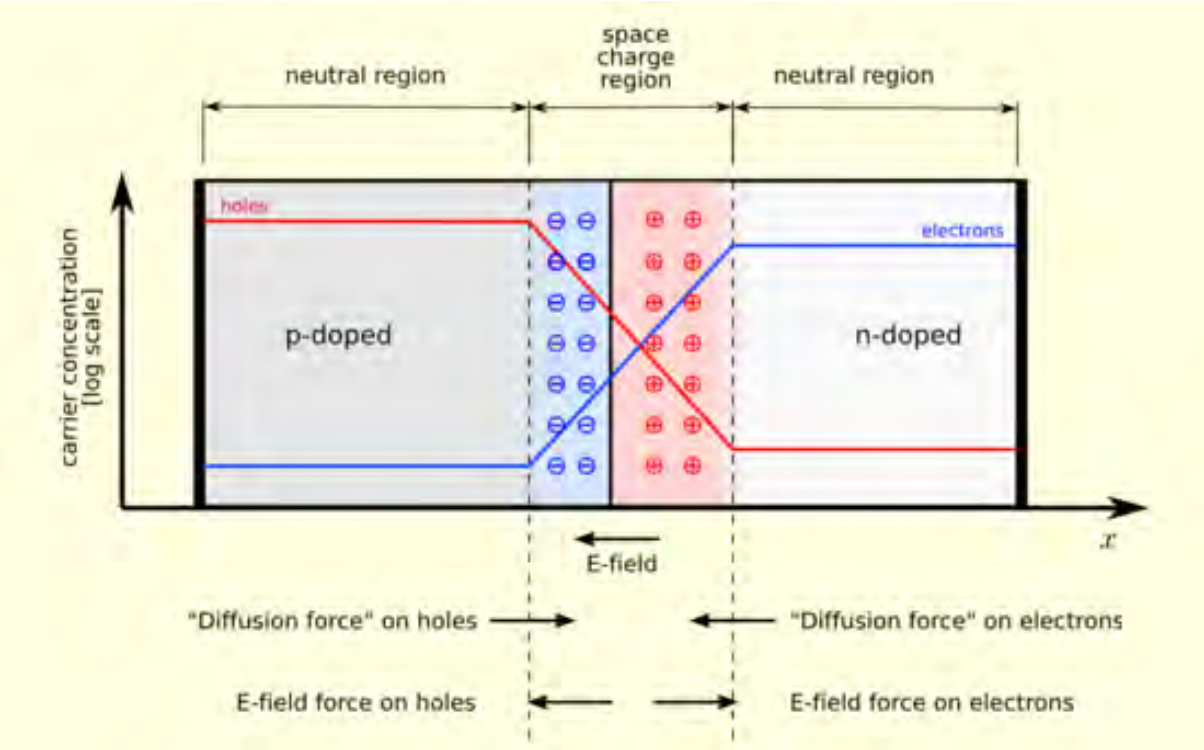


Figure 5.3: PN-junction Equilibrium schematic. Image from [29]

With the assumption of diffusion and drift current in equilibrium an expression can be found for the so-called in-build potential or diffusion voltage:

$$U_D = U_T \cdot \log(\frac{N_A N_D}{n_i^2}) \tag{5.2}$$

With U_T the thermal voltage equivalent (25.9 mV at 300K), N_A and N_D the doping concentration and n_i the intrinsic charge carrier concentration [21].

The dynamic of this system is described by the Poisson equation (eq. 5.3) and allows the calculation of the potential U, the electric field $E = \frac{dU}{dx}$ and the width w of the depletion zone from their charge density distribution $\rho(x)$ given by the doping concentrations, the dielectric constant ϵ_0 and the relative permittivity ϵ.

$$\frac{d^2U(x)}{dx^2} = -\frac{\rho(x)}{\epsilon_0 \epsilon} \tag{5.3}$$

The following calculations summon efforts [30], [31], based on [19] and [22], for the calculation of the depletion width w with a one dimensional model (x-direction perpendicular to pn-border). To carry out the integration of equation 5.3 several boundary conditions have to be defined. As spatial boundary we define x_p and x_n the extensions

of the depletion zone in the n- and p-doped area respectively. The pn-junction-interface is placed at $x = 0$ defining the depletion width as $w = |x_p| + |x_n|$. At the depletion zone boundaries the electric field E is assumed to be zero and the difference of the potentials on the boundaries should add up to the voltage applied between the two areas U_{Diode}.

Under these assumptions the Poisson equation can be interpreted as follows:

$$\rho(x) = \begin{cases} +eN_A & x < 0 \\ -eN_D & x >= 0 \end{cases} \tag{5.4}$$

describing a step-function-like doping profile.

A first integration with the predefined boundary conditions gives us the electric field $E(x)$:

$$E(x) = \frac{dU}{dx} = \int_{x_p}^{x_n} \frac{d^2U}{dx^2}\, dx = \begin{cases} -\frac{eN_A}{\epsilon_0\epsilon}(x - x_p) & x_p <= x < 0 \\ +\frac{eN_D}{\epsilon_0\epsilon}(x_n - x) & 0 <= x <= x_n \end{cases} \tag{5.5}$$

Further integration gives the potential U(x):

$$U(x) = \begin{cases} -\frac{eN_A}{\epsilon_0\epsilon}(\frac{x^2}{2} - x_p x) + C_n & x_p <= x < 0 \\ +\frac{eN_D}{\epsilon_0\epsilon}(\frac{x^2}{2} - x_n x) + C_p & 0 <= x <= x_n \end{cases} \tag{5.6}$$

Under the logical continuity condition that the potential needs to be the same at x=0 coming from both both sides, its clear that $C_n = C_p = C$. With the above defined boundary conditions we set $U(x_p) = U_0$ (U_0 is negative) and $U(x_n) = 0$ giving rise to equations 5.7 & 5.8

$$U(x_p) = U_0 = -\frac{eN_A}{2\epsilon_0\epsilon}x_p^2 + C \tag{5.7}$$

$$U(x_n) = 0 = +\frac{eN_D}{2\epsilon_0\epsilon}x_n^2 + C \tag{5.8}$$

The subtraction of $U(x_p)$ and $U(x_n)$ gives the applied voltage U_{Diode} and eliminates C:

$$U_{Diode} = U(x_p) - U(x_n) = U_0 = -\frac{e}{2\epsilon_0\epsilon}(N_D x_n^2 + N_A x_p^2) \tag{5.9}$$

With the help of the additional condition of charge conservation formulated as equality of charges in the depleted areas $N_A x_p = N_D x_n$ formulas for x_p and x_n can be deduced.

$$x_p = \sqrt{\frac{2\epsilon_0\epsilon(-U_0)}{eN_A(1 + N_A/N_D)}} \tag{5.10}$$

$$x_n = \sqrt{\frac{2\epsilon_0\epsilon(-U_0)}{eN_D(1 + N_D/N_A)}} \tag{5.11}$$

This gives the following expression for the depletion zone thickness/width w:

$$w = x_n + (-x_p) = \sqrt{\frac{2\epsilon_0 \epsilon U_0}{e} \frac{N_A + N_D}{N_A \cdot N_D}} \tag{5.12}$$

The approximation with $N_D \gg N_A$ gives $w \propto \sqrt{U_{Diode}/N_A}$, showing the depletion zones width dependence of the applied voltage and the lower dopant concentration.

A pn-junction also creates a dynamic capacity. In reverse biased mode it is referred to junction capacitance, created by the depletion zone which separates the mobile charge carriers like a plate capacitor. As known from electrostatics the capacitance of a plate capacitor is proportional to A/d, with A the plate area and d the plate distance. For the pn-junction the depletion zone width can be interpreted as plate distance equivalent, yielding $C_{pn} \propto \sqrt{U}^{-1}$.

5.4 Signal Generation & Charge Collection

As discussed in section 4 incident charged particles interact electromagnetically with the silicon causing ionization, which leads to the creation of electron-hole-pairs along the particles path. Soft X-ray photons will undergo photo effect in the material and produce a charge cloud. The mean creation energy for an electron-hole pair in silicon was measured in several experiments and is given in table 5.1.

The charge collection in a diode is driven by two processes: drift and diffusion, and therefore has two components. The fast component is the collection of the electron-hole pairs created within the depleted area, here they are collected rapidly by the electric field. Electron-hole pairs which have been created in the non-depleted region will diffuse undirected and most probably recombine. However, some will diffuse into the depletion zone and are collected via drift. This gives rise to a slow component, which is expected to be negligible for the MuPix sensors, as the signal will be dominated by charges collected from the depleted volume.

The collection time will depend on the average drift velocity of the electrons and holes in the electric field E. The velocity can be calculated from the mobility μ.

$$v_{drift} = v_d = E \cdot \mu \tag{5.13}$$

. As listed in table 5.1 the mobility differs for electrons and holes. However, for the HV-MAPS sensors only the fast electron component is relevant for the signal generation and holes are not considered any further.

In silicon the electron mobility is constant up to field strengths of $10^4\ V/cm$, for higher fields the electrons scattering with defects and the lattice causes a growing resistance, finally leading to a saturation drift velocity of $\sim 3 \times 10^6 cm/s$ for fields higher than $\approx 10^5\ V/cm$ [22]. A further effect coming up in this field region is the production of secondary electrons, due to primary electrons which could gather enough energy between two scatters to create an electron-hole pair. This can cause an avalanche in the high field region, leading to a signal enhancement and for even higher fields the diodes breakdown, a huge reverse current, most likely thermally destroying the diode.

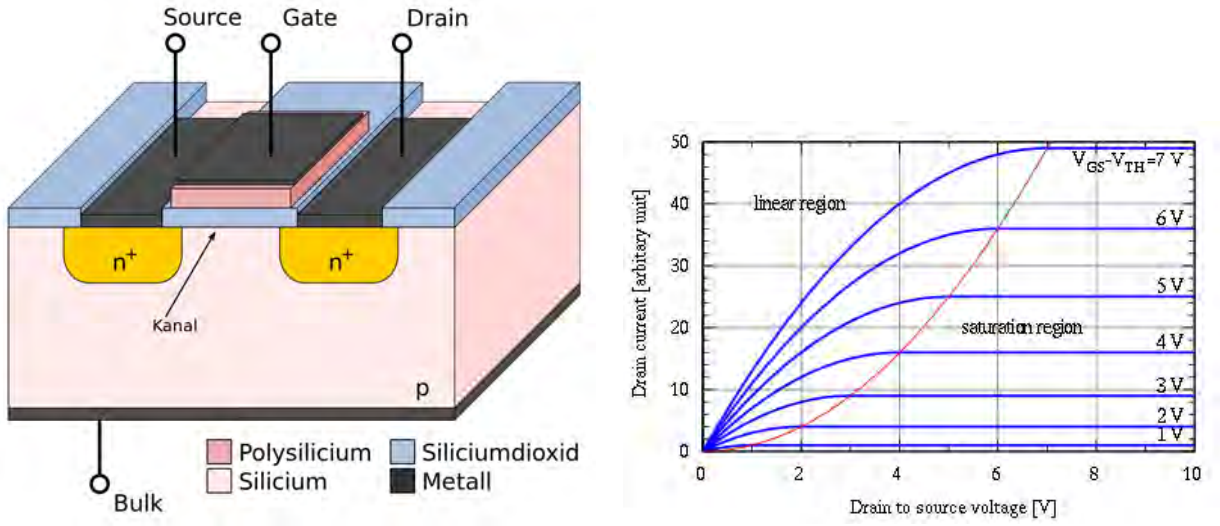
5.5 MOSFET Transistor

Metal-Oxide-Semiconductor Field Effect (MOSFET) transistors are the basic building blocks of all modern electronics. They can be implemented on semiconductor wafers by e.g. implanting two n-doped areas in a p-doped substrate (N-MOS) which are used as electrical contacts. On the surface between the two contacts a metal layer is placed, which is separated from the substrate through an oxide layer. This so-called gate is capacitively coupled to the substrate between the contacts, which allows a modulation of the charge carrier concentration below the gate, forming a conductive channel, allowing to steer the current flowing between the two contacts by changing the gate voltage.

The behavior of the transistor is not linear, the current flowing through the transistor depends on the gate voltage, as well as on the voltage between the two contacts (fig. 5.4(b)).

To understand the discussions in the following, two applications of transistors are important. In digital circuits the transistor can be used as a switch, with no current flowing for no gate voltage and a large current flowing for a high gate voltage. Further they can be used in analog circuits as adjustable resistors and currents sources, as the gate voltage allows to tune the current.

The inverse doping profile gives a p-MOS transistor. In general p- and n-MOS transistors are combined in circuits which is referred to as Complementary MOS (CMOS) technology.



(a) Layout of a n-MOS transistor.

(b) Example U-I-diagram for a n-MOS-transistor.

Figure 5.4: CMOS transistors. Images from [32]&[33]

6 Pixeldetectors and the HV-MAPS technology

6.1 Pixel detectors

Many present experiments, e.g. ATLAS, ALICE and CMS at LHC, make use semiconductor pixel detectors, as they can provide excellent 2D-spatial resolution. For semiconductor pixel sensors usually silicon or germanium wafers are used in a lithographic processes, which can introduce a pixelated doping structure on the wafer, e.g. simple detection diodes, which can be fully depleted. To readout these chips an additional readout chip is needed, which in general is bump bonded to the detection diodes, rendering these detectors a hybrid detector system. This introduces a lot of material causing multiple scattering and is therefore not compatible for the Mu3e experiment requirements.

This motivates the development of pixel detector chips with integrated readout electronics to reduce the material budget.

6.2 Monolithic active pixel sensors (MAPS)

A first step of this integration, made by the photo industry, was the development of Active Pixel Sensors (APS). Each pixel contains a detection sensitive area and digital part for the readout. Which renders the detection form factor rather small with only $\sim 30\%$. For particle detector how ever not only the semiconductor surface can be used for detection, but basically all wafer material below a pixel structure. This allows to build sensors using the full pixel size with electronics on the pixel surface and so $\sim 100\%$ fill factor. These sensor are the so-called Monolithic Active Pixel Sensors (MAPS). They are under way since the 90s and bring the benefit to be produced in commercially available Very Large Scale Integrated (VLSI) CMOS processes, which allows to make use of the industrial driven progress and keep the production cost low compared to specially developed fabrication procedures. Currently the first MAPS particle detectors have been installed in experiments, e.g. the MIMOSA chip [34] for the STAR vertex detector or for the EUDET beam telescopes [35]. The active detection volume for those sensors is the undepleted bulk material beneath the pixel electronics. A charge cloud of electrons and holes induced by a traversing charged particle will diffuse undirected in the semiconductor material and by chance meet the collection electrode. This shows a drawback of the MAPS technology compared to usage of depleted diodes as the diffusive Charge Collection (CC) is slow compared to drift collection in diodes.

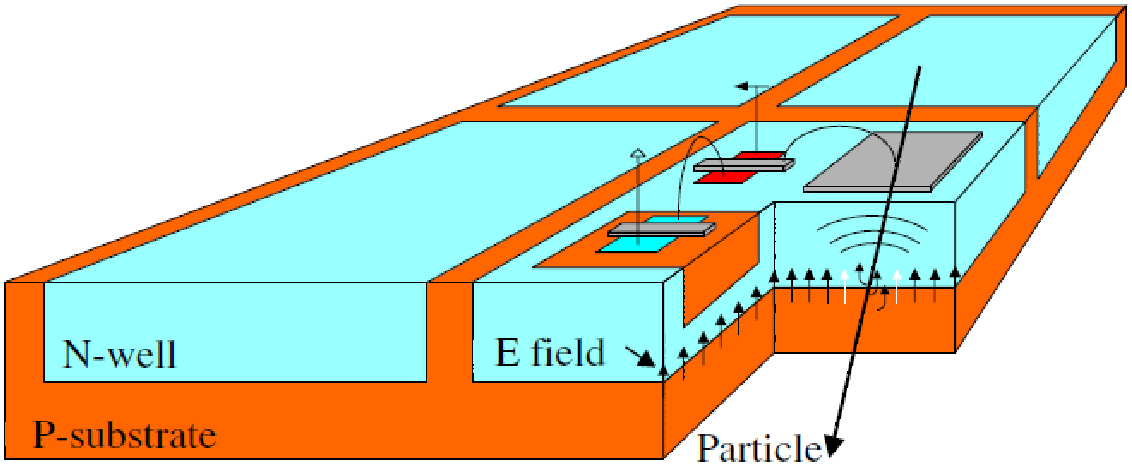


Figure 6.1: Sketch of HV-MAPS pixel diodes: p- and n-doped areas form a diode with an electric field, electrode and logic are implemented in the n-well [36].

6.3 High voltage monolithic active pixel sensors (HV-MAPS)

6.3.1 The Concept

A combination of the MAPS principle with a diode as active detection element, the so-called High Voltage Monolithic Active Pixel Sensors (HV-MAPS), will merge the advantages of both technologies. Each pixel is consisting of a diode and pixel electronics. The diode is made up by the p-doped silicon substrate and a so-called deep n-well as shown in figure 6.1. This design allows to reversely bias the diode by applying a negative voltage $\sim 60V$ at the substrate and create a depletion zone as detection volume with a very fast charge collection and at the same time implement analog and digital electronics using the deep n-well as substrate, this implementation is called floating logic. This new technology also maintains the advantage of commercially available high voltage CMOS processes used e.g. in the automotive or power industry which reduces the cost compared to customized production.

Further it will be possible to thin down the sensor to $\sim 50\mu m$ thickness with out cutting on his performance, as the depletion zone will only extend $\sim 10\mu m$ underneath the sensors surface, rendering the rest of the bulk material unused. This technology was first proposed by Ivan Perić in 2006 [36] and found to be a suitable candidate to fit the requirements for the tracker of the Mu3e experiment.

6.3.2 The MuPix Prototypes

To confirm the suitability of the HV-MAPS concept for the Mu3e experiment, it needs to be qualified and the performance has to characterized with the help of prototype sensors. These are produced in a High Voltage CMOS process in so-called Multi Project Wafer (MPW) runs, which allow a cost efficient prototyping of small Application Specified Inte-

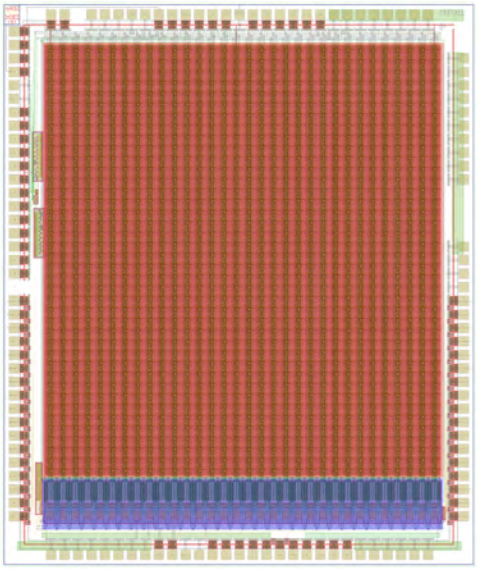


Figure 6.2: Layout of MuPix3: Red colored the pixel matrix, blue colored the peripheral digital part.

Prototype	Pixel Matrix	Pixel Pitch	Novelty	Theses	Year
MuPix1&2	42×36	$39 \times 30\ \mu m^2$	Proof-of-principle	[30], [31]	2011,2012
MuPix3	40×32	$92 \times 80\ \mu m^2$	digital readout	[37], [38]	2013
MuPix4	40×32	$92 \times 80\ \mu m^2$	digital readout	[37], [38]	2013
MuPix6	40×32	$102 \times 80\ \mu m^2$	additional amplifier	this thesis	2014
MuPix7	(40×32)	$(102 \times 80\ \mu m^2)$	full integration		2014

Table 6.1: Overview over present and future MuPix prototypes.

grated Circuits (ASICs). All so far produced MuPix prototypes show a similar structure as they consist of a pixel matrix with an in-pixel pre-amplifier, and discrimination and digital signal handling in a peripheral strip. As shown in table 6.1 several prototypes have been characterized in multiple bachelor and master theses.

The MuPix1 and MuPix2 prototypes are the first HV-MAPS sensors ever produced and served as proof of principle test for the HV-MAPS concept with a charge sensitive amplifier implemented on the pixels diode and already showed a good eligibility for the experiment.

In the further iterations a more involved digital processing of the analog pixel signals and zero suppression mechanisms have been incorporated in the periphery.

In the MuPix6 design an additional amplification stage was added in the periphery.

The recently arrived MuPix7 prototype incorporates a readout state machine and timestamp generator in the periphery, so it will be independent of external readout signals. This means all wanted components of the final chip are already implemented on this prototype.

The characterization of the MuPix6 prototype is the topic of this thesis.

Part II

Setup

7 The Mupix

In the framework of this thesis two prototypes are investigated. One prototype is the MuPix4, which has already been studied extensively [37]. This prototype is now also available in an industrial thinned version, which is studied with respect to a performance impact in the lab and on a testbeam campaign. The second is the MuPix6 prototype whose characterization poses the main part of this thesis.

7.1 Mupix4

The MuPix4 prototype was already characterized in the previous thesis [37]. Therefore the prototypes structure is only discussed briefly, as in most parts its very parallel to the MuPix6 structure described in the following section 7.2.

The MuPix4 consists of a 32×40 pixel matrix with a pixel size of column-pitch=$92\mu m$ and row-pitch=$80\mu m$, giving an active area of $2.944 \times 3.2mm^2$. The physical chip size covers an area of $3.5 \times 4.16mm^2$, giving a fill factor of 64.7% including pads. However, the important number is the ratio of digital part to active area, which is $380\mu m/3200\mu m = 11.2\%$. These numbers will improve further for a larger chip as the inactive area e.g. covered by pads or supply voltage lines will not scale with the chip size.

Each pixel is subdivided in a shorted 3×3 diode structure (fig. 7.4) with the central diode's deep n-well housing a charge sensitive amplifier (CSA) and a source follower (SF) to drive the high capacity line to the periphery.

In the periphery this signal is discriminated and passed to the digital readout system. This part is not fully functional, as for half of the pixel rows the address is deleted before it could be readout. This problem caused a distinct pixel hit pattern, referred to as the "Strixel "-problem (figure 7.1).

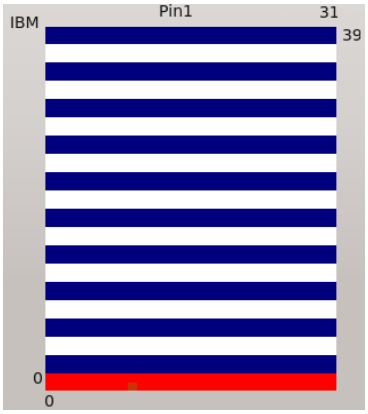


Figure 7.1: The strixel pattern of the MuPix4 prototype observed with the online monitor of the graphical user interface.

7.2 Mupix6

The MuPix6 (actually it is the fifth prototype) was submitted with a fix of the readout system which is supposed to solve the "Strixel"-problem. Further a new amplification scheme is tested by adding an additional amplification stage in the periphery before the discriminator with the intention of achieving a better Signal-to-Noise-Ratio (SNR). This guarantees a higher stability against possible digital cross talk caused by readout signals and timestamps. The intention is an additional amplification factor of three [39].

In the following the pixel and readout structure is discussed, from the initial diode signal to the readout data.

7.2.1 The Chip

As the MuPix6 is the direct successor of the MuPix4 it inherits the general layout structure as depicted in figure 7.2, but with slightly different sizes. The change in size is caused by the additional amplification stage, due to the fact that the column-pitch of the pixel is matched to the digital part extensions. In the column-pitch of one pixel two pixel periphery units can be placed as shown in figure. 7.4. This gives a new pixel pitch of $102 \times 80\mu m$, enlarging the detection area to $3.296 \times 3.2mm^2$. However, due to the symmetric expansion of pixel and digital part the ratio of active and digital part is conserved. Each pixel consists of a CSA and SF in the pixel and a corresponding digital element in

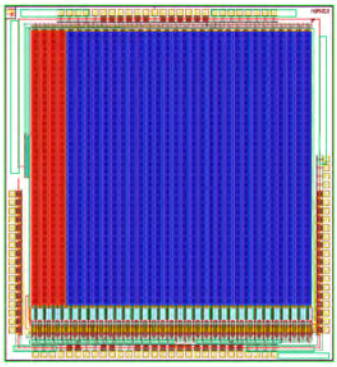


Figure 7.2: The MuPix6 Chip Layout exported from Cadence® Red: 1-staged pixel, blue: 2-staged pixel.

the periphery (fig.7.3). While the physical pixels are arranged in a 32×40 matrix, the digital parts are organized in a 64×20 matrix. The pixel addresses, readout in the end, are also generated in the digital part encoding the position in the digital part matrix, which makes a decoding to physical pixel addresses necessary. This mapping procedure was also described in [38] for MuPix4 and for MuPix6 in [40]. From this we can deduce a logical smallest unit cell shown in figure 7.3, which also enlightens the address scheme.

As shown in figure 7.2 in the MuPix6 prototype two types of pixels are implemented. 4 columns are manufactured in the "old "Mupix4 pixel design with only the CSA in the pixel, while the rest has an additional amplification stage in the periphery. This thesis focuses mainly on the 2-stage amplification pixels.

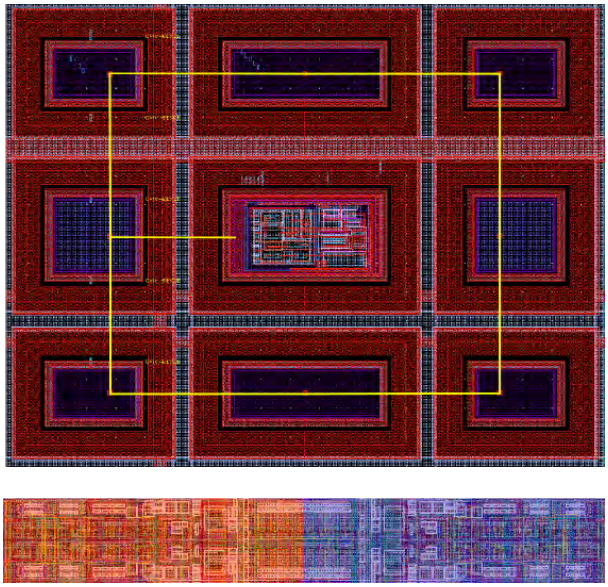


Figure 7.3: The MuPix6 Pixel Layout exported from Cadence®. Size matching of a pixel and 2 digital structures.

To steer the pixels performance two shift registers are placed on the chip whose values can be stored in RAM cells. One registers is controlling the so-called chip Digital-to-Analog Converters (chip DACs), which generate bias voltages for the pixels (6-bit), which will be discussed in the following. The other is used to set the so-called tune DACs and to select one pixel for a dedicated "hitbus"readout. The hitbus signal is the discriminator output of the selected pixel.

7.2.2 The Pixel

As depicted in figure 7.4 each pixel consists of 3×3 diodes. Each diode is made up by a deep n-well and the surrounding p-substrate. Within the deep n-well an additional shallow n-well is placed as electrode. The diode is connected via the resistive silicon-metal contacts as seen in figure 7.4 allowing to reverse bias the diode with a negative voltage on the p-substrate and a positive voltage on the n-well.

All n-well contacts of a pixel are shorted constructing one collection electrode. After the pixel is hit, e.g. by a charged particle, the collected charge is slowly feedback by a bias restoration circuit (making use of leakage currents).

The central diode also houses the in-pixel logic, the CSA and the SF. The CSA is capacitively coupled to the n-well contact, producing a voltage drop on the input if charge is collected by the electrode. This results in an increasing output voltage, charging the storage capacity. This capacity is then linearly discharged by the feedback circuit. As depicted in figure 7.5.

The CSA on its own is not designed to drive a high capacity line, which is why a driving SF is used to transmit the signal to the periphery. It is build of two transistors acting as resistors in a voltage divider, transmitting the output signal to the signal line.

To steer the performance of the CSA and SF five bias voltages are used, four are provided by the chip DACs and one is provided externally. Their origin and the effect is

Bias Voltage	Origin	Circuit Part	Function	Effect
VN	DAC	CSA	Current Source	On/Off switch steers current
VNLoad	DAC	CSA	Voltage divider	adjusts amplification
VPCasc	External	CSA		
VNFB	DAC	CSA	Resistance	linear CSA feedback
VNFoll	DAC	SF	Current source	SF output voltage control

Table 7.1: Summary of the pixels bias voltages.

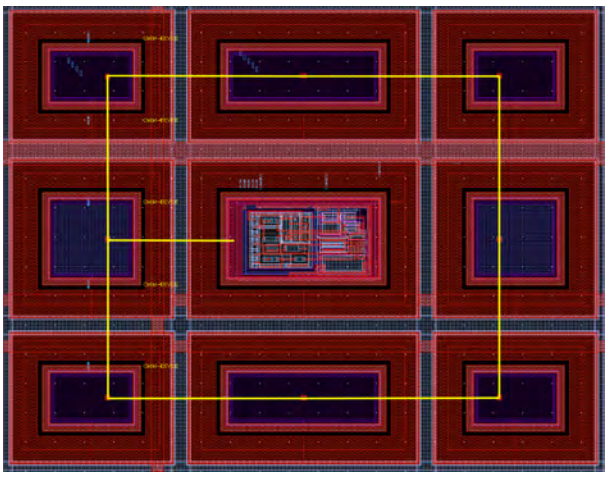


Figure 7.4: Layout of a single pixel 3x3 diodes.

listed in table 7.1.

7.2.3 The Digital Part

In the new amplification scheme the signal line driven by the SF leads to a capacitance on the input of the second amplification stage. It amplifies the signal in the same manner as the CSA in the pixel, also using 4 bias voltages as listed in table 7.2

The output of the second stage is capacitively coupled to the so-called Baseline (BL). The amplified signal modulates the BL. It is directly connected to a comparator stage which compares the BL to a Threshold voltage (THR). In case the BL voltage sinks below the THR due to the modulation, a normalized digital pulse is created on its output. The duration of this pulse is proportional to the time the BL voltage is lower than the THR voltage, this defines the so-called time-over-threshold[1] (ToT). The comparators performance can be steered by one bias voltage, which controls the main current of the comparator. A further bias voltage (BLRes) controls a transistor in resistor mode steering the BL restoration. It defines together with the comparators capacitance the main shaping element in the pixel, a high pass.

As chip production processes are known not to be completely homogeneous, the analog behavior of different pixels is expected to vary slightly. To compensate those differences

[1]This comparator is actually defining a time-under-threshold, but for historical reason it is ToT

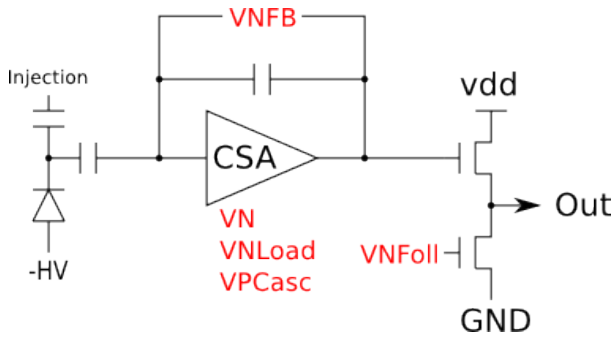


Figure 7.5: Simplified schematic of the in-pixel logic.

Bias Voltage	Origin	Circuit Part	Function	Effect
VN2	DAC	Amp2	Current Source	On/Off switch steers current
VNLoad2	DAC	Amp2	Voltage divider	adjusts amplification
VPCasc	External	Amp2		
VNFB2	DAC	Amp2	Resistance	linear CSA feedback
VPComp	DAC	Comparator	Current source	Current & speed control On/Off switch
BL	External	Comparator	Baseline	Voltage offset for signal Comparator input
THR	External	Comparator	Threshold	Comparator reference
BLRes	DAC	Comparator	Resitance	Shaping
VPDAC	DAC	Comparator		Tuning
VNDel	DAC	Edge detector		Delay

Table 7.2: Summary of the bias voltages of the digital part.

each pixel is provided with a 4-bit tune DAC (TDAC), which allows to feed an additional current to the comparator and shift the working point of the BL input for each pixel artificially. The maximal possible tune current is determined by VPDAC which is steering the transistors acting as current sources of the TDACs.

For the digital logic after the comparator it is only relevant, whether the BL voltage crossed the THR level and causes the comparator output to switch. This level shift of comparator output is detected with the help of a so-called edge detector, which produces a short digital pulse on a rising edge. In case a rising edge is detected, a latch connected to the edge detector stores a hit flag until it is readout.

Each digital element also houses 8 capacities used as timestamp bits. In the MuPix6 chip the timestamp pattern is externally provided and will be discussed later in detail (section 7.5.1). In case of no hit in a pixel, the timestamp capacities are either charged or uncharged according to the input pattern. When a pixel hit is recognized and the hit flag latch (hit latch) switches, the state of the capacities is frozen and stored for readout.

The comparator signal can also be multiplexed outside, referred to as the hitbus signal.

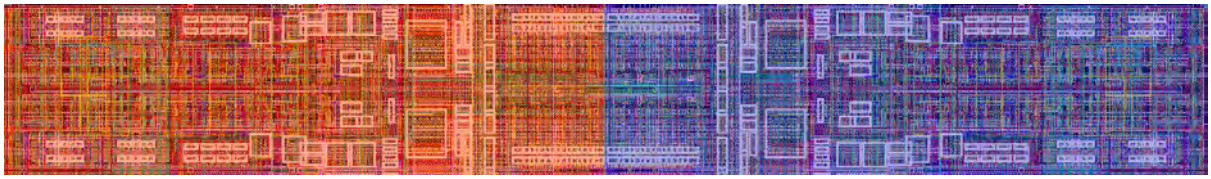


Figure 7.6: Layout of two digital elements, placed in a mirrored configuration.

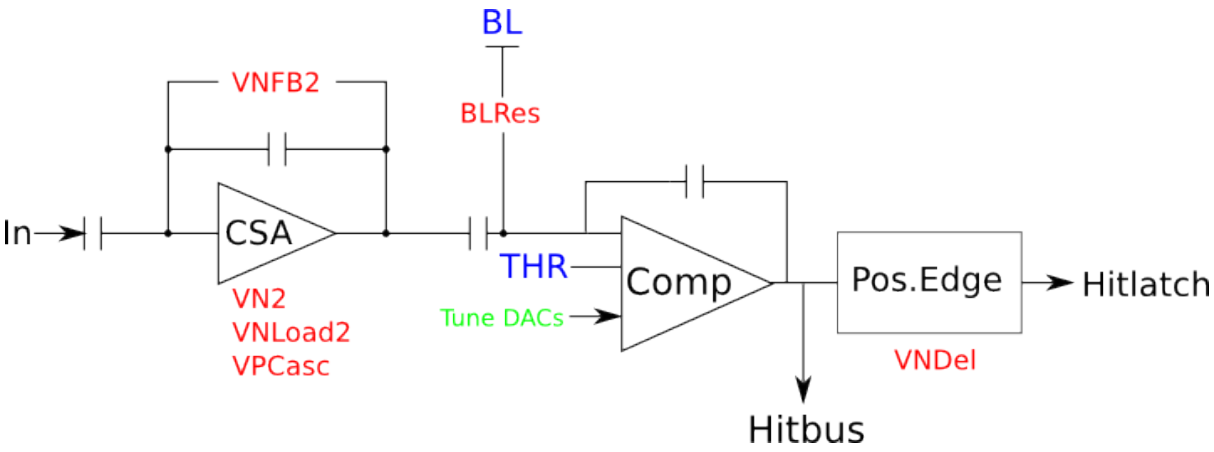


Figure 7.7: The comparator electronics and bias voltages.

7.2.4 Signal Shaping

All electric circuits have an intrinsic bandwidth which will cause a deformation of a treated signal. This property can be actively used to manipulate signals, which is called signal shaping.

RC-circuits provide a tunable band width and create a high- or low-pass behavior. A detailed discussion can be found in [22], [30], [38] and [31].

The signal shape is mainly influenced by the the amplifiers and the comparator.

The amplifiers, which are realized as special integrators, are provided with a feedback circuit which leads to a linear signal decrease instead of an exponential decay, as expected from the high-pass behavior of a standard integrator circuit.

Contrary, the comparator's capacitance is discharged via a resistance, yielding a normal high-pass behavior.

As described above only high-pass components are used for the signal shaping, which guarantees a fast first signal edge. Nevertheless the signals first edge is not infinitely sharp due to the circuit's intrinsic bandwidth, which gives rise to a threshold dependence of the signals latency, the time walk.

Mathematically the signal shape can be approximately described as the response of a high-pass low-pass filter combination to a rectangular input signal[22]

$$U(t) = U_0 \frac{\tau_1}{\tau_1 - \tau_2} (\exp^{-\frac{t}{\tau_1}} - \exp^{-\frac{t}{\tau_2}}) \tag{7.1}$$

with U_0 being the input signal's amplitude, τ_1 the time constant for the signal decay and τ_2 the time constant for the signal rise. This equation does not include the linear behavior of the feedback.

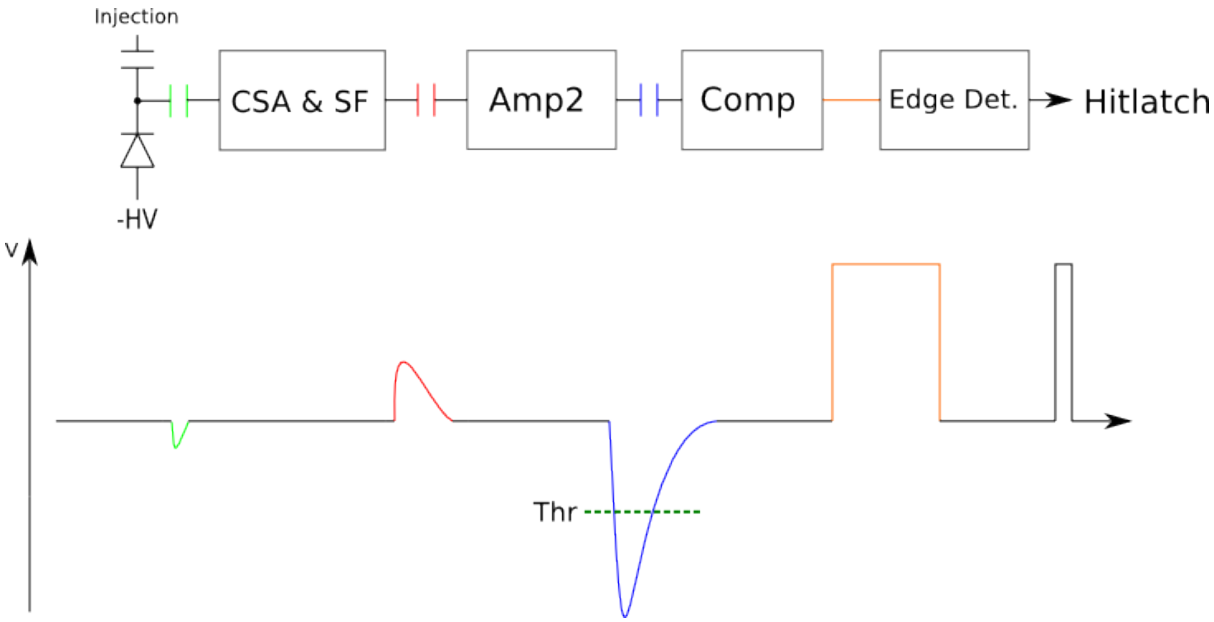


Figure 7.8: Shaping from the diode signal to the Hitlatch.

7.2.5 The Readout

Hit data has to be readout as fast as possible to prohibit dead times due to the occupation of the hit flag latch, which can not store a new hit flag until it is reset. This logic is fully implemented on the chip, but needs external readout signals (fig. 7.9). The pattern of these signals is fixed and provided by a state machine running on an FPGA with 50 MHz [41].

A priority encoded readout is used, generating a priority signal, which tells the external readout state machine whether there is data to be read. This allows in the case of a small sensor occupancy, as expected for the Mu3e experiment, a very fast and zero suppressed readout. For the MuPix chip two types of priority signals are present. Internally each digital column has a priority signal, indicating whether hit information is stored in one of the pixels. Further there is a priority signal created in the column logic, which is used by the state machine as shown in the following.

The first step in the readout scheme is the load pixel signal (LD_Pix), which loads the state of the hit latch to the so-called pixel latch. It is decoupled of the analog circuits and fully integrated in the readout logic and the column priority signal.

The next signal, the pulldown (PD), does not contribute to any readout step, but cleans the address and timestamp outputs on the chip by setting all address lines on a defined voltage, before the next signal, load column (LD_Col), is applied. With this signal the priority signal of each column is checked for hit flags and in case of a present priority signal, the hit information consisting of hit flag, the row address, and timestamp are copied to a column logic block denoted to that column. The column logic blocks are chained and produce the column logic priority signal. When the pixel information is copied to the column block, hit and pixel latch are reset, also re-enabling the timestamps. Then the hit latch is sensitive to new pixel hits.

The read column signal (RD_Col) then is applied repeatedly until the priority signal

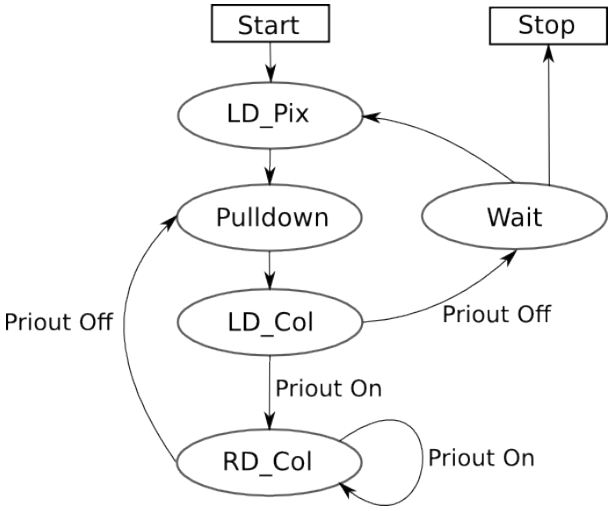


Figure 7.9: Schematic of the readout state machine.

(PriOut) vanishes and all column logic blocks with hit flags have been read. While the RD_Col is applied the read pixel's column address, row address, and timestamp signals are mapped to the chips parallel address and timestamp fan-out, allowing the sampling of the pixel information (fig. 7.10). When the column logic priority signal vanishes, the state machine has to start over from the PD signal checking again the columns for further hits, which then are readout in the same manner. In case the LD_Col signal does not give rise to a column logic priority signal, there is no more hit information stored on the chip and a new readout process can start with LD_Pix.

To have a better control of the readout cycles and the integration time between to readouts (LD_Pix to LD_Pix) an additional waiting state can be introduced, waiting a defined time till the next LD_Pix signal. This allows isochronous integration windows, which is a priory not guaranteed by the purely data driven priority readout, but needed for many measurements.

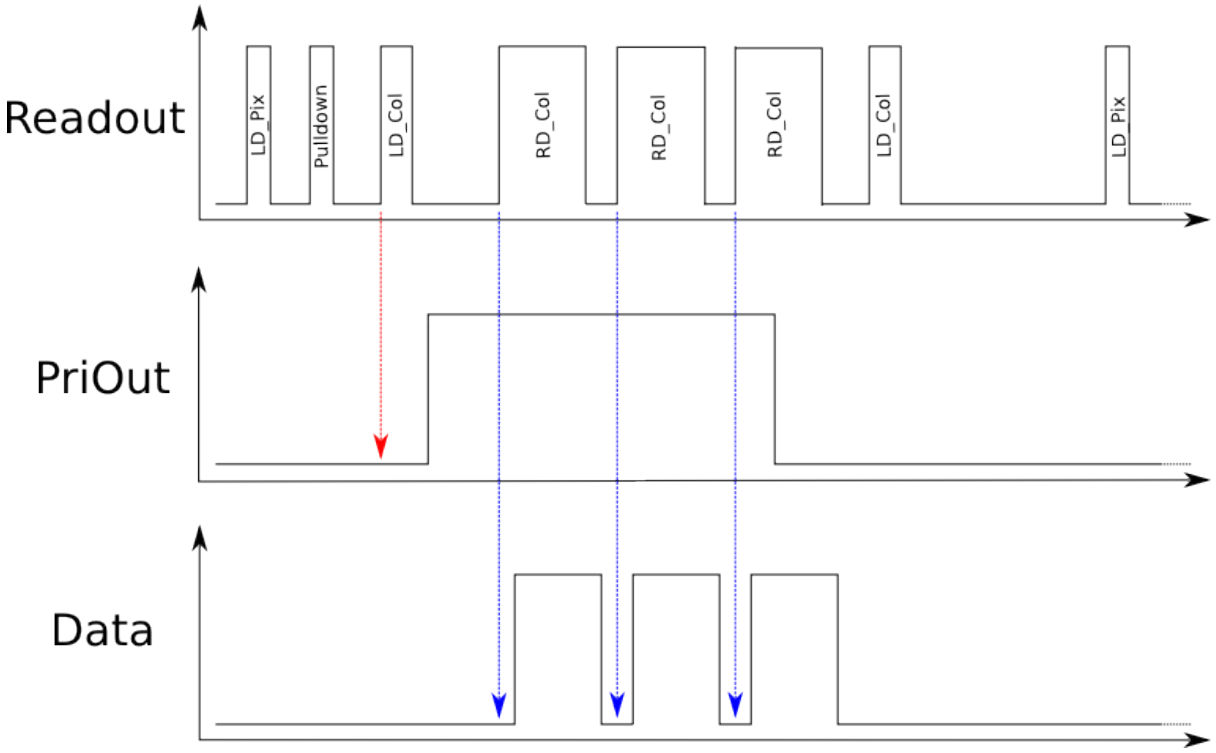


Figure 7.10: Readout pattern applied to the chip with 3 readout hits

7.2.6 The Sensor I/O

The sensor in- and output is provided via aluminum pads in the outer most periphery of the chip, which can be connected e.g. to contacts on a chip carrier via aluminum bonding wires.

The chip needs to provide connections for supply voltages and the high voltage (HV) essential for HV-MAPS. Furthermore it needs control pads for the shift registers used for the chip configuration, as well as inputs for external bias voltages as the BL and THR. As the MuPix6 chip needs external readout signals, inputs have to be provided for timestamps, LD_Pix, PD, LD_Col, and RD_Col plus the parallel fan-out for the pixel addresses and the stored timestamps.

The chip further provides some debugging in- and outputs as the injection signals, which are capacitively coupled to the center pixel electrode, allowing the injection of a tunable pulse to test the pixel electronics. Above all it provides a pad with the earlier mentioned hitbus signal giving us a probe to check the analog behavior of the pixel electronics. In addition it provides a new feature as it is possible to directly contact a deep n-well and through this study the diodes properties.

Signal	I/O	Function	# Pads
1.5V	I	Supply voltage	1
1.8V	I	Supply voltage	multiple
Ground	I	Supply voltage	multiple
High Voltage	I	reverse bias	2
LD_Pix	I	Readout	1
PD			1
LD_Col			1
RD_Col			1
PriOut	O	Readout	1
TimestampIn	I	Clock	8
TimestampOut	O	Digital output	8
Column Address	O	Digital output	6
Row Address	O	Digital output	6
Injection	I	Artificial pulse	2
Hitbus	O	Comparator output	1
Baseline(BL)	I	Bias current	1
Threshold(THR)	I	Bias current	1
VPCasc	I	Bias current	1
Shift register I/0	I/O	Slowcontrol	6

Table 7.3: Summary of the important in- and outputs pads.

7.3 The Single Setup

The single setup is a characterization tool for the MuPix prototypes, as it allows to check, debug, and measure all functions, signals, and properties of the chip.

In the following the baseline design is presented as well as the modifications and upgrades which aim to improve the setups performance.

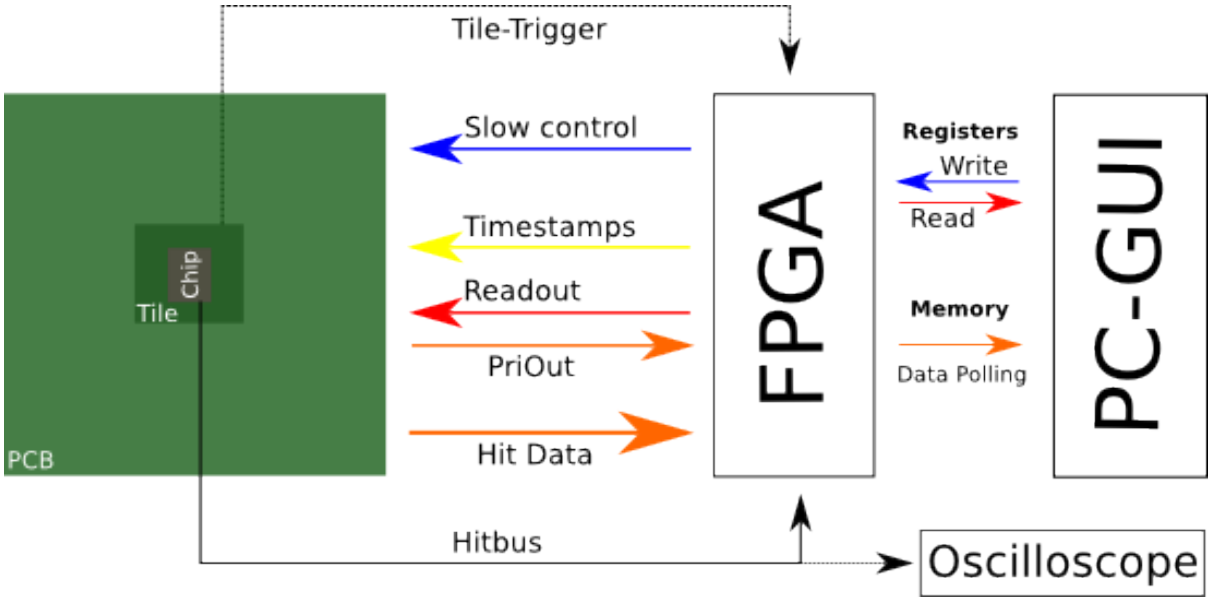


Figure 7.11: Schematic of the setup.

7.4 The Hardware

The main components of the single setup are a printed circuit board (PCB) which houses the chip and provides connections for all chip in- and outputs, and a Field Programmable Gate Array (FPGA) connected to the PCB for steering and readout. The FPGA is connected to a computer via a fast Peripheral Component Interconnect Express (PCI-E) to control the FPGA via register states. Supply voltages are provided by off-the-shell high and low voltage power supplies [42],[43].

7.4.1 The PCB

The PCB provides an interface for the chip either via a slot for a 84-pin ceramic carrier, which allows to test all chips housed on a ceramic carrier or via a gold pad fan-out which allows to glue and wire bond the chip directly to the PCB.

Currently two version of on-board chips are available: glued to the non-conductive PCB substrate which is thinned down to about 100 μm and the "floating"MuPix variant which is glued to a 25μm Kapton® foil. The thinning of the board and the usage of the Kapton® foil is motivated by the need for material budget reduction in test beam measurements. Further the floating MuPix poses a first feasibility study for sensors glued and bonded on a Kapton® foil as requested by the experiment.

The boards provides two 40-pole flat ribbon cable plugs for slow control and readout, and two SubMiniature version A (SMA) connectors as HV and 5 Volt low voltage input. This low voltage is converted on-board to 3.3 V, 1.8 V, and 1.5 Volt. 1.8 and 1.5 Volt are power lines for the chip and the chip's external bias voltages created with voltage dividers on board. The 3.3 V line is used as power source for three DACs places on the board, which are responsible for the external threshold and injection voltages. Further the 3.3 V is also supply voltage for inverters used as drivers for the chips digital output signals [44].

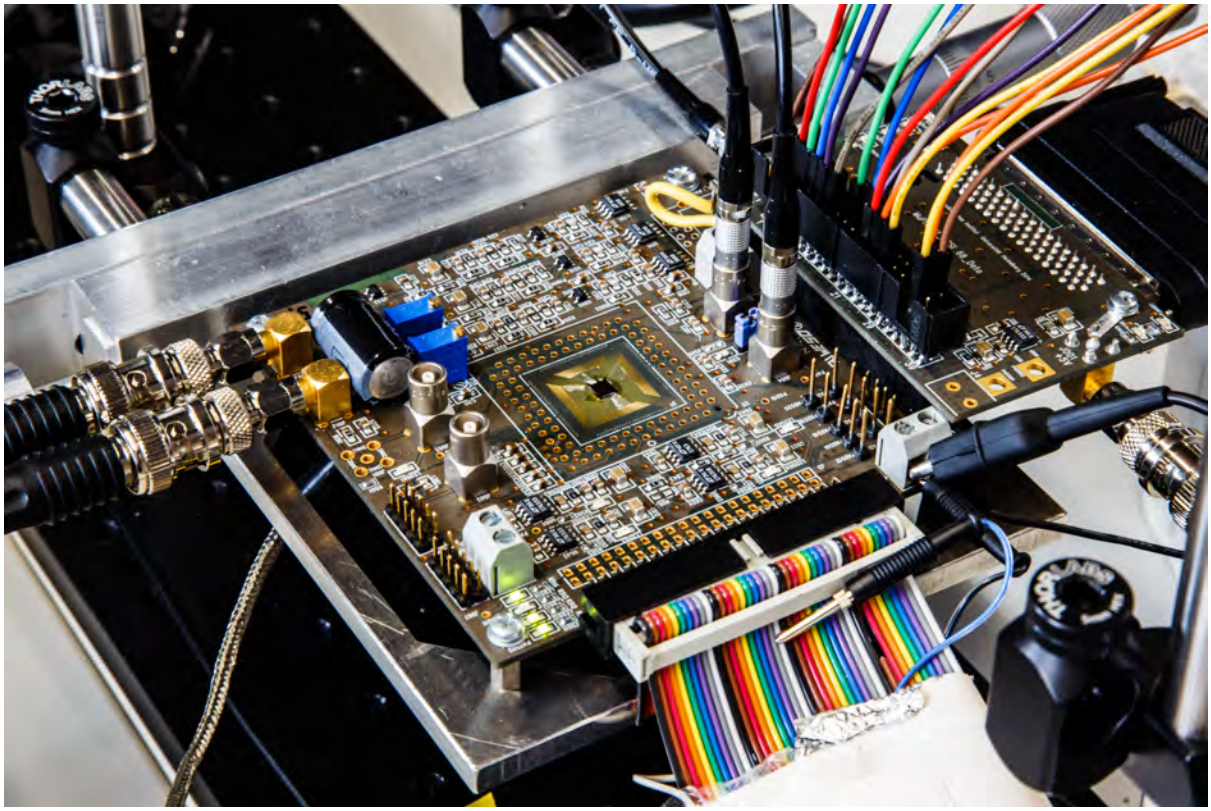


Figure 7.12: Fully connected PCB with on-board chip.

7.4.2 The FPGA

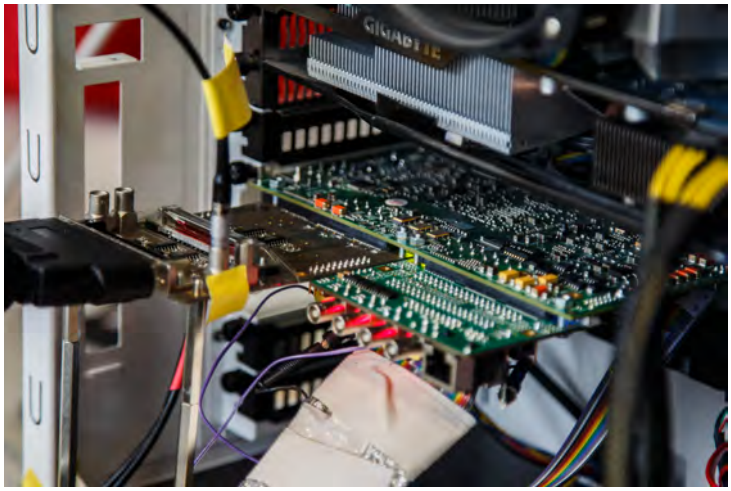


Figure 7.13: The Stratx FPGA board housed in the PC with adapter cards for readout (left) and slow control (right).

The Field Programmable Gate Array (FPGA) concept was developed in the 80s when the construction of more and more complex logic circuits as Application Specified Integrated Circuits (ASIC) was no longer a good choice due to high cost and development time. An FPGA consists of several thousand basic logic units which can be wired by programmable logic switches. This allows very high flexibility and time-efficiency in programming and debugging.

The setup uses a Stratix IV Development Kit directly plugged to a computers PCI-E card slot. It provides an on-board FPGA and two High Speed Mezzazine Card Connectors (HSMC) used to steer and readout the setup. As the baseline-board requires flat ribbon cables as signal input medium, there is HSMC-to-flat-ribbon adapter for slow control and readout HSMC respectively.

Besides the flat ribbon connectors the adapters also provides trigger inputs and signal lines which allow to synchronize and reset several Stratix boards as needed for the MuPix telescope [40],[45].

The development kit can be run in two modes: Either *runningmode*, executing the FPGA program, or *loadingmode* to load a new FPGA software into the flash-memory, which allows a maximal flexibility for software debugging and updating.

7.4.3 The Trigger System

To measure the time behavior of a system precisely a reference system is needed which provides a very good time resolution. For the MuPix characterization this plays a role especially for test beam measurements and in general measurements with charged particles. The reference system of our choice is a scintillating tile connected to a SiPM, a similar system as used for the Mu3e tile detector, fabricated at the Kirchhof Institut für Physik (KIP) [46].

The tile signals are discriminated and send to the FPGA's trigger input. Single tile or coincident tile setups are possible, which provide a time resolution of 100 ps and better.

7.4.4 The Mechanics

The mechanical support structure for test beam campaigns and lab measurements makes use of the mechanics developed for the MuPix telescope [40], which allows to construct a rigid and flexible setup based on Thorlabs® mechanics.

7.5 The Software

The software was newly developed in the context of this thesis. This was triggered by divergence of the previous single setup software and the new developed telescope software, which also required different FPGA programs.

To simplify the maintenance of both systems there is now only one FPGA program which can handle several or only one chip and combines the functionality of both setups. The required common basic software interface was developed in synergy with the telescope, allowing to profit from new developments on both projects. As a result, the software had to be rebuild completely to provide the old functionality and more.

7.5.1 The FPGA Firmware

The chip-setup is steered and readout via the Stratix Development Board. The firmware offers the possibility to configure and read data from the FPGA via registers as well as it provides a data memory [41]. To communicate with the FPGA a driver has been developed [47], which maps the FPGA registers and memory to the computers RAM. The computer can either use a Polling or a Direct Memory Access (DMA) protocol [38] to read the FPGA. In this thesis only the slower Polling protocol was used.

The current firmware provides the following features:

On-board DACs: The threshold and the injection voltage is generated by DAC units on the PCB, the FPGA provides routines to set those voltage limits and also to generate injection pulses with an adjustable length.

Chip Shift Registers: The FPGA provides a procedure to fill the chip's shift registers and load this configuration to Random Access Memory (RAM) cells, which steers the DACs and configuration bits.

Time: The FPGA provides an internal 48-bit time counter which runs at 400 MHz. This is the master clock from which all time information is extracted.

Timestamps: The MuPix6 chip does not produce timestamps on its own, but they can be provided externally. The FPGA can generate 8-bit time stamps, which are send to the chip's time stamp inputs. The time stamps can either be a fixed pattern or be extracted from the internal 400 MHz clock, covering 16 frequencies in a range from 400 MHz - 12 kHz which can be chosen via a division factor. The division factor describes the offset of the least significant bit (LSB) of the time stamps to the master clock.

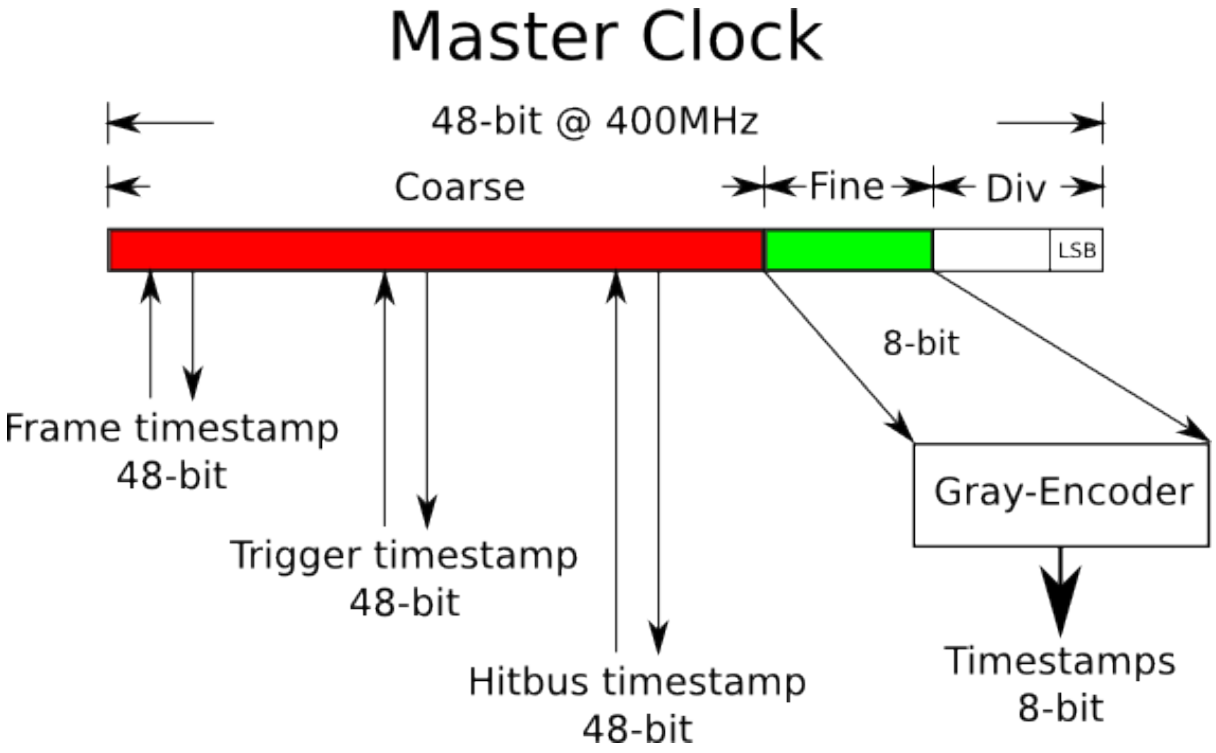


Figure 7.14: Main timing scheme of the FPGA: Division factor (Div), Coarse Time information and Fine time provided by the timestamps.

The time stamps are gray-encoded [40], guaranteeing only one bit-switch per count with the intention to minimize possible digital cross talk. To investigate this cross talk it is also possible to choose a mode which switches all bits at once.

Readout state machine: As explained in section 7.2.5, the chip needs a distinct pattern of readout signals to get out the hit information consisting of row-, column-address and time stamp. The firmware provides a state machine which produces the readout signals (LD_Pix etc.) in the correct order and samples the data. However, the duration and relative timing of the signals and sampling points can be adjusted manually via FPGA registers. This is important as the readout pattern depends on signal delays and quality. The sampled data is saved in the FPGA memory in the form of hit blocks as described in [45], containing the hit information and a 48-bit time stamp marking the begin of the readout.

Triggers & Hitbus: There are 4 trigger inputs of which two can be modified to sample the hitbus signal.

The trigger signals rising edge is sampled with 400 MHz and saved in a trigger block as 48-bit time stamp (fig. 7.14).

The same applies for the hitbus signal, for which additionally the pulse length (ToT) is sampled with 100 MHz. Further the FPGA offers the possibility to sample the ToT with an internal histogram and 4 ns bin size.

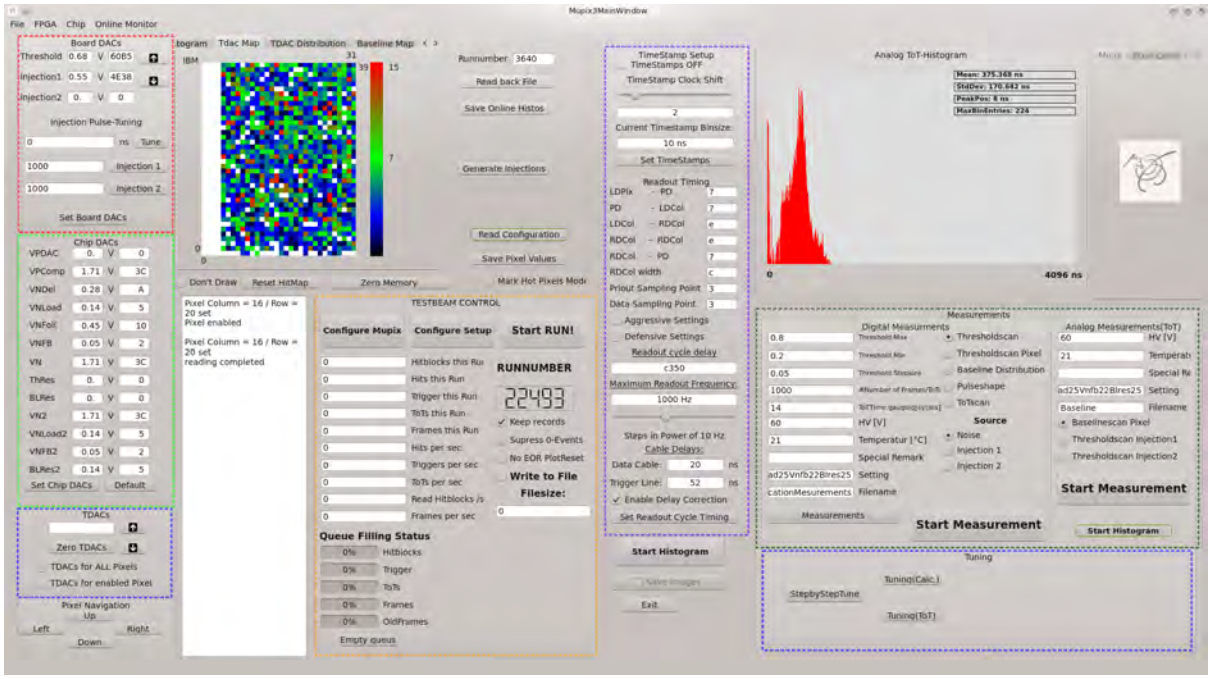


Figure 7.15: The Graphical User Interface Main Window: Red-Threshold and injection control, bright Green- The bias DAC settings, Blue-TDACs and tuning methods, Purpel-timestamp and readout pattern control, Orange-readout control panel, dark Green-automated measurements.

7.5.2 Graphical User Interface(GUI)

The GUI provides a user friendly interface, implemented in C++ using Qt- and boost-libraries, which allows to interact with the setup and test the chip's properties without knowing the FPGA details.

The main constituents are the mainwindow and the online monitoring window, but it also provides direct access to the FPGA registers and memory for debugging.

The mainwindow provides interfaces for all tunable setup parameters (fig. 7.15):

- Threshold
- Injection
- Chip DACs
- Tune DACs
- Hitbus Enable
- Readout Signal Pattern
- Timestamps

Further it provides the “testbeam control“ (TBC), enabling a continuous run-based readout, which runs stable and allows to take large data samples with constant settings. While running, the TBC provides online data rates and monitoring of many key quantities and correlations to check the data quality.

The continuous readout and the hitbus can be used to measure analog properties of the pixel electronics. Several measurement routines are implemented, which are used for the characterization (section 9).

7.5.3 Data Format

The setup produces three types of data: hit position and time, triggers, and the hitbus signal. They are saved in the FPGA memory in three respective data blocks hitblock, triggerblock, and hitbusblock. These blocks are made up of 32-bit words and labeled with begin- and end-of-event markers also indicating the block type. Further a block counter is including give a simple crosscheck possibility, whether blocks are lost [45].

The hitblock contains all hit information of one readout cycle and a 48-bit timestamp marking the starting time of the readout cycle.

The triggerblock holds 48-bit trigger times.

The hitbusblock incorporates 48-bit times marking the rising edge of the signal, equivalent to the trigger and 8-bit encoding the pulses length.

Word offset	Value	Comment
0	0xFABEABBA	Beginning of hit block marker
1	0 Hit block counter 14 Counter 47 down to 31	Simple crosscheck if blocks are lost
2	0 Counter 30 down to 0	Counting at 400 MHz
3	ChipMarker 12 bit	N Hits
	Column 6 Row 6 Time 8	
N + 2	0xBEEFBEEF	End of hit block marker

Table 7.4: FPGA Hit-Block Structure.

Word offset	Value	Comment
0	0xCAFECAFE	Beginning of trigger block marker
1	Trigger block counter	Simple Crosscheck if blocks are lost
2	Coarse counter	2.5 ns counter, bits 47 down to 24
3	Trigger fine counter	2.5 ns counter, bits 23 down to 0
$2 \cdot N + 1$	0xCAFEBABE	End of trigger block marker

Table 7.5: FPGA Trigger-Block Structure.

Word offset	Value	Comment
0	0xBADEBADE	Beginning of hitbus block marker
1	Hitbus block counter	Simple Crosscheck if blocks are lost
2	Hitbus info	Bit 28: 0 for front, 1 for back, 27 down to 0 upper bits of coarse counter
3	Hitbus info	Bit 28: 0 for front, 1 for back, 27 down to 8 lower bits of coarse counter 7 down to 0 length of hitbus pulse
$2 \cdot N + 1$	0xBEADDEED	End of hitbus block marker

Table 7.6: FPGA Hitbus-Block Structure.

7.5.4 Readout Software

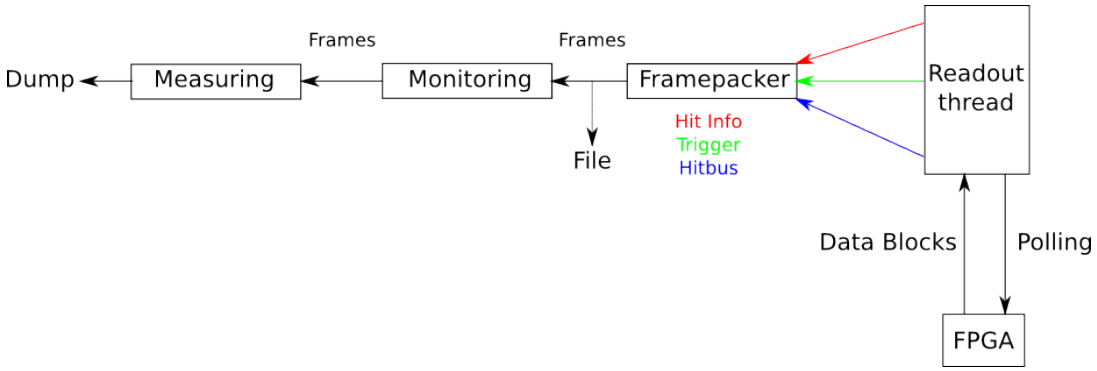


Figure 7.16: The readout chain.

The readout is programmed multithreaded allowing parallel execution of several tasks at a time on a multicore Central Processing Unit (CPU). This allows to implement a very fast readout structure. A safe communication between the threads is possible via a signal-slot-system. The data flow between the asynchronous threads is achieved via threadsafe queues, guaranteeing a save data transfer (fig. 7.16).

For the single setup the basic threads are the readout thread and the framepacker thread. The readout thread pulls data in blocks from the FPGA memory via a polling protocol [38] and sorts the blocks into three queues handling hit data, trigger data, and hitbus data respectively. The framepacker-thread reads the data from the queues and builds time slices, referred to as frames. Each time slice contains the hit data from one readout cycle and all triggers and hitbus events, which occurred before the hitblocks timestamp.

The frames are written to a frame-object [40] and stored in a binary file, which can be evaluated later on. However, to provide the possibility of online monitoring the frames are also queued to a further thread, which evaluates the data in real time and extracts important quantities and correlations. The gathered information is then plotted in the online monitoring window.

The data extracted from the chip does not always need to be stored on disk, but can sometimes be evaluated right away for measurements of chip properties (section 9). For this purpose a further thread is installed also using the frame data stream.

7.6 Setup Improvements

7.6.1 Cable Cross Talk

The single ended nature of the signals on the flat ribbon cable causes a lot of cross talk between different signal lines, especially for fast switching signals as the time stamps. This leads to wrong sampled signal levels and renders the chip basically unusable.

This can be solved either by extensive shielding of the signal lines or by the usage of differential signals. This triggered the development of a LVDS readout, which has to replace the flat ribbon of the readout.

The LVDS standard is realized with a pair of cables. A transmitter creates a constant 3.5 mA current flowing through one cable to the receiver and flow back from the receiver through the other cable. On the receiver side the line is terminated with 100Ω, causing a voltage of $\pm 350mV$ depending on the current direction. The current direction is given by the logic level on the transmitter. As the LVDS standard is very stable against cross talk, and no net current is flowing between transmitter and receiver side a charging or substantial ground current is prevented.

For the conversion from single ended to differential signals and adapter board has been developed, which connects to the flat ribbon plug on the board. This allows to minimize the length of the single ended lines. The signal is transmitted via a SCSI III cable, consisting of twisted and shielded differential pairs, which allows a cross talk free signal transmission. For the FPGA side a new HSMC adapter is used which can handle the LVDS signals from the SCSI cable and converts them to single ended signals, which allows to use the same HSMC pinout as before and does not require a substantial change of the FPGA software.

However, as there are still single ended signal lines on both ends, cross talk is not completely extinguished, but suppressed to a very small level and does not show a significant impact.

8 The MuPix Telescope

The MuPix telescope was successfully developed in the scope of a master thesis [40].

It uses a stack of 4 MuPix sensors to track charged particles, which are readout in parallel with two FPGAs. As the final version of the telescope had not been fully tested on a test beam campaign before, this was done in the context of this theses.

The general functionality was tested and data has been taken at two PSI testbeam campaigns. This data is used to check the tracking capability of the devise and refine the reconstruction mechanism. Furthermore the data can be used to extract an efficiency for the MuPix6 prototypes used as telescope layers, by using one layer as Device Under Test (DUT) and the remaining layers for tracking. In the same manner also the new thinned MuPix4 prototype has been investigated in DUT position.

With testbeams many scans of properties as HV or threshold have been carried out in parallel for single setup and DUT layer. However, the complete analysis of both setups is too much for the scope of this thesis and therefore the telescope data analysis is topic of a new bachelor thesis [48]. Also the further development of the telescope is now promoted in a bachelor thesis [49] aiming to accelerate the system, which was limited by readout speed.

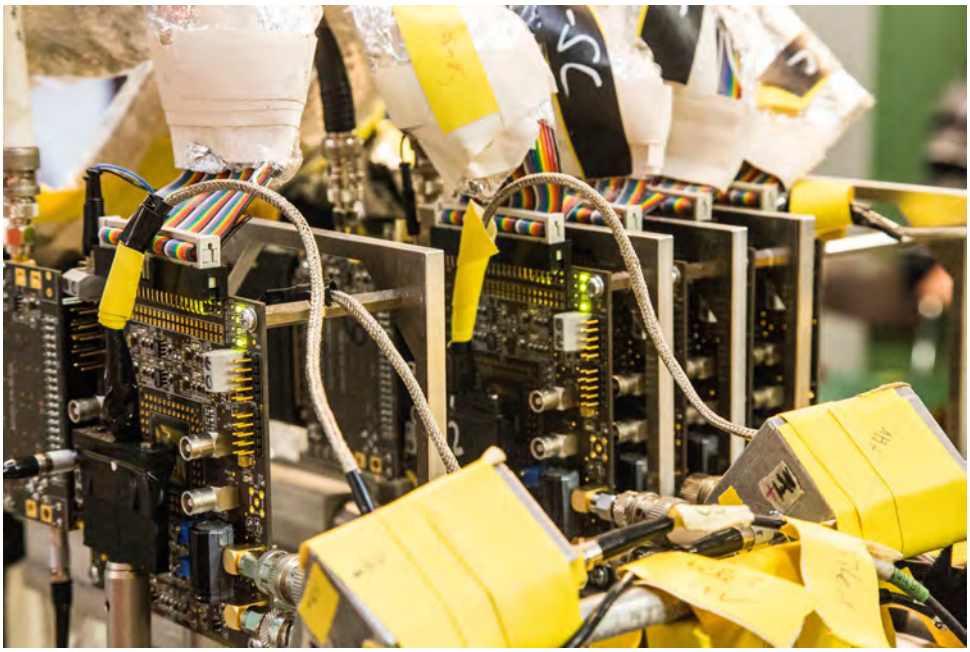


Figure 8.1: The testbeam setup: 1+4 layers, the single setup + 4 telescope tracking planes.

Part III

Measurements

9 Measurements Methods & Setups

In the following the setups and the methods to deduce pixel and chip properties from the prototypes are presented. The measured properties, as well as the signal generation with various sources are discussed and setup constellations described.

9.1 Measured Variables

In the setup we use tree different measurement techniques to characterize the chip.

9.1.1 The Hitbus

The hitbus signal is the comparator ouput signal of a selected pixel. It can be monitored either with the oscilloscope directly or it is transmitted via LVDS and sampled by the FPGA. It needs to be mentioned that the FPGA sampling measures always longer ToT times (fig.9.1). The prolongation is probably caused by the conversion from single ended to LVDS and vice versa and is therefore the same for all sampled pulses. This has to be taken into account for signal interpretation.

With the help of the hitbus signal it is possible to check the analog performance of the pixels in detail. It allows to reconstruct the analog pulse (section 9.4) and look in detail into noise effects near the comparator's baseline.

This measure has the disadvantage, that only one pixel at the time can be observed. Which is wanted for a detailed functional study, but not to do characterize each single pixel individually.

9.1.2 The Digital Hit Information

With the help of the digital readout information, as in general only available for the normal operating mode all pixels can be studied in parallel, which makes it candidate for a chip wide characterization and tuning methods. However, through the digitization the data only holds the information whether and when a pixel was triggered.

9.1.3 The Power Concumption

The power supplies [42],[43] providing the board's and the chip's supply voltages allow a measurement of the drawn current and through this their power consumption. To precisely measure the power consumption a board was modified, allowing to feed each supply voltage level individually.

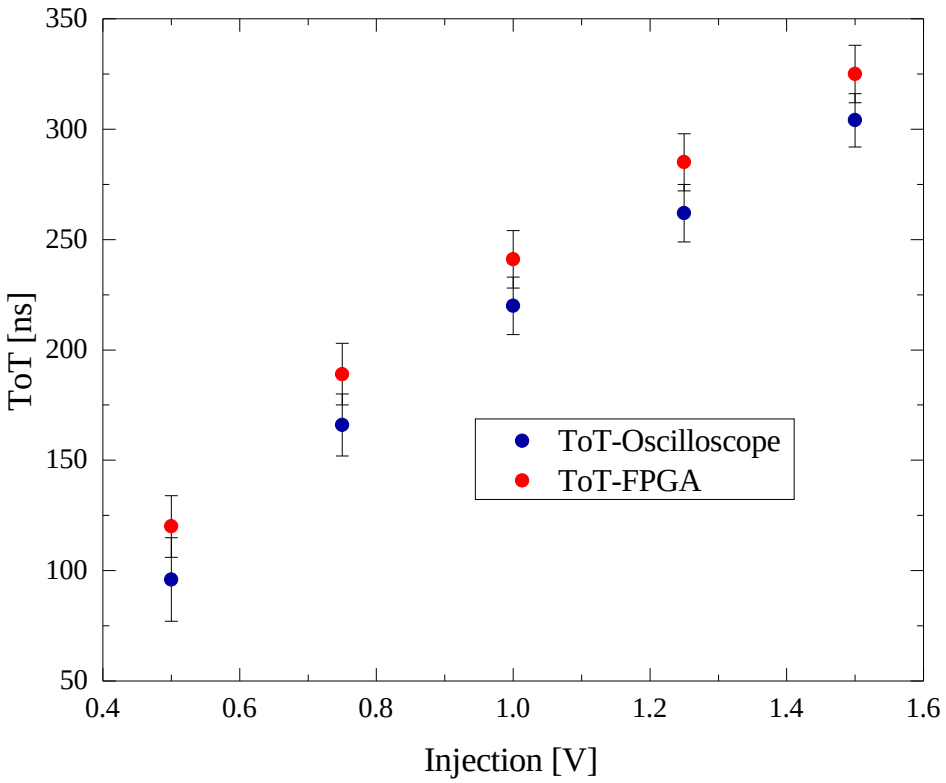


Figure 9.1: FPGA Oscilloscope Response Comparison to the same input signal.

9.2 Signal Sources

9.2.1 Injection

The injection signal is a function provided by the MuPix prototypes. It allows to apply a voltage pulse to a capacity build from a metal layer and n-well of the central pixel diode. If a positive voltage is applied electrons will be collected on the n-well side. When the voltage is released the electrons are collected by the electrode. This can be used to produce constant artificial signals and allows a detailed study of the analog pixel properties.

9.2.2 850 nm Infrared Laser

The infrared laser provides a 25 mW beam of $\sim 1.46\ eV$ photons. The absorption of light in matter is described by the Lambert-Beer-Law, which allows to calculate the intensity drop of a photon beam crossing a material with the absorption coefficient μ and the thickness x

$$I(x) = I_0 \cdot \exp^{-\mu x} \tag{9.1}$$

As the absorption coefficient for 1.46 eV photons in silicon (table 5.10 is only $\frac{1}{50} = \mu^{-1}$ the laser allows to penetrate the full depth of the depletion zone with a high intensity and is therefore most sensitive to changes in the depletion zone width.

The laser is pulsed with a function generator, producing a very steady signal which can also be used for detailed characterization.

9.2.3 5.9 keV Photons from Iron-55

Iron-55 (Fe-55) decays to Mn-55 via electron capture. The absorbed electron will be replaced by an electron of a higher shell leading to the emission of a *gamma* or an auger electron. For the lab test only the monochromatic 5.9 keV K_α line is important, as the auger electron can not leave the sources container and the K_β γs with 6.49 keV energy are suppressed compared to the K_α photons. The soft X-ray photons most likely transfer their energy to an electron via the photoelectric effect creating a 5.9 keV electron, which will create electron-hole pairs along its path. With this energy it will create in average 1650 electron-hole pairs. The fluctuation of this number is described by the Fano-factor $\sigma = 0.011 \equiv 17\ e-h\ pairs$[23].

The path length of the 5.9 keV electron is very short ($<1\mu m$) [20], thus the produced charge cloud is contained by the depletion zone which provides a rather exact value for the electron-hole pairs involved in the creation of the response signal.

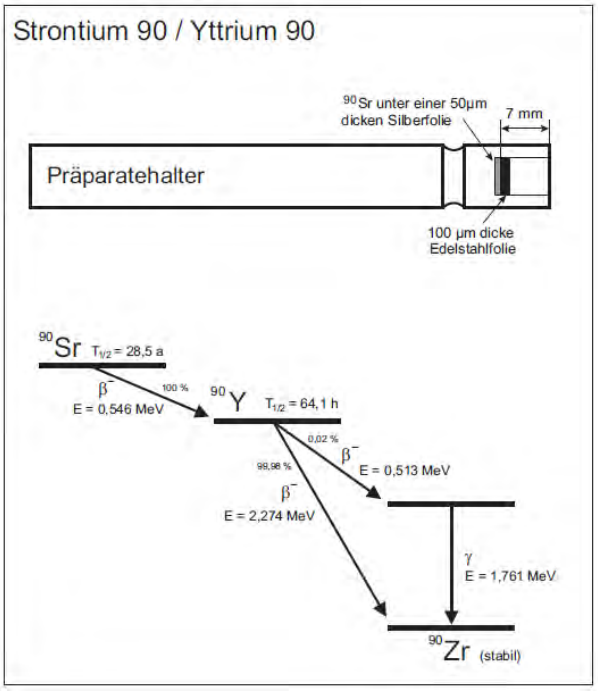


Figure 9.2: Source structure and decay channels [50].

9.2.4 MeV Electrons from Strontium-90

The Strontium-90 (Sr-90) source provides a decay chain producing decay electrons with a maximum energy of 546 keV and 2.28 MeV. However, the Sr-90 is sealed with a metal layer which will absorb low energetic electron, so the low energetic decay will most probably not contribute to the electrons leaving the container. The mean energy loss of the electrons traversing silicon can be extracted from the Berger-Seltzer plot in figure 9.3 and ranges from 5 to 3.5 MeV/cm. As the electrons can penetrate through the sensor, the Sr-90 source can be used for coincidence measurements.

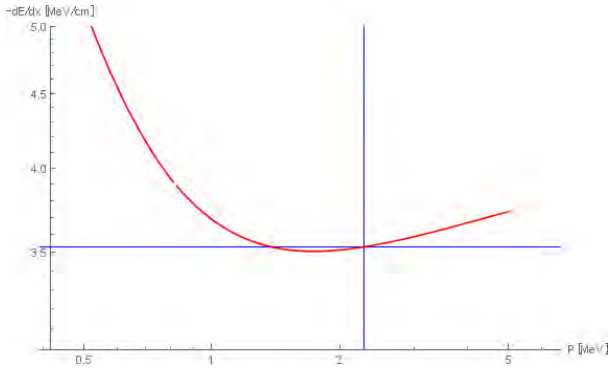


Figure 9.3: Berger Seltzer: Mean energy loss of an electron with the maximal energy from a Sr-90 decay.

9.3 Setups

9.3.1 Lab Setup

The basic lab setup only consists of the chip on the PCB, which is steered and readout by the FPGA. The data obtained in this way is used by the GUI to monitor important information and perform measurements, e.g. parameter scans.

The setup can be extended by a scintillating tile, which is placed on the back side of the PCB behind the chip. It allows to perform coincidence measurements with the Sr-90 source (section 7.3).

9.3.2 X-Ray Source Setup

The X-ray setup makes use of an X-ray tube from a practical course setup. Either a tungsten or a molybdenum anode can be used, which produce a continues bremsspectrum up to the maximum electron energy ($\sim 35keV$ for this setup). This spectrum is overlain by a discrete spectrum caused by the ionisation of the material. In case an electron of an inner shell is kicked out, it is replaced by an electron from a higher shell, nascent binding energy is then emitted in form of a x-ray photon. Therefore the discrete spectrum is called characteristic spectrum.

Further this setup provides a goniometer which allows to extract discrete photon energies via the oscillation method using bragg reflection [50]. This will allow to access smaller X-ray energies than produced by the Fe-55 and so an investigation of the 4 keV energy deposition which is expected for the signal electrons in the Mu3e experiment. However, this setup is only tested, but not extensively used in the scope of this thesis.

9.4 Important Measurements

9.4.1 Pulse Shape Measurement

The pulse shape can be indirectly extracted from the hitbus signal by measuring latency and Time-over-Threshold for various thresholds relative to a pulsed and steady input signal, e.g. a laser pulse from the function generator. By lowering[1] the threshold from the baseline till no hitbus signal can be detected any more the complete pulse shape can be reconstructed (figure 9.4 & 9.5).

As the pixel is not ideal, noise is influencing the signal shape leading to a jitter of the signal edges. Both the oscilloscope and the GUI have the possibility to obtain standard deviations for the measured values. Further the noise also leads to a smearing of the signal height, which renders the measurement of the signals maximum impossible.

For many applications it is not necessary to measure the complete pulse shape, but only use their main characteristics as latency and ToT at a fixed threshold and the pulse height which can be deduced as explained in the following section.

[1] the MuPix6 has negative pulses, all former prototypes produced positive pulses

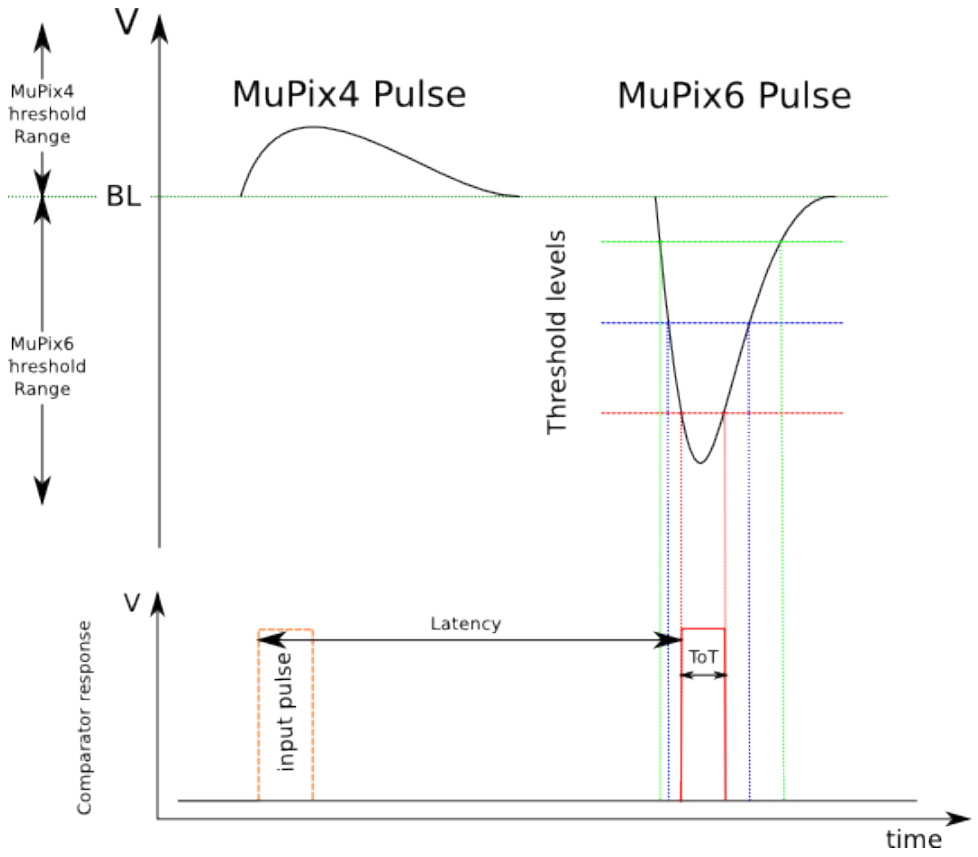


Figure 9.4: Comparison MuPix4 and MuPix6 pulse and pulseshape measurement procedure.

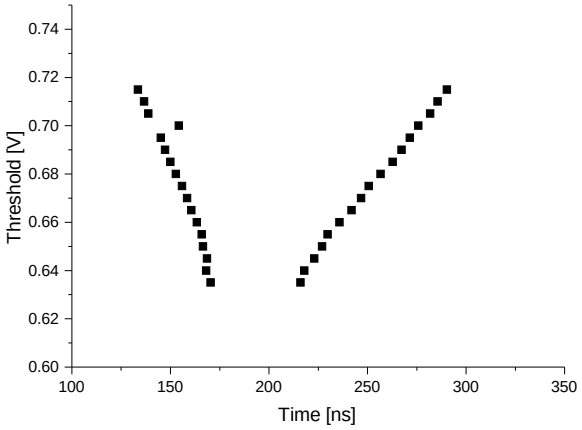


Figure 9.5: Pulse shape measured for the new MuPix6 pixels.

9.4.2 Threshold Scan

There are two possibilities to perform a threshold scan. Either the hitbus signal can be used to count the number of comparator pulses for a given threshold and a fixed time window or the digital hit information can be used to count pixel hits, which allows to perform the scan for all pixels at once.

The pulse counting can be combined e.g. with an injection signal which allows to compare the number of generated and counted pulses. This allows to measure a relative response for each threshold. The error on each measurement point is given by the statistical error $\sqrt{counts}$.

In case of an ideal pixel, there is no noise and the pixels response to a constant input signal is invariant. A threshold scan for such a pixel would give a step function, with the step occurring at the signals pulse height. For a real pixel however, noise plays a role and leads to pulse variations for a constant input signal, which smears the edge of the step function. This smeared out step-function can be described by an error function and allows to deduce the signal height and the noise from a fit to the data, using the following fit function parametrization (equation 9.2), describing the cumulative distribution of a normal distribution.

$$f(x) = \frac{1}{2}(1 + erf(\frac{x-\mu}{\sigma\sqrt{2}})) \tag{9.2}$$

With μ the expected value which can be interpreted as signal height, and σ, the standard deviation of the normal distribution, which is a measure for the noise.

The same can be done for the digital data, although here the complete integration window is subdivided in smaller windows, the frames. This can be interpreted as a Bernoulli experiment for each frame, either the pixel was triggered or not, leading to a binomial description of the measurement. For each measurement at a threshold n frames are observed leading to k observed pixel triggers. For a large number of observed frames the number of observed triggers should be approximate the expectation value ($k \approx \mu$), which is given as $\mu = np$ for a binomial distribution. This allows to calculate the trigger probability for the measurement $p = k/n$. The standard deviation, is calculated as $\sigma = \sqrt{np(1-p)} = k(1-k/n)$. The threshold voltage is known with a precision of 0.001 V, although there is a small constant offset between the value set in the GUI and the value measured on the board. The board DACs for injection and threshold allow a more precise adjustment (14-bit on 1.8 V $\sim 0.0001V$) precision, however, the board is not perfect, e.g. fast signals, as the timestamps, can couple into the threshold line.

The fit to the data allows to extract the signal height and the noise which enables the calculation of the signal-to-noise ratio (SNR) for a pixel(figure 10.14).

$$SNR = \frac{|\mu - b|}{\sigma} \tag{9.3}$$

μ is the signal height, b the baseline voltage and σ the noise.

Further more this measurement is used to investigate the noise, also for the noise a error function fit can be performed. Here μ describe the 50% noise level, that is the threshold for which in 50% percent of the frames the pixel was triggered by noise.

10 Lab Characterization

In the following sections first results from the lab characterization of the MuPix6 are presented, using the methods introduced before. If not mentioned explicitly in the respective section the standard measurement conditions use -60 Volts high voltage and the DAC values stated in the table below. The baseline voltage is adjusted to 0.8 V.

DAC settings	
DAC	Value
VN	60
VNLoad	5
VNFB	10
VNFoll	16
VN2	60
VNLoad2	5
VNFB2	10
VPComp	60
BlRes	10
VNDel	10
VPDAC	0

Table 10.1: The standard DAC settings.

10.1 Influence of HV

The high voltage applied to the diode is the key ingredient for the HV-MAPS technology. The HV-dependence of pulse shape parameters and the noise levels have been measured and checked for their consistency with our pixel knowledge by fitting functions with the respective behavior. However, the fits are purely qualitative to visualize the expected dependence and neglect the exponential description of the pulse (sec. 7.2.4).

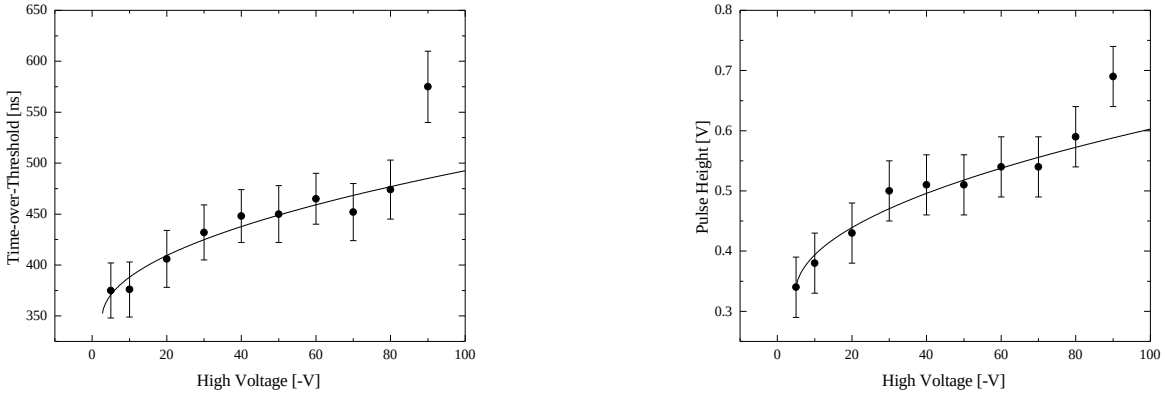
10.1.1 Pulse Shape Parameters

The pulse shape dependence has been extracted with the help of a pulsed laser beam. Both the pulse of the laser diode and the hitbus signal are monitored on the oscilloscope and errors on the values are extracted from the oscilloscopes statistic function by summing over several hundred signal pulses.

As presented in section 5.3 the high voltage influences the diodes properties, most important the depletion zones width and the active detector volume. The laser pulse, which can penetrate $\mathcal{O}(100\mu m)$ into the silicon, allows to probe the depth of the active

area. As the depletion zone grows $\propto \sqrt{U}$, also the amount of produced charge carriers increases with the depth and so the ToT and the pulse height. A qualitative fit was applied to visualize this behavior, ignoring the $\exp^{-\mu x}$ dependence of the absorption which would lead to a decreasing effect for large voltages.

This fit describes the general behavior quite well up to 80 V reverse bias, at 90 V however, a new component comes into play. Due to the high electric field in the depletion zone electron avalanche processes are possible and lead to an enhancement of the signal, before the diode breaks down at $\sim 93V$ reverse bias.



(a) Time-over-Threshold dependence.

(b) Pulse height dependence.

Figure 10.1: The pixel high voltage dependence measured with a pulsed laser diode.

A similar effect is observed for the latency which improves asymptotically for large voltages and even further for 90 V on behalf of the signal enhancement (fig.10.2).

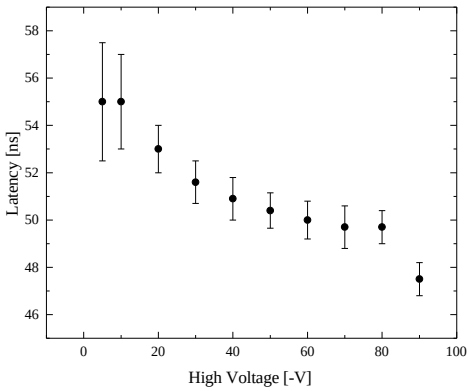


Figure 10.2: The HV dependence of the latency.

These observations are in agreement with the findings for the previous prototypes [30],[31],[37] and the theoretical pn-juntion behavior.

10.1.2 Noise

Further the dependence of the noise level on the HV was determined with the help of threshold scans close to the baseline voltage, determining the threshold for which 50% of the frames have been triggered via an error function fit the 50% noise level is given by μ and the error by the standard deviation. The result is plotted in figure 10.3 and shows a decrease of the noise level for increasing high voltage, so the high voltage does not only improve the signal strength, but reduces the noise at the same time.

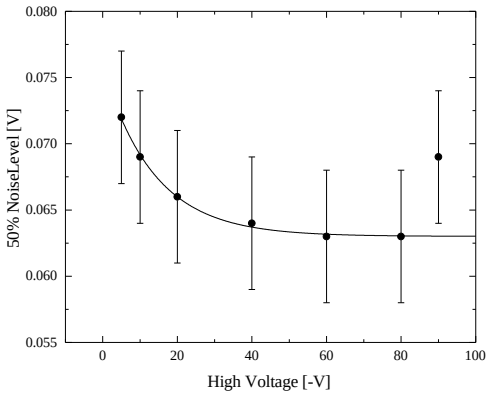


Figure 10.3: High voltage dependence of the 50% noise level obtained from threshold scans.

10.2 Influence of the DACs measured with pulse shape parameters

The influence of the DAC bias currents on the pixels performance has been tested. For this purpose all DACs have been set to their respective standard value and are varied one by one, in their dynamic range. As measures for the pixel performance the latency, ToT, pulse height and the noise are observed.

With the help of this measurement the effect of each bias current can be determined and important value ranges for each DAC can be extracted. This knowledge will help to perform an optimization of the DAC settings later on.

In the following only the results for the bias currents of second amplification stage (VN2, VNLoad2, VNFB2) are depicted, as the a similar measurement was already presented in [38]. The results and effects obtained for the remaining DACs are described.

VN2 steers the current flowing through the second amplification stage (section 7.2)

As shown in figure 10.4 the pixels performance is stable for a huge range of DAC values down to 10. At a DAC value of 3 the latency increased by 40 ns and the pulse height dropped by 100 mV compared to its nominal performance at 60. The second stage is switched of for small VN2 values.

The bias current VNLoad2 controls the gate voltage of a transistor on the amplifiers output which acts as a resistor. The higher the bias current the lower the resistance.

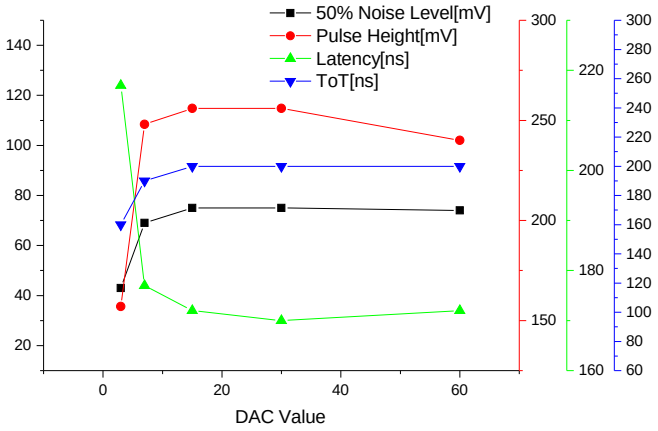


Figure 10.4: The influence of the VN2 DAC setting on the pulse shape parameters.

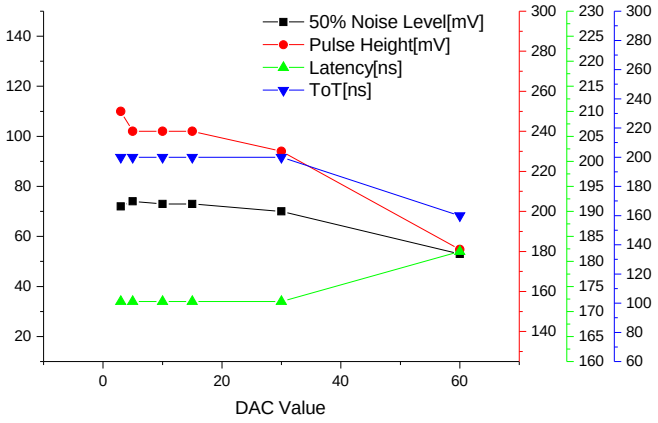


Figure 10.5: The influence of VNLoad2 DAC setting on the pulse shape parameters.

The results show an improvement of the pulse height for small bias currents, so for a higher resistance of the load transistor the gain of the amplifier improves slightly. But not only the signal is amplified, also the noise level is enhanced.

VNFB2 controls the feedback circuit between in- and output of the second amplifier (fig. 10.6).

An impact of the second stage feedback is almost not measurable, perhaps a small improvement, with a slightly larger pulse and ToT, is seen for small DAC values. However, it seems the signal shaping in the standard settings is almost not influenced by the VNFB2 bias current. Also a general malfunction can not be excluded here.

In the following the results for the remaining DACs are briefly summed up, the plots can be found in the appendix:

VN steers the current through the first amplifier. For a DAC value of 15 the signal height and the noise level increase both likewise relative to the standard setting with VN=60. For lower values the amplifier switches off.

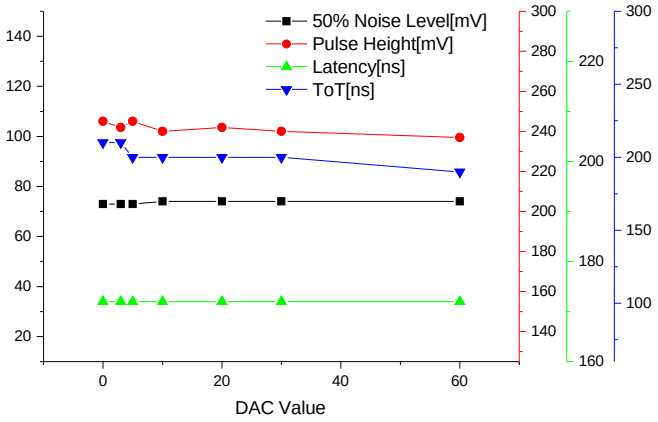


Figure 10.6: The influence of VNFB2 DAC setting on the pulse shape parameters.

VNLoad shows the same effect as VNLoad2. The signal quality improves for large load resistance ≡ small bias currents. For DAC values below 5 the latency increases, rendering the range from 5-10 as optimal.

In contrast to VNFB2, the feedback of the first amplifier, controlled by VNFB, shows a huge impact on the pulse shape. The higher the bias current, the stronger the feedback, resulting in small pulses. For an improvement of the SNR, the value should be chosen small, on the cost of a larger ToT.

VNFoll controls a voltage divider build from two transistors, the so-called Source Follower (SF). VNFoll sets the working point of the follower. The optimal value range for the standard settings is 20-30. For smaller values pulse height and ToT are reduced, showing a high-pass behavior of the circuit. Below values of 5 the follower is not working properly anymore, it is being switched off.

The comparators performance can be steered only by one DAC, controlling the current through the comparator. The more current is flowing (DAC >30), the faster the comparator can react to changes on the inputs, due to the fact that the comparators capacity can be charged quicker. For lower DAC values (<30) this effect is recognizable, as the latency increases and the pulses crow longer due to the slow switching. However, the noise level improves slightly for smaller values.

The last bias current, BLRes (Baseline Restoration) steers a transistor with resistor function, which is used as a feedback of the comparator capacity to the baseline voltage. This CR combination works as a high-pass filter and its time constant can be controlled via the resistance set by BLRes. The higher the DAC value, the lower the resistance, the smaller the time constant, the smaller the pulse height and ToT. Also a minimal increase of the noise level is visible, which might origin from noise coupling from the supply baseline to the comparator.

10.3 Power Consumption

To measure the power consumption of the chip a test board was modified to allow supply each voltage level individually and measure the respective currents. The test board requires 4 voltage levels which are by default provided by voltage converters on the PCB and only require 5 V supply voltage.

The board itself requires 5 V and 3.3 V for the operation of the on-board DACs, providing threshold and injection voltages. The chip requires 1.8 and 1.5 V and is the only user, beside two voltage dividers providing external bias voltages for the chip with a constant consumption of 0.2 mA ($\equiv 0.36mW$) each.

The power consumption of the chip is calculated as::

$$P_{Chip} = 1.5V \times I_{1.5V} + 1.8V \times I_{1.8V} - P_{external} \tag{10.1}$$

To get an idea of the power consumption contribution of the individual DACs, a measurement is performed starting with all DACs set to zero and a threshold value of 0.0 V. This measurement give a standby power consumption caused by leakage and the current the DACs themselves draw when the chip is powered.

Then each DAC is set individually to 60 and the current change is measured. The results are illustrated in table 10.2. This simple measurement clearly shows, as expected,

		Supply Voltage	
DAC	Value	1.5 V	1.8 V
		Current [mA]	
all zero		1.69	8.79
VN	60	+27.85	-0.12
VNLoad	60	+0	+11.8
VNFB	60	+0	+0
VNFoll	60	+0	14.37
VN2	60	+0	+19.3
VNLoad2	60	+0	+ 0.02
VNVNFB2	60	+0	+0
VPComp	60	+0	+12.03
BlRes	60	+0	+0
VNDel	60	+0	+0.02
VPDAC	60	+0	+19.23

Table 10.2: Current changes due to single bias currents.

that the currents through the amplifiers pose the largest contribution (VN,VN2), followed by the source follower and the comparator current (VNFoll, VPCOMP). Further this measurement shows the huge power consumption which is possible for large values of VPDAC, which is used to control the scale of the tune DAC influence.

In the following the 3 stages are treated individually by switching groups of bias DACs on and off. ON meaning their respective standard DAC value, OFF zero.

- The comparator: VNDel, VPComp, BlRes
- The second stage: VN2, VNLoad2, VNFB2
- The first stage: VN, VNLoad, VNFB, VNFoll.

	Supply Voltage Currents [mA]	
Stage	1.5 V	1.8 V
all zero	1.69	8.79
Comparator	+0	+12.4
Second Stage	+0	+18
First Stage	+24.25	+6.35
Comparator + Second Stage	+0	+30.11
All Stages	+24.17	+37.19
VN, VN2 and VPComp = 30	+12.49	+21.41
VN, VN2 and VPComp = 15	+5.74	+12.56

Table 10.3: The current drawn by the individual stages and for the interconnections.

In table 10.3 the results for the individual power consumption of the stages and for the interconnection are given, further the power consumption is measured for alternative settings with modified VN, VN2, and VPComp values. They show that each stage is almost independent of the other stages, so the currents for the chip can be handled additive stage by stage.

A change of the threshold voltage only shows an effect close to the baseline voltage, as the noise will cause many switches of the comparator and the inverters in the digital part which results in a large cross current. For normal threshold settings (0.6 V to 0.7 V) the power consumption is reduced as it shifts the working point of the comparator.

The overall power consumption for the chip in standard settings can hereby be calculated to 121.6 mW. It can be reduced drastically by using lower stage voltages VN, VN2, VPCOMP= 30 $\rightarrow$ 75.3mW and VN, VN2, VPCOMP= 15 $\rightarrow$ 49.5mW. However these adaptions do to not take into account the chips performance. A closer look into DAC optimization also with respect to power consumption is taken in section 10.7.

The figure of merit for the power consumption of the tracker is 150 mW/cm^2, to calculate this for the MuPix6 the active area of the chip has been measured. For larger chips the power consumption will scale to this area as it contains all power consuming parts of the chip: The pixel matrix, the digital part, and the main power lines. It can be measured with the help of Cadence® which gives a total active chip area of 13mm^2. This results in a maximal power consumption of 935mW/cm^2 for the standard settings.

Fast switching signals cause additional currents. This can also be an issue for the timestamp input circuits, as the fastest possible timestamp bit can switch with 100 MHz. The influence of the timestamps is plotted in figure 10.7 with respect to switched off

timestamps (constant timestamp input pattern). For low frequencies even a small current reduction is observed and a steep rise of the drawn current for very high frequencies. However, for the fastest bit switching with 25 MHz; a gray-encoded 10 ns time binning; the timestamp circuits consume almost no additional power (0.63 mW).

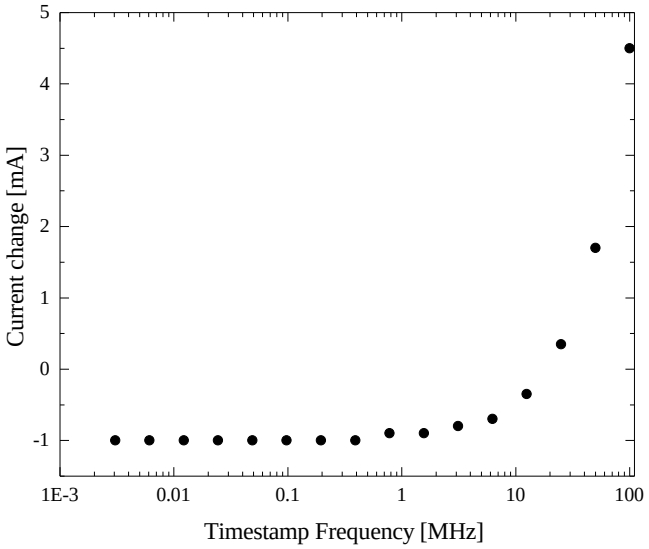


Figure 10.7: The additional chip current depending on the fastest timestamp bit frequency.

No high voltage dependence is observed for the power consumption of the low voltages.

10.4 Noise Measurement

The pixel can be divided in four substructures, the comparator, the second amplifier, the source follower, and the first amplification stage. This allows to determine the pixels noise behavior by switching them on one after the other, starting with comparator then adding the second amplifier and so on. To determine the noise behavior a threshold scan with the hitbus is performed, counting noise pulses. The result is plotted in figure 10.8.

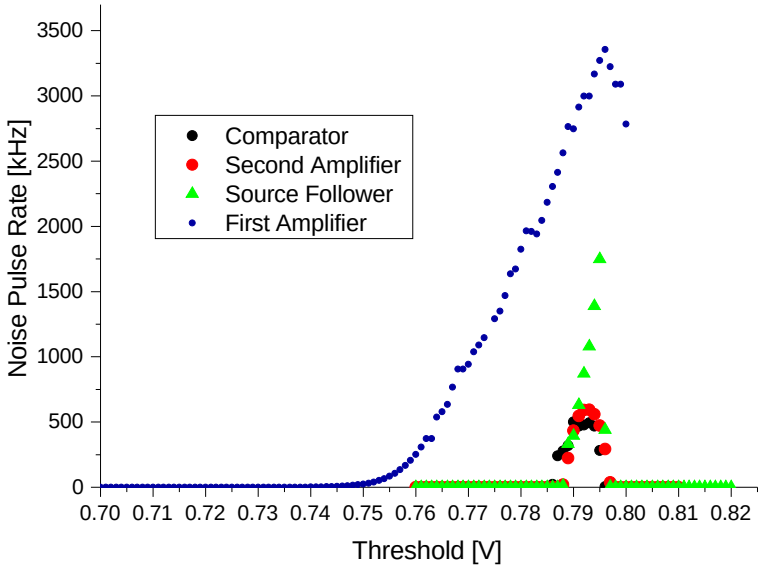


Figure 10.8: Noise contribution depending on different top instances of the signal chain.

It clearly shows no big noise contribution from the comparator and second amplifier in terms of a large offset to the baseline. For the comparator only, this measurement is basically only a direct comparison of the baseline (BL) and threshold (THR) plus noise contributions from the comparator circuit. However, the maximal noise count seemed to be limited so a more detailed analysis of this has been done with the help of the oscilloscope observing the hitbus (fig. 10.9)

A clear oscillation is visible with a maximal amplitude below 5 mV. The oscillation frequency shows a clear dependence of the BlRes DAC, so most likely the comparator capacity is involved. No further studies have been done so far investigating this process, whether it depends on VPComp or can be influenced by the tune DACs.

Returning to figure 10.8 an enhancement of the noise count rate is measured when switching on the source follower, however this is due to an unintentional change of BlRes in this measurement (60 instead of 10), showing the frequency dependence of the oscillation. As the distribution is not growing broader their is almost no additional noise due to the source follower.

The biggest influence on the noise is clearly caused by the first stage, which is connected to the pixel. This noise component is dominant and results in a larger noise offset from the baseline at 0.8 V, expanding from 5 mV noise, caused by the oscillation, to

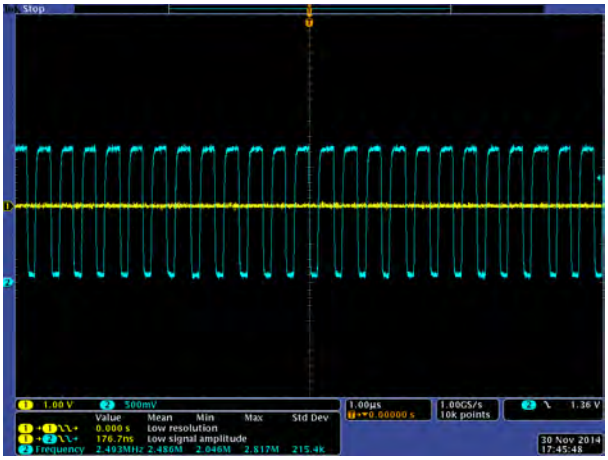


Figure 10.9: Comparator oscillation monitored with the oscilloscope at threshold 0.79V.

$\sim$ 50 mV = 0.8 − 0.75 as read from the diagram (starting threshold of the noise). Further the pulse rate is no longer limited to a maximal number given by the oscillation, as the noise creates pulses at random. For thresholds close to the baseline at 0.8 V the noise pulse rate reduces again, due to saturation. The rising ToT of the noise pulses can not be distinct anymore.

A further study has been done determining the effect of high frequency signals, namely the timestamps on the noise level, measured with the threshold scan method. The result is presented in figure 10.10 and shows no significant noise influence.

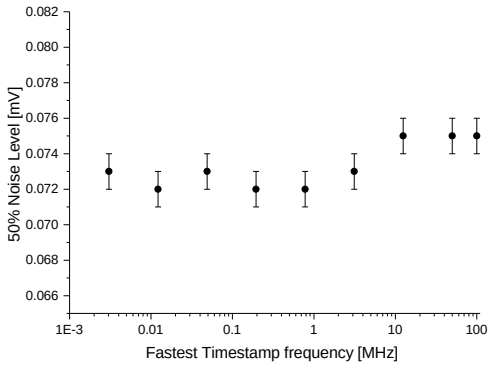


Figure 10.10: The 50% noise level offset to the baseline for different timestamp frequencies. In case the timestamps are switched off the level is at 0.0727 V.

10.5 Measurement with injection Signal

As described, the injection signal is generated by a n-well capacitance which is charged. The number of charges created on the n-well side is described by $Q = C \cdot U$ with C the injection capacity.

The injection signal was investigated for the standard settings, monitoring the ToT and the pulse height for different injection voltages. The results are presented in figure 10.12 and 10.5 show a non linear dependence of the ToT and the pulse height.

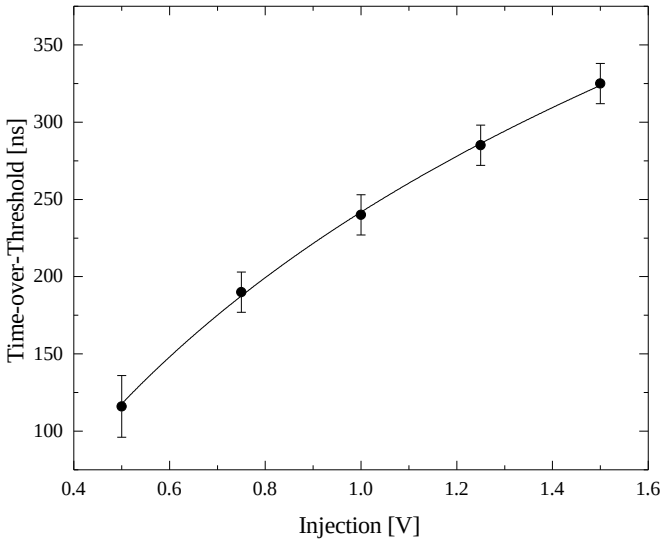


Figure 10.11: Hitbus ToT for different injection voltages.

This non-linearity can be explained by the pulse shape description (section 5.1). Although the pulse shape is described by a high-pass and low-pass component, the ToT is clearly dominated by the high-pass term for the approximation $\tau 2 \gg \tau 1$ rendering the output voltage description $\propto \exp^{-t/\tau}$ which gives a logarithmic behavior to the measured time $t \propto \log(U_0)$. The ToT depends logarithmic on the input voltage. This description in agreement with measurement, as the qualitative general log-fit indicates.

For the pulse height this behavior can not be described that easy, as high- and low-pass contributions come into play. However, also here a non-linear logarithmic-like behavior is observed, due to the domination of the high-pass behavior.

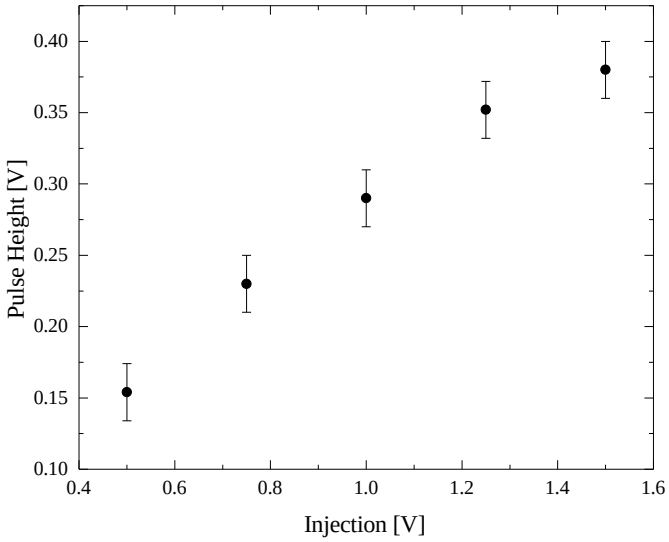
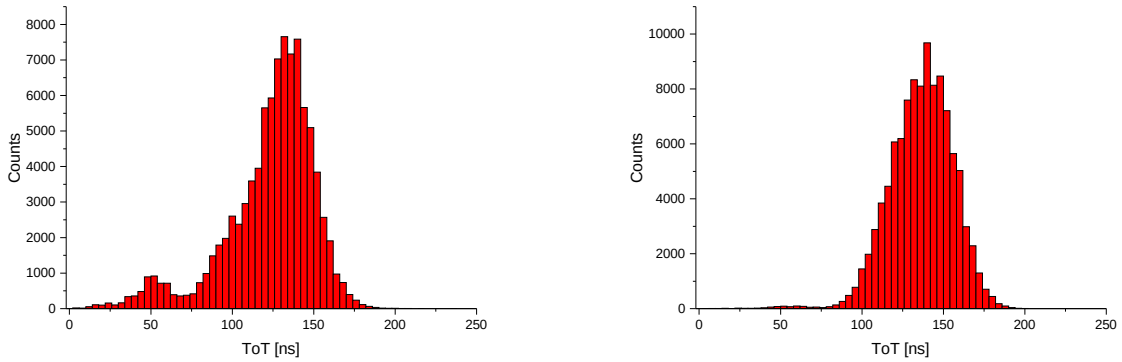


Figure 10.12: Measured pulse height (error function) for different injection voltages.

10.6 SNR of Fe55 signal

To extract a gauged SNR value for the new pixel architecture the Fe-55 source is used as reference for the signal height. The SNR measurement then is carried out with the help of an injection pulse tuned to the Fe-55 peak (fig. 10.13).



(a) Reference Fe-55 ToT spectrum

(b) The tuned injection peak with 0.55 V

Figure 10.13: Injection calibration to the Fe-55 peak.

The SNR can than be extracted from a threshold scan for the calibrated injection signal. For the data fit including the statistical errors one can only fit the step part of the function as the plateau conditions are anyhow guaranteed by the fit function. If the plateau regions are included to the fitted data range they dominate the χ^2 fit,

leading to an underestimation of the noise. The fit parameters yield a signal height of

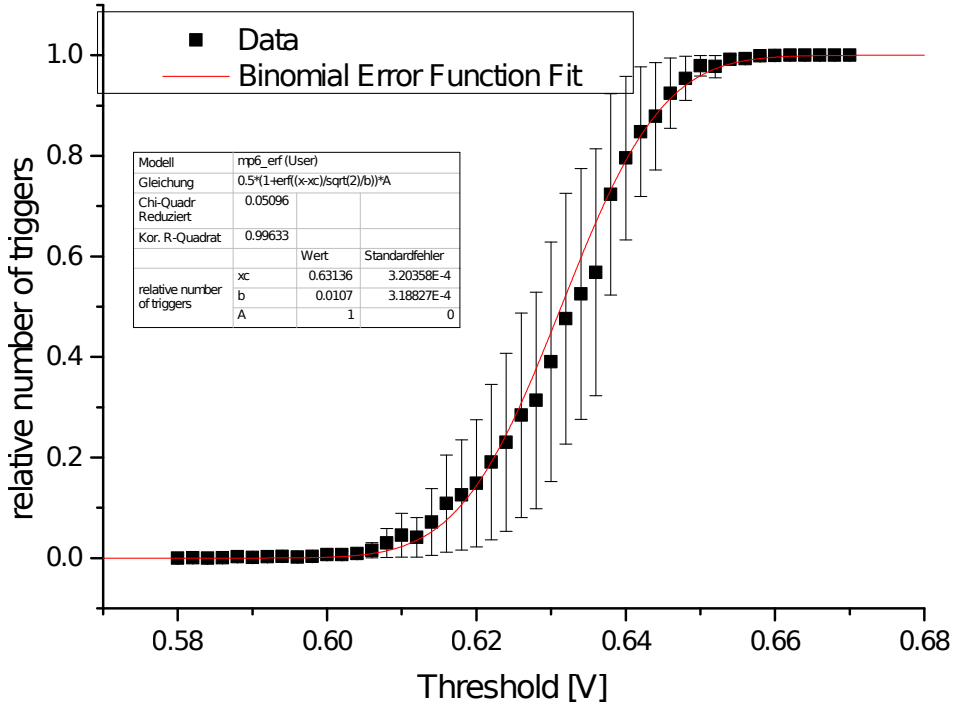


Figure 10.14: The threshold scan for the calibrated injection signal with the error function fit.

$\mu = 0.6313 \pm 0.0003\ V$ and a noise of $\sigma = 0.0107 \pm 0.0003\ V$. The baseline applied to the chip has been measured to 0.800 ± 0.002, which enables the calculation of the signal-to-noise ratio.

$$SNR = \frac{0.8 - 0.6313}{0.0107} = 15.8 \pm 2.6 \tag{10.2}$$

The error has been calculated via error propagation.

The same measurement can also done via the hitbus signal by measuring the fraction of recognized injection signals (fig.10.15). The error function fit to this data with statistical errors yields a smaller signal height $0.6580 \pm 0.0002\ V$ and larger noise $0.0156 \pm 0.0003\ V$, giving an SNR of 9.1 ± 1.2. This discrepancy is most likely originating by the fact that the hitbus signal has to be transported from the chip to the FPGA, which gives rise to further efficiency factors for the transport and the detection of the pulse e.g. by the LVDS transmitter.

As the first measurement was obtained under normal running conditions and does need any additional signal transport which can jeopardize the signal quality, this result is more trust worthy.

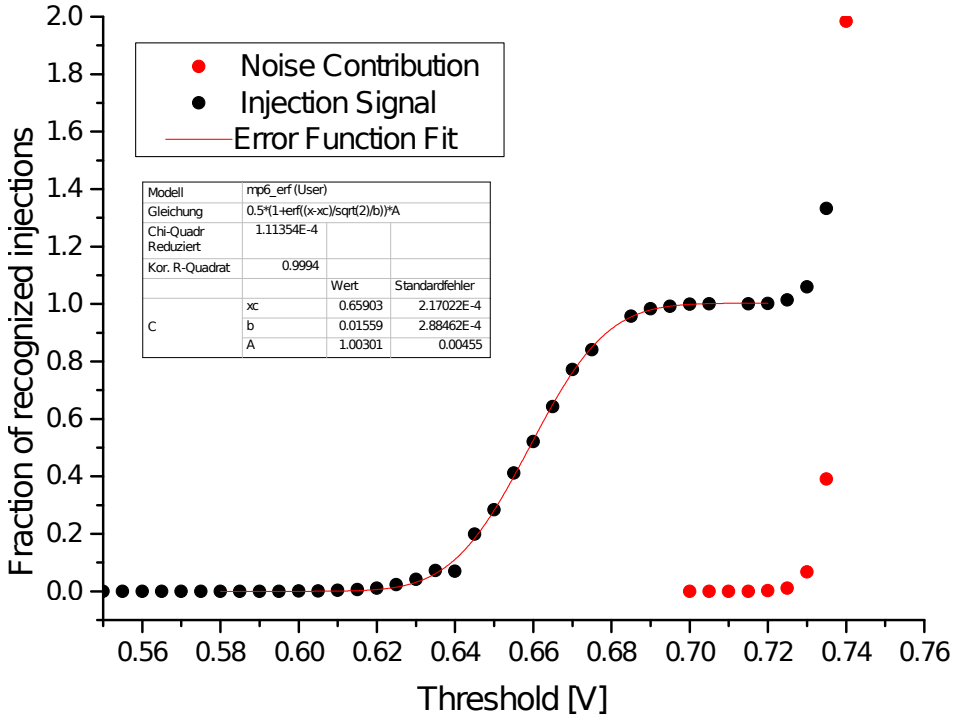


Figure 10.15: Measurement of the fraction of recognized injection pulses calibrated to Fe-55 and the measurement of the noise (red) scaled to the pulse measurement.

However, figure 10.15 nicely shows a plateau region for the efficient detection of a Fe-55 like signal with a width of $\sim 40mV$. This is important, as for the Mu3e electrons less energy deposition is expected as for 5.9 keV photon from a Fe-55 source. This plateau corresponds to $\sim 100\%$ efficiency for the Fe-55 equivalent, but it will shrink for smaller energy depositions.

The SNR value further allows to calculate the equivalent noise charge (ENC) via the following relation, as the number of charges (NoC) created by Fe-55 photon is known:

$$SNR = \frac{Signal}{Noise} = \frac{NoC}{ENC} \tag{10.3}$$

The error on the number of charge is given by the fano factor, for silicon $F_{Si} = 0.115$. The fano factor is defined as $F = \sigma^2/\langle NoC \rangle$, describing a statistical variation in production processes for electron-hole pairs. With an average electron-hole pair creation energy of $\omega = 3.66\ eV$, the NoC can be calculated $\langle NoC \rangle = E(\gamma)/\omega = 5898/3.66 = 1611.5\ e(electrons)$ with an statistical fluctuation of $\sigma = \sqrt{\langle NoC \rangle \cdot F} = 13.6\ e$

$$ENC = \frac{NoC}{SNR} = \frac{1611.5 \pm 13.6}{15.8 \pm 2.6} = 102.3 \pm 0.9e \tag{10.4}$$

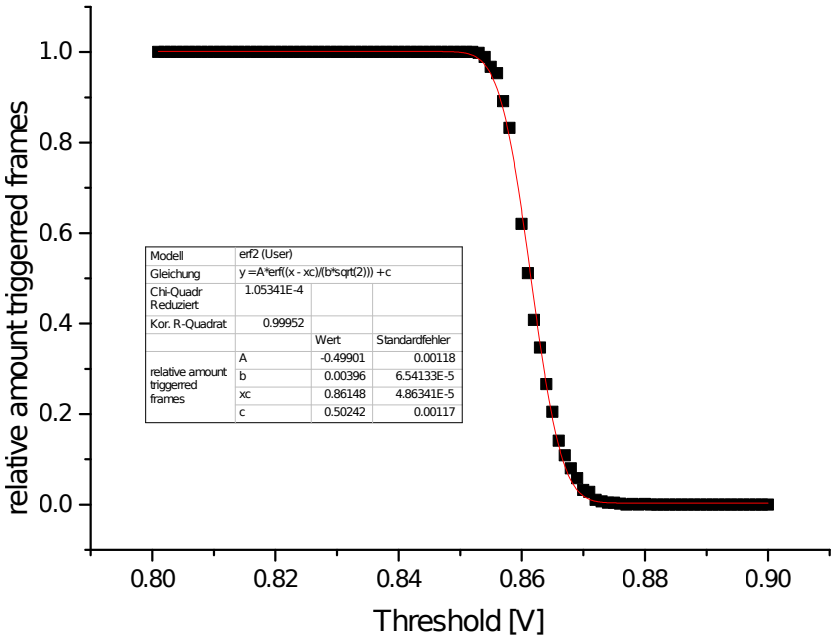


Figure 10.16: The threshold scan for a calibrated injection signal with the error function fit for a MuPix4 pixel.

For comparison the SNR was also measured for a MuPix4 pixel tuned to an Fe-55 signal (fig.10.16).

The fit yields: $\mu = 0.0615$ and $\sigma = 0.004$, giving an equivalent SNR of 15.3 and so also a similar ENC.

For MuPix2 however, a ENC of ~ 40 was measured [39].

So the enhancement of the ENC does not origin in the additional amplification stage, but the enlargement of the pixels.

Furthermore the signal and noise levels can be compared for MuPix4 and MuPix6.(tab. 10.4)

Value	MuPix4	MuPix6	Enhancement Mupix6/MuPix4
Pulseheight	0.0615	0.169	2.7
Noise	0.004	0.01	2.5

Table 10.4: A comparison of MuPix4 & 6 pulse height and noise performance.

Showing almost the intended factor 3 in enhancement. The noise is slightly less enhanced possibly due to the faster pulse shaping. But more detailed study is needed to measure those factors precisely.

10.7 DAC optimisation

As mentioned before the power consumption of the chip is 935 mW which is more than 6 times more than the target value of 150 mW. So it is obvious that has to be optimized. As seen in section 10.3 the power consumption depends strongly on the DAC settings, so a variation of the DACs, a reduction of the currents drawn by the stages is required.

In the following only the general idea and techniques are presented which have been used to optimize the DAC settings with the goal to reduce the power consumption.

The power consumption itself can easily be monitored with the modified setup. Further the pulse shape parameters Latency, ToT and pulse height have to be monitored while changing the DACs as in the end the pixels should stay functioning and preserve a good SNR.

For this optimization however, only in the end the pixel SNR is remeasured and the DACs are varied or not varied by observing the positive or negative effects on the pulse shape for a injection signal calibrated to the Fe-55 source.

The starting point of the optimization are the standard settings. As learned from section 10.3 the main knobs to influence the power consumption are the current steering DAC values (VN,VN2,VPComp), which can be used to half the power consumption. Starting from these low current setting the other DAC values can now be varied one by one similar to section 10.2. However, during the optimization this DAC is not varied back to its starting point, but keeps the value of the best performance. This procedure is iterated for all DACs several times, also trying to reduce the current further and further by reducing VN,VN2 and VPCOMP. But as observed in section 10.2 for very low values the stages start to be turned off.

The following table presents the new power saving settings obtained in this way. The

DAC settings		
DAC value	Full power	Low power
VN	60	5
VNLoad	5	2
VNFB	10	3
VNFoll	16	10
VN2	60	5
VNLoad2	5	2
VNFB2	10	3
VPComp	60	10
BlRes	10	10
VNDel	10	10

Table 10.5: The standard and low power DAC settings.

impact on the pixel performance can be measured for a Fe-55 equivalent injection signal. The change in the pixel performance are listed below. The measurements have been obtained for the same pixel the SNR has been determined in section 10.6.

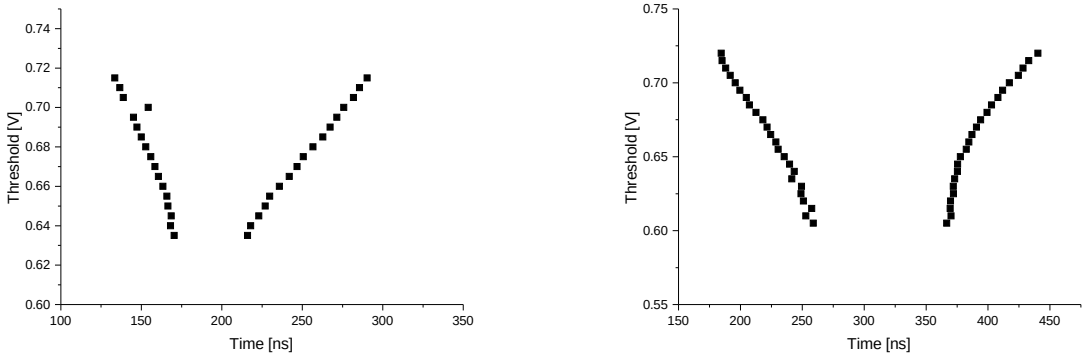
The first thing to be noticed is that the required injection voltage to produce a Fe-55 like signal is reduced, a possible explanation could be a change of the effective input

Pixel measures			
Measure	Unit	Full power	low power
Fe-55 equivalent injection	[V]	0.55	0.47
ToT	[ns]	135	185
Latency	[ns]	177	240
Noise	[V]	0.0107	0.0169
SNR	-	15.8 ± 2.6	10.5 ± 0.7
Power consumption	$[mW/cm^2]$	935	223

Table 10.6: Comparison of important pixel measures for the full- and low-power settings.

capacity of the first amplification stage due to shift in the amplifiers working point. A further indication of this effect is the enlarged noise. Following $Q = C \cdot U$, less charge is required to produce the same signal for a smaller capacity. For the noise a smaller capacity means a larger impact of small charge changes due to noise effects.

Further the SNR was remeasured (fig.10.18) which is reduced to 2/3 of the initial SNR. However, an SNR of 10 is still sufficient as it allows a clear distinction between signal and noise.



(a) High power settings

(b) Low power settings

Figure 10.17: Pulse shapes measured for the Fe-55 like injection signal.

The ToT is increased, which is caused by the reduction of VNFB considering the observation in section 10.2.

A big draw back of the power reduction becomes visible for the latency. The latency values above are the peak positions of the generated injection pulse read from the online monitor, they are not gauged values. The absolute latency of the signal can be measured with the help of the oscilloscope, observing the injection and the hitbus pin on the chip. This yields an absolute latency of the signal pulse of $\sim 57\ ns$ for the full power settings. The shift in latency however, can be determined with monitoring values and is more than doubling the absolute latency to $\sim 120\ ns$. Further, as illustrated with the monitor plots in figure 10.19(a) and 10.19(b), the jitter, the fluctuation of the latency, becomes more prominent and worsens the time resolution of the pixel.

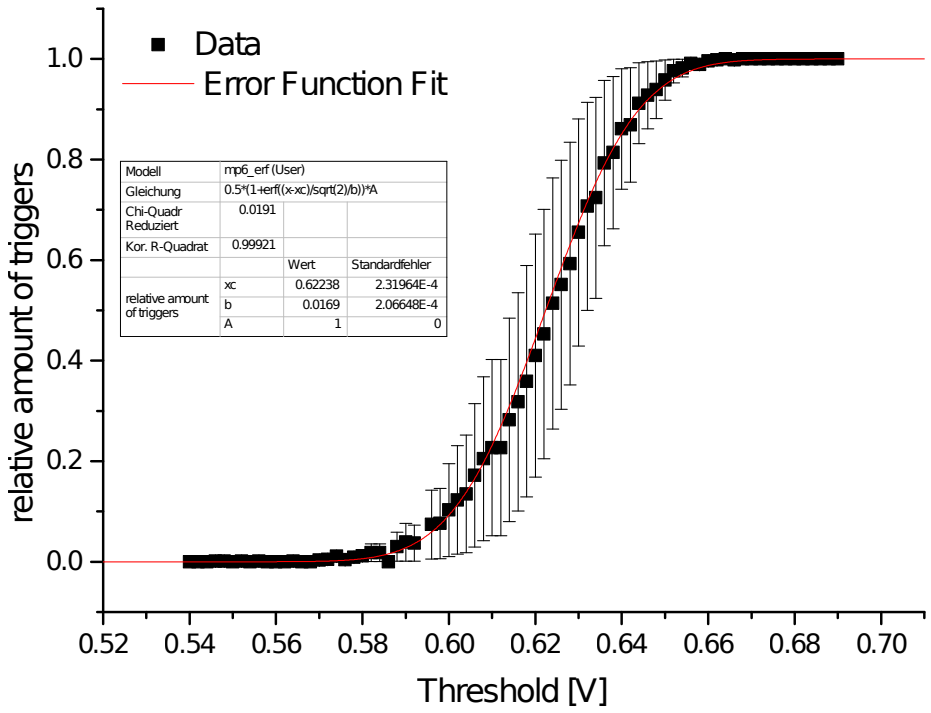
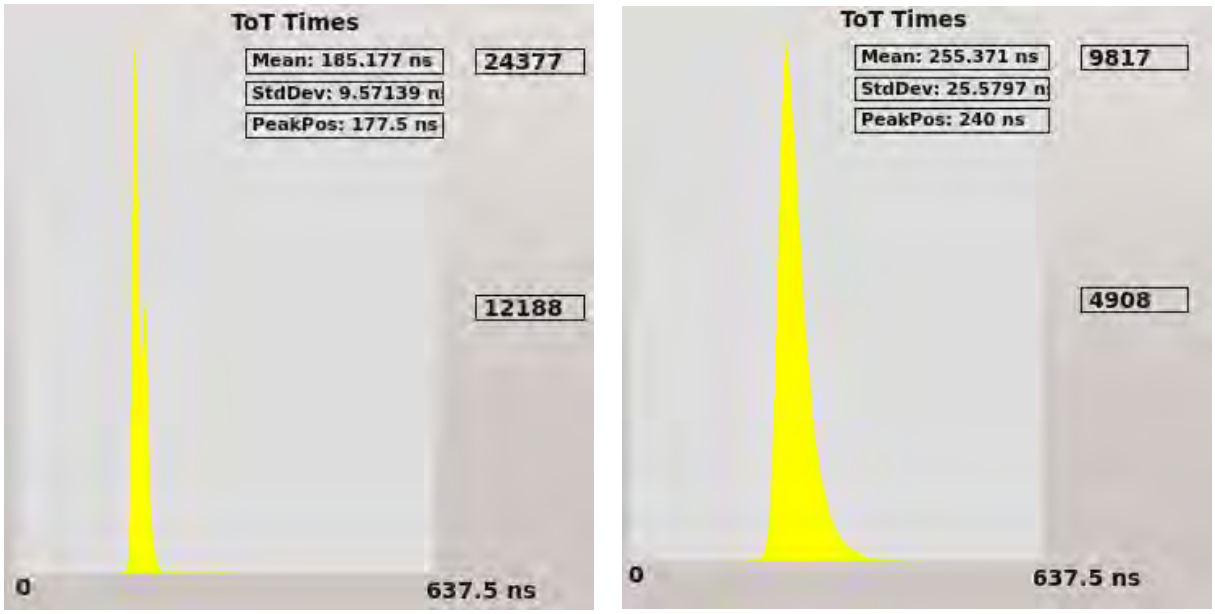


Figure 10.18: Thresholdscan and SNR fit for the low power settings.

Whether the low power settings shrink the efficiency of the pixel needs to be determined on a test beam or in a pseudo efficiency measurement in the lab with a coincidence setup and the strontium source.



(a) Full power settings

(b) Low power settings

Figure 10.19: Latency plot for the Fe-55-like injection pulse extracted from the online monitoring.

10.8 Spread of Pixel properties

Up to now only properties of a single pixel have been measured and discussed. But the MuPix chip consists of 1280 pixel of which 1120 pixel are manufactured in the two staged amplification architecture. Due to flaws and small differences in the fabrication process all pixels will have slightly different properties, which also effect their performance. These small variations have already been observed for the previous prototypes and with the tune DACs an entity is provided to compensate these differences.

10.8.1 SNR and Noise

While investigating the SNR of pixels it was noticed that each pixel requires an own calibration to the Fe-55 photon reference. Further it showed that some pixels would produce pulse heights beyond the measurable scale (<0.0 V) for an injection pulse which hardly triggered other pixels.

One of these pixels was picked and an SNR measurement was performed, as shown in figure 10.20. The injection voltage equivalent to the Fe-55 photons was calibrated to 0.45 V, 100 mV less then for the previous described pixel. The explanation for this difference is as already discussed in the optimization section a smaller detection capacitance, which induces more signal height, but also more noise. The fit yields a SNR of 9.7 ± 0.7 smaller than the value extracted before, but acceptable. The noise distortion of the pulse is tripled in comparison to pixel investigated in before.

However, most pixels in the matrix resemble the pixel behavior presented in the sections before.

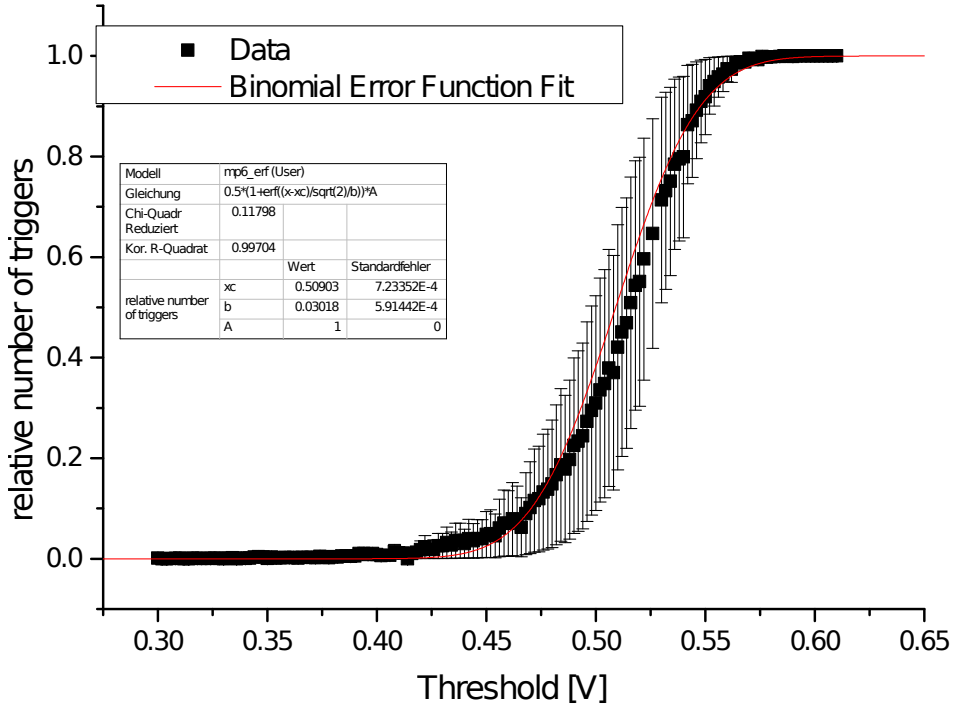


Figure 10.20: Thresholdscan and SNR fit a large signal pixel.

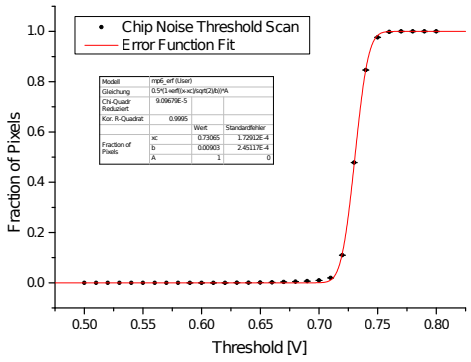
A further option that the GUI offers is a threshold scan which counts all pixel hits occurring in the matrix for a threshold. This allows to measure the noise level of the chip (figure 10.21).

A fit of an error function (fig. 10.21(a)) seems to describe also the pixel threshold distribution rather well and reveals a narrow deviation of only 9 mV, which is good as it tells that the baselines and the noise levels of all are not wide spread. However, a look into the hit distribution with a log-scale reveals a irregularity, a few pixels with a larger noise level which clearly are distinguishable from the main body of the noise distribution. They are referred to as hot pixels, as they produce noise hits for thresholds in a rather large distance from the baseline.

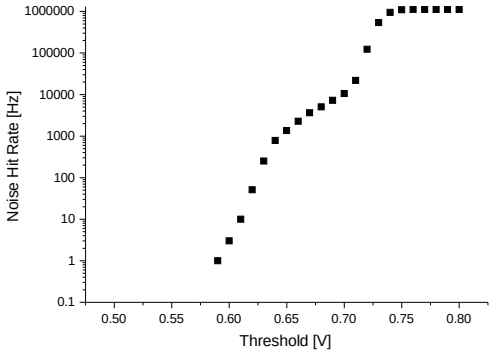
A further tool which is provided by the GUI is a threshold scan which samples the 50% noise level for each pixel and sums the result in a histogram (fig.10.22(a)). Here also the hot pixels are clearly visible as outliers.

This method can also be used to observe possible changes due to a change of the DAC settings, e.g. from full power to low power settings. The result of the scan for the low power settings is plotted in figure 10.22(b).

For the low power settings its clearly visible that more hot pixels are produced. Especially three pixels which also create for the maximal threshold distance to the baseline at 0.0 V. It has to be tested whether this effect can be tuned.

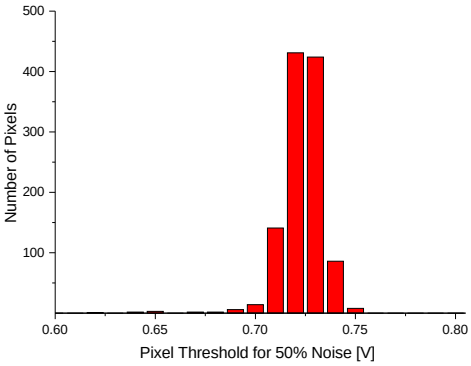


(a) Error function fit to the chip thresholdscan.

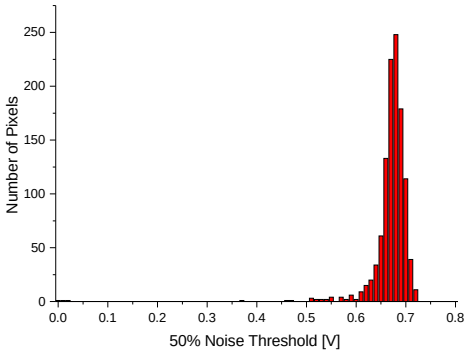


(b) Noise in the log-scale revealing hot pixels below 0.7 V.

Figure 10.21: Noise threshold scan for the whole chip with standard settings.



(a) High power settings.



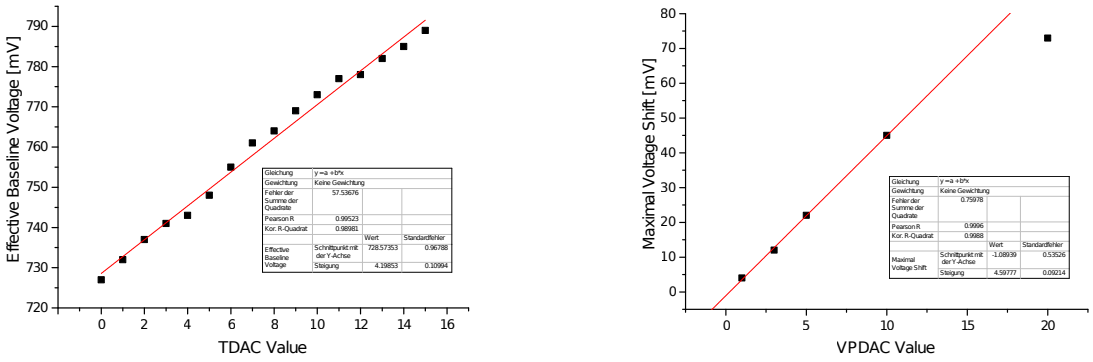
(b) Low power settings.

Figure 10.22: Chip distribution of the pixels 50% noise level.

10.8.2 Tuning

As described in section 7 the tune DACs enable an adjustment of the baseline voltage, which can be used to compensate pixel differences. They are configured with a 4 bit-value, the maximal offset is given by the chip DAC VPDAC. The higher the value, the more current the tune DACs can supply, the larger the possible shift by the DACs, e.g. with a VPDAC of 10 a shift of 50 mV can be realized.

The effect of the tune DACs is illustrated in figure 10.23. In figure 10.23(a) the 50% noise level of a pixel is plotted. The shift of this level reflects the shift of the baseline voltage. For the chosen VPDAC value it shows an approximately linear behavior with 4 mV per TDAC increase. The dependence of the maximal achievable shift on VPDAC is plotted on the right, showing a linear behavior for VPDAC values up to 10 with a range extension of 4.6 mV per VPDAC. For higher VPDAC value the transistors cause a breakdown of the linearity and smaller extensions of the TDAC range per VPDAC.



(a) Tune DAC influence for VPDAC=16. (b) The dependence of the tuning range of VPDAC.

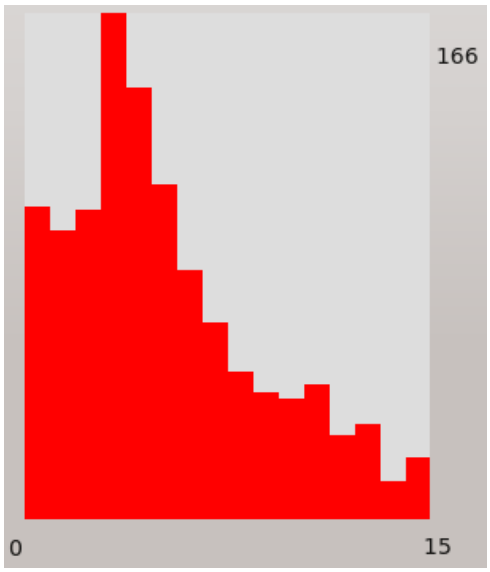
Figure 10.23: The tune DAC behavior.

Further it has to be considered that the power consumption measurement shows a huge impact for VPDAC, so also VPDAC should be as small as possible.

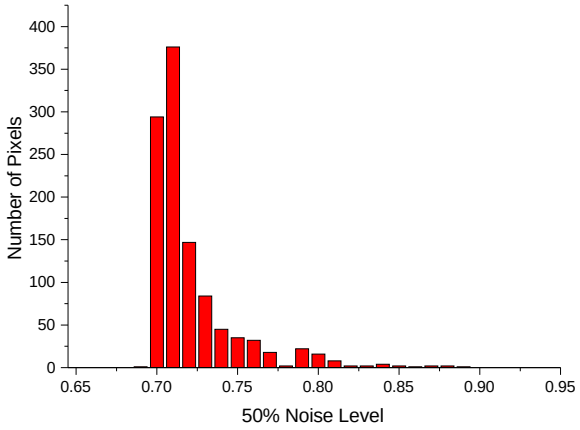
A few simple tuning procedures have been implemented. The most rigid procedure is presented in the following. This procedure aims to improve the noise level by suppressing the noise at a given threshold, but at the same time allow to approach closest to the noise which should also maximize the efficiency. For a threshold close to the noise also rather small signals can be detected. The basis of this tuning procedure is the fact, that the baseline can only be shifted to higher values. As seen before the 50% noise levels follow a distribution and there are even some outliers which need to be tuned back to the main bulk of the distribution. Over all a tuning procedure should also aim to reduce the width of the chip noise distribution. For this procedure one starts by setting a threshold, optimally in the middle of the noise distribution which also allows to compress it by shifting pixels from left of the threshold to higher levels on the right.

First all TDACs are set to zero than number of hits in absence of a signal is measured. If hits have been registered for a pixel its TDAC is increased. This is repeated 15 times until the maximal possible TDAC value is reached.

In figure 10.24 the results of such a tuning are presented. The tuning has been carried out for the low power settings with the noise distribution presented before. The impact on



(a) TDAC value distribution as monitored in the GUI.



(b) The tuned noise level distribution.

Figure 10.24: The result of tuning attempt for low power settings with threshold 0.68 and VPDAC=10.

the noise level distribution is clearly visible,it produced a sharp cut at 0.68 V. The number of pixels in the main peaks has increased, but some pixels also seem to be overtuned, as the distribution now extends rather far to high noise levels. But of course this procedure is not jet optimized to minimize the distribution.

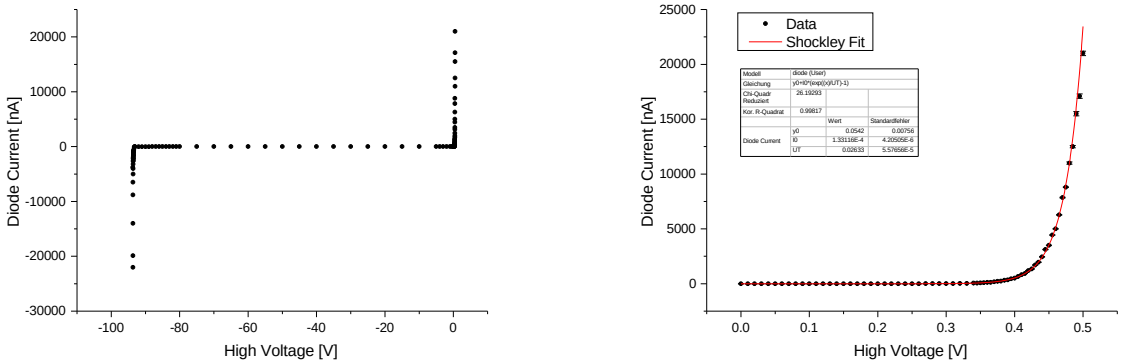
But this also shows that the extreme hotpixels observed for the low power settings around 0.0 V threshold could be tuned to reasonable noise levels, as no larger outliers are registered anymore. This is a little bit unexpected as the maximum voltage shift for VPDAC=10 obtained above only manages a shift of 50 mV. One possible explanation would be a connection between hot pixels and the comparator oscillation which was observed in the noise study. As the TDAC current is also flowing into the baseline branch of the comparator circuit, it may have an influence on the comparator stability.

10.9 The Detection Diode

10.9.1 Measurement Setup

The MuPix6 prototype also provides a new feature with a direct electric contact to one of the pixel diodes in the top row. So in total this contact is connected to 32 pixel diodes in parallel. This allows a precise measurement of the diode properties (figure 10.25).

10.9.2 The U-I-Diagram



(a) Full U-I Diagram of the pixel diodes with the high current regions for.

(b) Zoom into the forward-bias region.

Figure 10.25: U-I Diagram for the 32 pixel diodes.

It shows the typical diode behavior. In forward direction[1] the current starts to grow exponentially as described by the Shockley equation:

$$I(U) = I_0 * (\exp^{\frac{U}{U_T}} - 1) \tag{10.5}$$

In reverse-bias direction[2] the diode current approaches the reverse leakage current I_0 with 2.3 nA at -60 V and breaks down at -93.3 V.

10.9.3 Reverse Engineering of the N-Well Doping Concentration

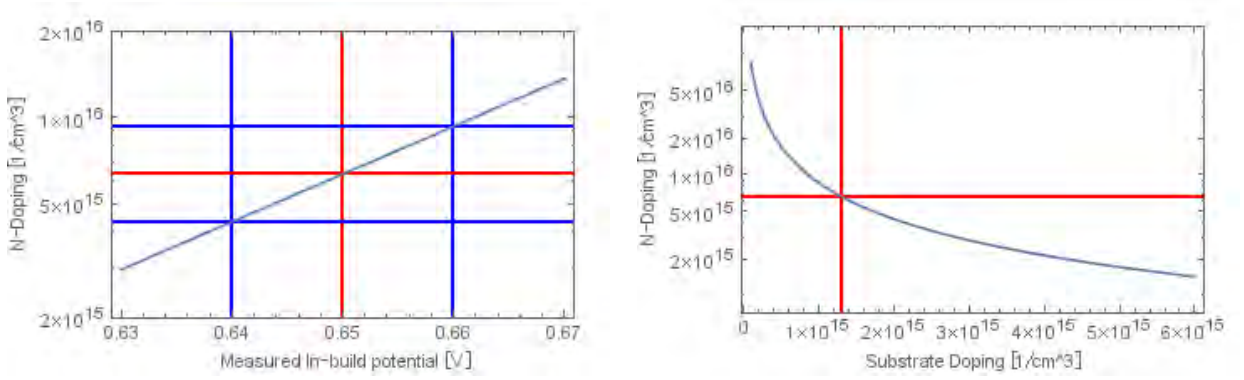
As described in section 5.3 the in-build potential can be calculated from the doping concentrations. But per se, the doping concentration used for the production of the sensors is a company secret. However, the assumption can be made to know the doping concentration of our p-substrate as a low resistivity substrate was requested, a value of 10 Ωcm is assumed for the low resistivity substrate, which corresponds to 1.32×10^{15} cm^{-3} boron concentration. The doping concentration of the n-well is still unknown but could be calculated, if we can measure the in-build potential.

[1] positive diode voltage
[2] negative diode voltage

This is however not trivial as it can not be read from the U-I diagram. The idea for the concept of the measurement, presented in the following, is inspired by photovoltaics as here the depletion zone created by the in-build potential is used to extract a current, originating from electron-hole pairs created by photo conversion in the depletion zone. The application of an external forward voltage will result in a reduction of the depletion width, shrinking the photo current. When the external voltage is equal to the in-build potential, the depletion zone has vanished and no photo current is produced anymore.

However, by enlarging the forward voltage also the forward current increases, which is much larger than the photo voltage which is flowing in reverse direction. However, by switching on and off a strong light source deviations of the absolute current are visible also for large forward currents ($\mathcal{O}(10\ mA)$. This procedure allows to get at least a lower boundary for the in-build potential. For the MuPix6 diode structure this resulted in $0.65 \pm 0.01\ V$.

This measured value allows to estimate the n-well concentration: With the assumption



(a) N-Well concentration based on the measurement value(red) and error band (blue).

(b) N-well concentration for variation of the p-doping (Calculated).

Figure 10.26: N-well doping concentration calculated from the photo measurement.

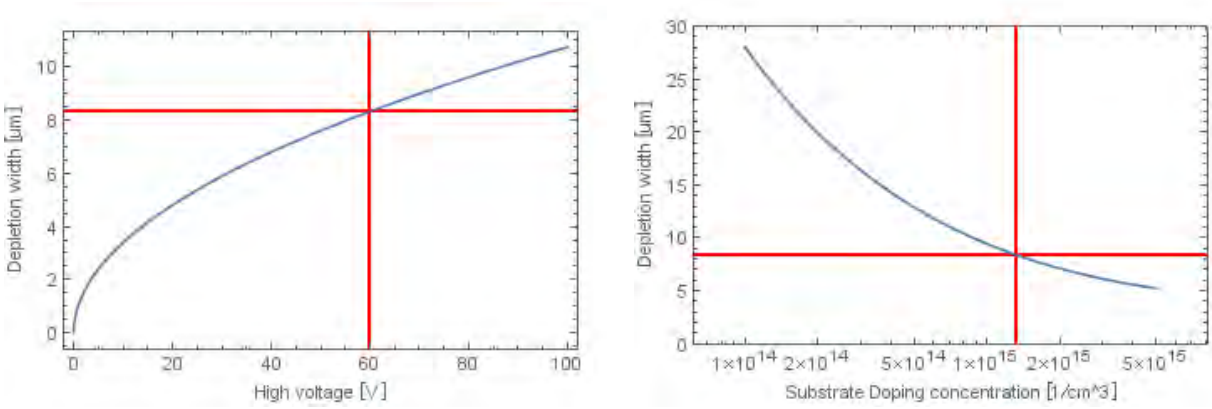
made above this gives a n-doping concentration of (fig.10.26):

$$N_D(U) = \frac{ni^2}{N_A} \cdot \exp^{\frac{U}{U_T}} = 6.5 \times 10^{15}\ \frac{1}{cm^3} \tag{10.6}$$

However, due to the exponential behavior the uncertainty on the value from this value is $\sim 50\%$ and as shown in figure 10.26(b) the impact of the substrate doping concentration is large.

But still, depletion widths and field strengths can be calculated, based on this estimate. The illustrations (fig. 10.27) show the depletion width dependence of HV and substrate doping concentration. Which gives an estimation for the depletion width at 60 V, the nominal setting, of $\sim 8\ \mu m$. Further dependence of the substrate doping concentration is plotted to show up the boost in effective detection area by using a smaller doping concentration[3].

[3]high resistivity substrate



(a) HV-dependency.

(b) Substrate Doping Concentration.

Figure 10.27: Depletion zone thickness calculated for the 1D-model.

Further the electric field in the depletion zone is calculated for 40, 60, and 80 V reverse bias voltage and plotted in figure 10.28 and shows already for 80 Volts a $\sim 1\mu m$ critical field regions.

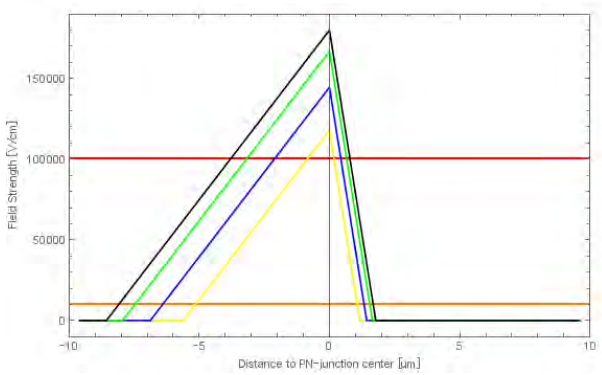


Figure 10.28: Electric Field in the depletion zone for different voltages: 40V (yellow), 60V (blue), 80V (green). With the orange and red line critical field strengths are marked:At 10 kV/cm (orange) the drift velocity starts to saturate, at 100 kV/cm (red) the probability for avalanche effects starts to rise significantly.

This input can be used for a Technology Computer Aided Design (TCAD) simulation carried out at Heidelberg and try to recreate the diode behavior of the pixel cells and get a better understanding of the depletion zone and possible inefficencies due to inhomogeneities in its expansion.

A first study with a simple diode structure, build with the doping concentrations determined above, yielded a different U-I behavior. Especially the simulated breakdown voltage was much higher $\sim 200V$.

However, as the pixel itself consists of several n-well diodes spacial effects might come into play. To check this the spacial pixel structure was extracted from Cadence®and rebuild in a TCAD simulation as presented below (figure 10.29).

This doping structure shows a lower breakdown voltage for the extracted doping concentrations, so structural effects play a role.

The TCAD simulation allows to extract 2D-maps of e.g. the doping profile, depletion zone, and electric field. Which boosts the understanding of the pixel structure.

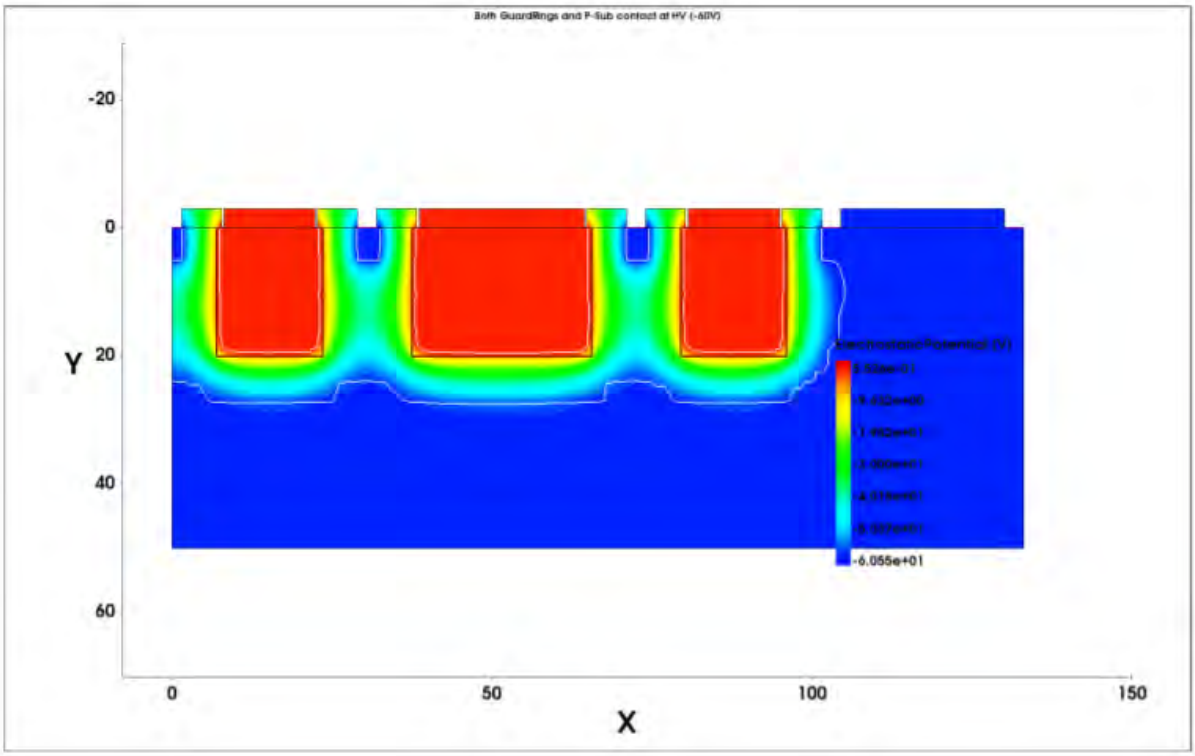
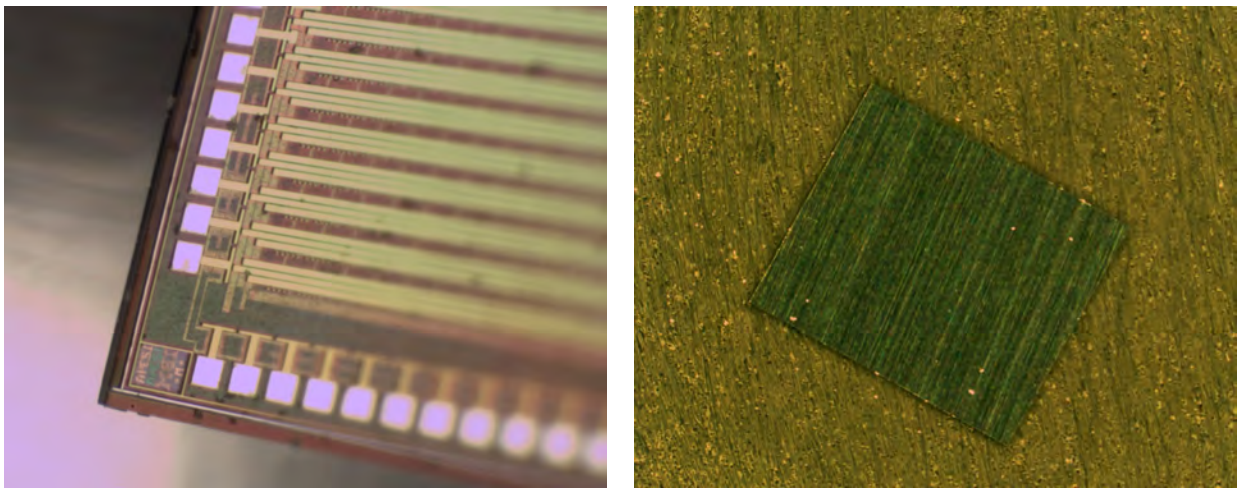


Figure 10.29: TCAD simulation of the electrostatic potential with the calculated doping values and the layout extracted from Cadence®. [51]

10.10 Thinned Mupix4 Observations

Additional to the MuPix6 prototype also industrially thinned, $50\mu m$ thick MuPix4 sensors have been tested in the lab for the first time. As MuPix4 itself has already been characterized [37], the performance of the thinned sensors had to be compared to the results obtained for the un-thinned $250\mu m$ sensors.

The thickness of the sensors has been verified with a μm thickness gauge (figure 10.30(a)). Further back side of the sensor was examined for any marks of the thinning process(figure 10.30(b)).



(a) Thinned MuPix4 chip: As size comparison the aluminum pad with 70 microns side length

(b) Substrate after thinning with clear scratch marks

Figure 10.30: The thinned MuPix4 chip.

The marks of the whetting are clearly visible, which poses the question if negative effects are expected from the tinning process. One problem that may occur after thinning of a HV-MAPS sensor is cutting into the active detection volume given by the expansion of the depletion zone. This would reduce the efficiency and even more cause a lot of noise due to trapping processes on the substrates surface. As the scratch marks indicate the sensor was undergoing mechanical stress in the thinning process. This might also induce lattice defects which trap charged particles and reduce the charge collection efficiency and cause more noise.

As a first step the thinned sensor had to be bonded, this turned out to be no problem for properly glued sensor. The thinned silicon sensor itself does not have the mechanical stability to withstand the pressure which the bonding machine uses to welt the aluminum wire to the bond pad. It simply can break with no proper back support, which is provided by the glue.

Also no problems came up when powering. Neither for the low voltage, nor for the high voltage a difference was observed in the draw currents. For lattice defect, as explained above, an enlargement of the HV current would have been expected.

Further also the the performance of the thinned sensors has been tested and compared to the thick sensors. No significant effect has been observed so far and the thinned MuPix4 has been routinely operated on a testbeam campaign.

11 Testbeam Characterization

11.1 Testbeam Campaigns

Two successful test beam campaigns in July and October of this year (2014) have been performed at the πM1 beamline of the HIPA facility at PSI. This beamline provides a mixed beam with a tunable momentum between 100-500 MeV/c. The beam is a secondary beam extracted from target M in the HIPA complex (fig. 3.5 & 11.1). It provides predominantly π^+, with small fractions of μ^+ and e^+ ($\mathcal{O}(1\%)$) at very high rates of $\mathcal{O}(100MHz)$.

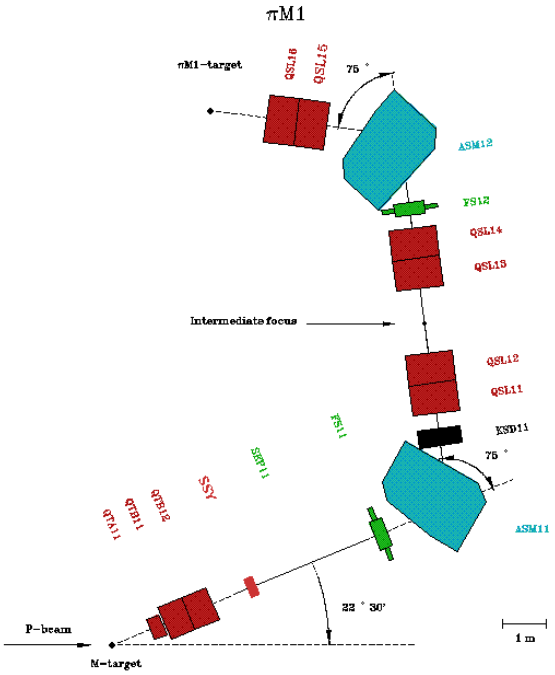


Figure 11.1: PiM1 Beamline layout [52].

The beam momentum was tuned to 250 MeV/c, a well established setting and the rate was controlled with the help of the shutters, collimators which can be used to reduce the beam rate.

With a momentum of 250 MeV/c the pion are rather low energetic and are therefore subject to large multiple scattering effects. The average energy loss of the pions is 4 MeV/cm this is comparable to the energy loss of electrons in the Mu3e experiment (fig.4.1.2).

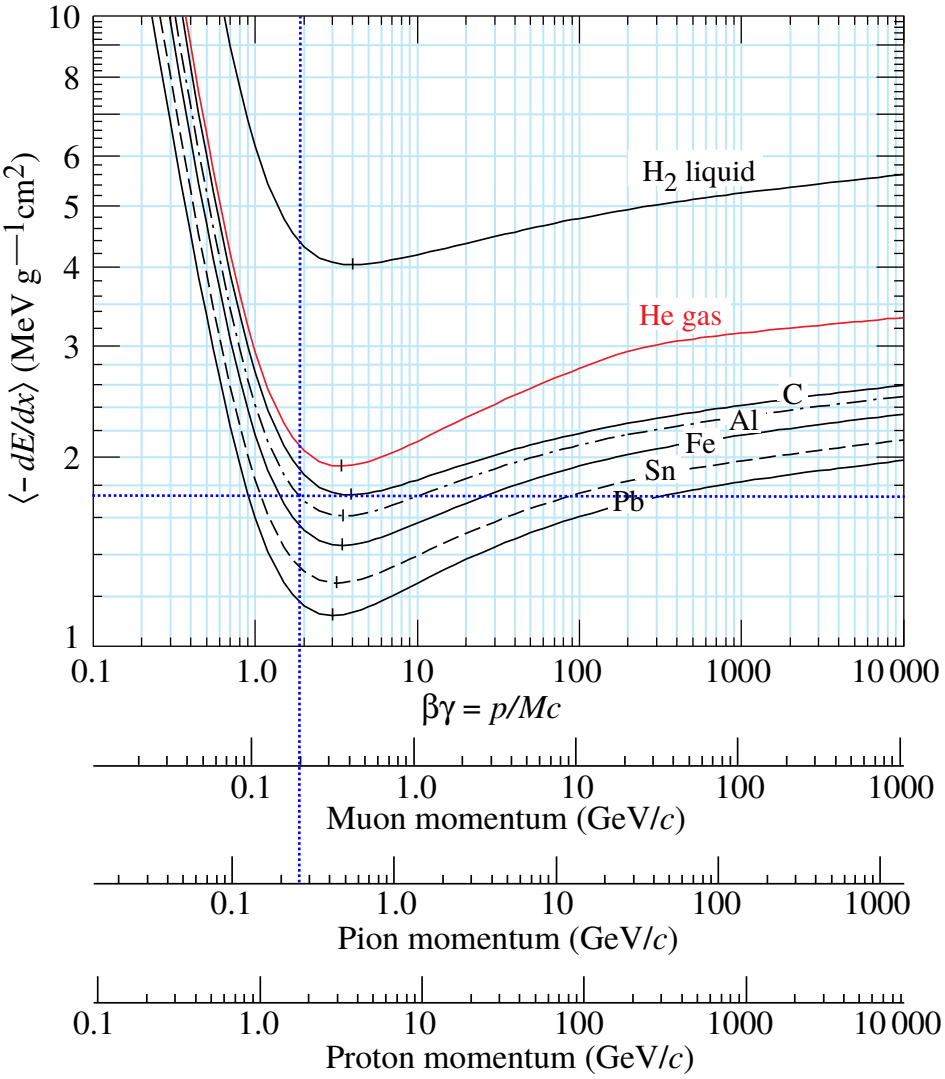


Figure 11.2: Mean energy loss for pions in matter, the Al curve can be taken as reference. Adapted from [17].

11.2 Setups

At the testbeam campaigns both setups, the single MuPix setup and the MuPix telescope [40], have been tested. They are arranged on one Thorlabs® stage, using the mechanics developed for the MuPix telescope as shown in figure 11.3. The single setup is placed closest to the beam window in the nominal focus point of the beamline. Further each setup is provided by time and trigger information with the help of two scintillating tiles which frame single setup and telescope respectively. This trigger system is used to monitor the particle rate, as well as to provide precise time information for the single setup. The slow control and readout of the setups is achieved just as in the lab. Both setups are hooked up to their readout PCs in the testbeam area which can be monitored and controlled remotely from outside.

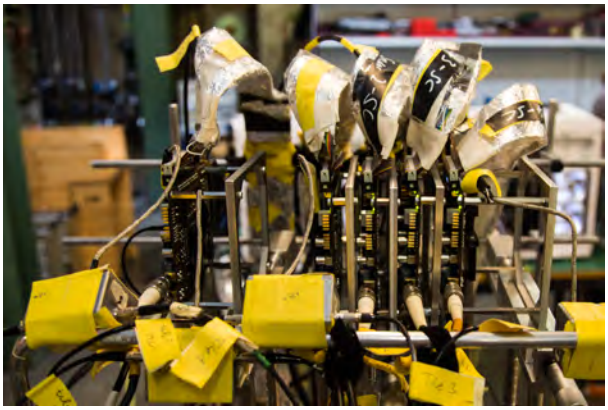


Figure 11.3: Testbeam setup: Thorlabs® stage housing 1+4 sensor planes and 4 scintillating tiles.

11.2.1 July Testbeam

At the July testbeam single setup and telescope were running with 250 μm MuPix6 sensors on thinned PCB boards. As the software of the setups was revised earlier in the year, this was the first time the setups were used at a testbeam campaign in this new configuration. But the extensive testing and debugging of the setups in the lab payed off and only minor adjustments had to be done before the data taking started. Both setups performed threshold and HV-scans in parallel, the telescope used the second layer as DUT. The setups were running stable, also over night, without crashes and the single setup took $\sim$ 150 GB data corresponding to approximately 3 billion observed chip hits, a comparable number of triggers and 3 million hitbus signals.

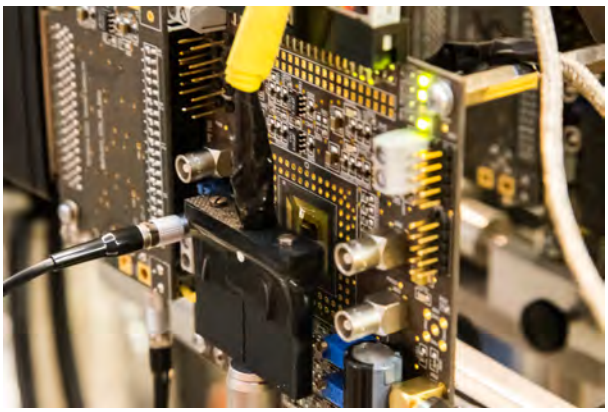


Figure 11.4: Single MuPix setup: The scintillating tile housed in the light tight holding structure and the on-board MuPix6.

11.2.2 October Testbeam

For the October testbeam the new floating MuPix sensors have been introduced. The single setup was running with a floating MuPix6 sensor and using the new accelerated readout software. In total 1 TB of data was recorded

The MuPix telescope used 3 tracking planes made of floating MuPix6 sensors. As DUT a floating MuPix6 and a floating and thinned MuPix4 were used. For the MuPix6 sensors both setups performed scans of bias currents, aiming to reduce the power consumption, but maintain the sensors efficiency.

With the help of the MuPix telescope further the efficiency of a thinned MuPix4 sensor was investigated.

11.3 Mechanical Alignment

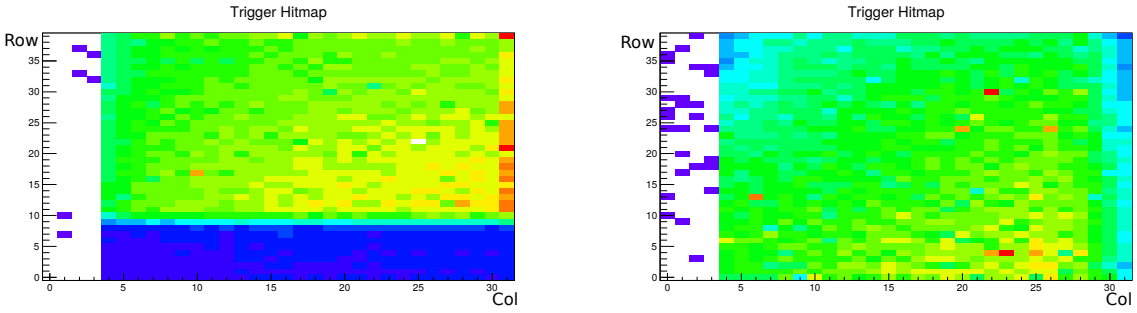
For the position of the beam coming from the beam window, there are only very rough indicators. So the beam has to be located after a coarse alignment with the help of markers on the ground and most recently also a laser system indicating the beam height from the ground. From the mechanical point of view the setup can be aligned very nicely due to the telescope mechanics. The horizontal alignment perpendicular to the beam axis can be done very precise with the help of μm-screws. For the alignment in beam direction the rails of the Thorlabs® stage can be used to adjust the position with millimeter precision. Here the goal is to minimize the distance between the layers of the telescope to reduce the influence of multiple scattering on the resolution. The vertical alignment is the hardest as there were no precision tools available so it had to be done by hand with the help of rulers.

The first thing which has to be done is to fix the rotational alignment which can be achieved e.g. by observing the hit rates in the first and the last scintillator and maximize them. Now everything in between has to be aligned properly. The problem for the tiles is that they can only be aligned vertically which reduces the flexibility of the setup as every layer has to aligned relative to them. Further the tiles are not fully identical, so even if they are perfectly aligned vertically there is still the possibility of horizontal offsets.

For the telescope the hit correlations from the online monitor can be used to align the layers properly. The shifts in the hit correlations can be used to align the telescope precisely and determined as they also indicate the direction of the shift.

The sensor of the single setup is only aligned with respect to the scintillating tiles and aims to achieve a large overlap. For the July testbeam this alignment was done by eye and rate considerations of time coincidences, as no tool was present then which provided spacial correlations between the tiles and the chip. This is of course not optimal and as a result the overlap between tiles and chip was not completely perfect, as the data revealed later and triggered the development of an alignment tool which is integrated into the online monitor. Which allows a perfect alignment and is only limited by the fabrication differences of the tiles and the alignment of the whole stage.

For the next testbeam campaign, in march at DESY new tools will be available, triggered by the lessons learned from the PSI testbeams. To be able to adjust the vertical orientation of the setups more precise new Thorlabs® add-ons have been specified to allow a μm alignment after a first coarse alignment procedure. Further the tiles will gain more flexibility by adding horizontal adjustability, allowing a perfect alignment.



(a) July alignment

(b) October alignment

Figure 11.5: Alignment of the tiles for July and October.

11.4 Measurements

The telescope takes hit data with all 4 detection planes in parallel, which allows to track charged particles. A particle track can be determined with the 3 tracking planes and the expected hit position on the DUT can be extrapolated. The efficiency can now be calculated by counting the number of reconstructed tracks and the number of DUT hits which could be matched to a track. In the following however, only preliminary results are presented for the telescope, as the analysis is a bachelor thesis of its on [48].

The target of the single setup is especially the investigation of the analog and timing behavior of the chip for particles comparable to. This can be achieved due to a very good time resolution which is provided by the scintillating tiles trigger system. The spacial distance between the tiles and the chip is as minimal as the Thorlabs® allows, to reduce the rate loss due to multiple scattering.

The coincidences of the discriminated tile signals are sampled by the FPGA. Each trigger indicates a particle penetrated both tiles. The tiles are roughly $4 \times 4\ mm^2$ wide, so they can cover the sensor. However, for the coincidence the overlap of both scintillators plays a role, which can also be smaller than the sensor. So here a unknown geometrical form factor comes into play.

As the readout software produces time ordered frames. All triggers, hits and hitbus signals are collected belonging to the same time slice. A good time ordering is possible, as the software allows to incorporate setup delays, which are corrected on the run, guaranteeing all setup systems are running time synchronized. Only at the boarder of two frames miss-matches may occur.

11.5 Data Sets

In the following the properties of the data set used in the analysis are presented.

11.5.1 July

DAC	Value
VPDAC	0
VPComp	30
BlRes2	30
VNDel	10
VN2	30
VNLoad2	5
VNFB2	10
VNFoll	16
VN	30
VNLoad	5
VNFB	A

Table 11.1: DAC settings.

Parameter	Value	Value	Impact
Timing Setting	0x77EE7C33		stable running
Readout Throttle	0xF4		$\sim 5\mu s$ frame length 200 kHz readout
Hitbus Pixel	16/20	col/row	central pixel
HV	-60	[V]	
Threshold	0.64	[V]	acceptable noise
Tuning	none		

Table 11.2: July default run settings.

In the July testbeam only functional tests along with threshold and high voltage scans have been performed. The well functioning DAC settings from the lab have been used. But as a first attempt to reduce the enormous power consumption the three main biases have been halved (VN, VN2, VPComp = 30), on the cost of a higher noise level. During this testbeam it was realized, that the software can not handle the large data rates provided by the FPGA when no readout throttle is applied (Readout rate >1 MHz). So a good throttle level was determined which allowed stable running (tab. 11.2).

In the following analysis the data for the threshold and HV scan is used. The threshold was varied between 0.66 V and 0.0 V. The high voltage scan covers the range from -5 to -80 V.

Additionally a subset of the threshold scan data consisting of 10 runs at 0.64 V threshold has been extracted to investigate the chips behavior at standard running settings.

11.5.2 October

DAC	Value
VPDAC	20
VPComp	30
BlRes2	30
VNDel	10
VN2	30
VNLoad2	5
VNFB2	10
VNFoll	16
VN	30
VNLoad	5
VNFB	A

Table 11.3: Default DAC settings.

Parameter	Value	Unit	Impact
Timing Setting	0x77EE7C33		Stable Running
Readout Throttle	0x80		$\sim 3\mu s$ frame length 333 kHz readout
Hitbus Pixel	16/20	col/row	central pixel
HV	-60	[V]	
Threshold	0.65	[V]	acceptable noise
Tuning	none		

Table 11.4: October default run settings.

The main goals of the October testbeam was the test of the new accelerated readout. The setup could be successfully operated to values up to 500 kHz, as a safety margin $\sim 333kHz$ have been set for the testbeam. The readout is now only limited by the CPU-FPGA-communication (Polling) not by the readout speed of the GUI. Further a bigger emphasis was put on power consumption considerations and the chips analog performance, so a scan of different DACs was performed.

11.6 Data Quality

The data quality is ensured by the only monitoring. Any failure, e.g. the DACs have not been set properly, will show an impact and can be noted. To enable also an easy post-run quality check, a snapshot of the online monitoring window is taken automatically at the end of a run (fig. 11.6).

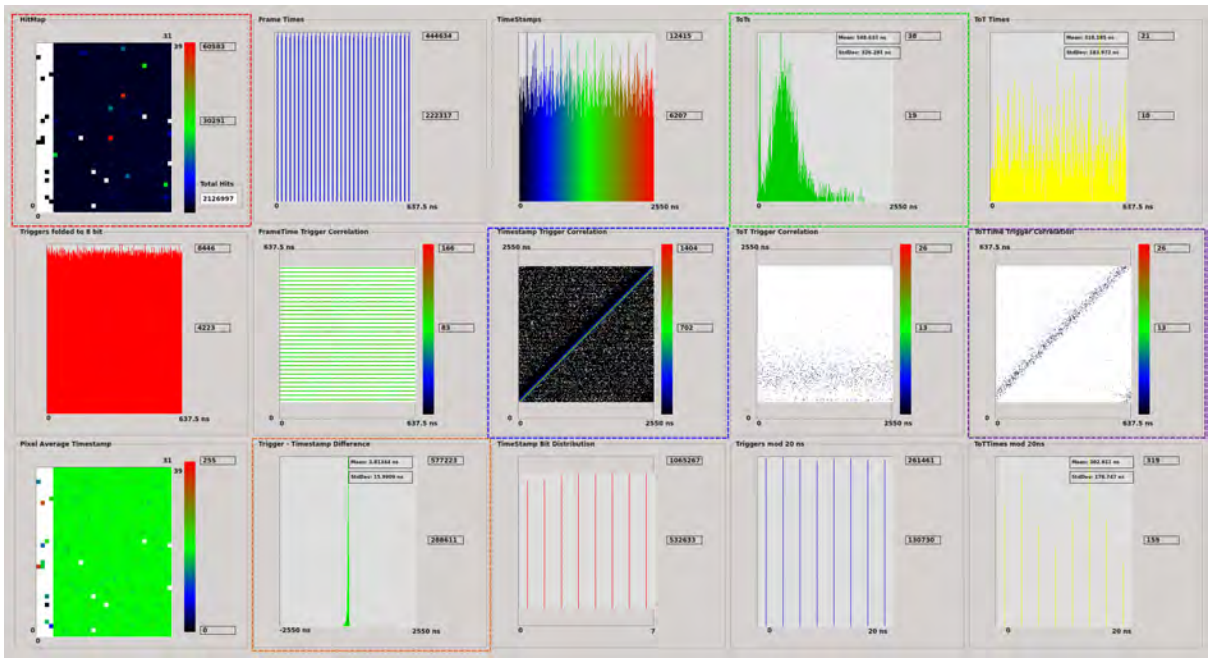


Figure 11.6: An automatic snap shot of the online monitor (July). The most important windows are marked: Red-the hit map, Blue-the coincidence between timestamps and triggers, Orange-the difference between trigger and timestamp times gives an online time resolution estimate, Green-the ToT spectrum measured from the hitbus, Purpel-the correlation between hitbus signals and triggers.

11.7 Data Analysis

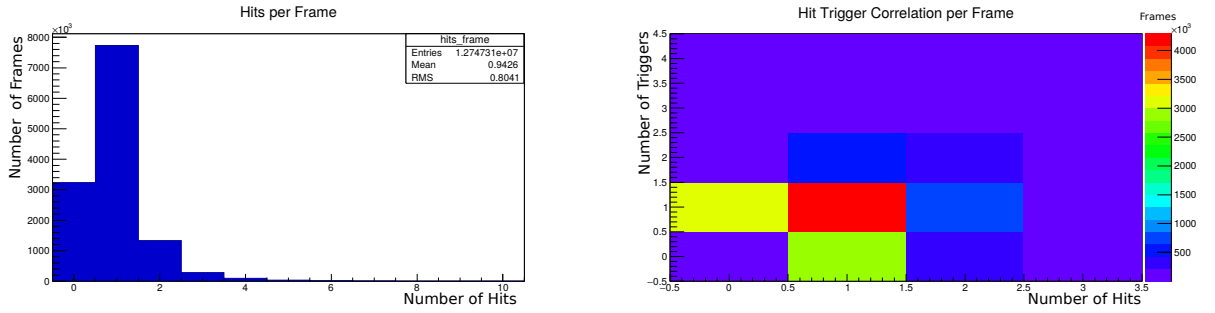
The main goal of the testbeam analysis is the extraction of the chips intrinsic time resolution. To extract the time resolution and further measures ROOT scripts have been developed which allow an easy manipulation of the testbeam data.

11.7.1 Time Resolution Chip

Each pixel of the MuPix6 can provide a 8-bit timestamp which encodes the time it was triggered. The precision of this time information can be tuned with the timestamp frequency. For the used data set a time binning of 10 ns was chosen. They are provided externally and are directly extracted from the 48-bit master clock on the FPGA. The trigger times are also extracted from this clock.

Due to the sandwich structure of our setup a time correlation is expected for particles which hit the sensor, as it most probably also penetrated both scintillating tiles, causing a trigger signal.

The correlations can be extracted very easily as the frames are already time ordered and incorporate possible correlated hits and triggers. However, if a frame contains more than one hit or trigger, multiple assignments are possible. This ambiguities cause random background as they are most like not correlated at all. So preferably only frames containing one hit and one trigger are used for this analysis. As figure 11.7(b) shows this cut does not reduce the data sample as this combination is the most likely frame type.

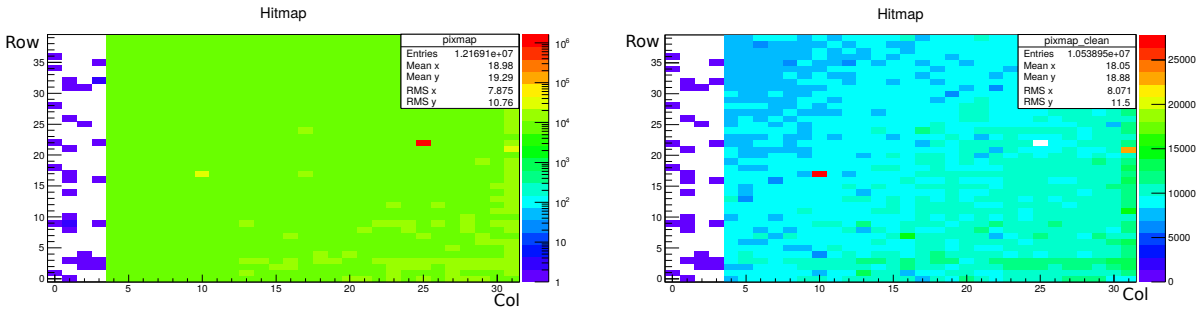


(a) Hits per frame

(b) Correlation of trigger and hit numbers per frame

Figure 11.7: Hit and trigger frame occupancies

But still a serious background source remains, as noise hits may cause this constellation together with a trigger only event, which come naturally as the area covered by the tiles is larger than the chip and even more not perfectly aligned (fig.11.5). Single trigger and hit frames make up a large portion of the data frame accidental coincidences are very probable. The coincidence of the tiles makes fake triggers very unlikely and there would be no mean to counter act them. Noise hits however, are possible and will most probably be caused by hotpixels. As easily seen from figure 11.8(a) the data sample is highly polluted by a single hotpixel. To clean the data set this pixel is cut out completely (fig. 11.8(b)). By doing so two noisy pixel dominate the hitmap, but with an acceptable occurrence, so no more additional cuts are applied pixel-wise. The remaining data set contains 4 million frames.



(a) Hitmap dominated by the hot pixel

(b) Cleaned Hitmap

Figure 11.8: Hitmaps of the dataset before and after cutting out the hotpixel

Now the timestamp-trigger-correlation can be plotted of the remaining data set (fig.11.9). The time resolution of the chip can then be determined by observing the time difference between the correlated timestamps and trigger times (figure 11.10).

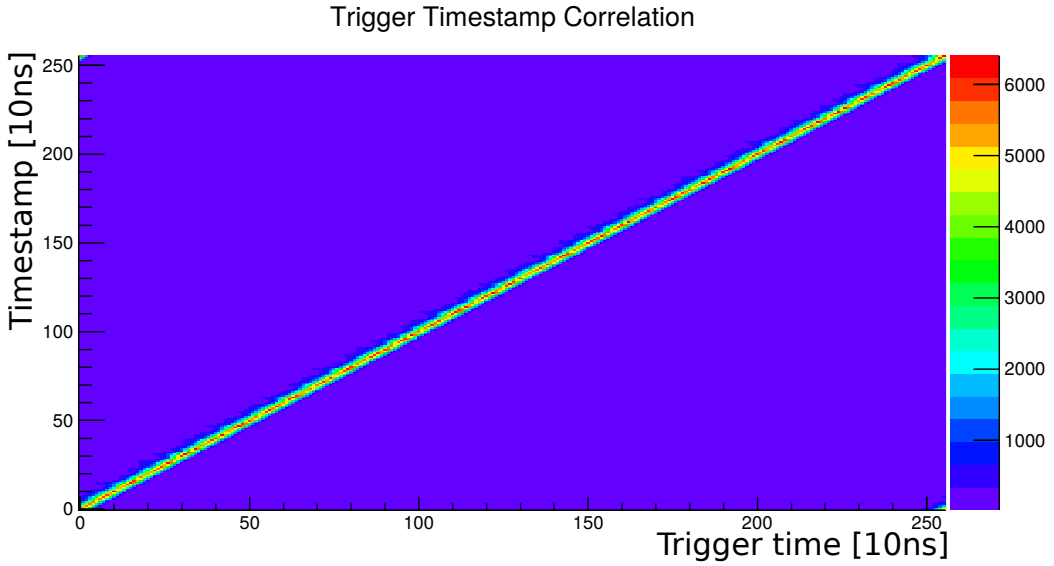


Figure 11.9: Timestamp trigger correlation with a binning of 10 ns.

The time difference plot shows a very clean peak, which has a tail to larger time differences. This tail was also observed for the low power settings (section 10.7). The origin of this is most likely the pulse shape behavior which causes a logarithmic behavior relative to the input signal.

However, the main body of the distribution can be approximated by a gaussian fit, yielding a standard deviation of $\sigma = 10ns \cdot 1.548 \pm 0.001 = 15.48 \pm 0.01ns$. This is an upper limit for the time resolution of the chip.

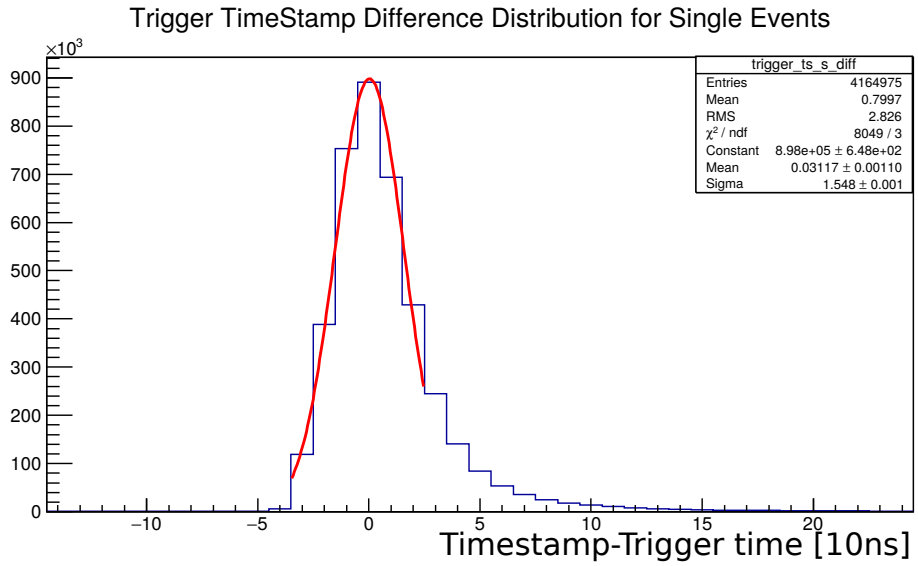


Figure 11.10: The timestamp trigger difference distribution.

11.7.2 Single Pixel Time Resolution

The same analysis can be done for the hitbus signal, which allows to measure the time resolution provided by the comparator. Here, both the trigger time and the rising edge of the hitbus signal are sampled with 400 MHz giving finer time bins. The same cuts are applied for this analysis plus the condition that the frame contains a hitbus signal. This shrinks the data set by roughly a factor thousand, as only one of the 1120 pixels produces a hitbus signal. To increase the sample size the data of 10 consecutive runs at a threshold of 0.64 V and -60 V high voltage are used.

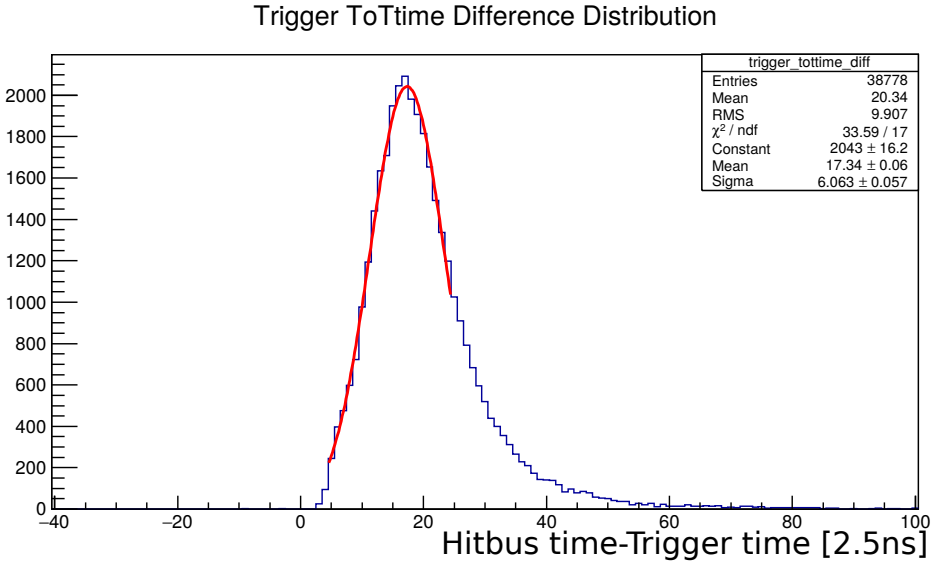


Figure 11.11: The hitbus time trigger difference.

As presented in figure 11.11 the single pixel shows a very similar behavior. The gaussian fit reveals here a time resolution of $\sigma = 2.5ns \cdot 6.063 \pm 0.057 = 15.1 \pm 1.4ns$, slightly better than the timestamp resolution.

Also here the distribution has a notable tail. Therefor it is not a pixel to pixel smearing effect. The hitbus time trigger time difference is basically a latency. From pulse shaping considerations it is known that as well latency, as ToT depend on the strength of the input signal, the deposited energy. This triggers the investigation of the correlation between ToT as a measure of deposited energy and the latency.

11.7.3 Timewalk

As each hitbus signal provides both the starting time and the length, the ToT can be very easily correlated with the latency. This distribution shows as expected, an anti-

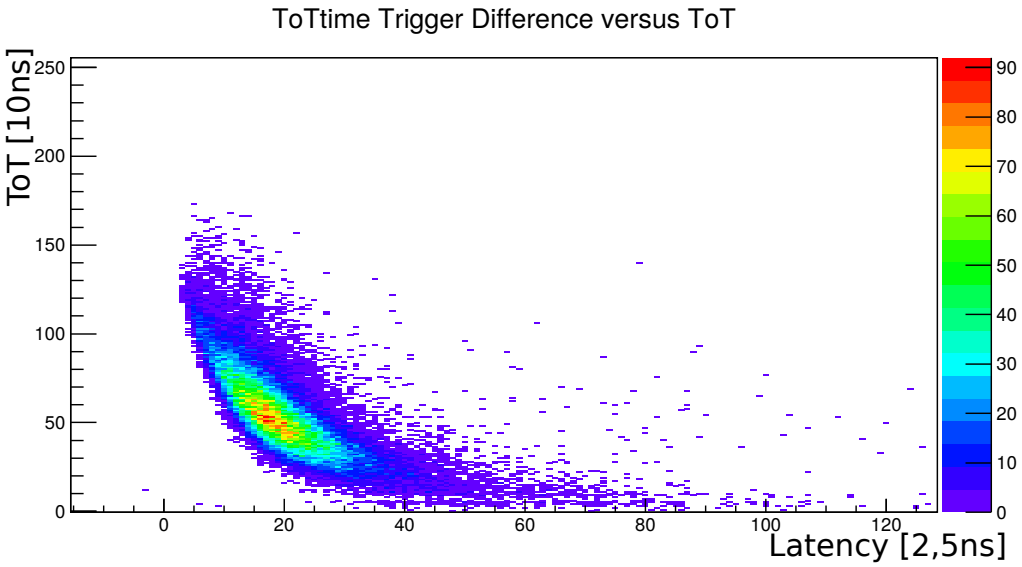


Figure 11.12: The latency ToT correlation plot.

correlation. The larger the ToT, the smaller the latency for a constant threshold, the time walk effect. Out going from the pulse shape description we can find an approximation for this behavior.

For sufficiently large pulses or a small threshold and $\tau_2 \ll \tau_1$, we can approximate the rising edge of the pulse with $U(t) \propto U_0 * (1 - \exp^{-t/\tau_2})$ and the falling edge with $U(t) \propto U_0 * \exp^{-t/\tau_1}$.

With this approximation simple expressions can be found for the latency and the ToT. For a given threshold an expression can be found for U_0 depending of the latency or the ToT likewise. E.g. $U_0 \propto U_{Thr}/(1 - \exp^{-latency/\tau_2})$. Using this with the falling edge equation gives an expression for the ToT depending on the latency $ToT \propto -\log(1 - \exp^{-latency/\tau_2})\tau_1$.

ROOT allows to extract a profile function for this distribution and the above extracted relation can be fitted more general as:

$$ToT(latency) = -\log(1 - \exp^{-latency/\tau_2})\tau_1 + offset \tag{11.1}$$

The fit is shown in figure11.13 with p0 as $\tau 2$, p1 as $\tau 1$, and p2 as offset.

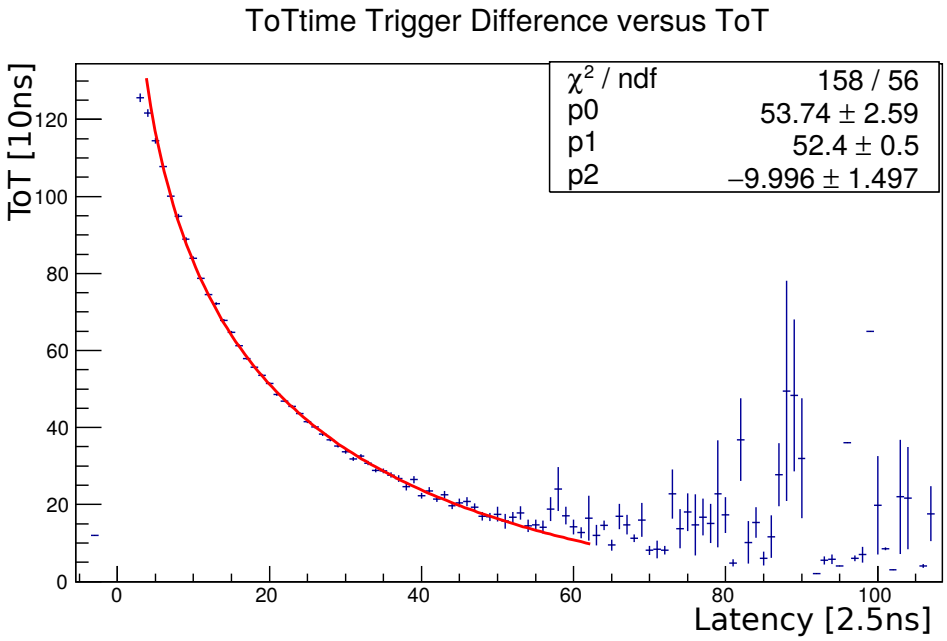


Figure 11.13: Fit to the profile of the timewalk distribution.

The description fits the distribution quite well, although the fit results do not fit to the $\tau_2 \ll \tau_1$ condition.

Part IV

Discussion

12 Discussion & Summary

12.1 Discussion

The Mu3e experiment searches for the lepton flavor violating decay $\mu^+ \to e^+e^-e^+$, which is heavily suppressed in the Standard Model to a branching ratio $<10^{-54}$, below any experimental reach. Thus, any observation of the decay $\mu^+ \to e^+e^-e^+$ would be a clear sign for new physics.

The experiment projects a branching ratio sensitivity $<10^{-16}$, four orders of magnitude smaller than previous experiments [8]. To achieve this goal the tracker consists of $50\mu m$ thin pixel sensors, thus minimizing the material budget and thus reducing multiple scattering, which is crucial to achieve a good vertex and momentum resolution. For the Mu3e experiment the novel High Voltage Monolithic Active Pixel Sensor (HV-MAPS) technology is a suitable choice as it provides fast charge collection times and the possibility to thin the sensors down to $50\mu m$ without reducing the detection sensitive volume.

In this thesis the setup for the HV-MAPS prototype characterization has been refined and optimized for the analysis of the HV-MAPS prototype MuPix6. First characterization results have been obtained in the laboratory and on testbeam campaigns.

The characterization setup was refined and extended as well on the hardware, as on the software side. The software now offers a fast digital readout and a very flexible interface which will allow an easy integration of future prototypes and simple transfer of new characterization findings to the telescope setup. On the hardware side, the setup now provides a low voltage differential signal readout which minimizes cross talk and enables a bit error safe data transmission, also while applying timestamps with frequencies up to 400 MHz.

The MuPix6 prototype has been characterized in the laboratory with the in-build method of injection signals, a infrared laser and radio active sources. The observation of the High Voltage (HV) dependence revealed the same behavior as observed with previous prototypes, an increase of the signal due to expansion of the depletion zone $\propto \sqrt{U}$, but also a reduction of the noise level. The signal-to-noise ratio (SNR) of pixels was measured to values between 10 and 16. The pixel performance can vary due to inhomogeneity in the fabrication process, thus the spread of the pixel was analyzed with respect to their noise level. Showing the existence of a few pixels with a significant larger noise level, but otherwise a very uniform behavior.

To counteract pixel inhomogeneities a tuning possibility is provided which allows to shift the baseline voltage of each pixel and thus to adapt the pixels noise level. This tuning procedure was investigated and a first simple automated tuning method was presented which successfully alters the pixels noise level and allows even to adapt the noisy pixels.

By adding a second amplification stage in the MuPix6 pixel electronics also the number of bias currents used to control the pixels performance are increased. To get a better understanding of their function scans have been performed for each bias current, monitoring their impact on the pulse shape and the power consumption of the chip. The power con-

sumption of the standard settings, which have been used for the characterization of the prototype and also the subset of bias currents which were used on previous prototypes, was measured to be 935 $\frac{mW}{cm^2}$ which heavily violates the design goal of 150 $\frac{mW}{cm^2}$. Thus an optimization of the bias settings with the power consumption as main objective is necessary. With the help of an iterative method and the knowledge acquired from the bias current scans, the power consumption could be reduced to 223 $\frac{mW}{cm^2}$ while preserving a good pixel behavior. However, the SNR of a pixel reduced from 15 with the standard settings to 10 with the low power settings and the latency of the pixel response to a injection pulse doubled.

Further the performance of the $50\mu m$ thin MuPix4 sensors has been investigated and no significant impact of the thinning could be detected.

On the testbeam campaigns the timing behavior of the pixels could be studied very well and an intrinsic chip time resolution of 15.48 ns has been measured.

12.2 Summary

The MuPix6 was successfully integrated in a test setup and the first characterization results obtained for the pixel performance are consistent with the results obtained for MuPix4, with the additional advantage of a larger signal and thus a safety margin against digital cross talk which was observed for MuPix4. The measured time resolution already meets the requirement posed by the Mu3e tracking detector. The power could be reduced to an acceptable level, as the cooling setup also shows a much higher cooling capability compared to the design goal. So the two staged amplification introduced in MuPix6 seems to be a suitable technology in terms of rigidity against digital signals on the chip, however the additional power consumption caused by the second stage has to be considered, but seems to be reducible to an acceptable level.

12.3 Outlook

Due to the limited time frame, the possibilities of the setup and the acquired testbeam, with the single setup and the MuPix telescope, could not be fully explored in this thesis. But a detailed analysis of the test beam data and a detailed investigation of tuning possibilities will be carried out in future bachelor projects [48] and [53].

The next testbeam campaign is already appointed for March at DESY and will allow to measure the pixel efficiency for MuPix6 and test our own telescope setup with 5-6 GeV electrons.

The MuPix7 prototype chip which was submitted in august just arrived and first chips have been bonded and are now under investigation in the laboratory. It introduces a new readout scheme with the state machine, timestamp generator and LVDS drivers integrated on the chip, so the first prototype iteration which incorporates all components of the final chip.

Part V

Appendix

A Additional Plots

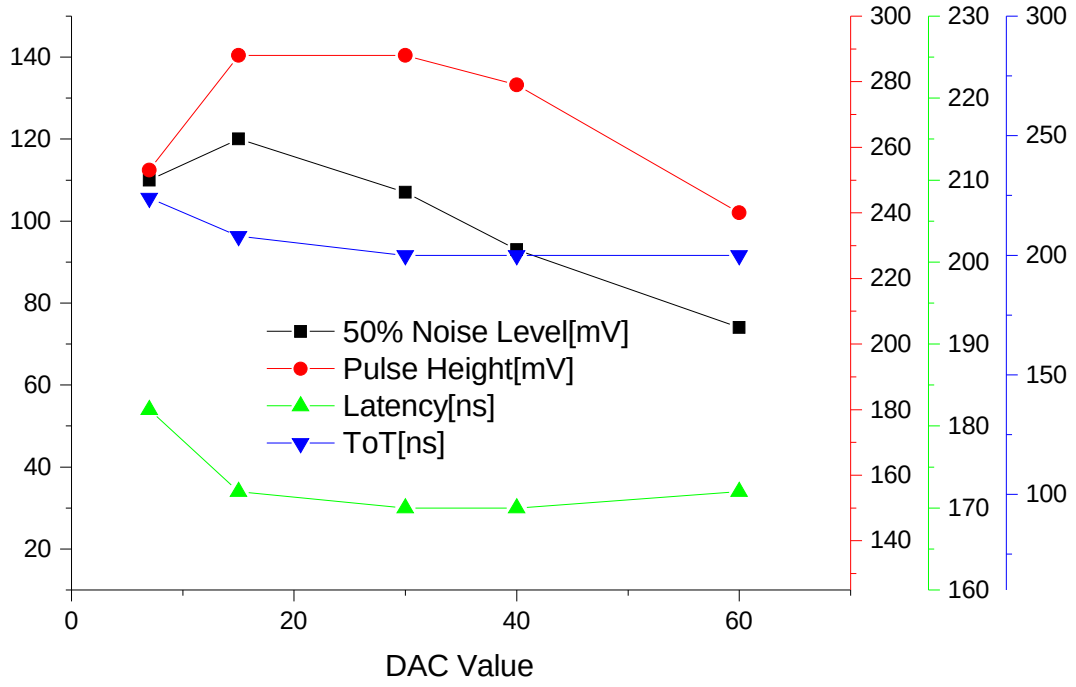


Figure A.1: The influence of the VN DAC setting on the pulse shape parameters.

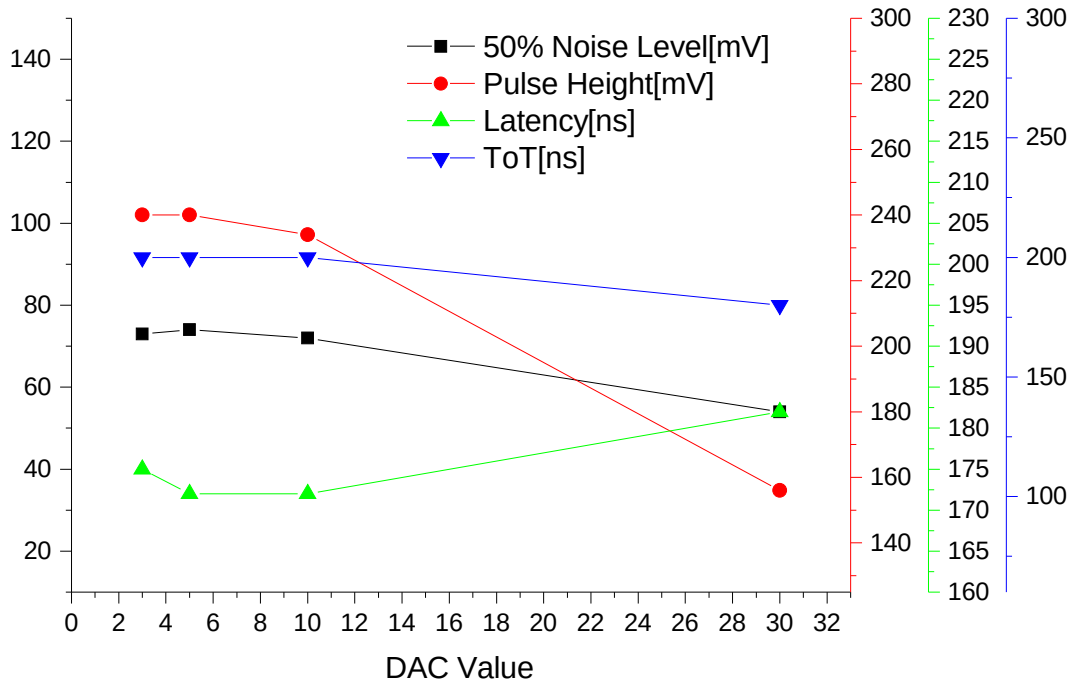


Figure A.2: The influence of the VNLoad DAC setting on the pulse shape parameters.

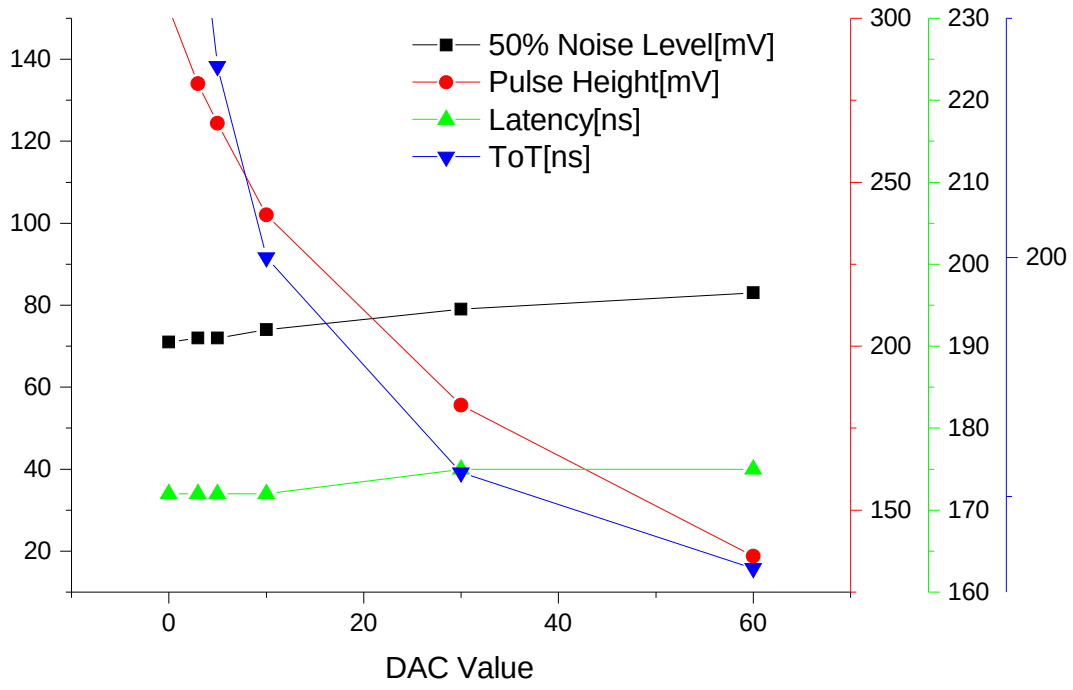


Figure A.3: The influence of the VNFB DAC setting on the pulse shape parameters.

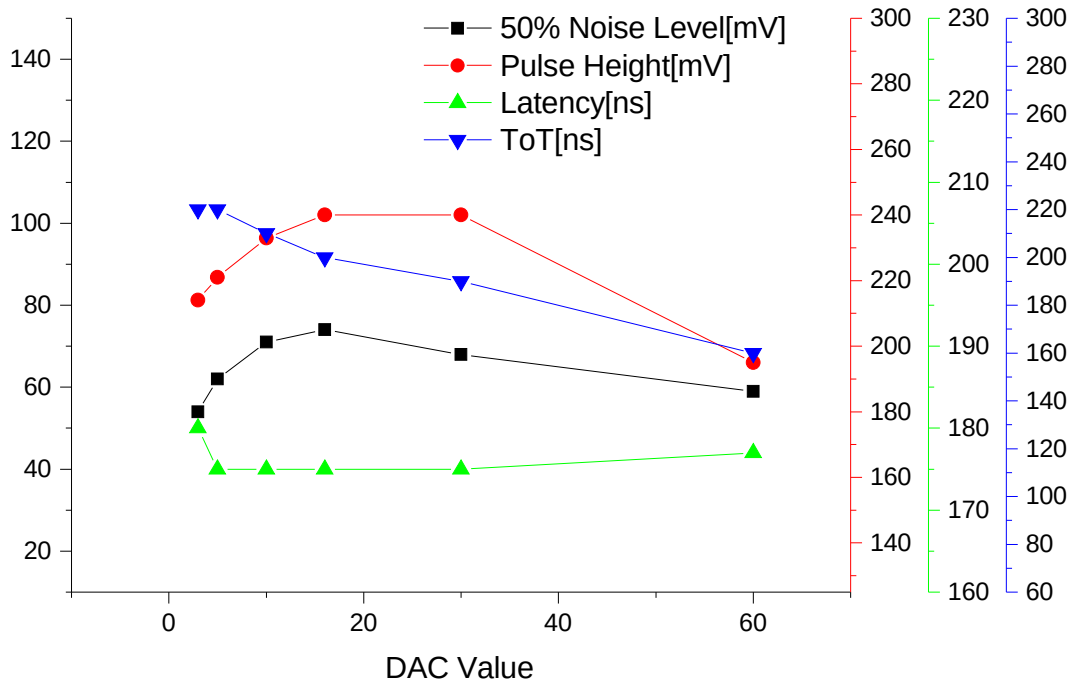


Figure A.4: The influence of the VNFoll DAC setting on the pulse shape parameters.

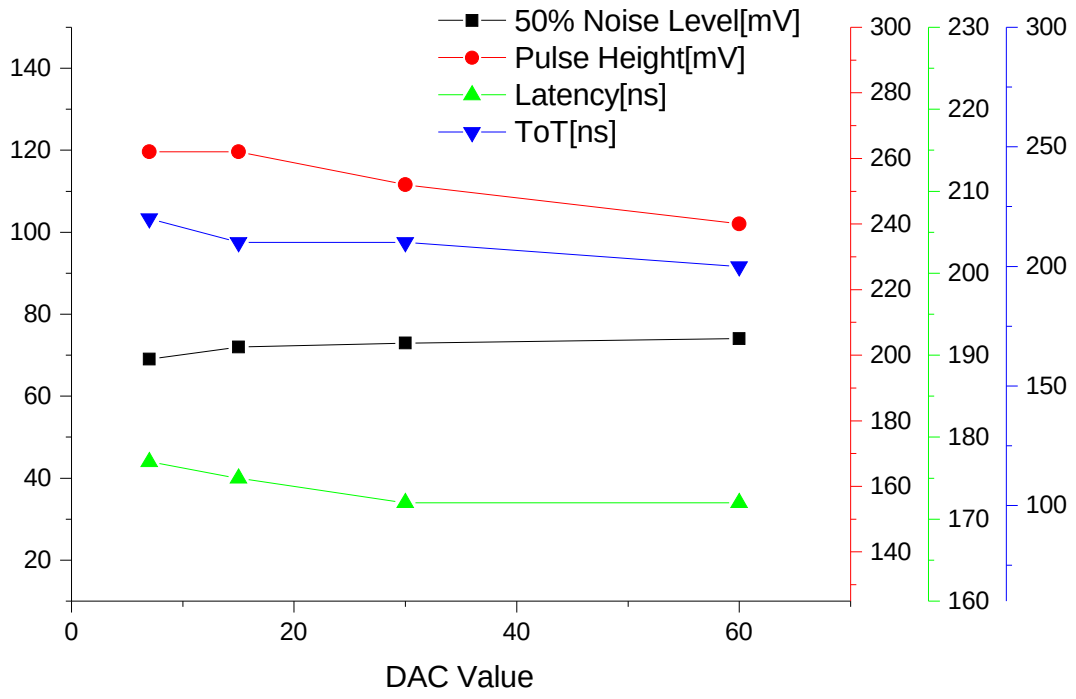


Figure A.5: The influence of the VPComp DAC setting on the pulse shape parameters.

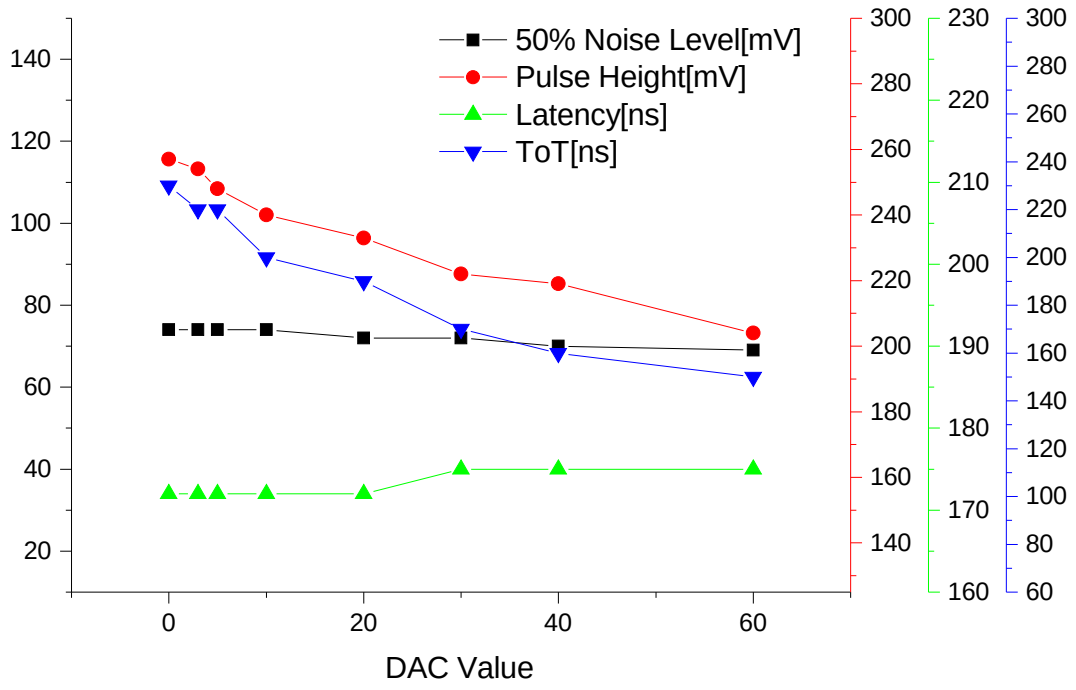


Figure A.6: The influence of the BLRes DAC setting on the pulse shape parameters.

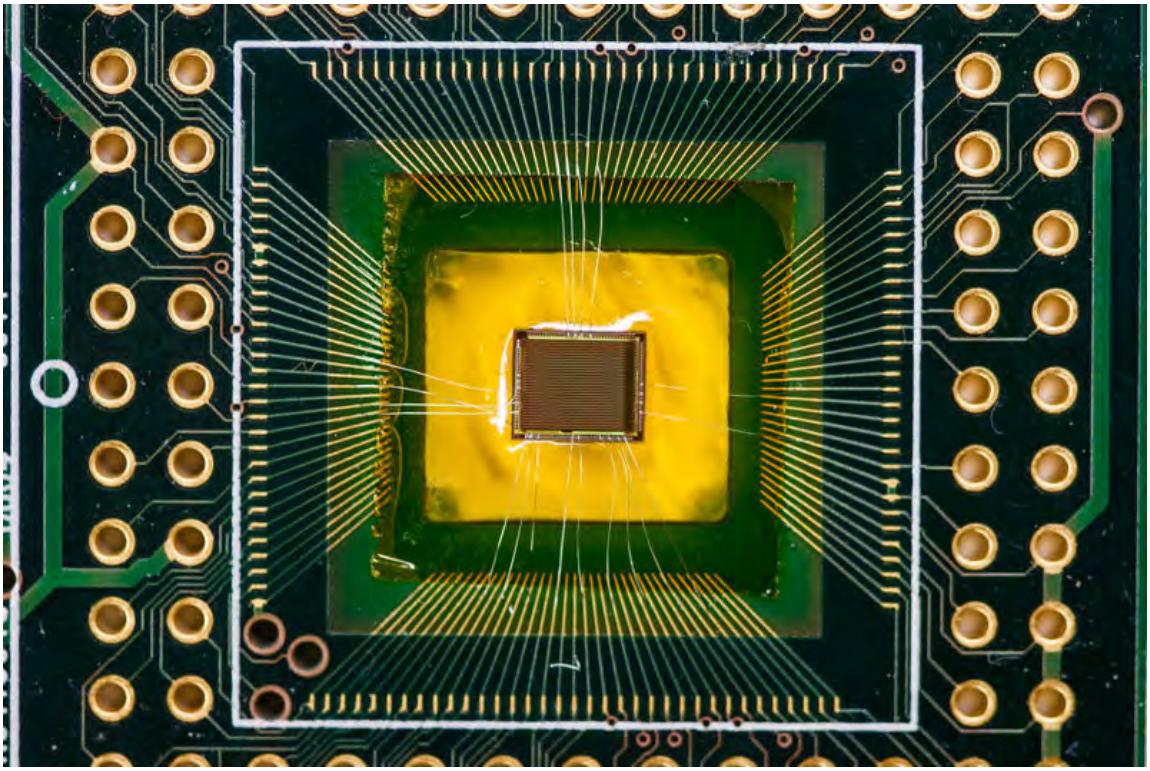


Figure A.7: A prototype glued to a Kapton®-frame for material budget reduction. The so-called Floating-MuPix.

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C Lists

C.1 List of Figures

C.2 List of Tables

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Erklärung

Ich versichere, dass ich diese Arbeit selbstständig verfasst und keine anderen als die angegebenen Quellen und Hilfsmittel benutzt habe.

Heidelberg, den 15. Dezember 2014,

. . . . . .

Formale Überarbeitung und Aktualisierung am 19.06.2015