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submitted by

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Flexprint design and characterization for the Mu3e experiment

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Abstract

The Mu3e experiment searches for the charged lepton flavor violating muon decay $\mu^+ \to e^+e^-e^+$ aiming for a sensitivity of one in 10^{16} decays. In order to observe this strongly suppressed decay within the vast background of non violating decays, the Mu3e detector needs to be very precise in vertex, time and momentum resolution. As the momentum resolution is limited by multiple scattering, the detector is equipped with High Voltage - Monolithic Active Pixel Sensors with very low material budget and an efficiency >99%.
This thesis deals with designing and characterizing trace structures on thin aluminum layers on polyimid, in order to connect the sensor chips. A high data transmission reliability is important.
Two different layouts are designed. One to connect nine sensor chips for data transfer and power supply. It is primarily used for design studies and is not produced yet. The other layout is designed for data trace structure characterization as well as reliability tests of the manufacturing process. Five flexprints based on this layout were produced and then characterized for their electrical behavior. Besides characterization, bit error rate tests were performed successfully at a BER$< 5.5 \cdot 10^{-13}$ at 95% CL with a bit rate of 1250 Mbit/s.

Das Mu3e Experiment sucht nach dem Leptonflavorzahl-verletzenden Myonzerfall $\mu^+ \to e^+e^-e^+$ mit einer Sensitivität von einerm Zerfall aus 10^{16}. Der Mu3e Detektor benötigt eine hohe Impuls- und Zeitauflösung, sowie eine präzise Bestimmung des Zerfallsortes, um diesen Zerfall unter allen anderen Hintergrundzerfällen nachweisen zu können. Da die Auflösung hauptsächlich durch Streuung limitiert ist, wird ein "High Voltage - Monolithic Active Pixel Sensor" eingesetzt, welcher gedünnt einen geringen Beitrag zum Materialbudget leistet und eine effizienz >99% besitzt.
Diese Arbeit beschäftigt sich mit dem Designen und Charakterisieren von Leiterbahnstrukturen in dünnen Aluminiumfolien, welche genutzt werden, um die Sensorchips elektrisch zu verbinden. Entscheidend dabei ist die Zuverlässigkeit der Datenübertragung.
Zu diesem Zweck wurden zwei Layouts erstellt. Das eine soll neun MuPix Chips für Datentransfer sowie Stromversorgung verbinden. Das andere Layout wurde erstellt, um verschiedene Strukturen auf den Flexprints zu testen, sowie um die Zuverlässigkeit des Herstellungsverfahrens zu testen. Hiervon wurden fünf Prototypen hergestellt und auf ihre Datenübertragungscharakteristiken untersucht. Neben Charakterisierungen wurden ebenfalls Bit-Fehlerraten-Tests erfolgreich durchgeführt, mit einem Ergebnis von BER$< 5.5 \cdot 10^{-13}$ bei 95% CL mit einer Bitrate von 1250 Mbit/s.

Contents

1 Mu3e

1.1 Mu3e experiment

The Mu3e experiment is based on the idea of discovering physics beyond the Standard Model. Its target is to observe the charged lepton flavor violating decay $\mu^+ \rightarrow e^+e^-e^+$. In Standard Model with the addition of the theory of neutrino mixing, this decay is highly suppressed at a branching ratio of $<10^{-54}$ [GV13]. Other theories beyond the Standard Model, like for example Super Symmetry, can enhance the observation probability to a measurable level. If this decay cannot be found during operation time, the goal is to set a new upper limit on the branching ratio of $<10^{-16}$ at 95% confidence level (CL) [B$^+$12b]. The current limit was set by the SINDRUM experiment (1983-1986) with a branching ratio of 10^{-12} at 90%CL [B$^+$88]. In order to achieve the aimed sensitivity, a high decay rate with an intense muon beam is needed. The muons are stopped at a target and decay at rest. The highest energy for one of the three resulting particles is approximately $\frac{1}{2}m_\mu c^2 \approx 52\,\mathrm{MeV}$, due to energy and momentum conservation. The most dominant background is the internal conversion decay $\mu^+ \rightarrow e^+e^-e^+\nu_e\bar{\nu_\mu}$. In order to reject the background, by measuring the missing energy which is transferred to the neutrinos, a momentum resolution better than 0.5 MeV/c is necessary. The low momentum of the electrons and positrons results in multiple scattering dominated momentum resolution.
The multiple scattering is mostly Gaussian distributed over the scattering angles, except for 2% of the particles at higher scattering angles. Hence the scattering is measured with its RMS (Root Mean Square) angle θ_{RMS}. According to Molière, this scattering angle depends on the momentum p and the charge z of the scattered particle as well as the radiation length X_0 of the medium [B$^+$12a].

$$\theta_{RMS} = \frac{13{,}6\,\mathrm{MeV}}{\beta cp} z \sqrt{\frac{x}{X_0}}[1 + 0.038 \ln(\frac{x}{X_0})];\ \beta = \frac{v}{c} \tag{1}$$

Therefore the scattering can be reduced by choosing thin materials with long radiation lengths.

1.2 Mu3e detector

The muon beam hits the target in the center of the barrel shaped Mu3e detector (see fig. 1), where the muons stop and decay. The target is a hollow double cone. The muons decay near the target surface. Because of a 1 T solenoid magnetic field and the charge of the particles, the trajectory is curved, which is necessary to determine the momentum [B+13]. First, the particles pass the inner detector layers. The inner detector part consists of two short pixel layer barrels. Close to the two longer outer pixel layers, scintillating fibers enhance the time resolution. Hits in the outer detector layers add important information for momentum determination. At each end of the barrel, there is another pair of outer detector layers to measure the recurring electrons and positrons, which increases momentum resolution [B+12b]. All detector layers are polygonal tubes. They consist of a polyimid support structure, the MuPix chips and the connecting structures. The MuPix chips are overlapping on each kink of the polygon, in order to compensate for in active area e.g. for electrical bonds. The last station are the scintillator tiles, where the electrons and positrons are stopped. This detector component increases the time resolution significant.

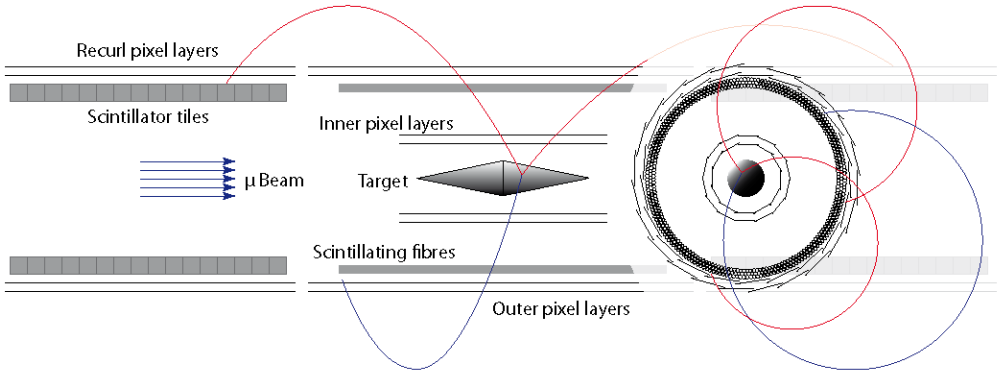


Figure 1: Mu3e detector sketch

1.3 MuPix

The MuPix is a High Voltage - Monolithic Active Pixel Sensor (HV-MAPS) chip. The HV-MAPS design of the pixels (see sketch in fig. 2) leads to a low profile chip with a small material budget. It consists of a p-doped substrate and an N-well, which act as a diode. Particles can be detected from electron-hole-pairs in the depletion zone. The approximately 10 µm thick depletion is created by applying a reverse bias High Voltage (HV), which makes the depletion zone more efficient by faster charge collection. Inside the N-well, the first part of the readout logic is implemented. Instead of an electrical bonding solution as commonly used in hybrid pixel detectors, this saves material. It can be thinned down to 50 µm. The final chip is under development. But expected dimensions and requirements are roughly know. A preliminary chip design for the final chip exists, which is the basis for the following layout studies.

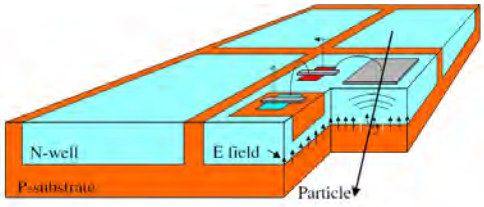


Figure 2: Sketch of a High Voltage-Monolithic Active Pixel [Per07]

2 Flexprints

The MuPix pixel chip is designed with a low material budget, but the chips still need to be connected for readout and power. One pixel layer, including support structures and connections, has to have a thickness to radiation length ratio of $\frac{x}{X_0} \leq 0.1\%$ to achieve the required momentum resolution. For this reason and to add as little material as possible, flexprints are used for data and power connections. Flexprints are high density circuits which are flexible because of the small thickness. But flexibility is not needed for these connections. Current technologies allow for flexible circuits with a material budget of about $0.05\,\% X_0$ using thin aluminum layers, fulfilling the requirements for Mu3e. A small structure size is important to get a high number of data traces on the flexprint with a minimum amount of layers. Data is transmitted with Low Voltage Differential Signaling (LVDS) for high speed signal transmission over longer distances up to 20 cm. Differential signaling needs two traces for each data line but saves more material, because no shielding material between traces is needed in order to reduce crosstalk. Most external distortions are induced as common mode on both traces of the differential pair. In the receiver, ideally every common mode signal is rejected and the differential signal stays undisturbed [Ins12]. All flexprints, designed for this thesis, are designed for differential signaling and to fit the manufacturing process (see chapter 2.1).

2.1 Manufacturing process and SpTAB technology of LTU

Up to now, most flexprint vendors use copper as conductor material. For the reason of radiation length, aluminum is prefered for the Mu3e experiment. The company LTU, located in the Ukraine [LTU13], is capable of producing flexprints with aluminum electrical layers and a reasonable structure size.
In case of the prototypes produced for Mu3e, the starting point is an approximately 14 µm thin aluminum foil. A layer of polyimid is used as a carrier as well as an insulator. From this, cutouts and trace separations in the aluminum and the polyimid are done by photolithographic etching. The photomasks for this purpose can be produced with a 7 µm grid. The minimal structure size is around 60 µm. After etching, two electrical layers with a isolating layer in between are glued together. In order to connect the electrical layers, a method called Single point Tape Automated Bonding (SpTAB) [aC14] is used for vias. As it can be seen in figure 3 there is a cutout in the polyimid layer at the bond spot. This allows to bend a short part of the aluminum trace down to make the contact to the bottom layer. To avoid

breaking the trace during bending the cutout has to be large enough to keep the bending angles as low as possible. For the purpose of the test structure flexprint (chapter 2.4), the length of the cutout is 203 µm. The width of the trace is 63 µm and the cutout width is 154 µm. With the same technique it is possible to bond from the bottom layer to another metal surface, for example a bond pad of a PCB or a MuPix.

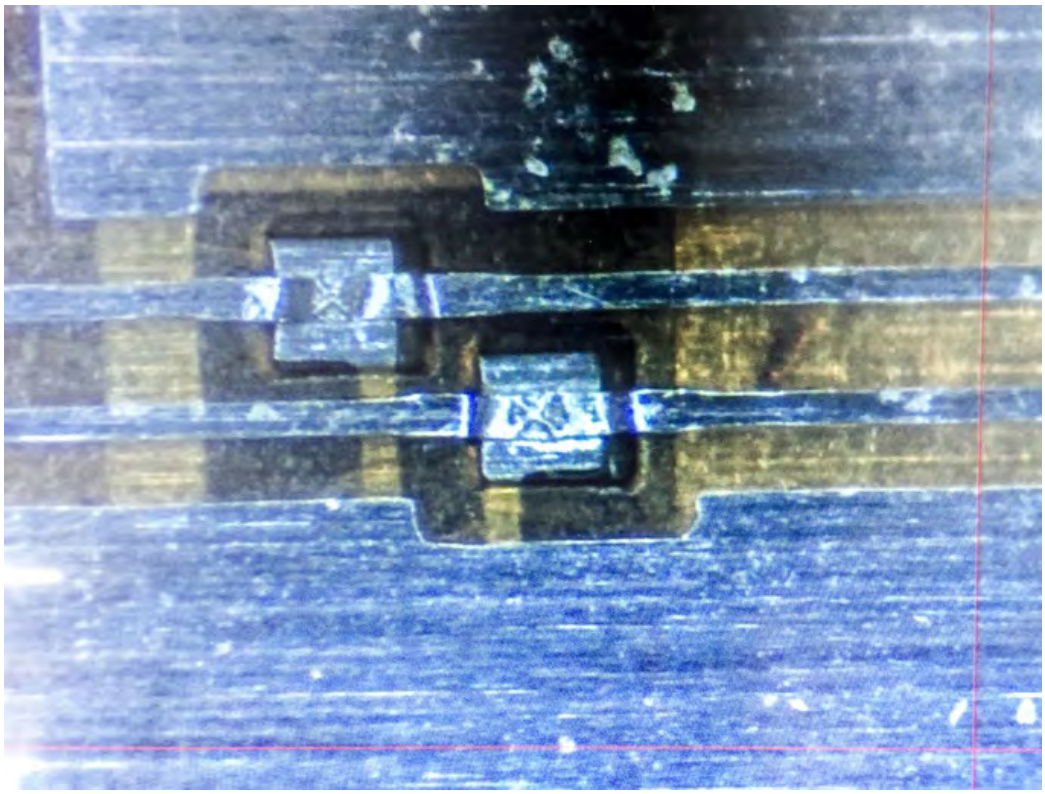


Figure 3: SpTAB connecting the top and bottom layer

2.2 Flexprint for inner detector layers

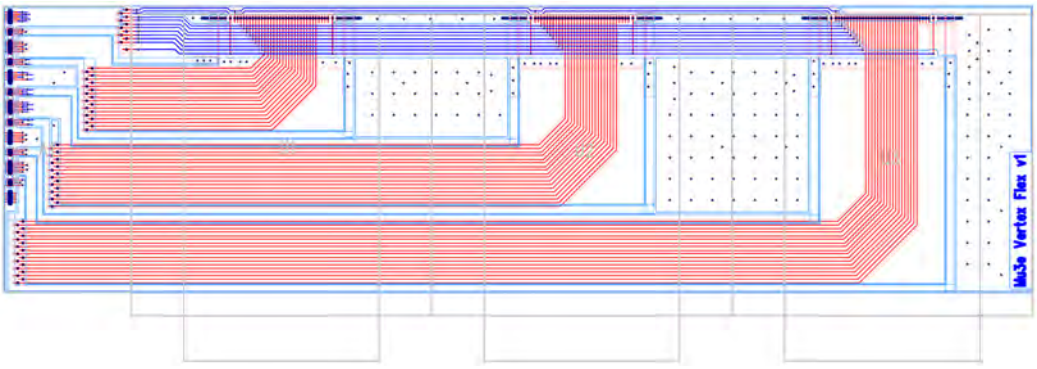


Figure 4: Flexprint layout for inner detector layers for design studies with LTU technology [B+16]. Red is the bottom layer and blue the top layer. Only outlines of the power lines on the top layer visible. Separated layers in fig. 32.

The inner detector layers were chosen for an initial flexprint layout study (fig. 4) using the LTU technology [B+16]. This layout has been taken as a reference for the two following flexprint layout (chap. 2.3, chap. 2.4), but is not designed with all of LTUs requested design rules. The inner flexprint connects only 3 MuPix. The connection to the MuPix chips is on the top edge of the flexprint. On the left edge, there is the connection to a readout Printed Circuit Board (PCB). The flexprint consists of two electrical layers. On these layers, there are traces for data transmission between the chips and the PCB. Some of them are needed for a high data throughput, in order to handle the high hit rates on the inner layers. Others are not essential for the final setup but are needed for better chip control and error analysis during chip testing. Hence, the flexprint has a high density of data traces, which are partially differential and partially single trace routed. Most of the traces are routed on the bottom layer, where the chip will be mounted on. Bus traces located on the top layer are crossing the other traces on the bottom layer and distribute common signals, e.g. a reference clock. Buses are used to reduce the total amount of traces. If every chip needs the same signal, for example a clock, it is convenient to use a bus trace. The flexprints do not only serve for data transmission, they also supply power to the chips. Four power connection pads are foreseen on the chips connection footprint. The preliminary pad layout is based on the current demands for MuPix connections. The routing of the power traces considers the impedance control

of the data traces. A homogeneous conducting and dielectric environment leads to good impedance control. Hence the power lines have been routed like a metal plane over the data traces on the top layer.

2.3 Flexprint for outer detector layers

A stave for the outer detector layers consists of 18 MuPix in a row. They all need to be connected to two PCB at both end of the stave. The staves are electrically divided into half staves. Thus, nine MuPix are connected at each end of one stave. Therefore, the flexprint for the outer layer has to provide the data traces and power for nine MuPix.
The same MuPix connector pad footprint as for the inner detector layers was used. This flexprint layout also consists of two electrical layers, using the manufacturing process guidelines of LTU. As the same sensors will be used in the inner and outer detector layers, the flexprint should also have a similar width as the inner detector layer flexprints. Due to the fact that already on the inner detector layer flexprints the data traces are very dense, it is impossible to fit three times as many traces on the flexprint in order to connect three times as many MuPix with the same number of traces. The solution to this is to reduce the number of data and bus traces to a minimum. This contains a bus structure of differential trace pairs for a clock signal, reset signal and for a data input to program the MuPix as well as a single trace for high voltage. Due to the lower expected hit occupancy, only one serial link per chip is required. For all differential signals the impedance needs to be $100\,\Omega \pm 10\,\%$ to reduce reflection at the transition to the $100\,\Omega$ termination resistor. With the help of the software "Saturn PCB Design, Inc. - PCB Toolkit V6.88" [SPD16] as well as the software "HyperLynx" from the Mentor Graphics PADS 9.3 [Cor16] for crosscheck, the trace width as well as the gap between the two differential traces have been determined. Because of the photomask grid of 7 µm, a trace width W (conductor width) of 63 µm has been chosen. To match the differential impedance, the gap S (conductor spacing) between both traces of the differential pair has been set to 133 µm. In order to reduce crosstalk, it is helpful to choose a distance between two differential pairs which is greater than twice the gap. With these assumptions, the total width required for a single differential trace pair can be calculated:

$$w_{\text{differential}} = 2 \cdot W_{\text{single trace}} + S + w_{\text{between diff. pairs}} \tag{2}$$

$$w_{\text{differential}} = 2 \cdot 63\,\mu\text{m} + 133\,\mu\text{m} + 266\,\mu\text{m} \tag{3}$$

$$w_{\text{differential}} = 525\,\mu\text{m}\,. \tag{4}$$

Because bonding from flex to PCB or MuPix always takes place on the bottom layer and every via from top to bottom might influence the trace impedance, the data traces are determined to be routed on the bottom layer. Correspondingly, the bus structure needs to be on the top layer to cross the traces without any interference with as few vias as possible. The width composition in comparison to the total available width of 19 mm can be seen in figure 5. On the bottom the remaining space is used for ground (GND) and on the top for the supply voltages VSSA and VDD. Each voltage has two connection pads for a better voltage distribution and lack of active voltage control on the MuPix chip. VSSA provides 1.5 V for the first stage amplifier and supplies around one third of the total power consumption. VDD provides 1.8 V for the digital components and supplies around two thirds of the total MuPix power consumption. For simplification, the free space on top has been distributed such that VSSA gets a total width of 5 mm and VDD gets 10 mm. The rest is left for layout optimization and can easily be filled with ground in the end.

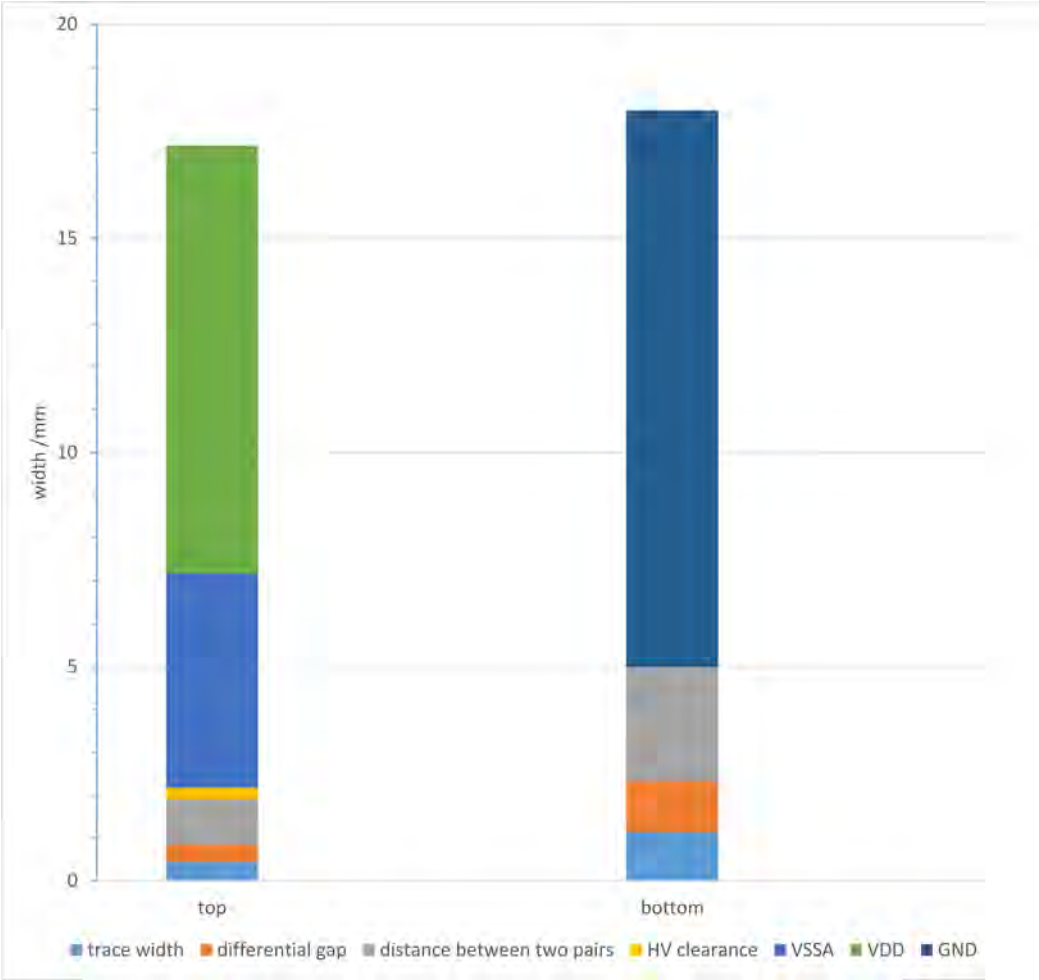


Figure 5: Width composition compared to the total available width for the outer detector layer flexprint.

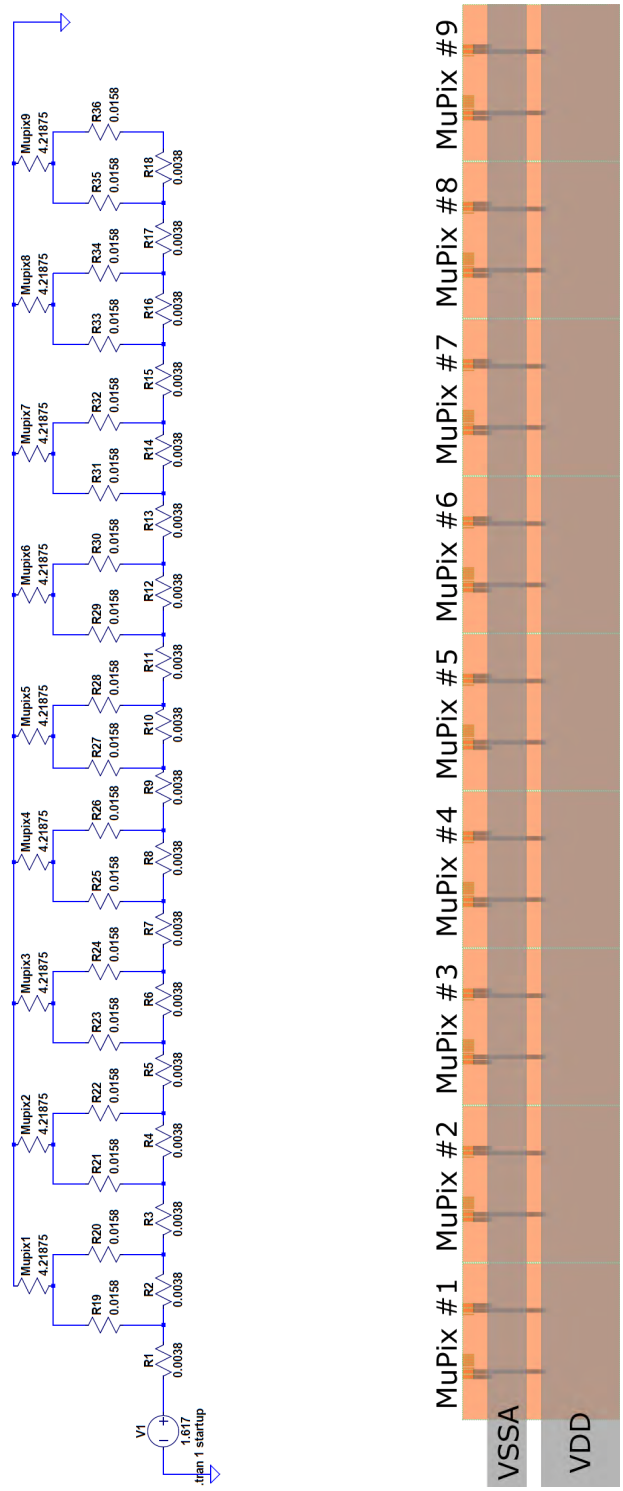
2.3.1 Powerlines for the outer detector layer flexprint

With the first idea of a total width for VSSA and VDD the next question is how to supply the voltages. A voltage tolerance of 20 mV has been given by the MuPix layout designers. In contrary to the voltage difference between the MuPix connectors, the power efficiency has lower priority in the layout design. In case of passive voltage distribution to the MuPix connectors, there are two different options.
The simplest design is to use a thick stripe, going from the left end of the flexprint to the right end. Thin and short stripes go straight up to the connectors as it is shown in figure 6(b).
The second option is to provide every connection with its own power line. In this case it is expected to have lower voltage differences using width variation. For both cases, a model with ohmic resistors has been created and then simulated in the software "LTSpice IV" [Tec16]. Because of the minimal structure size and because the VSSA power line has a the smaller width, the calculations are made first for VSSA and are then scaled up for VDD for this concept.
The MuPix is modeled as an ohmic resistor for following calculations. For the Mu3e experiment, the MuPix is specified with a maximum power consumption of up to $400\,\mathrm{mW\,cm^{-2}}$. Having a MuPix with an area of approximately $2 \times 2\,\mathrm{cm^2}$, it consumes up to 1.6 W. Considering that VSSA provides one third of the power and supplies a voltage of 1.5 V, the MuPix ohmic resistance for VSSA is $R_{\mathrm{MuPix}} = 4.218\,75\,\Omega$. The VSSA connection pad pitch is estimated to nearly 10 mm and the pads are equidistantly oriented to the vertical center line of the MuPix. In order to simulate the voltage drop, the resistance of the power lines is modeled as a series of resistant segments. In case of the first option with the shared power trace, the thick stripe can be divided into segments of same length of 10 mm and same resistance. At the end of each segment, the vertical smaller stripes can also be estimated with equal resistances.

Assuming a regular, real conductor as a resistor, the resistances for the model as shown in the schematic in figure 6(a), have been calculated with:

$$R = \rho_{\mathrm{Al}} \cdot \frac{l}{t \cdot w} \ . \tag{5}$$

In this case, $\rho_{\mathrm{Al}} = 0.0265\,\Omega\,\mathrm{mm^2\,m^{-1}}$ is the specific resistance of aluminum [Wik16a], l is the segment length and thickness times width $t{\cdot}w$ is the conductors cross section [Gia10]. As it can be seen in the schematic in figure 6(a), the resistors R1 to R18 are the resistors of the segments with a value of $0.0038\,\Omega$ and the resistors from R19 to R36 are the resistors for the small



(a) Schematic VSSA

(b) VSSA and VDD design

Figure 6: Shared power line design: MuPix footprint illustrated as orange boxes, four vertical thinner stripes per MuPix in dark gray (two short ones for VSSA and two longer ones for VDD) on bottom layer to avoid shorts between VSSA and VDD when crossing the wider stripes (in light gray).

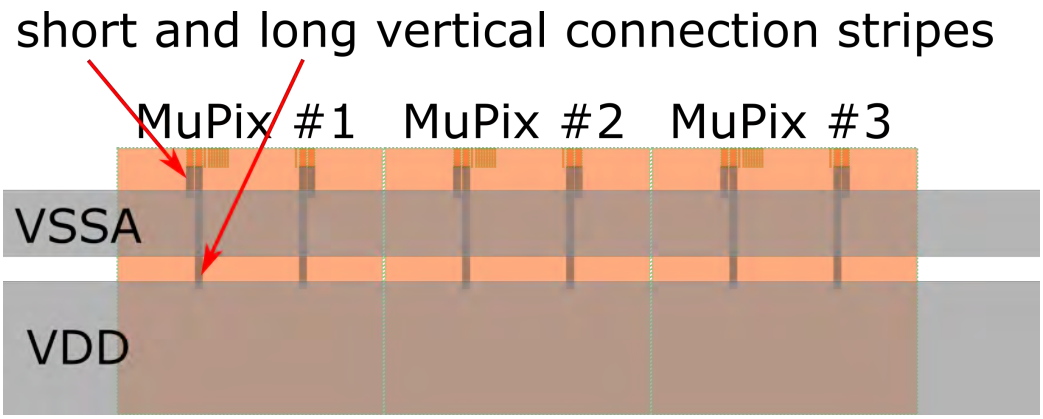


Figure 7: Shared power line design magnified from fig. 6(b)

connection stripes with a value of 0.0158 Ω. The input voltage V1 is set to 1.617 V. From the circuit simulation with LTspice IV, the voltages right in front of the MuPix resistors can be measured against ground. The values are listed in table 1.

MuPix	Voltage
1	1.596 V
2	1.575 V
3	1.557 V
4	1.542 V
5	1.529 V
6	1.519 V
7	1.511 V
8	1.506 V
9	1.503 V

Table 1: VSSA results from LTspice IV simulation for shared power trace schematic (fig. 6(a))

Because every resistor causes a voltage drop, it is not surprising that the largest difference between two voltages is between the first and the last MuPix. The difference here is much higher than the tolerance of 20 mV. Therefore, this is not feasible for the power traces.
The other option is routing separate traces. Separate traces without width variations do not lead to a better result. The idea is to compensate the longer traces with a bigger width. In an ideal situation, a trace that is n

times longer than another trace has to be n times wider so they both have the same resistance. This leads to the same voltage drop meaning that the voltage difference between sensors is zero. With this relation, the width of the shortest power trace can be calculated depending on the total available width for all traces. Again, the estimation that the pitch p between two VSSA connector pads is nearly 10 mm is used. The n-th trace that is connected to the n-th VSSA pad counted from left to right is n times longer than the shortest trace which is only $1 \cdot d$ long. Hence, the n-th trace is also n times wider than the first and shortest power trace which has a width of w. So the total width W_{total} can be calculated as the sum of all widths.

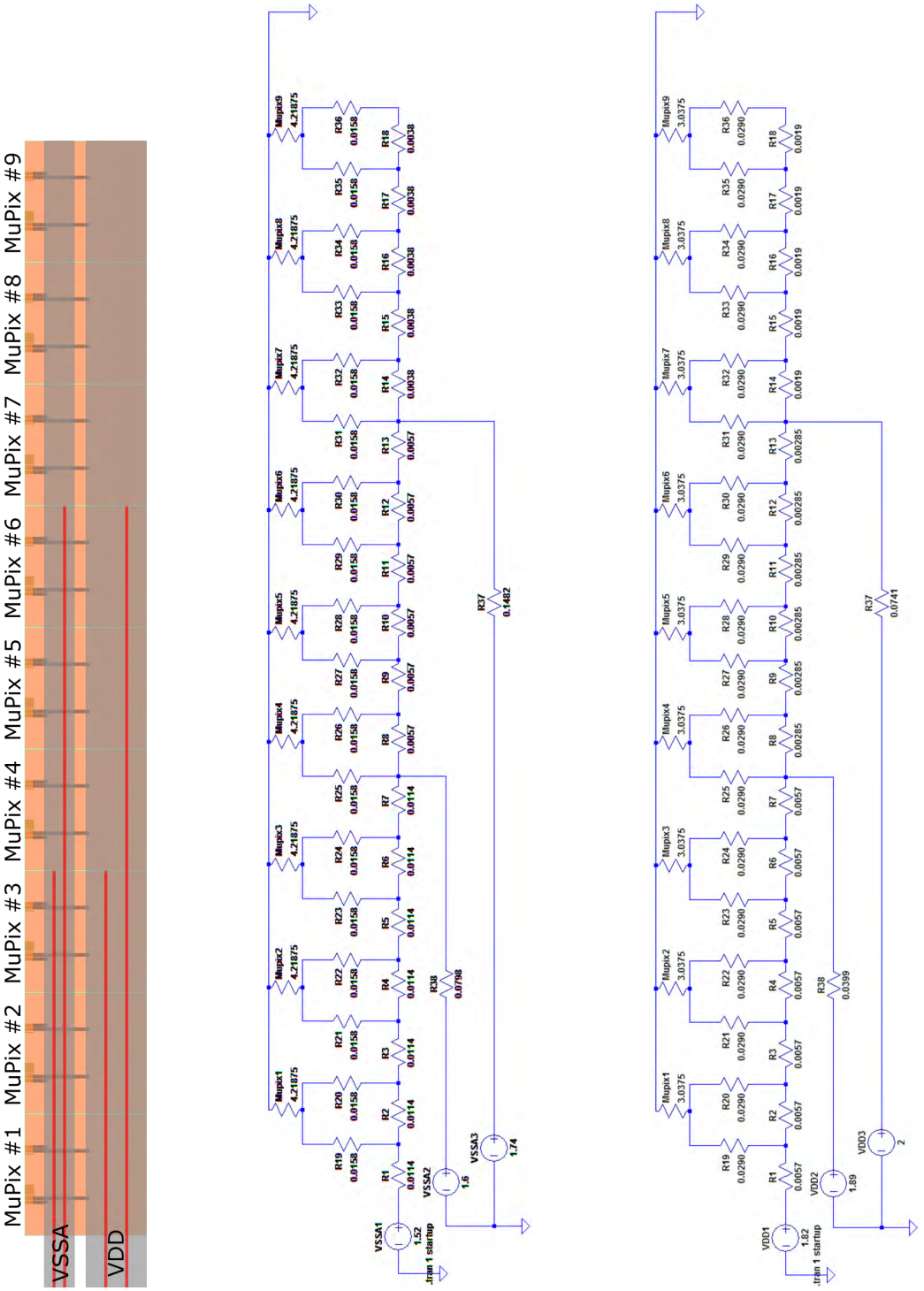
$$W_{\text{total}} = N\,w + (N-1)\,w + (N-2)\,w + ... + 3\,w + 2\,w + w \tag{6}$$

$$\Leftrightarrow W_{\text{total}} = \sum_{n=1}^{N} n\,w \tag{7}$$

$$\Leftrightarrow W_{\text{total}} = \frac{N(N+1)}{2}\,w \tag{8}$$

$$\Leftrightarrow w = \frac{2\,W_{\text{total}}}{N(N+1)} \tag{9}$$

With a total width of $W_{\text{total}} = 5$ mm and a total number of traces of $N = 18$ – for each MuPix two VSSA connections – the first trace has to be 29 µm wide which is less than half of the minimal structure size, without taking any gaps for isolation into account.
With these two models failing, the idea of distributing the voltages passively might be not feasible. But maybe a semi-passive way can be considered before each trace gets its own power regulator for full active voltage control. The idea is to have a mixture of both passive options to use as few as possible different voltages for the power input. This semi-passive design is based on the shared power line, see figure 6(b), with slices to separate the voltages over a certain distance as it can be seen in figure 8(a). The corresponding schematic can be seen in figure 8(b). The power stripe is sliced into three stripes. So the remaining stripes have a third of the whole width and join again after certain lengths. There are three different Voltages VSSA1, VSSA2 and VSSA3. The first voltage is the foundation for the voltage distribution. It is connected to the first stripe which is directly connected to the first three MuPix. After the third MuPix, the second stripe joins the first one and the connected second voltage VSSA2>VSSA1 can than be used to support VSSA1 and compensate the voltage drop. The same idea is used for the third stripe and voltage VSSA3 which joins the other two stripes after they passed the sixth MuPix.



(a) Design idea with slices marked red

(b) VSSA Schematic, needs three different voltages

(c) VDD Schematic, needs three different voltages

Figure 8: Semi passive voltage supply

Again, the according schematic (fig. 8(b)) has been simulated with LTspice IV. The voltages VSSA1= 1.52 V, VSSA2= 1.6 V and VSSA3= 1.74 V have been chosen. The voltages on the MuPix are listed in table 2.

MuPix	**Voltage**
1	1.508 V
2	1.503 V
3	1.505 V
4	1.510 V
5	1.508 V
6	1.508 V
7	1.510 V
8	1.505 V
9	1.503 V

Table 2: VSSA results from LTspice IV simulation for sliced power trace schematic (fig. 8(b)).

Regarding the results from table 2, the biggest voltage difference is approximately 8 mV, which is well below the limit of 20 mV. This layout is also transferred to the VDD dimensions. As it can be seen in figure 8(c) the voltages that are used to get nearly 1.8 V on the outputs are VDD1= 1.82 V, VDD2= 1.89 V and VDD3= 2.0 V. Again, the results from the simulation are satisfying as it can be seen in table 3.

MuPix	**Voltage**
1	1.804 V
2	1.800 V
3	1.802 V
4	1.806 V
5	1.804 V
6	1.804 V
7	1.805 V
8	1.801 V
9	1.799 V

Table 3: VDD results from LTspice IV simulation for sliced power trace schematic (fig. 8(c))

Besides the good voltage control in this layout, the amount of needed voltages is also acceptable. In addition, every current is floating away from the

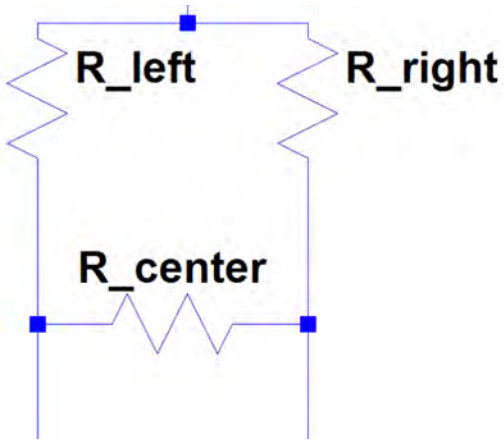


Figure 9: MuPix model with voltage drop between terminals.

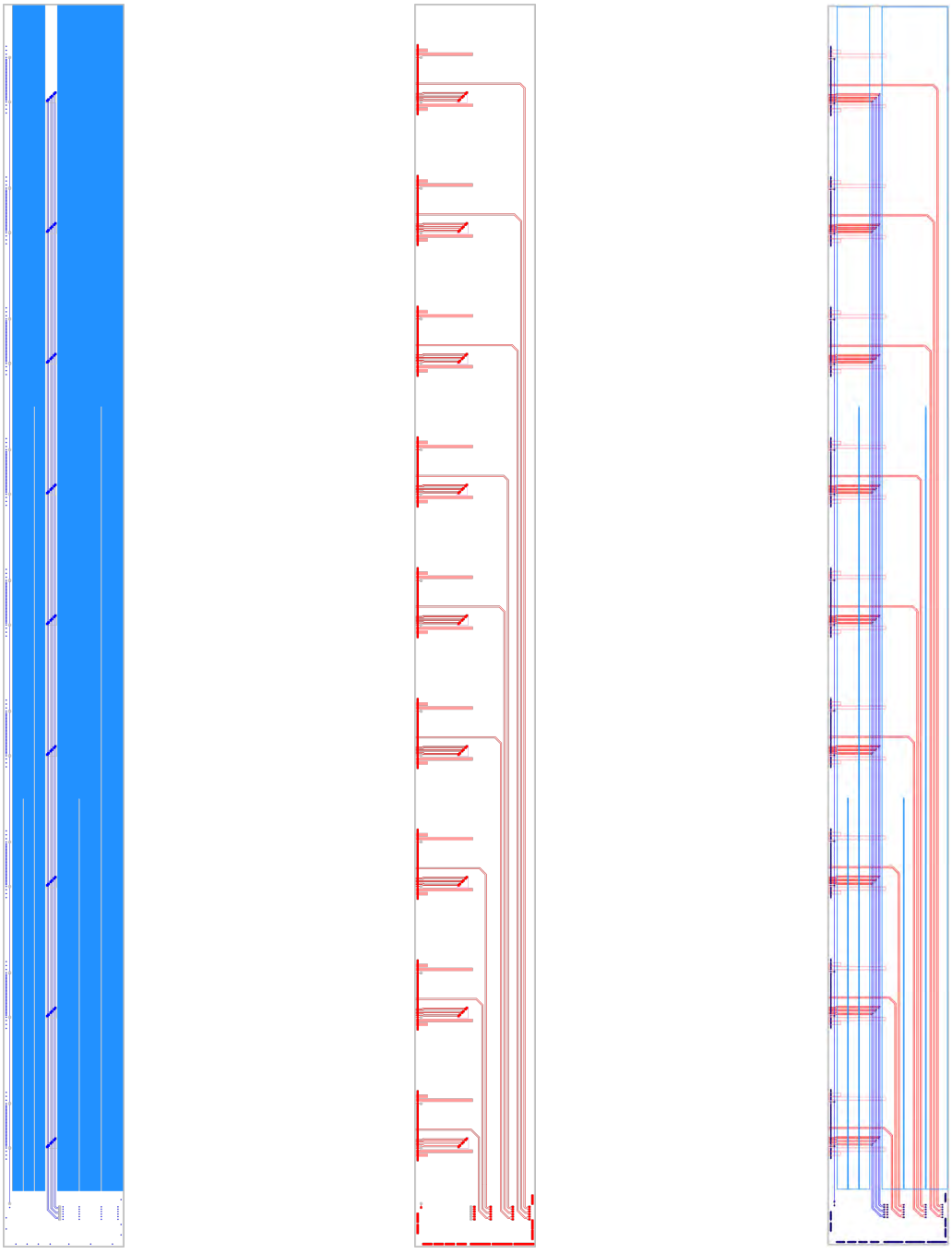
voltage sources. Due to the fact that the data traces get a good impedance control under these wider VDD lines like on the inner detector layer flexprint (chapter 2.2), more slices are counterproductive. More slices reduce the power line width and reduce the homogeneous environment of the data traces.
In fact the MuPix is not an ohmic resistor as it consists of many active components. The model that was chosen is only a estimation at maximum power consumption. This model does not consider a voltage drop in the chip between the two terminals for one voltage supply. Therefore the MuPix is simulated with three ohmic resistors according to the model in figure 9. The two parallel resistors fulfill the dependencies $R_{\text{left}} = R_{\text{right}}$ and $R_{\text{left}} \parallel R_{\text{right}} = R_{\text{MuPix}}$ (R_{MuPix} from previous simulations). The third resistor R_{center} can be estimated as $2\,\Omega$ from measurements on prototype chips. R_{center} can also be estimated from the MuPix layout plans as a aluminum stripe with dimensions $1\,\mu\text{m} \cdot 100\,\mu\text{m} \cdot 1\,\text{cm}$. This leads to a resistance of $2.65\,\Omega$. To take variations into account, the effect of the third resistor is simulated with different values between $50\,\Omega$ and $5\,\text{m}\Omega$. The simulations of the semi-passive power design with this new MuPix model show only small differences to the simulations with the previous MuPix model. The voltage drop between the two terminals of one chip is approximately 1 mV. The largest voltage difference between two of the 18 terminals is 10 mV for VDD and 10 mV for VSSA with optimized supply voltages (VDD1 = 1.81 V, VDD2 = 1.89 V, VDD1 = 1.99 V; VSSA1 = 1.52 V, VSSA2 = 1.60 V, VSSA1 = 1.74 V). These results show, that the voltage difference is still below the tolerance limit.

2.3.2 Layout

The last step is to route all data, power and bus traces from the left edge to the top edge of the flexprint. For routing the software "Pads Layout" and "Pads Router" have been used. The design rules have been set according to the previous sections about the dimensions of the structures. Table 4 shows a summary of the most important design rules. With these design rules the layout that can be seen in figure 10 has been created.

Design rule	**Value**
Trace width	63 µm
Differential gap	133 µm
Gap between copper pours	98 µm
Copper pour to trace	266 µm
Trace to trace	266 µm

Table 4: Design rule summary for the outer detector layer flexprint



(a) Top (b) Bottom (c) Top and bottom combined

Figure 10: Outer detector layer flexprint layout

2.4 Test structure flexprint

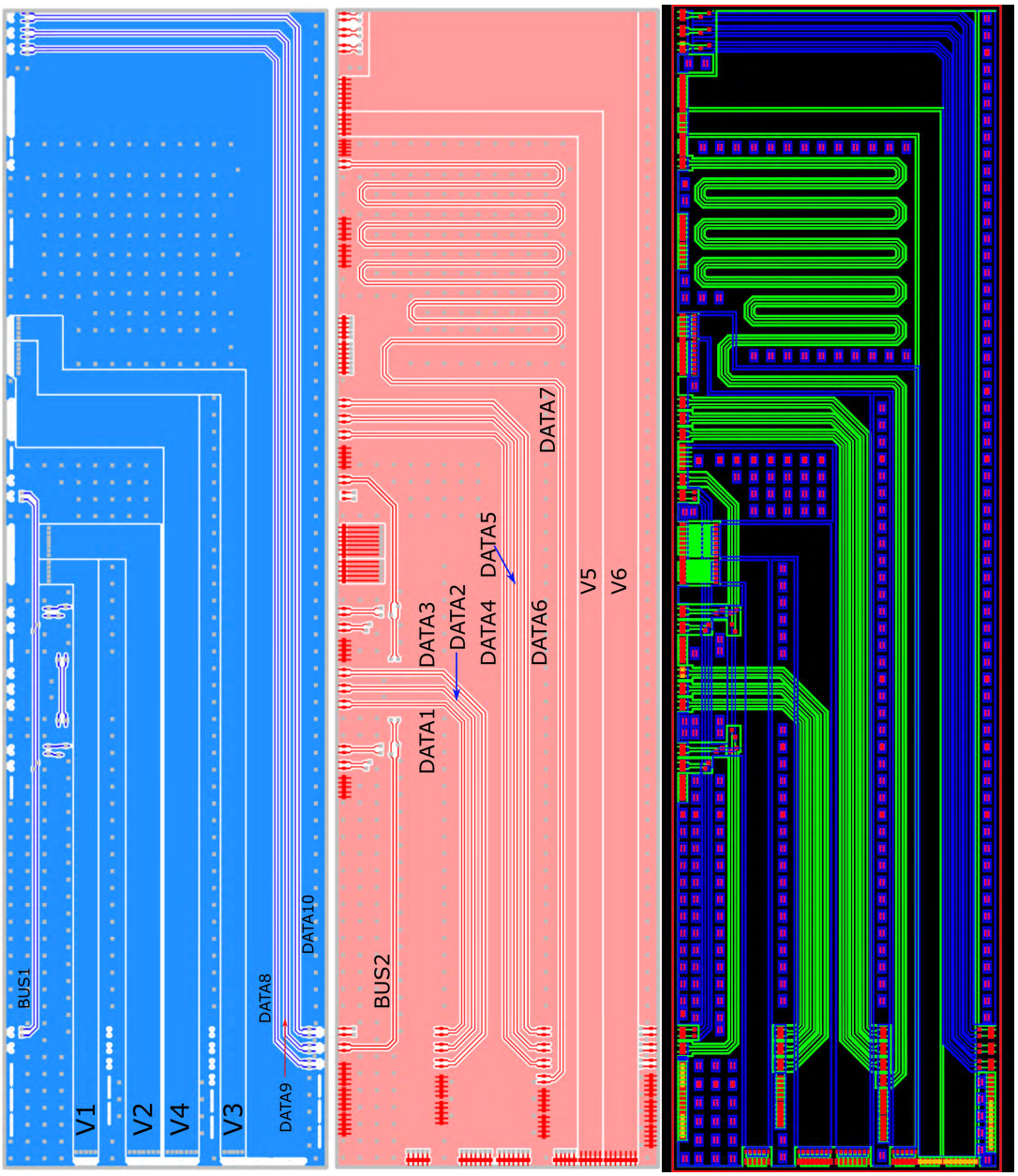
The previous designs rely on idealized parameters, because there is no experience with the LTU technology for flexprints and differential signaling. Therefore, it has to be made sure that the parameters work and match the expectations in the final setup. It is important to know how reliable the flexprints are produced and how the manufacturing processes effect the properties of the flexprint. All this information is necessary to compensate occurring problems beforehand in the final layout for the flexprint. A test structure flexprint is designed to measure the characteristics and capabilities of the LTU flexprints. To avoid several iterations for the inner and outer detector layer flexprint, the test structure flexprint combines features of both.

2.4.1 Layout

The test structure flexprint consists of two electrical layers (see layer stack fig. 11). These two layers contain six power lines, ten differential data traces and two differential traces as a bus structure. The data trace width is 63 µm, same as on the outer detector layer flexprint. The most important part of the flexprints is fast data transmission, which depends on the trace impedance. Besides the ohmic resistance, the impedance is also defined by capacitive and inductive characteristics. They are highly influenced by the dielectric environment. Because of lack of information about the final thickness of the different glue and polyimid layers after the manufacturing process, the impedance is one of the most important parameters. For impedance variety for the test, the ten data traces on the test structure flexprint are grouped into three triples and one separate differential trace. In each triplet the traces have very similar properties, except for the gap between the single traces of each differential pair. The gap size is oriented on the outer detector layer flexprint and varies from this base by nearly ±20%. The gap values are shown in table 5. The different gaps lead to different differential impedances. The distance between two differential traces is at least 350 µm. The data triplets can also be used to measure crosstalk between data traces. For worst case impedance tests, the first triplet also crosses a bus structure of two differential traces. Both bus traces are running differentially with a gap of 133 µm and a trace width of 63 µm. The first bus trace is on the bottom layer and changes to the top layer to cross the data traces and avoid shorts. The second bus trace is routed mainly on the top layer. Because every transition is realized with LTUs SpTAB vias, the difference between the signal transmission of both bus traces gives information about the quality of the vias. Not only one bus trace but also the third data triplet is on the top layer in order to see

Figure 11: Layer stack of the test structure flexprint (Al=aluminum, PI=polyimid)

how well the traces perform with a different dielectric environment. In order to see if long data traces, as they are required for the outer detector layer flexprints, are feasible, a long trace (DATA7) is realized. The theoretical impedances of all data traces can be extracted from table 5. These values are approximations with a glue and polyimid environment on both sides with an estimated average dielectricity of $\epsilon_r = 3.4$.
The second important parameter is the resistance of the power lines. For this reason there are a variety of different widths and lengths of power lines on the top and bottom layer. According to equation 5, the only unknown parameter is the true thickness of the aluminum layers. This gives information about material losses during the manufacturing process. The power lines are also important for impedance control for precise parameter determination. Therefore they are distributed, such that the data traces are not influenced by material or electric potential changes from the opposite layer. The flexprint layout, created with these features, can be seen in figure 12. This layout has been translated by LTU to a layout compatible with the photomasks (fig. 12(c)), that are needed for the manufacturing process.



(a) Top (b) Bottom (c) Top and bottom combined, LTU photo mask

Figure 12: Test structure flexprint layout

DATA	Layer	Gap between differential pair	Expected diff. impedance ($\epsilon_r = 3.4$)	Single trace length
1	bottom	112 µm	108 Ω	28 mm
2	bottom	133 µm	110 Ω	30 mm
3	bottom	154 µm	112 Ω	30 mm
4	bottom	112 µm	108 Ω	49 mm
5	bottom	133 µm	110 Ω	49 mm
6	bottom	154 µm	112 Ω	48 mm
7	bottom	133 µm	110 Ω	175 mm
8	top	112 µm	121 Ω	79 mm
9	top	133 µm	123 Ω	79 mm
10	top	154 µm	125 Ω	79 mm

Table 5: Specification overview of data traces according to the layer stack fig. 11; triples: DATA$\{1,2,3\}\{4,5,6\}\{8,9,10\}$; DATA7 represents long traces from the outer detector layer flexprint layout

3 Flexprint to SMA connector adapter PCB

A PCB test board is developed to which the flexprint is bonded. In order to characterize the test flexprint, SMA (SubMiniature version A) connectors have been chosen because all tools, that have been available in the laboratory, can be connected via high speed SMA to SMA coaxial cables that are rated with 50 Ω single trace impedance. Used as a pair, it yields a differential impedance of 100 Ω. The traces on the PCB are designed to match the 100 Ω impedance.
Four-terminal sensing achieves accurate resistance measurements, thus every single power line on the flexprint is connected with four traces to pin connectors [Wik16b]. The adapter PCB carries 56 SMA connectors and 32 pin connectors (four for ground). In order to save space and reduce error sources on the PCB, the PCB has been designed with six electrical layers. The top and bottom layer are used for differential traces and two middle layers are used for power traces. The two layers between the power trace layers and top and bottom are used for ground and shielding. The final layout is shown in figure 13. On the top layer there are five areas free of solder mask, similar texture to the bond pads for the flexprint. They provide test areas for bonding tests, to find the right settings for solid bonds. These areas can be easily seen on the final product (fig. 14).

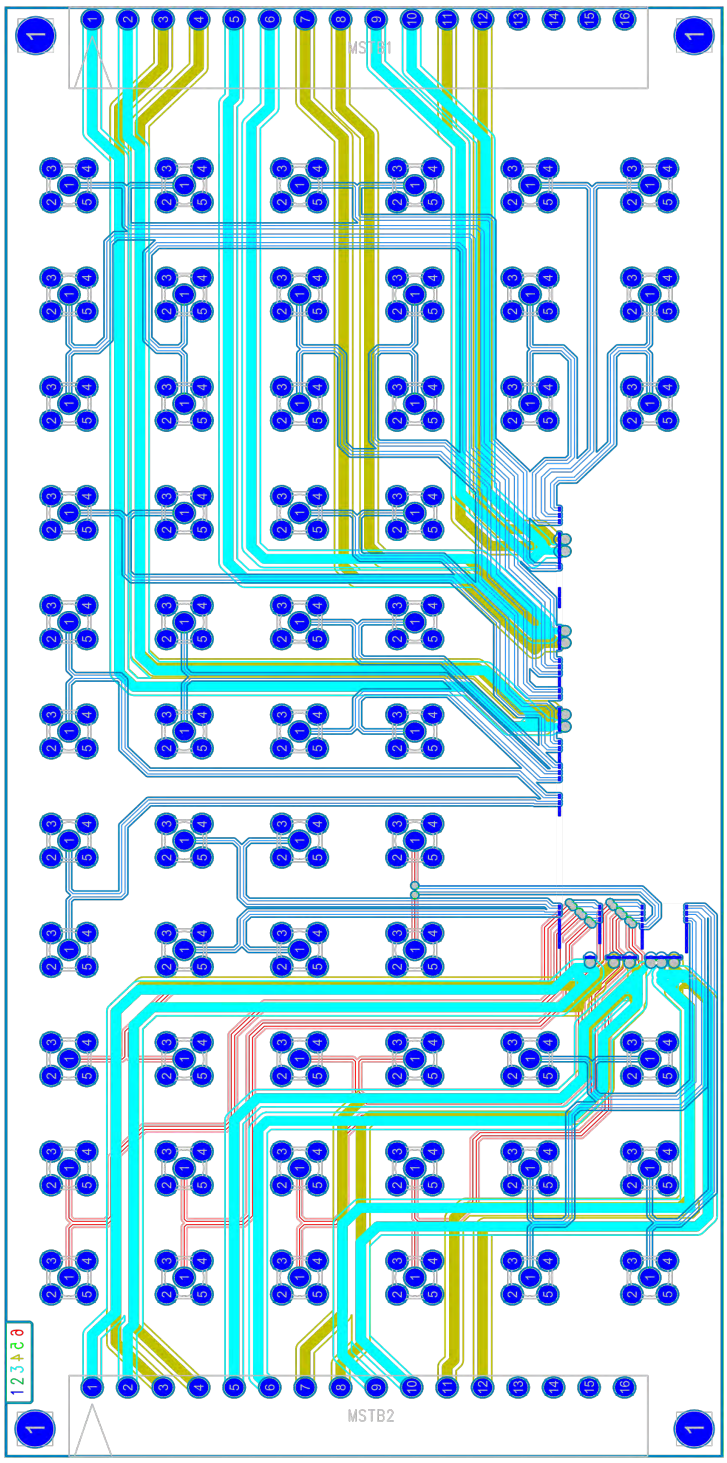


Figure 13: Adapter PCB layout, all layers stacked, flooded and separated in appendix fig. 34, 35, 36, 37.

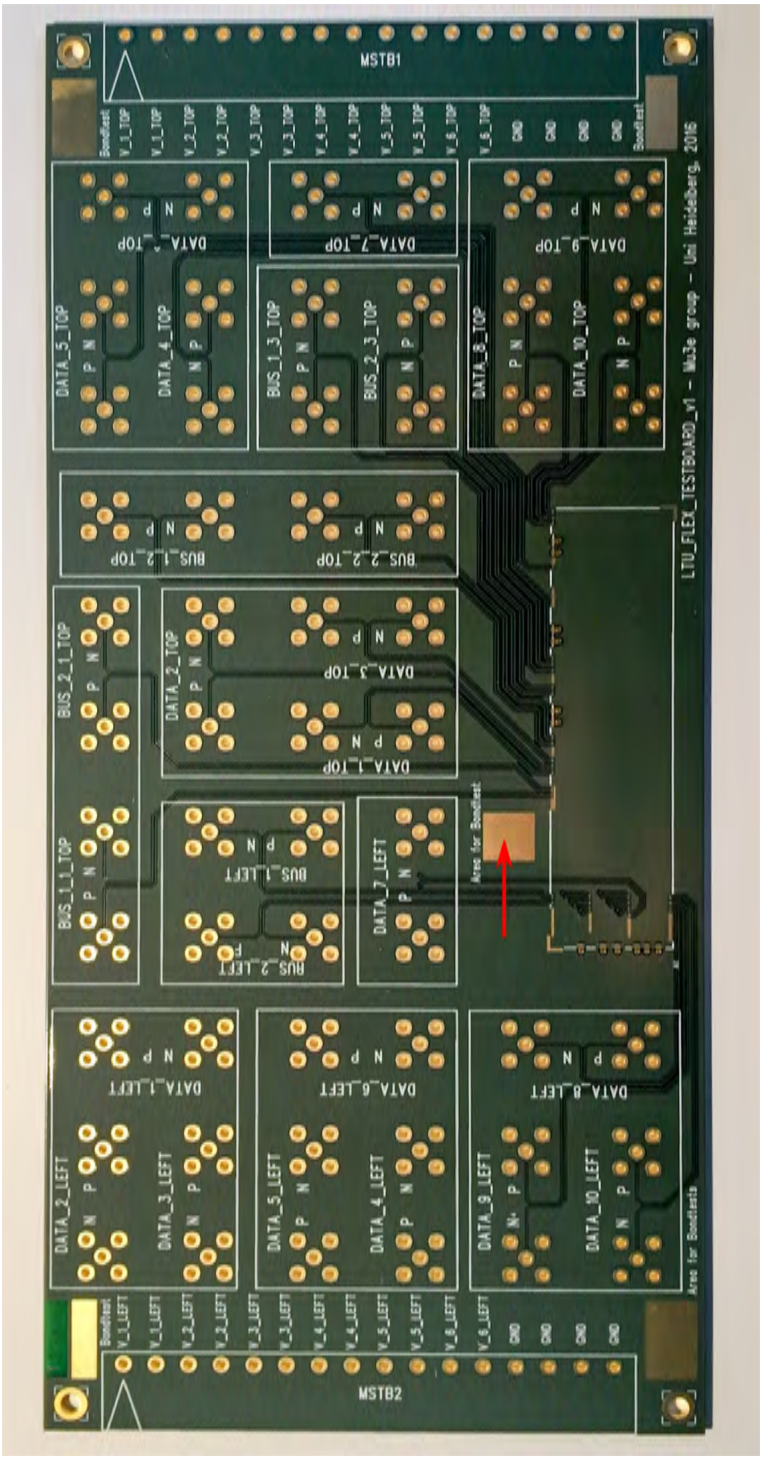


Figure 14: Adapter PCB not assembled, Area for Bondtest marked with a red arrow.

4 Measurements and characterization of the structure test flexprint

LTU bonded five prototype flexprints to the adapter PCBs. The SMA and pin connector assembling is done in the laboratories in Heidelberg. The complete assembled board can be seen in figure 15. The first three of the following subsections are concerning the power line measurements of their ohmic and heat resistance as well as their isolation. The remaining subsections concentrate on the characteristics of the data traces, including the impedance measurement with Time Domain Reflectometry as well as Eye-Diagrams and transmission spectra. Bit error rate tests are also conducted as well as the clock transmission over the bus structure.

Figure 15: Adapter PCB assembled with 4x8 pin connectors, 56 SMA connectors and the flexprint covered with polyimid foil for protection during soldering.

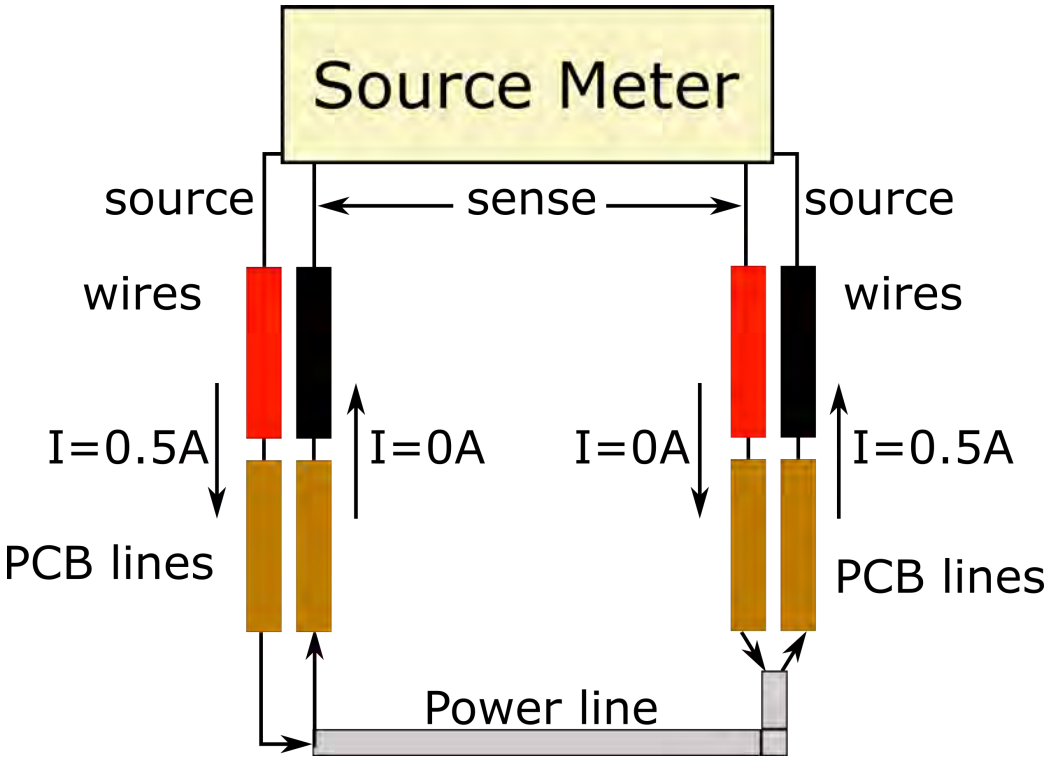


Figure 16: Four-terminal sensing setup

4.1 Power line resistances

The resistance measurement of the power lines have been conducted, in order to evaluate the material loss in the layer thickness during the manufacturing process. A Keithley 2611B SourceMeter [KI13] has been used for four-terminal sensing. Four-terminal sensing is chosen to minimize the influence of the connecting wires. Two wires are connected to both ends of each line. One of each is connected with a current source and the other one with a high impedance voltage meter (see fig. 16). There is nearly no current on the sense wires and therefore no losses from wiring and connections. Knowing the current and the voltage drop over the resistor, the resistance can be calculated applying Ohm's law.
The current has been set to 0.5 A and the voltage limit to 5 V. Besides the resistance, the exact current, the voltage and the power have been measured, too. The complete set of all measured quantities can be found in table 10 in the appendix. The most important information here is the resistance. The other values are mostly for crosschecking any unexpected results.

For evaluation, the following assumptions are used: The thickness t is a constant over all power lines. The power lines are modeled as normal resistors, with the specific resistance of aluminum $\rho_{Al} = 0.0265\,\Omega\,\mathrm{mm}^2\,\mathrm{m}^{-1}$ [Wik16a], using equation 5. As none of the power lines is a straight conductor, the ratio l/w can not be simply determined. Shapes and dimensions of the power lines can be seen in figure 17. In order to find the dimensions of an equivalent straight line, the power lines have been divided into straight segments. Each segment can be assigned with a length l_i and a width w_i. The dimensions of the horizontal and vertical segments are given by their rectangular shape. The length of a corner segment is calculated applying the Pythagorean theorem of the half widths $w_A/2$ and $w_C/2$ of the neighboring vertical and horizontal generic segments A and C (transition stage 1 to stage 2 in figure 18).

$$l_{corner} = l_B = \sqrt{\left(\frac{w_A}{2}\right)^2 + \left(\frac{w_C}{2}\right)^2} \tag{10}$$

The width is estimated with the mean of the neighboring straight segments widths.

$$w_{corner} = w_B = \frac{w_A + w_C}{2} \tag{11}$$

The equivalent resistance of a straight conductor is estimated as the sum of all of these segment resistances R_i (stage 3 in fig. 18). The measured resistances can be associated with this equivalent calculated resistor and therefore with its equivalent ratio of length and width (see eq. 14).

$$R = \sum_i R_i \tag{12}$$

$$R = \rho_{Al} \cdot \frac{1}{t} \cdot \sum_i \frac{l_i}{w_i} \tag{13}$$

$$R = \rho_{Al} \cdot \frac{1}{t} \cdot \left(\frac{l}{w}\right)_{equivalent} \tag{14}$$

The error of the equivalent ratio is calculated with Gaussian error propagation. The length and width of each segment is measured manually in graphics software from the photomask layout in figure 12(c). This is done because the photomask is the exact model for the physical flexprint. The scale is calibrated with known structure dimensions like the trace width. Considering the grid of the photomask is 7 µm, the error for every measured length and width is estimated freely as 10 µm for the Gaussian error propagation of the ratio l/w.
In order to calculate the thickness of the aluminum layers, the equivalent

ratios are plotted against the measured resistances (fig. 19). A χ^2 -fit of equation 15 is performed for each flexprint (see different colors in fig. 19).

$$\left(\frac{l}{w}\right)_{equivalent} = (R - R_0) \cdot \frac{t}{\rho_{Al}} \tag{15}$$

An offset R_0 is added to the fit function in order to consider the parasitic resistance from the transition from four to two traces (four-terminal sensing) on the PCB and to take the resistance of the bonds into account. Compared to equation 14, the dependence is interchanged, because the software used for the χ^2 -fit considers only the error margin of the ordinate. The error of the ratio l/w is much higher than the error of the Resistance measurement. Hence the more significant error margin $\Delta l/w$ is oriented in y-direction. The slope of the liner fit equals the ratio t/ρ_{Al}. The resulting thicknesses are listed in table 6.

Flexprint	**Thickness**
1	$12.22\,\mu m \pm 0.58\,\mu m$
2	$12.24\,\mu m \pm 0.58\,\mu m$
3	$12.30\,\mu m \pm 0.61\,\mu m$
4	$12.40\,\mu m \pm 0.64\,\mu m$
5	$12.27\,\mu m \pm 0.61\,\mu m$

Table 6: Thickness determination from the linear fits in fig. 19.

The results from the fit show, that the determined thickness (avg. $12.29\,\mu m \pm 0.27\,\mu m$) is less than the expected $14\,\mu m$. As the thickness loss is much higher than what is expected from spontaneous oxidiation ($< 100\,nm$) [J+02], it is most likely caused by the etching during the production of the layers and the cutouts.
Concerning the fit quality, it should be noted, that the χ^2 is in the range of $12.1 < \chi^2 < 14.4$. On the one hand, resistance measurement is a very precise measurement, caused by the four-terminal sensing and the high sensitive source meter. But on the other hand, the errors of the model are under estimated. The error margins consider the errors from the dimension determination, but the model, especially for the corner segments, is a rough estimation.

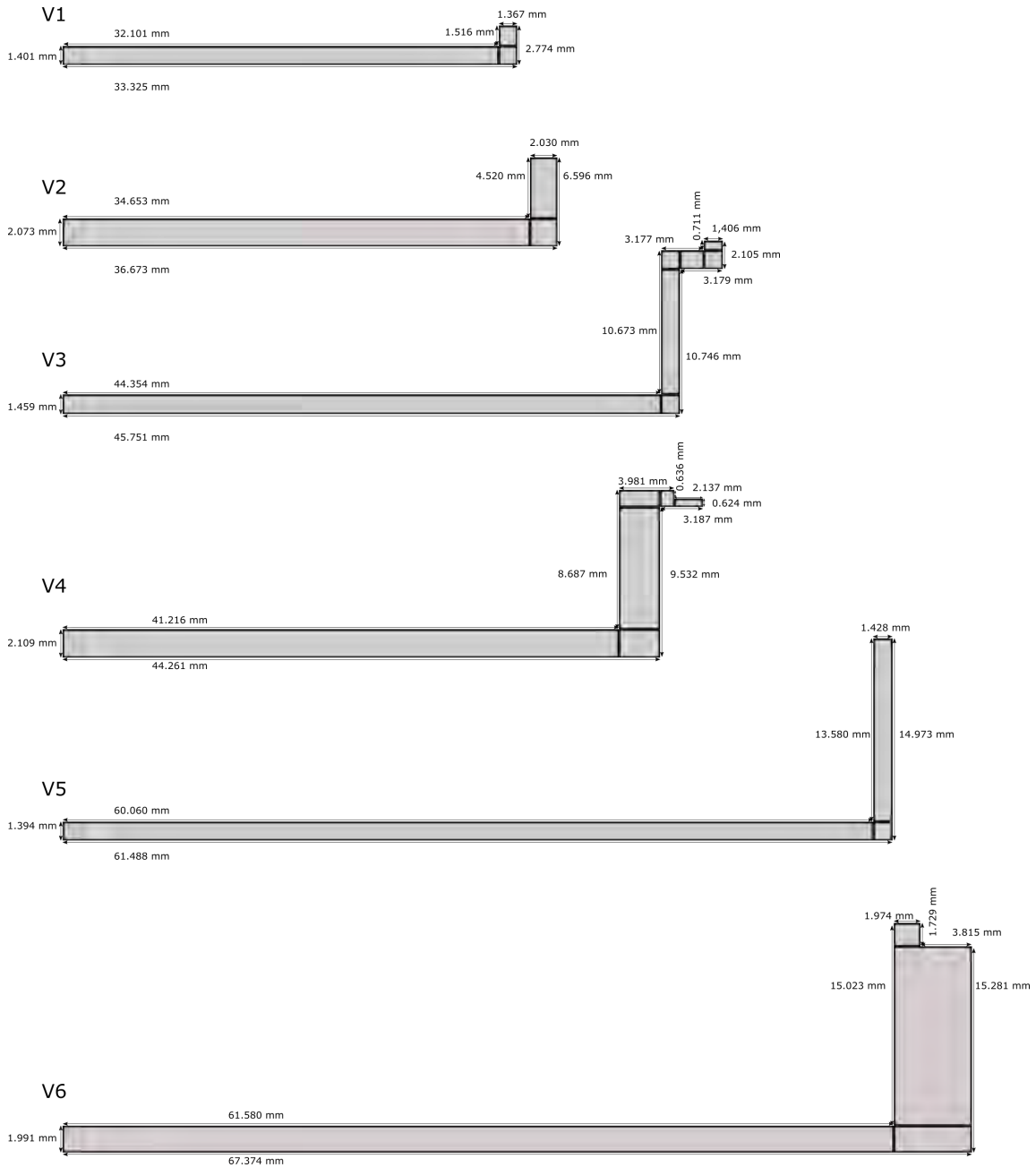


Figure 17: Power line shapes and segments

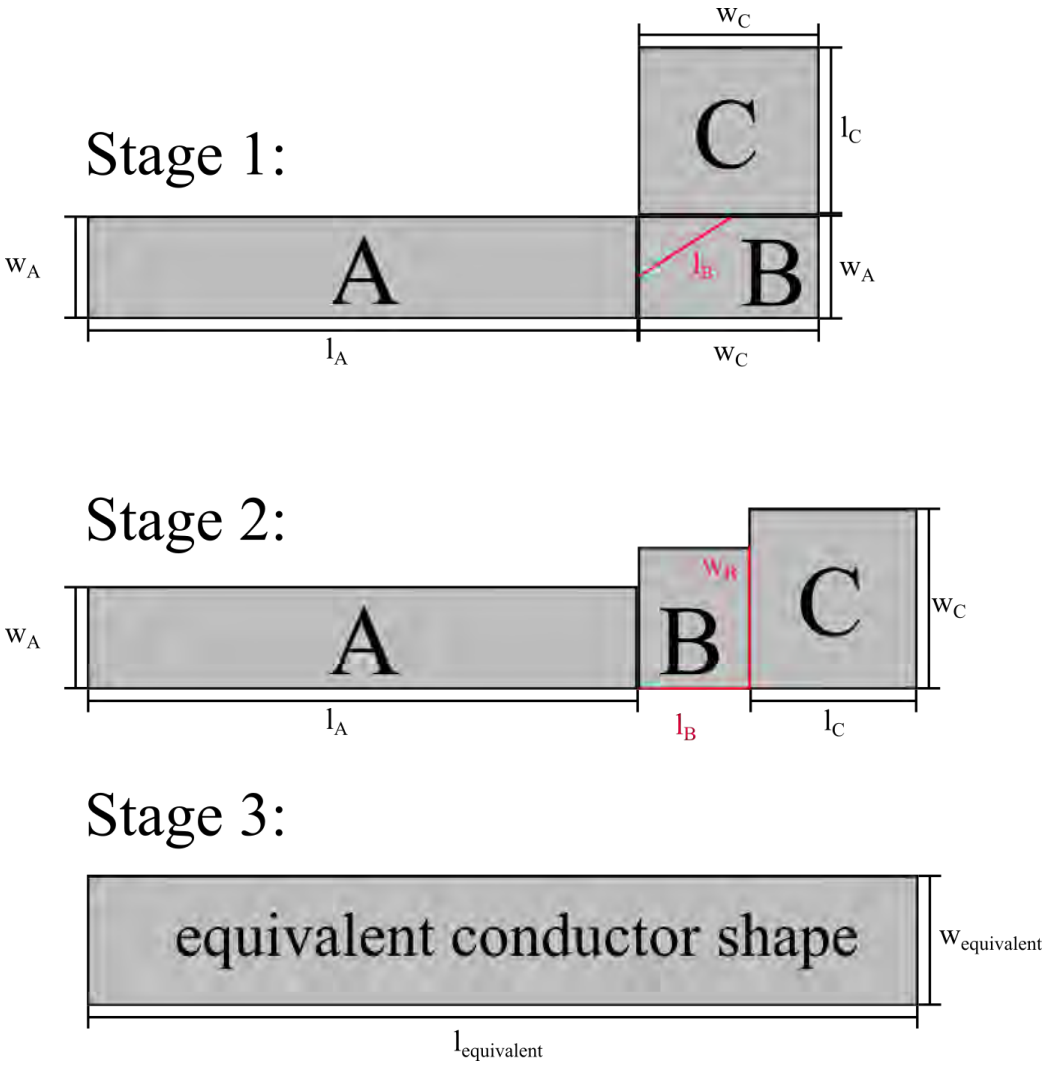


Figure 18: A simple example of the power line transformation to the equivalent conductor shape in three stages. A represents a horizontal segment, B a corner segment and C a vertical segment.

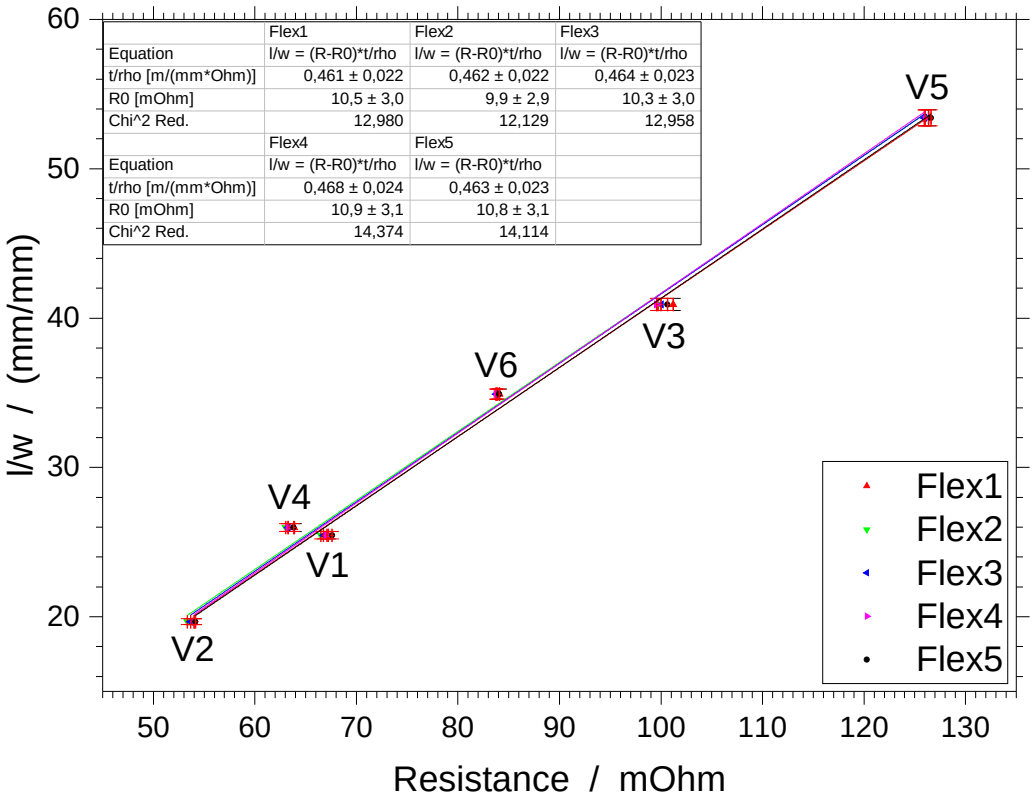


Figure 19: Electrical layer thickness determination

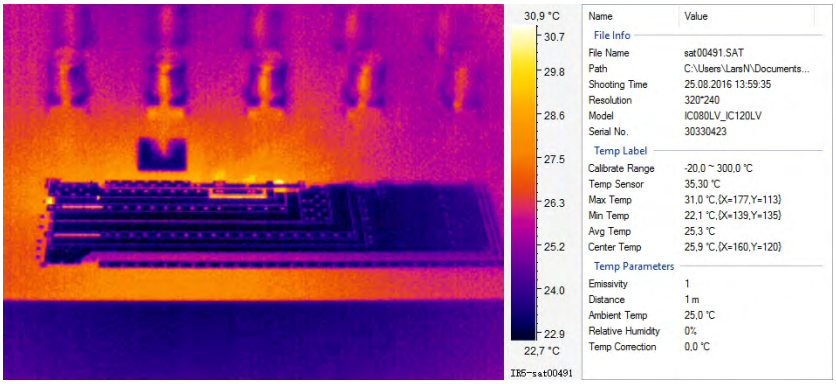
4.2 Breakdown voltage

The MuPix requires a high voltage of about 85 V. In order to see, if the isolation in the flexprint can handle this potential difference, the breakdown voltage has been measured with the Keithley 2611B SourceMeter. The source meter has been set up as a voltage source with a current limit of 100 nA. A potential difference of up to 200 V has been applied to the neighboring power lines $V1$ and $V2$ without closing the circuit. The smallest distance between $V1$ and $V2$ is $91\,\mu m \pm 10\,\mu m$, with the error approximated from the photomask as in chapter 4.1. The same has been done with $V6$ and ground, which are on different layers but above each other. Due to the layer stack (see figure 25), the expected distance between $V6$ and ground is 45 µm. During measurement, the current never rose above $0.32\,nA \pm 0.03\,nA$. This leads to an approximate isolation of $\rho_{\text{isolation V1-V2}} > (6.8 \pm 1.0) \times 10^9\,\Omega\,\mu m^{-1}$ between $V1$ and $V2$ and $\rho_{\text{isolation V6-GND}} > (1.4 \pm 0.1) \times 10^{10}\,\Omega\,\mu m^{-1}$ between $V6$ and ground.

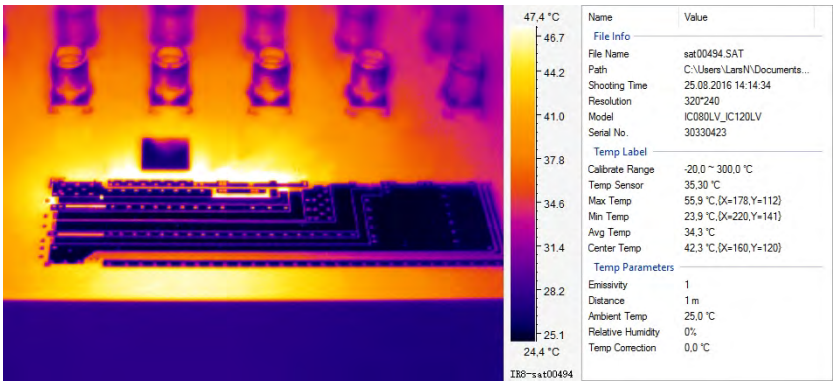
4.3 Thermal heating

The expected current on a final outer detector layer flexprint is approximately 4 A. In order to see how much a power line heats up at different currents, a Hameg HMP4040 [Gmb09] has been used as a current source. The voltage limit has been set to 3 V. The heating process has been observed with an IR camera, the TROTEC IC080LV [TRO16]. The glue might get soft at high temperatures [Hun12]. Hence the current has been applied in a range from 0 A to 7 A to the lines $V1$ and $V5$, located on the top and bottom layer. As shown in figure 20 for $V1$ at 4 A, the highest temperature measured by the IR camera is about 31.0 °C and at 55.9 °C about 7 A. V5 on the bottom layer gets even hotter, with temperatures up to 64.4 °C, because of its isolated position. The maximum temperatures are measured close to the bonds, because the traces used for the bonds are thin and thus have a higher resistance. The remaining part seems to stay at room temperature. That is because the aluminum reflects the IR rays from the laboratory environment which are captured by the camera. Thus, the real temperature of the whole power line cannot be measured correctly with this method. It can be seen in the temperature distribution at the heatsinking PCB surface in figure 21(b) that the center section is significantly warmer than the environment. Because of this common weakness of IR cameras, the temperature can only be estimated from the bond areas, where the securing glue on the bonds is not as reflective as aluminum, or from the heatsinking of the PCB underneath.
In the final combination of the flexprint and the MuPix, the chips will in-

troduce even more heat. But the whole detector will be cooled with Helium gas, which will also cool the flexprint. The passive cooled power line with $\Delta T < 13\,\mathrm{K}$ at $4\,\mathrm{A}$ seems less critical, if the gaseous cooling is strong enough.

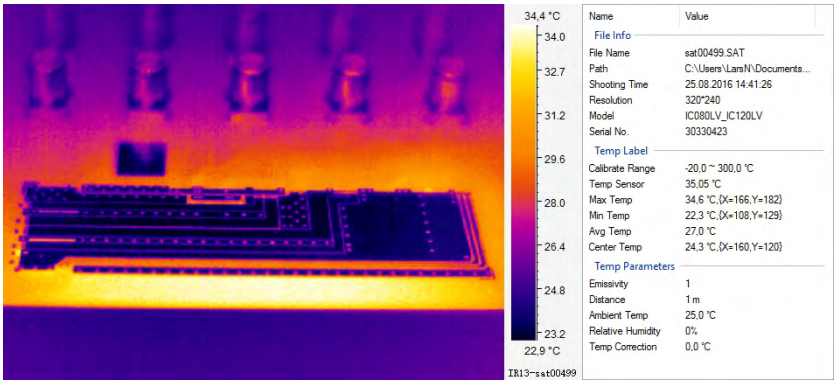


(a) V1 heated with 4 A.

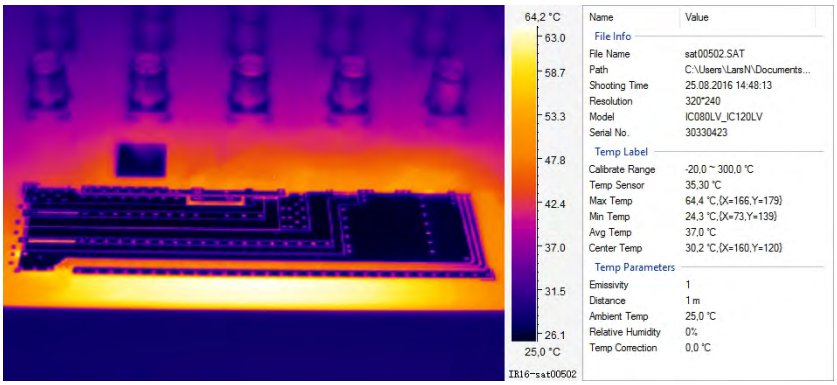


(b) V1 heated with 7 A.

Figure 20: IR camera pictures; V1 heating



(a) V5 heated with 4 A.



(b) V5 heated with 7 A.

Figure 21: IR camera pictures; V5 heating

4.4 Time Domain Reflectometry (TDR)

In order to get more information about the dielectric environment and to check, if the chosen parameters for the differential pairs match the requirements, the differential trace impedance has been measured with the Time Domain Reflectometry (TDR).
TDR is a measurement of reflections in the transmission line. A step function generator emits a signal (in this case a 300 kHz square wave) which is transmitted over the tested data traces. During propagation, the signal gets reflected every time the impedance changes. These reflections are measured with an oscilloscope, which calculates the impedance from the amplitude of the reflection. This impedance information is plotted against the propagation time in the TDR graph. Therefore the impedance of a trace can be interpreted intuitively within the time domain [Tec13].
Before measuring the impedance of every differential pair, it is necessary to determine the right time domain, to measure just the flexprint. This can be done by calculating the signal propagation time for each segment on the board (PCB – Flex – PCB). This has been done by dividing the theoretical trace length by two thirds of the speed of light. Because of reflections at the end of the trace, the signal propagates twice the length and therefore the time has to be multiplied by two. The calculated values can be abstracted from table 9 in the appendix. This is just a rough estimation because the propagation speed depends on the dielectric environment. The time domain can be found more precisely by manipulating the dielectricity around the traces. If the dielectric environment changes locally, the impedance changes within a short time domain. By analyzing the realtime TDR measurement while changing the impedance in different places, the start and end point of the flexprint time domain can be determined for measurements.
All TDR measurements were made with the Tektronix DSA8300 [Tek16]. An example of these measurements is shown in figure 22. Both traces of the differential pair are measured simultaneously. The sum of both waveforms results in the white waveform and equals the differential impedance. The measurement domain is set between the two white vertical measurement makers. This is the flexprint time domain. The plot in figure 24 shows the measured mean values of this domain for all traces on all five flexprints. The RMS around the mean is chosen for the error margin for the mean value, representing the impedance flatness. It can be seen in figure 23 or in the examples in the appendix (fig. 38), that only in a few cases homogeneously the impedance is flat, but in most of the cases it describes a rising function. Regarding the mean values, the impedances of the traces on the bottom layer are too low and the impedances of the traces on the top layer are too high,

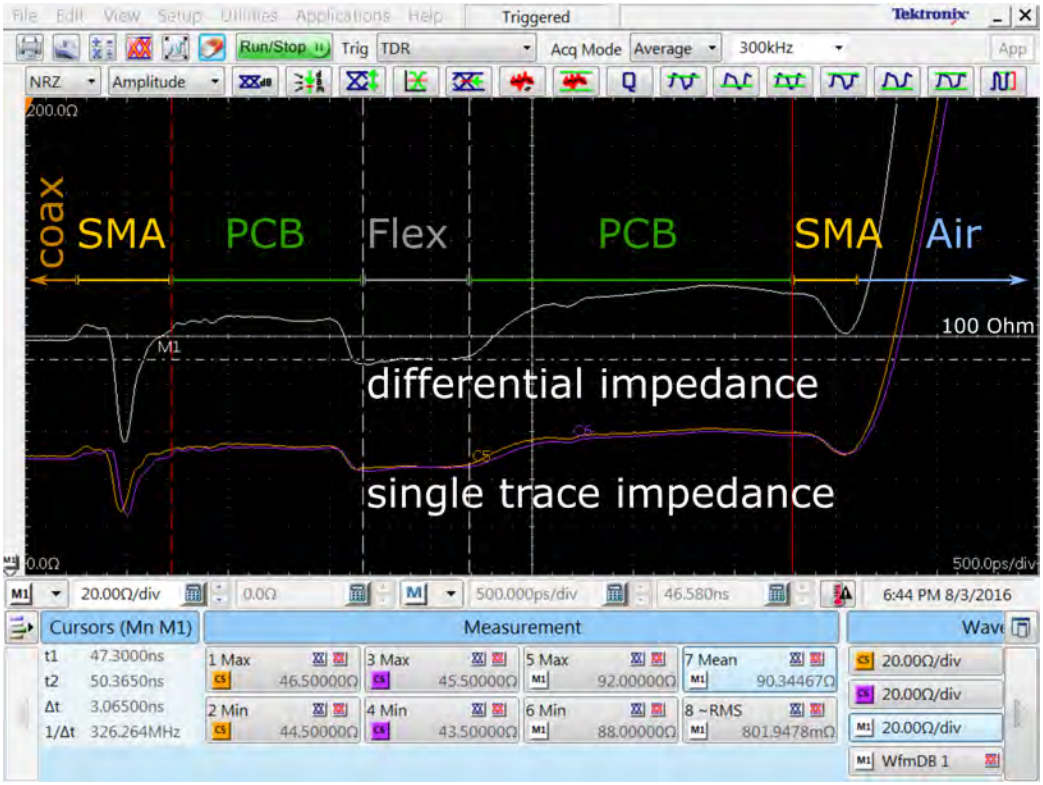


Figure 22: TDR example, time domains labeled

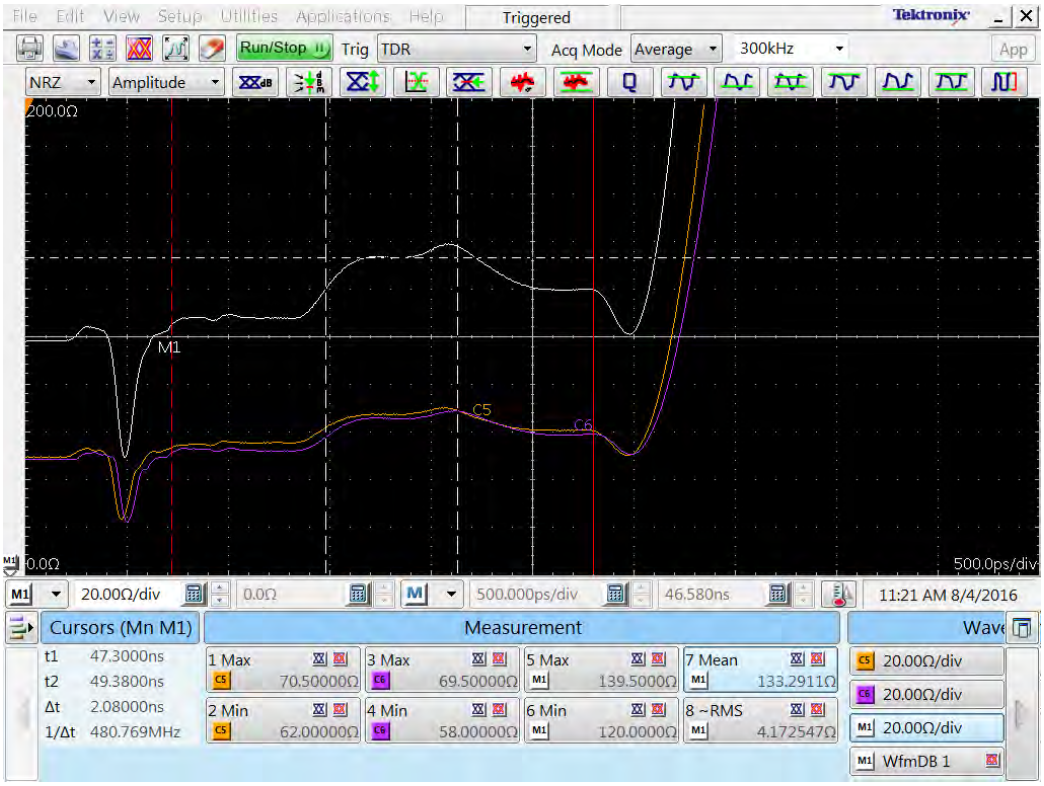


Figure 23: TDR example of rising impedance, DATA9

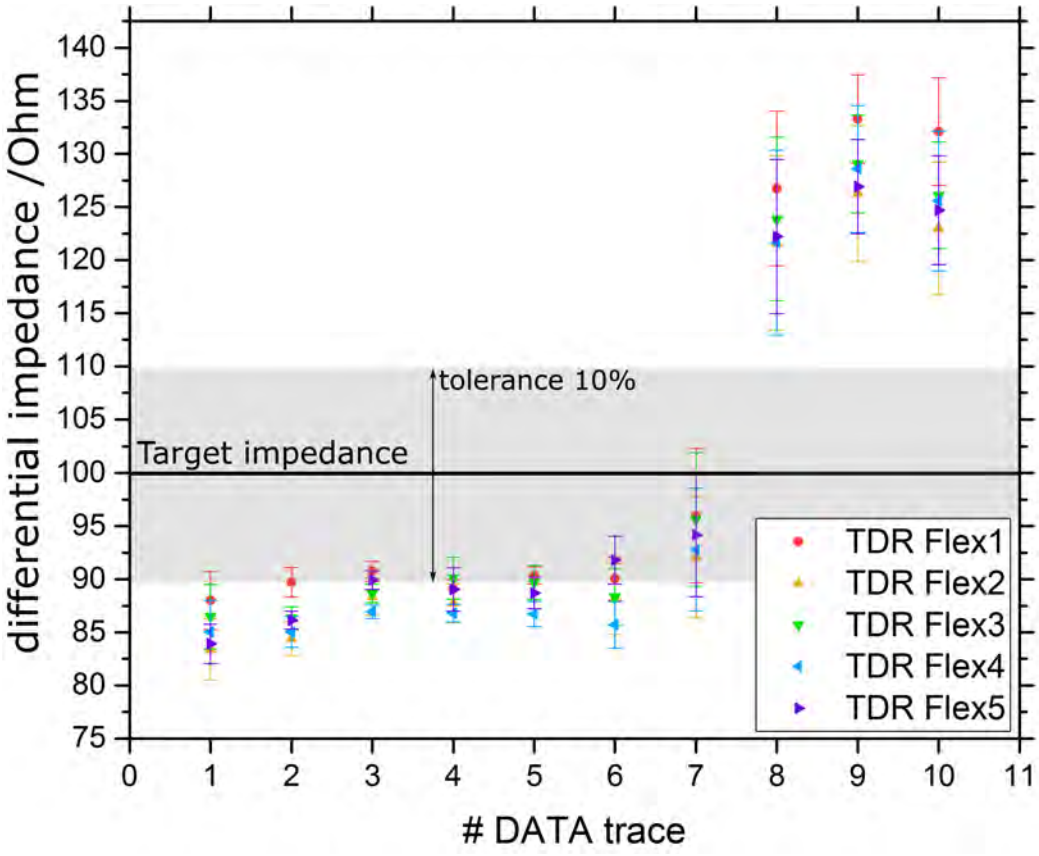


Figure 24: TDR measurements: mean impedance plotted against data trace numbers, RMS around mean of impedance taken as error margin.

compared to the target impedance of 100 Ω. The traces on the top layer are expected to be above the tolerance margin of 10% (compare tab. 5). This is because of the dielectricity of the air directly above the top layer. But the impedance of the traces on the bottom layer are much lower the theoretical values from table 5. In the initial calculations, the impedance has been calculated for the flexprint only. In fact the flexprint is bonded and glued on the PCB. Therefore, the layer stack looks like figure 25. In table 7 the impedances with the PCB in consideration can be abstracted.

DATA	**Layer**	**Gap between differential pair**	**Calculated differential impedance with PCB**
1	bottom	112 µm	73 Ω
2	bottom	133 µm	73 Ω
3	bottom	154 µm	73 Ω
4	bottom	112 µm	73 Ω
5	bottom	133 µm	73 Ω
6	bottom	154 µm	73 Ω
7	bottom	133 µm	73 Ω
8	top	112 µm	122 Ω
9	top	133 µm	125 Ω
10	top	154 µm	126 Ω

Table 7: Theoretical impedances, calculated with 12.2 µm aluminum thickness, 5 µm glue ($\epsilon_r = 3.2$) [Hun12], 12.7 µm soldermask ($\epsilon_r = 3.3$) and 35 µm copper plane under the bottom layer in order to consider the PCB.

The top layer impedances are now consistent with the measured data, but the bottom layer impedances are much lower compared to the measurements. There are additional sources for the mismatch, that have not been accounted for, like air between the flexprint and the PCB. According to LTU, the glue is not applied as a whole layer, but as small spots. Beyond that, the dependence of the differential impedance on the differential gap disappeared. This behavior is also observed in the measurement. There is a difference between the mean values, but the errors are too large to determine any significant difference.
In order to get the impedance of the traces closer to the target impedance, the trace parameters have to be changed. In case of the traces on the top layer the best way might be decreasing the single trace impedance by increasing the trace width. On the bottom layer the trace width has to be smaller, in order to raise the single trace impedance. Due to manufacturing limits, a smaller width is not feasible.

Figure 25: Layer stack of the test structure flexprint on the PCB (Al=aluminum, PI=polyimid)

As presented before, the impedances are not flat in the flexprint time domain, but almost always shows a rising pattern. All traces are measured from the left to the right side. This suggests, that there might be a dielectricity gradient from the left to the right side of the flexprint. This might be caused again by a non-homogeneous glue distribution between the top and bottom layer. Because the glue is applied in small dots between the structures, the amount of glue on the right side might be different than on the left side, caused by different structures on the flexprint. Additionally, air could be trapped between the two layers, too. Depending on the glue dot density the air decreases the average local dielectricity differently. The problem can be mitigated by using a different method of applying the glue or implementing a homogeneous glue dot distribution in the flexprint layout.

4.5 Eye-Diagrams

In general an Eye-Diagram shows samples of transmitted digital bits. Pseudorandom bit words are transmitted from a bit source via the data traces under test and measured with a serial analyzer. Dependent on the measurement time the analyzer captures a certain amount of samples of every transmitted bit word, triggered from a synchronous clock signal. By overlaying the samples in one graph, an eye pattern develops after many samples [Tek10]. The Eye-Diagrams have been taken with the Tektronix DSA8300 (Digital Serial Analyzer) in the eye-mode. As a source, an Altera Stratix V Field Programmable Gate Array (FPGA) [Alt16] has been used to transmit random words in a PRBS7 (Pseudorandom binary sequence) pattern. As a trigger another output of the FPGA has been used. In order to connect the FPGA and flexprint adapter PCB, the High Speed Mezzanine Card (HSMC) port of the FPGA has been used with an adapter card from HSMC to SMA. The input signal for the flexprint, coming out of the HSMC-SMA adapter, can be seen in figure 26.

The FPGA, the structure flexprint PCB and the serial analyzer always have been connected via coaxial cables with SMA to Miniature CoaX (MCX) connectors and a MCX to SMA adapter to have an SMA to SMA connection. Concerning vertical eye opening, the best and worst Eye-Diagram with the PCB and flexprint in the transmission line can be seen in figure 27.

These are eyes at the Mu3e target bit rate of 1250 Mbit/s. The worst Eye-Diagram belongs to DATA7, the longest trace. The eye height is under worst conditions $261.4\,\mathrm{mV} \pm 0.2\,\mathrm{mV}$ with an amplitude of $633.0\,\mathrm{mV} \pm 0.1\,\mathrm{mV}$ and the eye width is about $621.7\,\mathrm{ps} \pm 0.1\,\mathrm{ps}$. The eye opening is mostly influenced by the higher ohmic resistance caused by the additional length. In combination with the trace capacitance and inductance, the signals cannot rise as fast to the high or low state of the bit as the input signal does. The most worrying part of the Eye-Diagrams is the low slope on the rising edge. It seems that higher frequencies are damped.
The total RMS jitter is acceptable for data transfer. The average jitter is $18.34\,\mathrm{ps} \pm 0.01\,\mathrm{ps}$. It should be noted, that the trigger signal also has jitter. But adds not significantly to the initial jitter in the measurement.

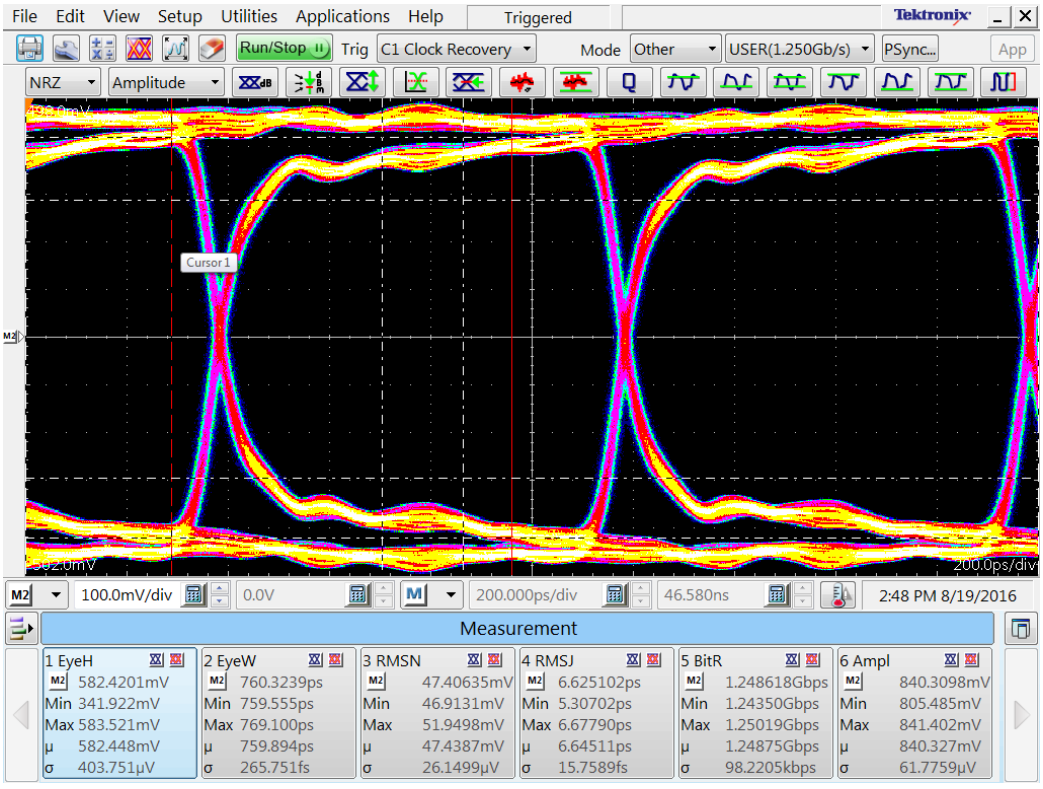
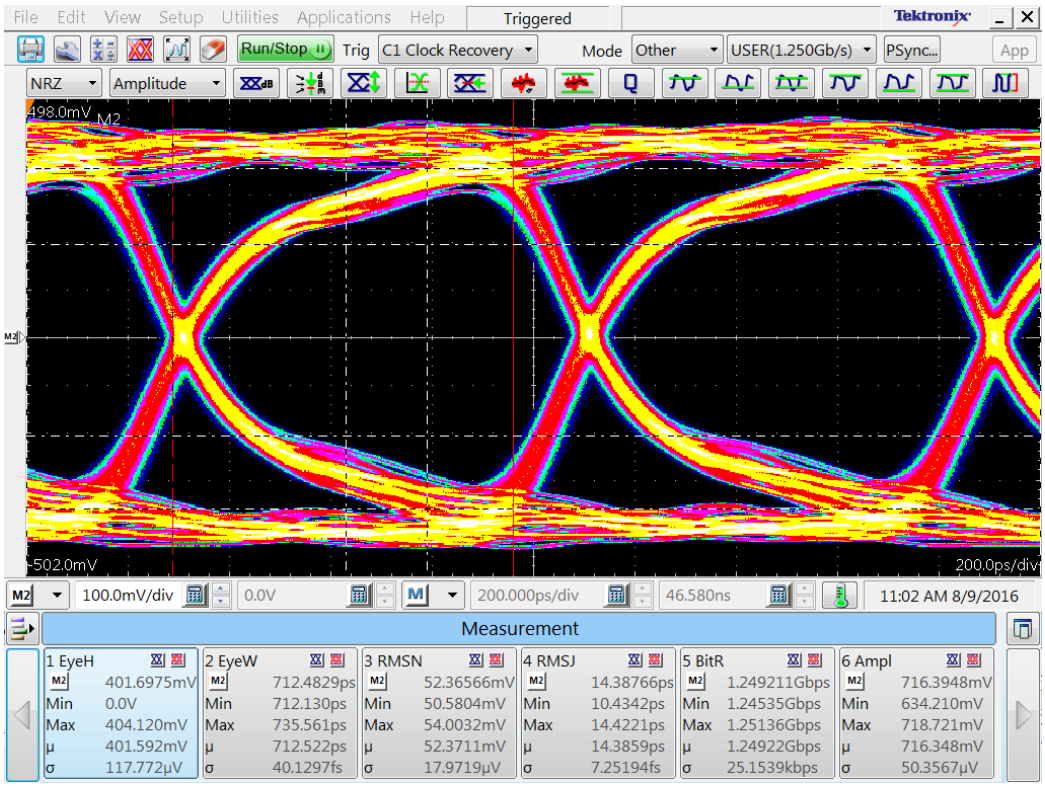
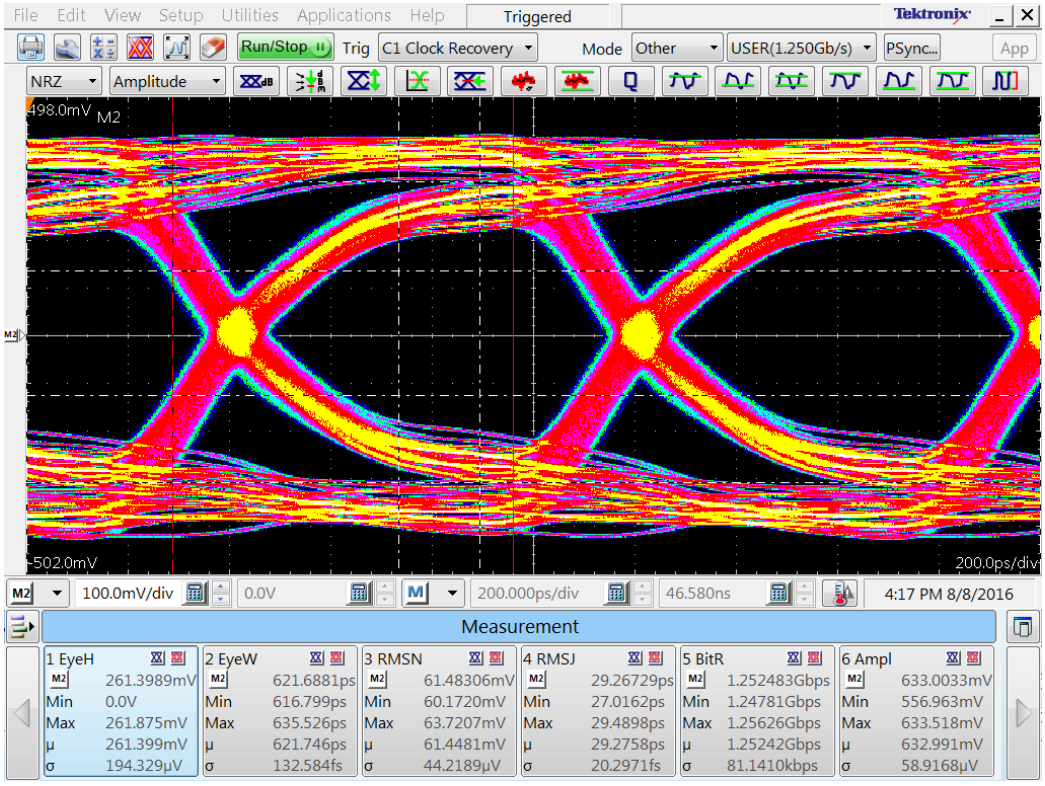


Figure 26: Eye-Diagram of the input signal at 1250 Mbit/s



(a) DATA1



(b) DATA7

Figure 27: Eye-Diagrams at 1250 Mbit/s

4.6 Frequency spectrum as Bode-Diagram

Based on the observation of the slowly rising edge in the Eye-Diagrams, it is important to understand which frequencies can be transmitted by the data traces. Therefore, the transmission spectra are taken with a Rohde & Schwarz FSU spectrum analyzer [Sch16]. The range of the analyzer has been set to 10 MHz - 20 GHz in a logarithmic scale. To generate the signal, an Anritsu MG3692C [Anr11] has been used to sweep in the same range with 2000 logarithmic equidistant steps. During sweeping, there is only one frequency transmitted at the time. Hence the spectrum analyzer is set to hold the highest measured power for each frequency in order to capture the whole spectrum. Therefore all values are highest values, instead of averages. Because of input limitations, Bode-Diagrams are measured in single trace mode. A Bode-Diagram is usually a frequency spectrum with a logarithmic frequency scale and the amplitude measured in dB.
All traces are measured separately. The transmission line includes the coax cables, which have their own transmission spectrum. To correct for this, the coax cables have been measured separately and subtracted from the data. The PCB and the connectors on the PCB can not be measured separately. Hence, they can not be corrected for. An example Bode-Diagram in shown in figure 28. All Bode-Diagrams show a lowpass characteristic with a cut-off frequency around 1.4 GHz (extrapolation in fig. 28). This characteristic confirms the supposed damped higher frequencies in the Eye-Diagrams. Especially the cut-off frequency seems critical, because it is below the third harmonic of the 1250 Mbit/s, which is at 1875 MHz. Looking back to the TDR measurements, there are two things that should be noted.
First, the TDR measurement signal which is a square wave with a frequency of 300 kHz, is far away from the cut-off frequency and therefore in the plateau range of the spectrum. Hence the impedance might be higher at around 1 GHz. Secondly the impedance of the transition from the SMA connector to the PCB is an issue. Regarding the TDR measurements, there is a huge drop in impedance, which definitely causes reflections for higher frequencies. Lower frequencies are not effected as much as higher frequencies because of the short time domain of this transition. Unfortunately the PCB and the SMA connectors are needed, in order to connect the flexprint with the signal generator and the spectrum analyzer. Probably the flexprint itself has a better transmission spectrum.

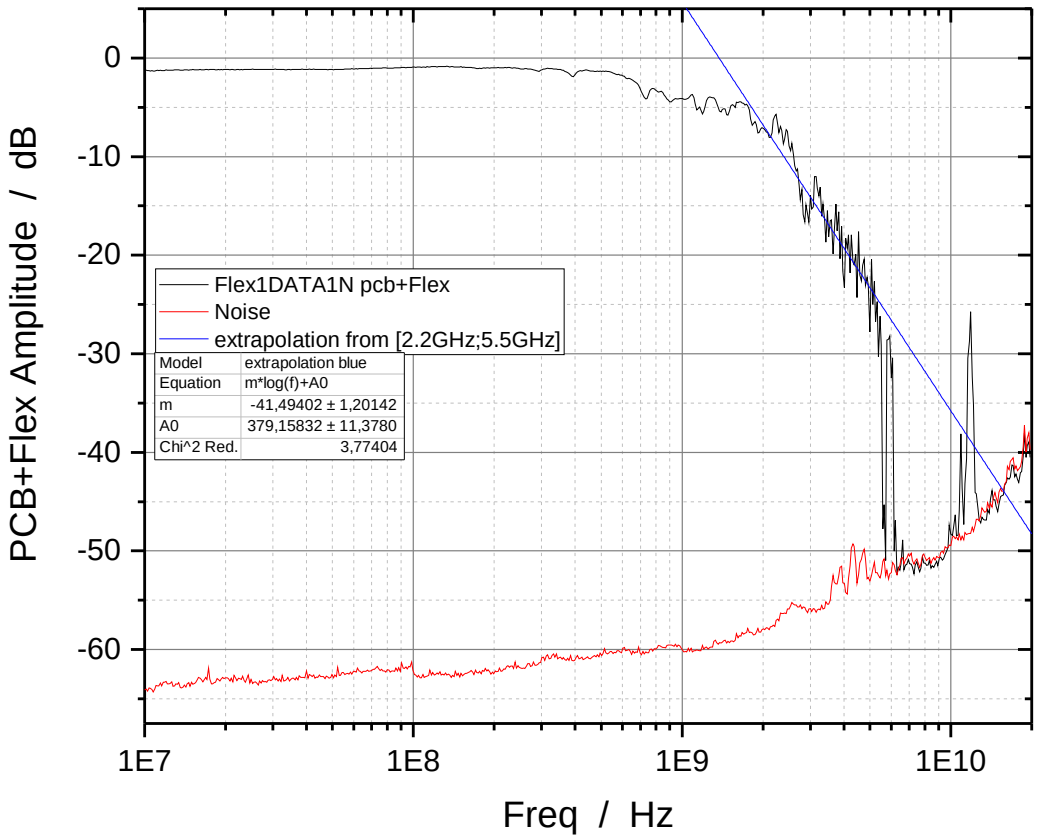


Figure 28: Example Bode-Diagram

4.7 Bit Error Rate Test (BERT)

Reliability is one of the goals of data transmission. The simplest way to test for reliability is to transmit data and check for errors in the output data. For the Bit Error Rate Tests the Stratix V FPGA has been used again to generate PRBS7 bit words. The same FPGA has been used to receive the transmitted bits and check them for errors. The used transmission line, shown in figure 29, contains many connectors and adapters. Hence, there are many potential error sources for the transmitted bits. The data traces have been tested in different combinations at the target Mu3e bit rate of 1250 Mbit/s. Due to increased electro-magnetic coupling between two traces at shorter distances, more crosstalk and therefore more bit errors are expected when traces of the same triple are tested at the same time. Each trace has been started at a different time, in order to avoid identical random bit sequences on two traces. The combination of traces tested at the same time and Bit Error Rates (BERs) can be seen in table 8.

Bit rate	**DATA combination**	**BER @95% CL**
1250 Mbit/s	$1+2+3+\text{BUS2}$ (@125 MHz) $+V1 = 1500\,\text{mV} + V2 = 1800\,\text{mV}$	$< 2.6 \cdot 10^{-14}$
1250 Mbit/s	$4+5+6$	$< 5.5 \cdot 10^{-13}$
1250 Mbit/s	7	$< 9.9 \cdot 10^{-15}$
1250 Mbit/s	$8+9+10$	$< 4.1 \cdot 10^{-14}$
2500 Mbit/s	$7+8+9+10$	$< 5.9 \cdot 10^{-13}$
3200 Mbit/s	$8+9+10$	$< 4.1 \cdot 10^{-15}$
3200 Mbit/s	7	failed
4000 Mbit/s	$8+9+10$	failed

Table 8: Bit error rates from different trace combinations, BER dependent on bit rate and measurement time

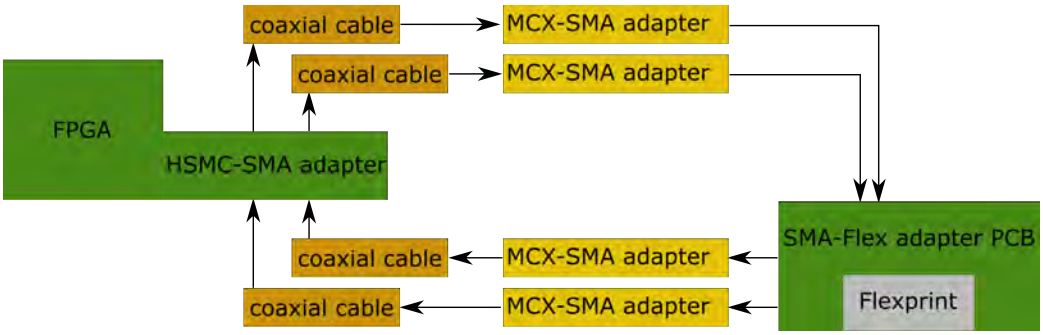
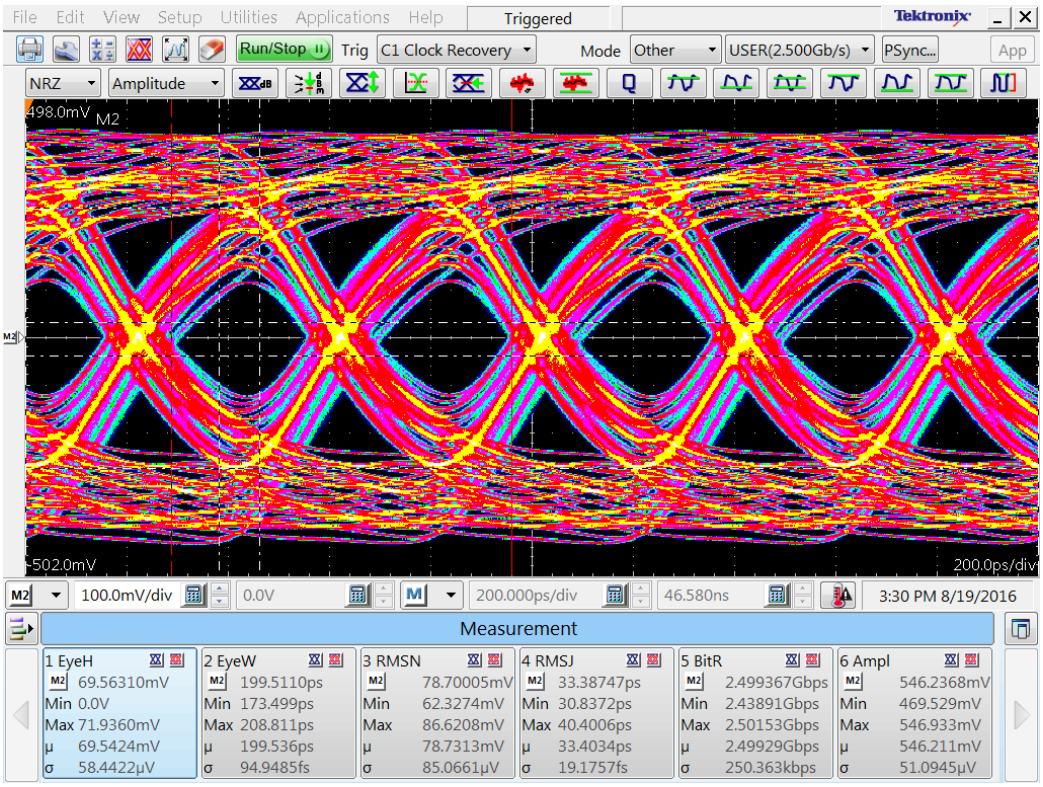


Figure 29: Sketch of the BERT transmission line for one differential trace

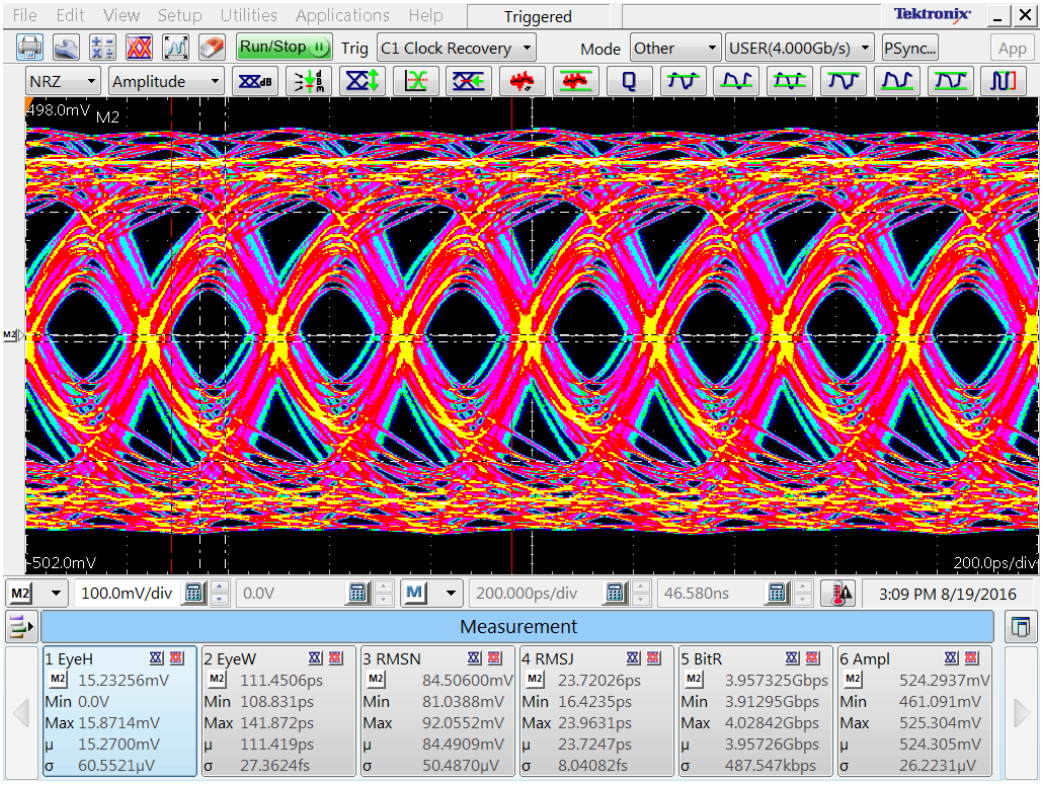
No bit errors were observed, hence upper limits at $CL = 95\%$ confidence level are given. Assuming a Poisson distribution, the BER upper limit is calculated with equation 16, where N is the total number of bits tested [Nar00].

$$BER < \frac{-ln(1 - CL)}{N} \tag{16}$$

In order to increase the chance for bit errors, the first triple has been tested with a simultaneous clock signal of 125 MHz on the bus as well as disturbing the electrical potential by connecting a 1.5 V source to $V1$ and a 1.8 V source to $V2$ as it would be expected on the flex in the detector. All tests were successful and no bit errors occurred.
Because of the lowpass characteristic of the traces, upper bit rate limits have been searched for. Bit rates of 2500 Mbit/s can still be transmitted flawlessly. At 3200 Mbit/s DATA7 failed and at 4000 Mbit/s the third triple also failed in transmission. It can be seen in the Eye-Diagrams in figure 30, that the bits are still transmitted but the eye opening is probably too low for the receiver.



(a) DATA7 at 2500 Mbit/s



(b) DATA10 at 4000 Mbit/s

Figure 30: Eye-Diagrams at higher bit rates

4.8 Jitter and noise

An increased jitter and noise can be an indication for crosstalk. None of the previous measurements showed any attendance of crosstalk. The Tektronix DSA8300 is able to analyze the jitter and noise on the transmitted signal further. It can breakdown the noise and jitter into random and deterministic components. If there is any noticeable crosstalk between two differential pairs, the jitter and noise should be increasing and maybe bound to some bit pattern or some periodicity. For comparison the data has been take once with random bits propagating over only one data trace and once with additional random data transmission on neighboring traces. Both sets of measured data of jitter and noise can be seen in figure 39 in the appendix. The taken measurements show no significant difference between both cases. Hence it is safe to say, that this differential signaling setup with a distance between two trace pairs of 350 µm is free of significant crosstalk.

4.9 Bus signal

For the MuPix, common signals are foreseen to be distributed via bus on the flexprint. The common mode signals have less demand on bandwidth. However a good signal quality is crucial. Using the test structure flexprint, the feasibility of this approche has been studied on a bus trace with three signal outputs. The transmitted 125 MHz clock signal can be seen in figure 31. One of the waveforms (fig. 31(a)) shows a high influence of the reflection on the not terminated PCB trace ends. The other one shows a quite rectangular clock signal. This one is terminated with 50 Ω at the unconnected outputs. Because of Kirchhof's current law the amplitude is lower with termination than without. The reflection pattern can also be seen if the oscilloscope is connected to the other outputs. The problem is the length of the output branches on the PCB. The long traces on the PCB lead to a greater retardation between initial signal and reflection.

(a) Clock on BUS1, oscilloscope connected with output 1, output 2 and 3 not terminated

(b) Clock on BUS1, oscilloscope connected with output 1, output 2 and 3 terminated with 50 Ω

Figure 31: Bus signal on the oscilloscope after transmission

5 Conclusion

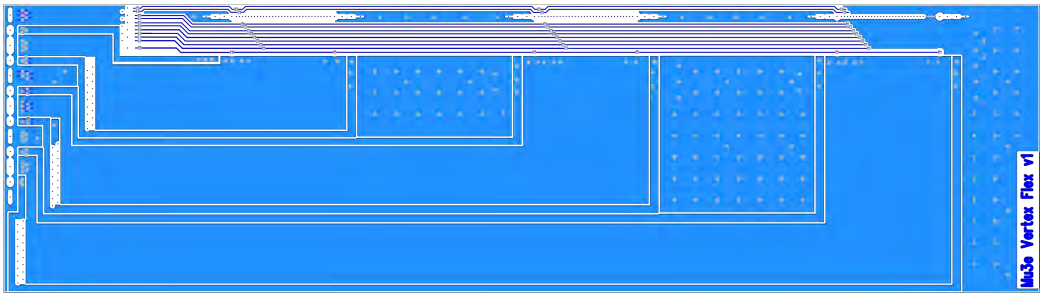
For the purpose of connecting the MuPix chips for the Mu3e detector, a flexprint for the outer pixel layers is developed. A possible solution for the power distribution is found. The solution is not as initially planed a passive distribution. Instead, it is a semi-passive solution, which needs three different voltage sources to distribute one voltage evenly over nine MuPix chips. In order to test a first prototype of a manufactured flexprint, a test structure flexprint is created. This prototype was manufactured five times and each bonded on a separate PCB for connections to the measurement tools. Several characterizing measurements are made. From the resistance measurements, the thickness loss during the manufacturing process has been determined. The final thickness of one aluminum layer is $12.29\,\mu m \pm 0.27\,\mu m$, from a starting point of $14\,\mu m$ thickness. The thickness is mostly important for the resistance of the power lines but also influences the impedance of the signal traces. The breakdown voltage measurement shows, that the HV can be applied safely with a distance of $91\,\mu m$ to other conducting traces, because of the well isolating materials that are used. Considering that the heating tests were performed with passive radiative cooling only, the temperature measurement looks promising at 4 A with a $\Delta T < 13\,K$.
The TDR measurements show, that with the trace width of $63\,\mu m$ and gap of $133\,\mu m$ $\pm 20\%$, the impedances are on the bottom layer at least $15\,\Omega$ too low and on the top layer at least $25\,\Omega$ too high, due to a mismatch of the single trace impedance parameters. More related to the dielectric environment is the fact that the impedance is not constant in one trace. This cannot be corrected with trace parameters, but with improved glue application.
Concerning the critical SMA connector to PCB transition, the test setup is not perfectly suited for the Eye- and Bode-Diagrams. The signal propagation seems to be highly influenced by the impedance drop at the SMA connector and soldering to the PCB. The Bode-Diagrams show a lowpass characteristic with a cut-off frequency of approximately 1 GHz. The Eye-Diagrams are looking rather good, except for a decreased slew-rate. The eye height is under worst conditions $261.4\,mV \pm 0.2\,mV$ with an amplitude of $633.0\,mV \pm 0.1\,mV$ and the eye width is about $621.7\,ps \pm 0.1\,ps$ at 1250 Mbit/s.
The transmission line works reliably as the BERTs show (BER$< 5.5 \cdot 10^{-13}$ 95% CL). This indicates, that the SpTAB bonds are of good quality. The bonds to the PCB as well as the vias at layer transitions are nearly not noticeable in the TDR measurements. It seems to be a very reliable technology with a small amount of discard. Only one via on a bus trace was found to be broken (DATA5 on flexprint 2 is always missing in the measurements, because it has a defect on one end of the PCB, but on the flexprint trace which

is still working, tested with the TDR from the other side). The flexprint is working and only a few more iterations are needed until the final flexprint can be produced. The test setup can be further optimized, but it is possible to measure the most critical characteristics of the flexprint.

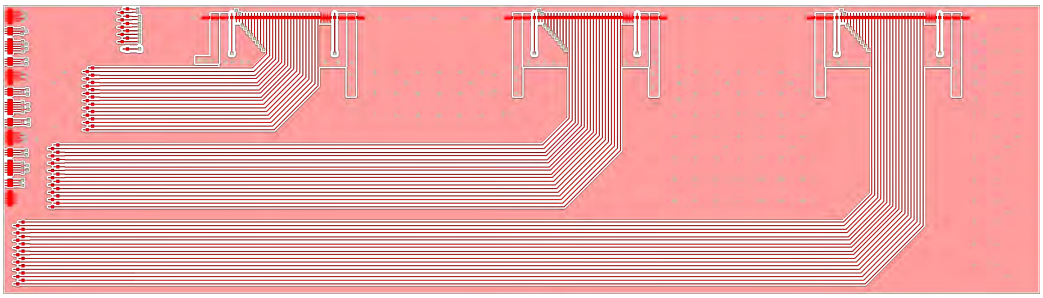
6 Outlook

The electrical layer thickness as well as the breakdown voltage are well understood. But there is a need for more heating tests, especially under real conditions with an attached and running MuPix, with all power lines under load and gaseous Helium cooling.
The TDR measurements show, that for next iterations in flexprint design the parameters should be changed, in order to shift the impedances towards 100 Ω. On the top layer the mismatch can be compensated by choosing a different trace width and another gap. Recommendations are a trace width of 98 µm and a gap of 154 µm. The impedance of the bottom layer can be increased by undercut the minimal structure size by 30 µm.
Also tests on the now existing flexprint should be done with an additional layer of polyimid on top of the top layer, simulating the support structure on this side of the flexprint. Instead of a polyimid layer above the top layer, a MuPix like layer would be even more interesting. The MuPix layer on which the flexprint will be bonded with the MuPix is mostly made of aluminum. But this layer is not like the PCB a metal plane, it is more like several coats of interrupted grids of aluminum. Therefore the impedance is expected to be very different compared to a solid metal plane.
An improvement for the impedance could be a flexprint design with three layers, in which the middle layer is used as ground and stabilizes the impedance. But it is not clear at the time of writing, if this is possible with LTU.
Better results from Eye-Diagrams and especially from the Bode-Diagram could be achieved with a different type of connection which reduces the impedance drop of the soldering or with a differential probe. Even higher bit rates could be feasible in the BERT. Also a larger version with the dimensions of the outer detector flexprint would be interesting to test. More variation could be tested on a three times larger flexprint and it could be tested, if the power distribution actually works as simulated.
There are also other manufacturers that should be considered. Not all of them can produce aluminum flexprints but some are offering a combination of copper layers and aluminum layers. This might be interesting for the problem of the low impedance on the bottom layer, because the minimal structure size for copper layers can be much smaller.

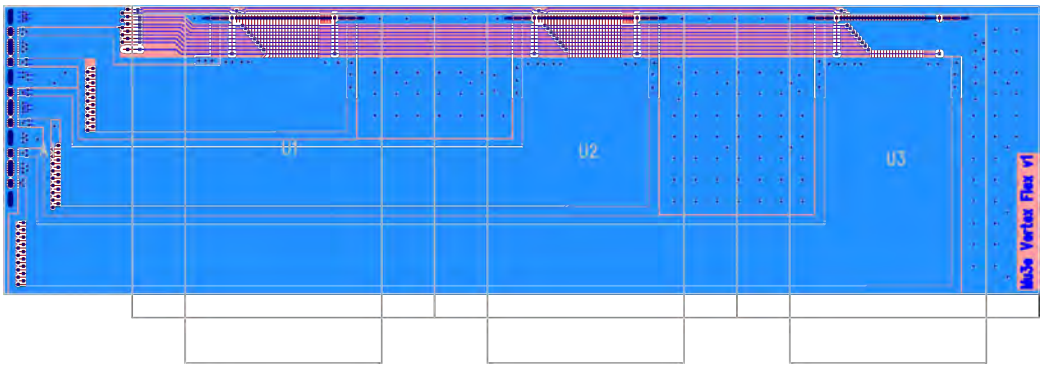
7 Appendix



(a) top



(b) bottom



(c) combined

Figure 32: Flexprint layout for inner detector layers

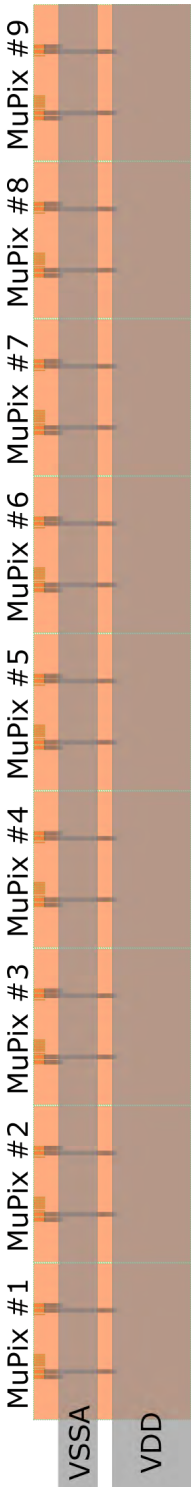


Figure 33: Shared power line designe, magnified and with full lenght

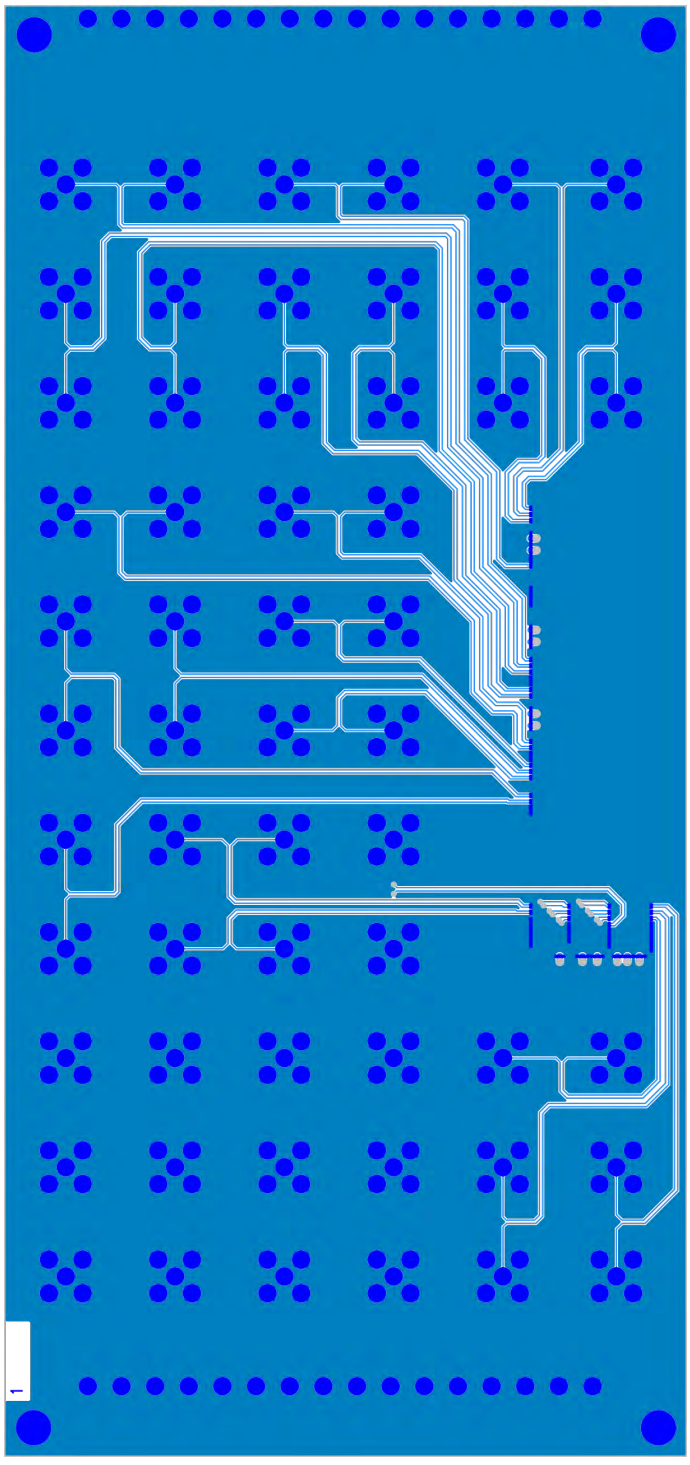


Figure 34: Flexprint-SMA adapter PCB top layer flooded

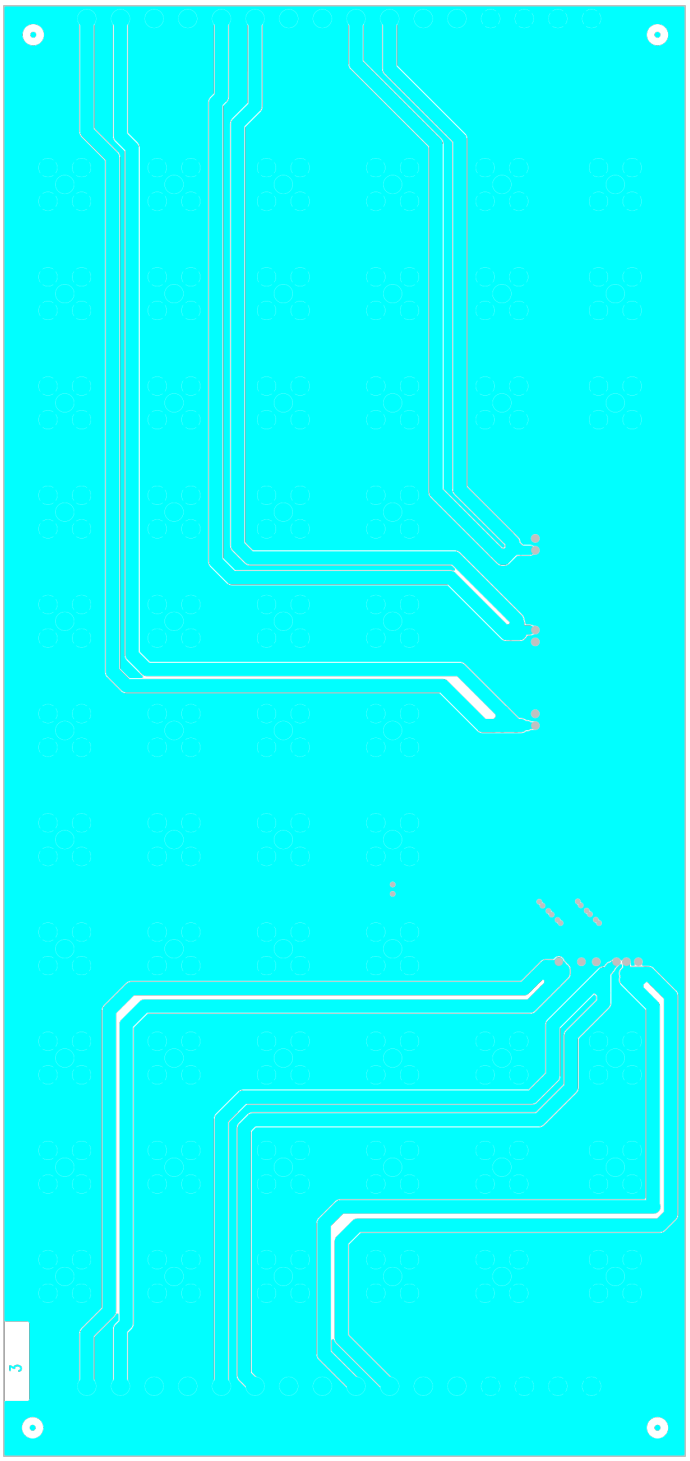


Figure 35: Flexprint-SMA adapter PCB third layer flooded

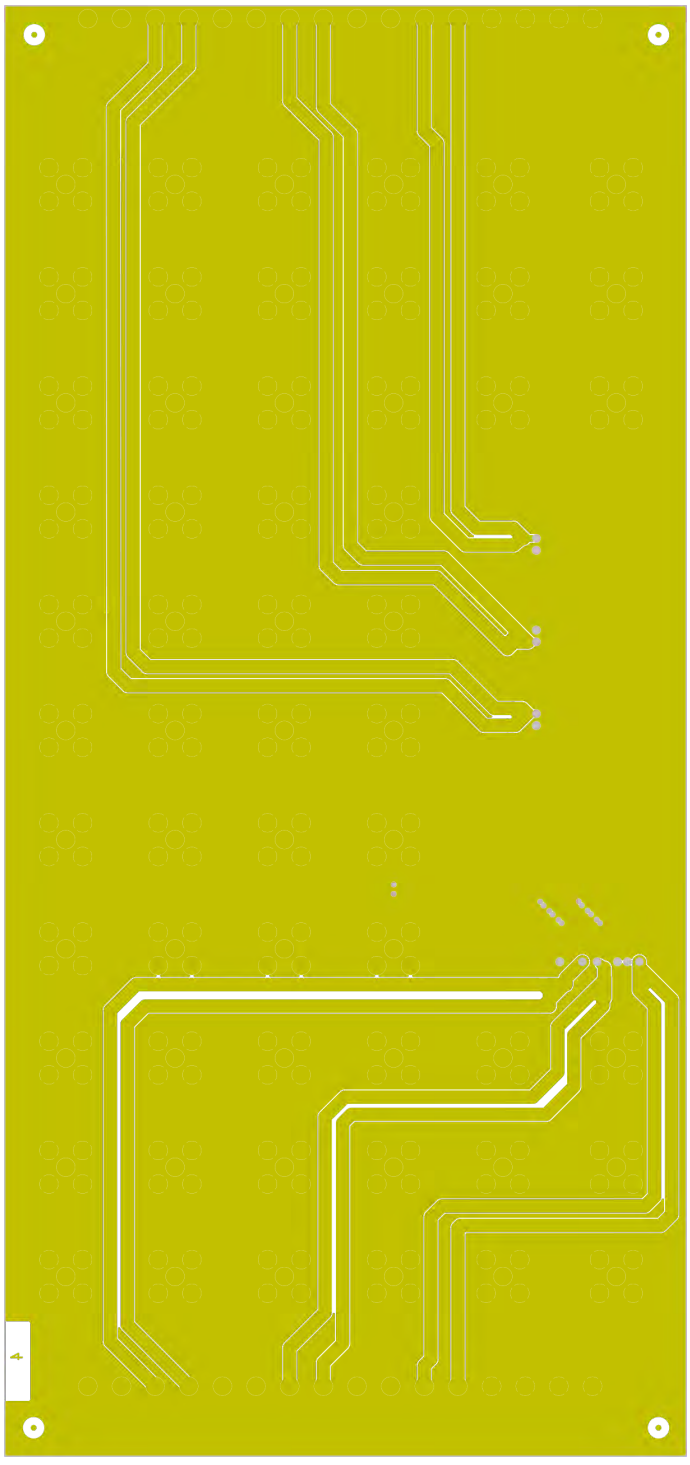


Figure 36: Flexprint-SMA adapter PCB fourth layer flooded

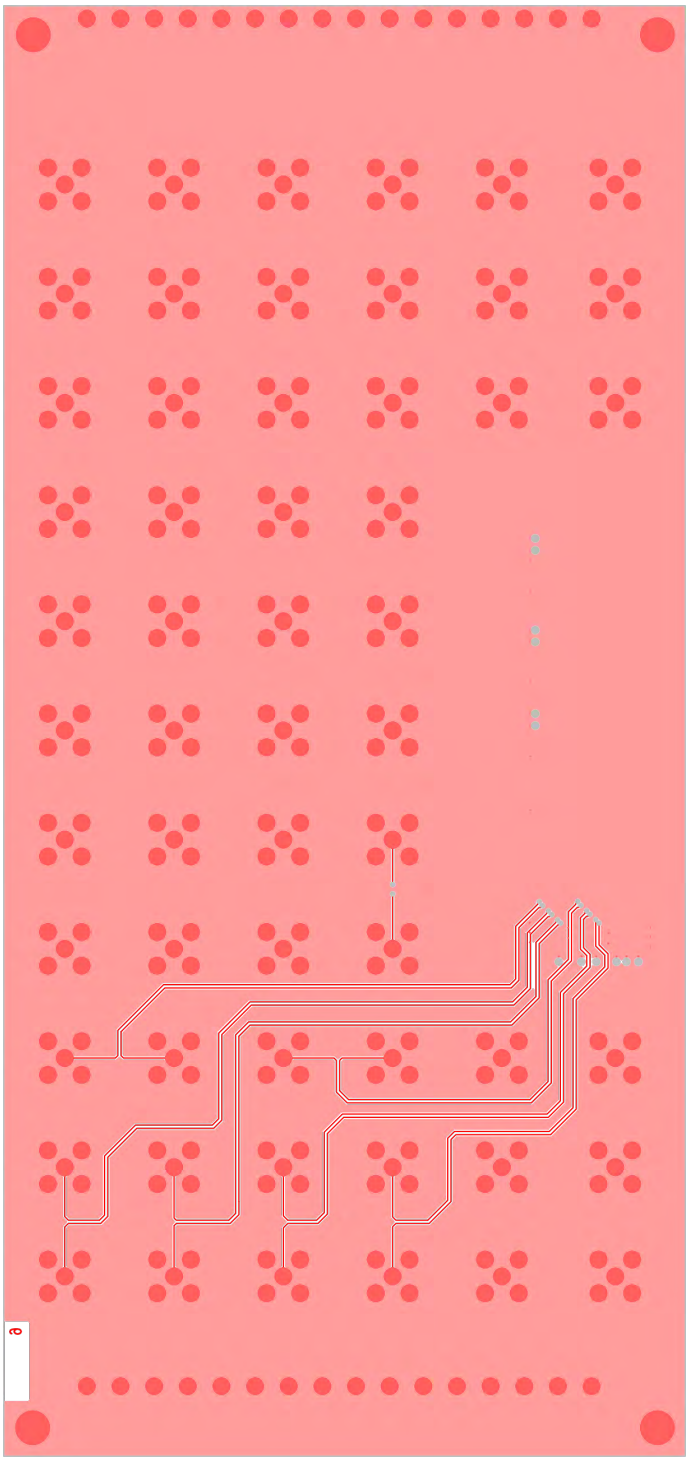
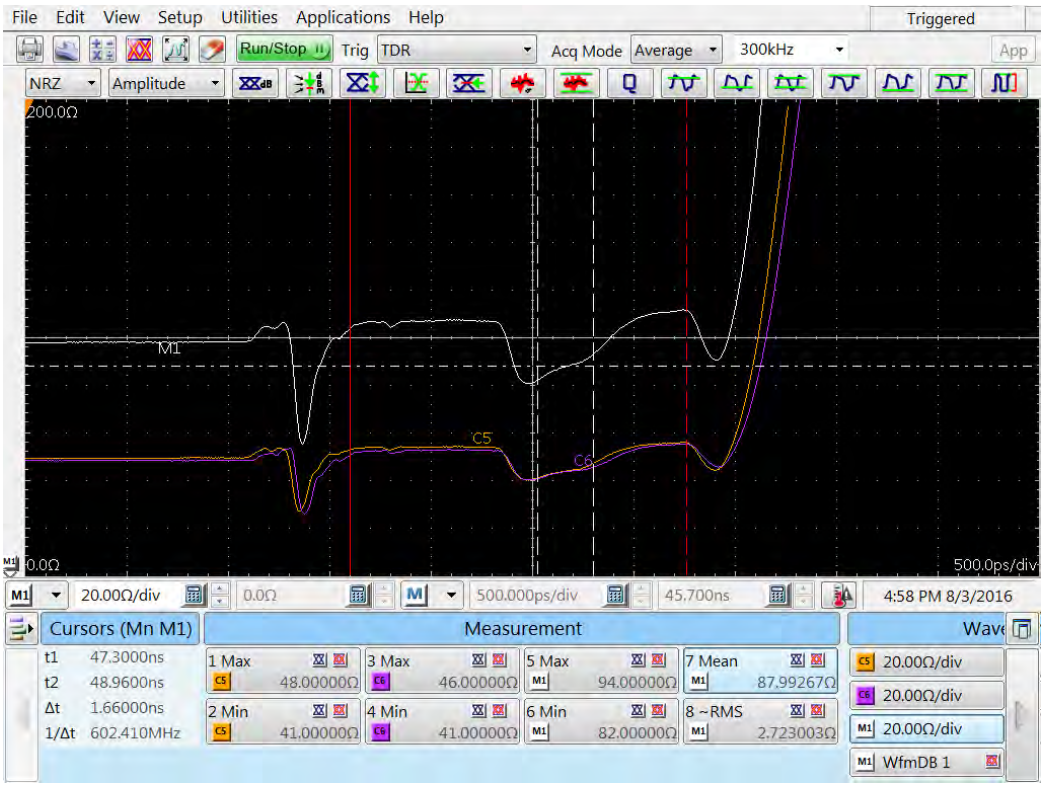


Figure 37: Flexprint-SMA adapter PCB bottom layer flooded

Trace	Start	End	Length [mm]	Propagationtime 2/3 c [ns]	TDR time [ns]	TDR Sum [ns]
Data 1 P	PCB left	Flex left	92,940	0,465	0,929	0,929
Data 1 P	Flex left	Flex top	27,341	0,137	0,273	1,203
Data 1 P	Flex top	PCB top	46,700	0,234	0,467	1,670
Data 1 N	PCB left	Flex left	91,888	0,459	0,919	0,919
Data 1 N	Flex left	Flex top	27,885	0,139	0,279	1,198
Data 1 N	Flex top	PCB top	47,574	0,238	0,476	1,673
Data 2 P	PCB left	Flex left	120,712	0,604	1,207	1,207
Data 2 P	Flex left	Flex top	29,527	0,148	0,295	1,502
Data 2 P	Flex top	PCB top	67,142	0,336	0,671	2,174
Data 2 N	PCB left	Flex left	120,690	0,603	1,207	1,207
Data 2 N	Flex left	Flex top	30,177	0,151	0,302	1,509
Data 2 N	Flex top	PCB top	67,190	0,336	0,672	2,181
Data 3 P	PCB left	Flex left	106,967	0,535	1,070	1,070
Data 3 P	Flex left	Flex top	31,838	0,159	0,318	1,388
Data 3 P	Flex top	PCB top	48,969	0,245	0,490	1,878
Data 3 N	PCB left	Flex left	106,903	0,535	1,069	1,069
Data 3 N	Flex left	Flex top	32,558	0,163	0,326	1,395
Data 3 N	Flex top	PCB top	48,197	0,241	0,482	1,877
Data 4 P	PCB left	Flex left	80,359	0,402	0,804	0,804
Data 4 P	Flex left	Flex top	48,557	0,243	0,486	1,289
Data 4 P	Flex top	PCB top	143,046	0,715	1,430	2,720
Data 4 N	PCB left	Flex left	80,504	0,403	0,805	0,805
Data 4 N	Flex left	Flex top	48,560	0,243	0,486	1,291
Data 4 N	Flex top	PCB top	144,740	0,724	1,447	2,738
Data 5 P	PCB left	Flex left	98,415	0,492	0,984	0,984
Data 5 P	Flex left	Flex top	48,524	0,243	0,485	1,469
Data 5 P	Flex top	PCB top	152,094	0,760	1,521	2,990
Data 5 N	PCB left	Flex left	98,487	0,492	0,985	0,985
Data 5 N	Flex left	Flex top	48,522	0,243	0,485	1,470
Data 5 N	Flex top	PCB top	152,266	0,761	1,523	2,993
Data 6 P	PCB left	Flex left	80,386	0,402	0,804	0,804
Data 6 P	Flex left	Flex top	48,478	0,242	0,485	1,289
Data 6 P	Flex top	PCB top	135,184	0,676	1,352	2,640
Data 6 N	PCB left	Flex left	79,771	0,399	0,798	0,798
Data 6 N	Flex left	Flex top	48,481	0,242	0,485	1,283
Data 6 N	Flex top	PCB top	134,440	0,672	1,344	2,627
Data 7 P	PCB left	Flex left	47,636	0,238	0,476	0,476
Data 7 P	Flex left	Flex top	174,489	0,872	1,745	2,221
Data 7 P	Flex top	PCB top	90,921	0,455	0,909	3,130
Data 7 N	PCB left	Flex left	47,721	0,239	0,477	0,477
Data 7 N	Flex left	Flex top	175,149	0,876	1,751	2,229
Data 7 N	Flex top	PCB top	90,106	0,451	0,901	3,130
Data 8 P	PCB left	Flex left	52,772	0,264	0,528	0,528
Data 8 P	Flex left	Flex top	78,558	0,393	0,786	1,313
Data 8 P	Flex top	PCB top	46,291	0,231	0,463	1,776
Data 8 N	PCB left	Flex left	55,677	0,278	0,557	0,557
Data 8 N	Flex left	Flex top	78,420	0,392	0,784	1,341
Data 8 N	Flex top	PCB top	46,345	0,232	0,463	1,804
Data 9 P	PCB left	Flex left	77,239	0,386	0,772	0,772
Data 9 P	Flex left	Flex top	78,982	0,395	0,790	1,562
Data 9 P	Flex top	PCB top	65,175	0,326	0,652	2,214
Data 9 N	PCB left	Flex left	78,820	0,394	0,788	0,788
Data 9 N	Flex left	Flex top	78,945	0,395	0,789	1,578
Data 9 N	Flex top	PCB top	63,795	0,319	0,638	2,216
Data 10 P	PCB left	Flex left	63,555	0,318	0,636	0,636
Data 10 P	Flex left	Flex top	79,280	0,396	0,793	1,428
Data 10 P	Flex top	PCB top	43,250	0,216	0,432	1,861
Data 10 N	PCB left	Flex left	65,159	0,326	0,652	0,652
Data 10 N	Flex left	Flex top	79,277	0,396	0,793	1,444
Data 10 N	Flex top	PCB top	41,796	0,209	0,418	1,862

Table 9: Propagation times and time domains



(a) DATA1

(b) DATA7

Figure 38: TDR examples of rising impedance over flexprint length

Flex	Power line	current	err current	voltage	err voltage	power	err power	resistance	err resistance
		A	A	mV	mV	mW	mW	m	m
1	1	0,49996	0,00001	33,610	0,010	16,807	0,002	67,23	0,01
1	2	0,50000	0,00001	27,010	0,010	13,505	0,003	54,02	0,01
1	3	0,50001	0,00001	50,590	0,010	25,304	0,003	101,22	0,01
1	4	0,50000	0,00001	31,940	0,010	15,971	0,003	63,89	0,01
1	5	0,49999	0,00001	63,160	0,010	31,580	0,010	126,36	0,01
1	6	0,50001	0,00001	42,070	0,010	21,035	0,003	84,10	0,01
2	1	0,49991	0,00001	33,240	0,010	16,622	0,003	66,50	0,01
2	2	0,49998	0,00001	26,670	0,010	13,327	0,003	53,35	0,01
2	3	0,50000	0,00001	49,850	0,010	24,920	0,002	99,69	0,01
2	4	0,50002	0,00001	31,514	0,004	15,758	0,003	63,03	0,01
2	5	0,50002	0,00001	62,983	0,003	31,492	0,002	125,95	0,01
2	6	0,50002	0,00001	41,940	0,010	20,975	0,003	83,88	0,01
3	1	0,50003	0,00001	33,370	0,010	16,682	0,003	66,75	0,01
3	2	0,50001	0,00001	26,840	0,010	13,410	0,010	53,67	0,01
3	3	0,50002	0,00001	49,990	0,010	25,005	0,003	100,01	0,02
3	4	0,50003	0,00001	31,630	0,010	15,810	0,010	63,26	0,01
3	5	0,50002	0,00001	62,970	0,010	31,486	0,003	125,96	0,01
3	6	0,50001	0,00001	41,889	0,002	20,943	0,003	83,76	0,01
4	1	0,50005	0,00001	33,557	0,003	16,778	0,003	67,09	0,01
4	2	0,50001	0,00001	27,002	0,003	13,502	0,003	54,01	0,01
4	3	0,50001	0,00001	49,789	0,003	24,892	0,003	99,56	0,01
4	4	0,50003	0,00001	31,639	0,003	15,823	0,003	63,28	0,01
4	5	0,50002	0,00001	63,021	0,003	31,509	0,003	126,03	0,01
4	6	0,50004	0,00001	41,888	0,003	20,942	0,003	83,75	0,01
5	1	0,50003	0,00001	33,799	0,003	16,895	0,003	67,60	0,01
5	2	0,50001	0,00001	27,099	0,003	13,542	0,003	54,15	0,01
5	3	0,50003	0,00001	50,319	0,003	25,167	0,003	100,65	0,01
5	4	0,50000	0,00001	31,914	0,003	15,962	0,003	63,82	0,01
5	5	0,50001	0,00001	63,304	0,003	31,645	0,003	126,60	0,01
5	6	0,50000	0,00001	42,030	0,003	21,017	0,003	84,06	0,01

Table 10: Resistance measurements

Data Source: MATH2 SSC: Off Phase Reference: None	Data Rate: 1.6 Gbps Pattern: 127 bits Sample Count: 14.20 M	Filter: False Channel: False Equalizer: None

Jitter (Decision Threshold: -7.30 mV)			**Noise** (Sampling Phase: 0 UI)		
Random Jitter			**Random Noise**		
RJ (RMS)	=	3.50 ps	RN (RMS)	=	989.58 uV
RJ(h) (RMS)	=	3.47 ps	RN(v) (RMS)	=	989.46 uV
RJ(v) (RMS)	=	415.19 fs	RN(h) (RMS)	=	15.01 uV
Deterministic Jitter			**Deterministic Noise**		
DJ	=	78.39 ps	DN	=	243.74 mV
DDJ	=	68.21 ps	DDN	=	238.22 mV
DCD	=	2.41 ps	DDN(level 1)	=	232.12 mV
DDPWS	=	44.79 ps	DDN(level 0)	=	241.98 mV
BUJ(d-d)	=	1.97 ps	BUN(d-d)	=	4.90 mV
PJ	=	6.44 ps	PN	=	3.26 mV
PJ(h)	=	6.29 ps	PN(v)	=	3.26 mV
PJ(v)	=	1.37 ps	PN(h)	=	27.21 uV
NPJ(d-d)	=	1.22 ps	NPN(d-d)	=	3.58 mV
Total Jitter @ BER			**Total Noise @ BER**		
TJ (1E-12)	=	117.07 ps	TN (1E-12)	=	256.13 mV
Eye Opening (1E-12)	=	507.93 ps	Eye Opening (1E-12)	=	432.07 mV
			Eye Amplitude	=	688.20 mV
Dual Dirac			**SSC Modulation**		
RJ(d-d)	=	3.85 ps	Magnitude	=	0 ppm
DJ(d-d)	=	62.85 ps	Frequency	=	0 Hz

(a) DATA2 only

Data Source: MATH2 SSC: Off Phase Reference: None	Data Rate: 1.6 Gbps Pattern: 127 bits Sample Count: 12.06 M	Filter: False Channel: False Equalizer: None

Jitter (Decision Threshold: -7.47 mV)			**Noise** (Sampling Phase: 0 UI)		
Random Jitter			**Random Noise**		
RJ (RMS)	=	3.41 ps	RN (RMS)	=	980.71 uV
RJ(h) (RMS)	=	3.39 ps	RN(v) (RMS)	=	980.38 uV
RJ(v) (RMS)	=	409.41 fs	RN(h) (RMS)	=	25.58 uV
Deterministic Jitter			**Deterministic Noise**		
DJ	=	77.68 ps	DN	=	252.90 mV
DDJ	=	62.85 ps	DDN	=	246.16 mV
DCD	=	1.09 ps	DDN(level 1)	=	233.34 mV
DDPWS	=	49.57 ps	DDN(level 0)	=	249.51 mV
BUJ(d-d)	=	2.44 ps	BUN(d-d)	=	4.57 mV
PJ	=	5.00 ps	PN	=	5.79 mV
PJ(h)	=	4.37 ps	PN(v)	=	5.79 mV
PJ(v)	=	2.42 ps	PN(h)	=	33.03 uV
NPJ(d-d)	=	1.89 ps	NPN(d-d)	=	2.61 mV
Total Jitter @ BER			**Total Noise @ BER**		
TJ (1E-12)	=	113.12 ps	TN (1E-12)	=	263.60 mV
Eye Opening (1E-12)	=	511.88 ps	Eye Opening (1E-12)	=	427.04 mV
			Eye Amplitude	=	690.64 mV
Dual Dirac			**SSC Modulation**		
RJ(d-d)	=	3.54 ps	Magnitude	=	0 ppm
DJ(d-d)	=	63.20 ps	Frequency	=	0 Hz

(b) DATA2 measured with disturbing signal from DATA1, DATA3 and BUS2

Figure 39: Jitter and noise breakdown

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Erklärung

Ich versichere, dass ich diese Arbeit selbstständig verfasst und keine anderen als die angegebenen Quellen und Hilfsmittel benutzt habe.

Heidelberg, den .....,