MuTRiG: A Silicon Photomultiplier Readout ASIC with High Timing Precision and High Event Rate Capability

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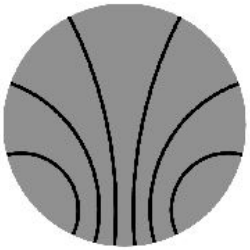
12.09.2017



Kirchhoff-
Institut
für Physik

Outline

- Motivation - Mu3e Experiment
- MuTRiG ASIC
- Jitter Measurements
- Maximum Event Rate Measurements
- Serial Data Link Measurements
- Summary

Motivation - Mu3e Experiment

Goal

Search for $\mu^+ \rightarrow e^+e^+e^-$ at 10^{-16} level

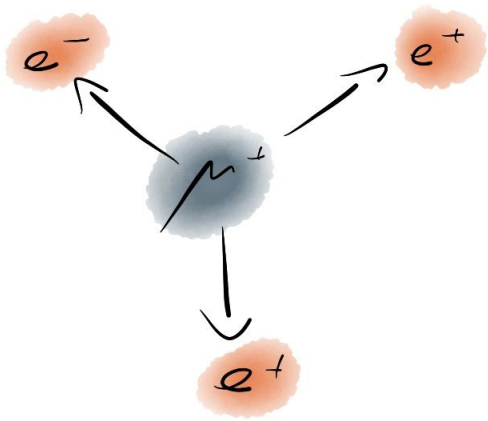
Forbidden in standard model (BR < 10^{-52})

Clear sign for new physics

Challenge

Observe 1x10^{17} muon decay within a reasonable measurement time

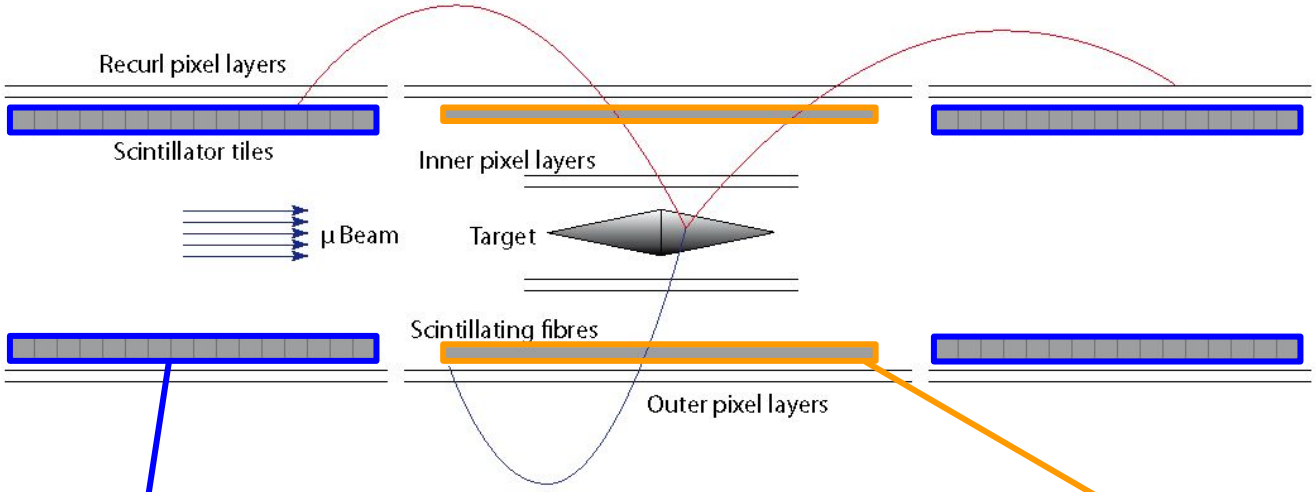
Require high event rate, high geometrical acceptance and high efficiency

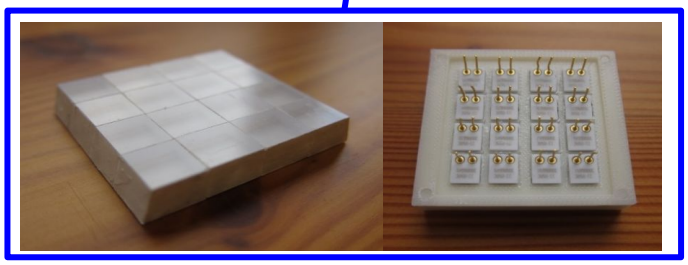


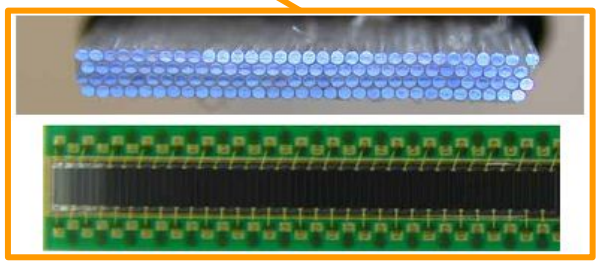
Suppress background to below a level Of 10^{-16}

Require good momentum, vertex resolution (HV-MAPS) and timing resolution (Tile/Fiber detector, MuTRiG)

Mu3e Experiment Requirement (Phase I)







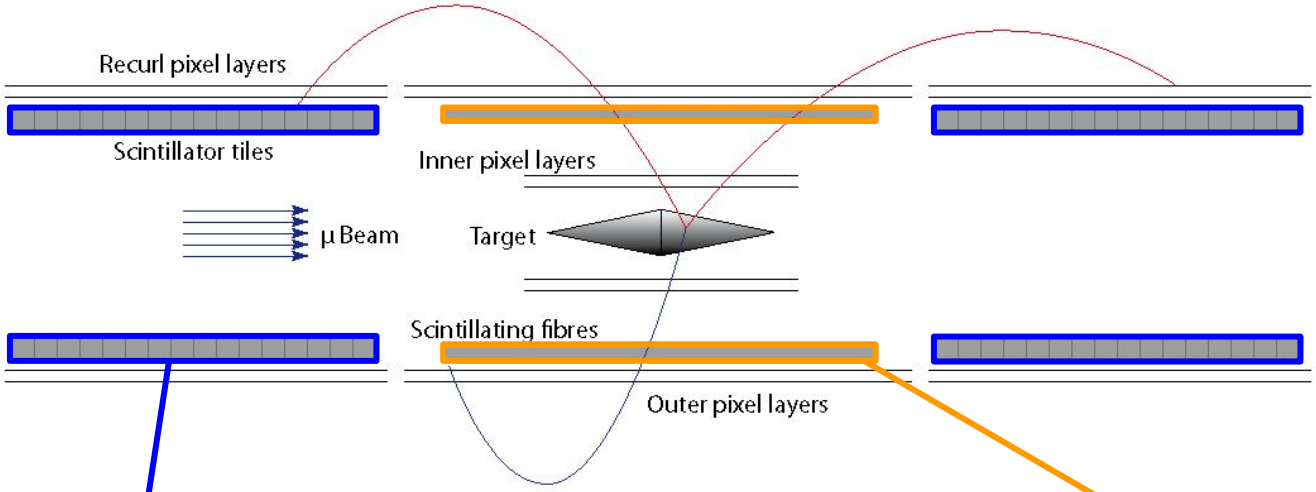
Mu3e tile detectors requirements (6272 SiPM channels):

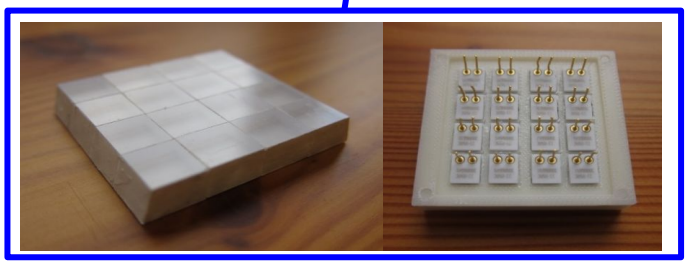
- Timing: 100 ps
- Event rate : 60 kHz/ch

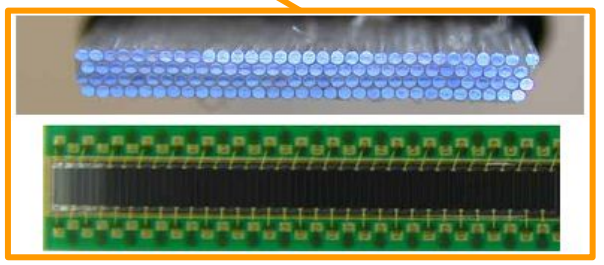
Mu3e fiber detectors requirements (3072 SiPM channels):

- Timing: 500 ps
- Event rate : 700 kHz/ch - 1 MHz/ch

Mu3e Experiment Requirement (Phase I)







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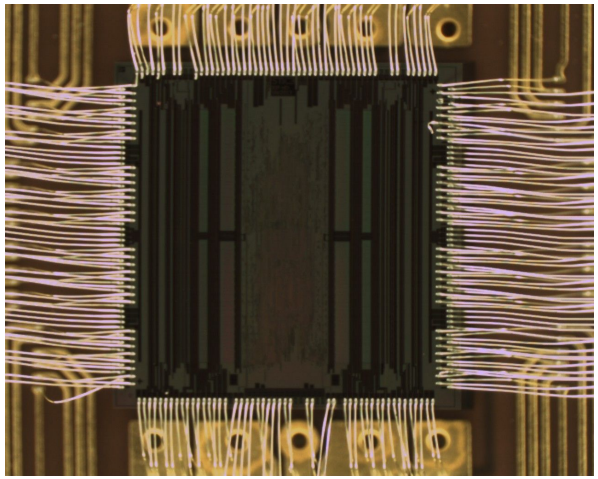
From STiC to MuTRiG

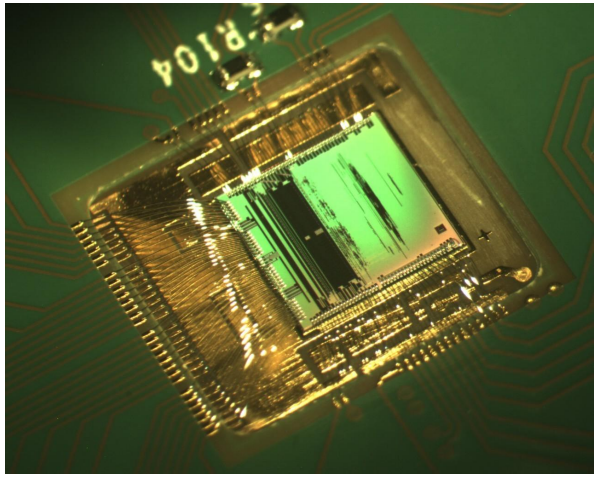
STiCv3 ASIC

- 64-channel mixed-signal SiPM readout ASIC for precise timing applications
  - Fully-differential analog front-end
  - 50 ps time binning TDC
  - On-chip digital circuit for event data processing
  - Transferring data to DAQ over 160 Mbps serial data link (max. event rate: ~40 kHz/ch)



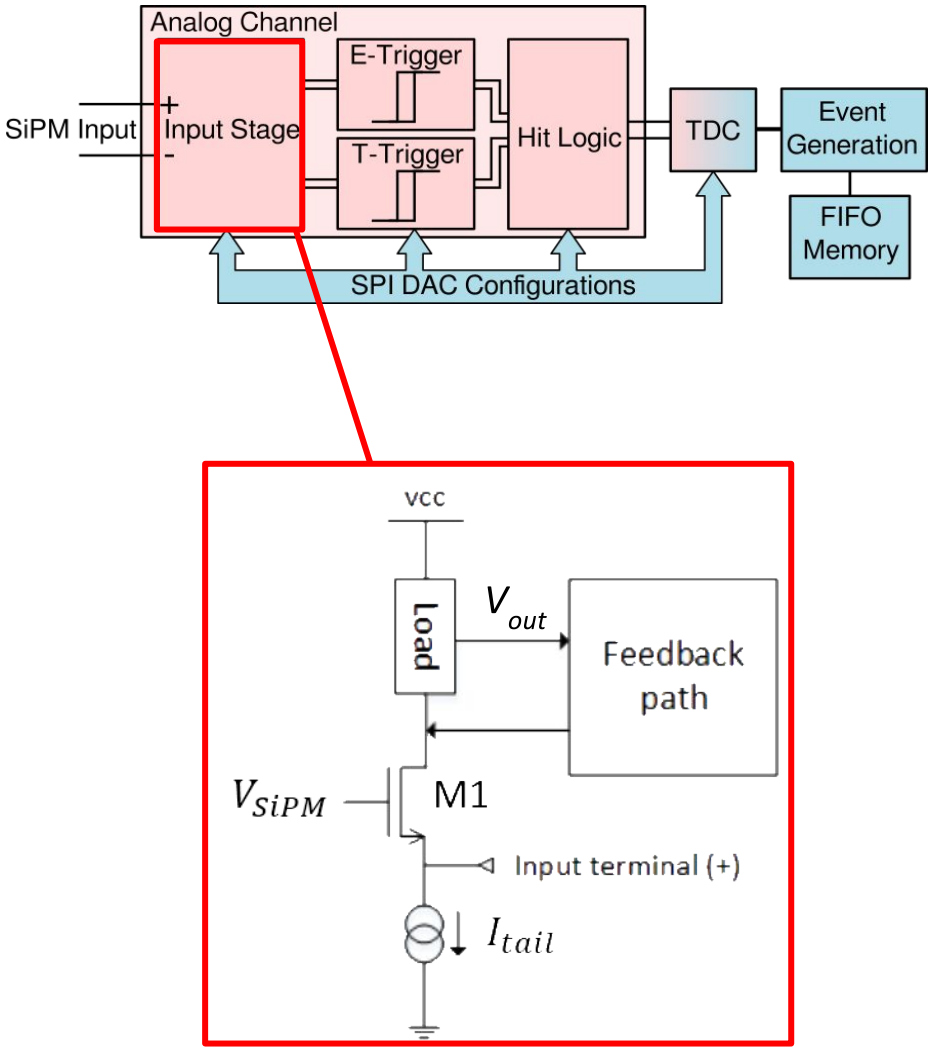
MuTRiG ASIC

- 32 channels successor of STiCv3
- Preserve the timing performance
  - Same Analog FE/TDC as STiCv3
- Increase the event rate capability
  - Gigabit serial data link (1.25 Gbps)
  - Switchable event length
- Add more digital functionalities



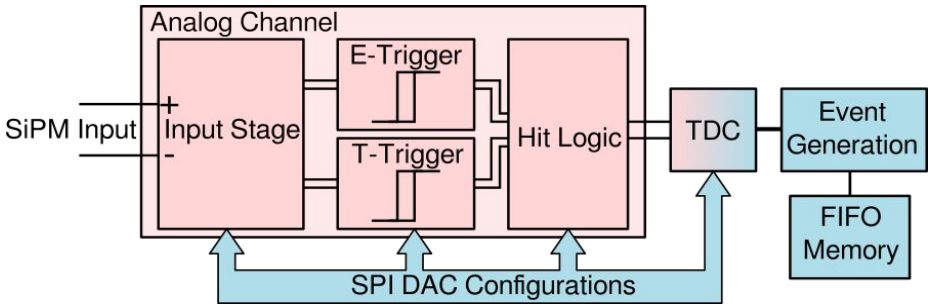
Front-End and Trigger Principle

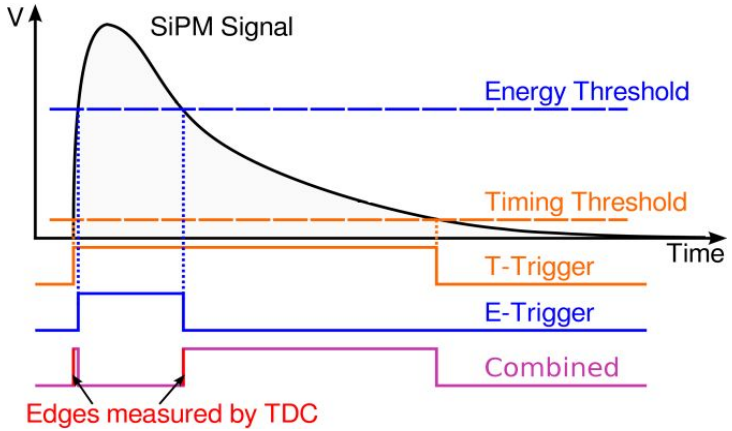
- SiPM bias tuning (V_{SiPM})



Front-End and Trigger Principle

- SiPM bias tuning
- Separate timing and energy threshold tuning
- Energy measurement based on linearized Time-over-Threshold (ToT) method
- Encode arrival time and energy information into two rising edges of the combined signal

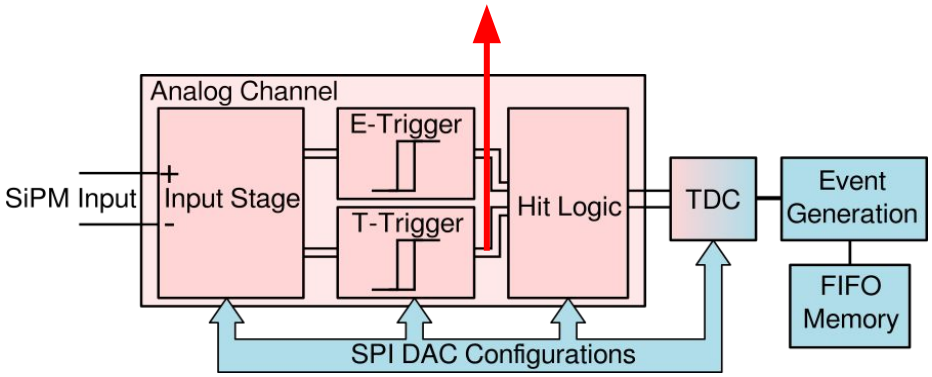


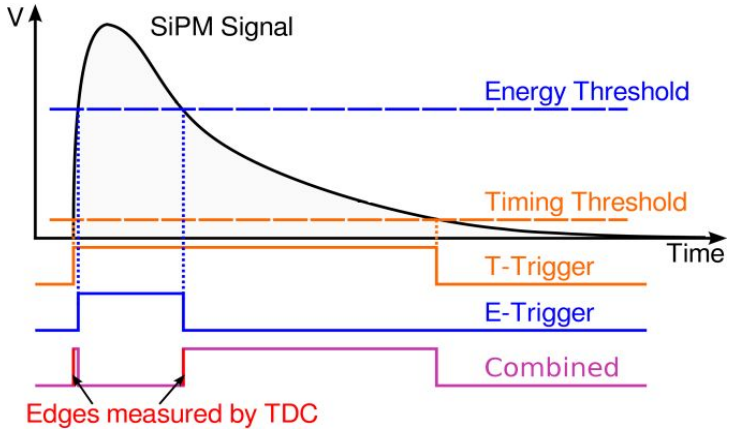


Front-End and Trigger Principle

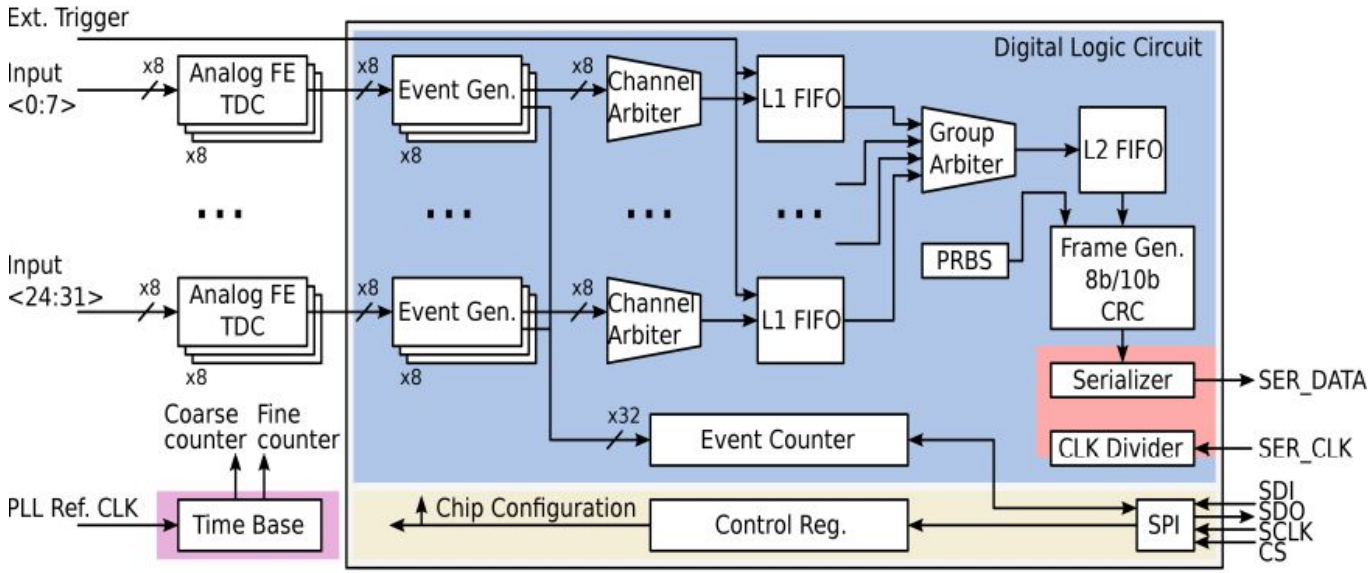
Monitor output for characterisation

- SiPM bias tuning
- Separate timing and energy threshold tuning
- Energy measurement based on linearized Time-over-Threshold (ToT) method
- Encode arrival time and energy information into two rising edges of the combined signal



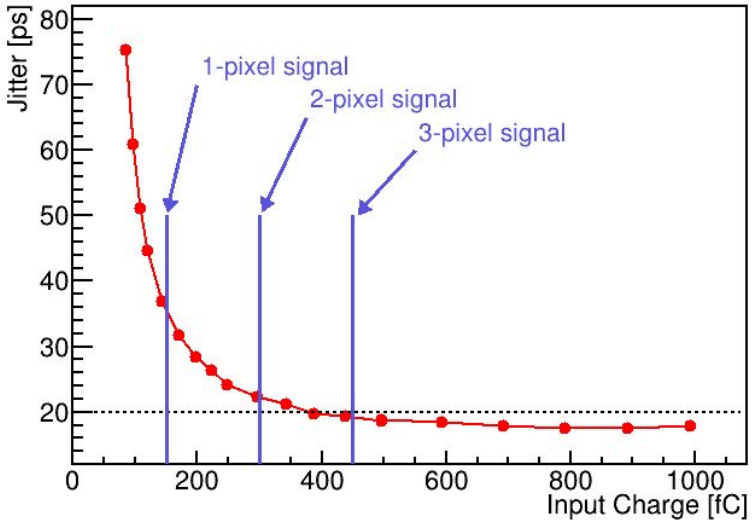


MuTRiG Chip block diagram

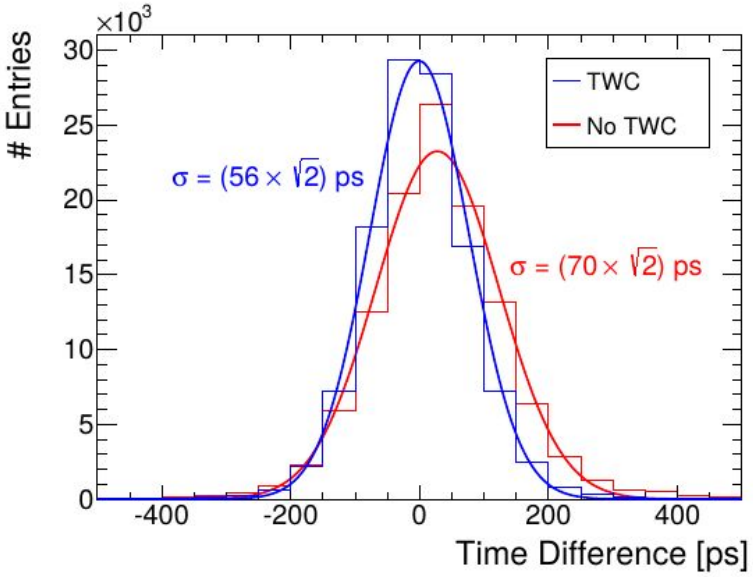


- Gigabit serial data link
- Standard/ short event length
- External trigger
- Channel event counter
- CRC for data transmission error detection
- PRBS

Reminder of STiC measurement results



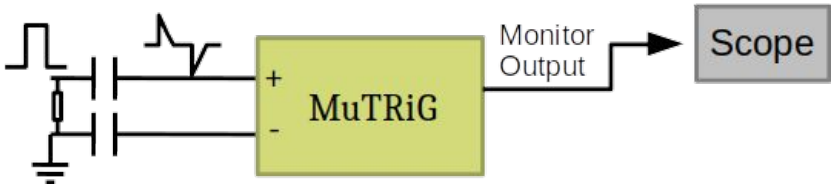
Front-End Jitter measurement[1]

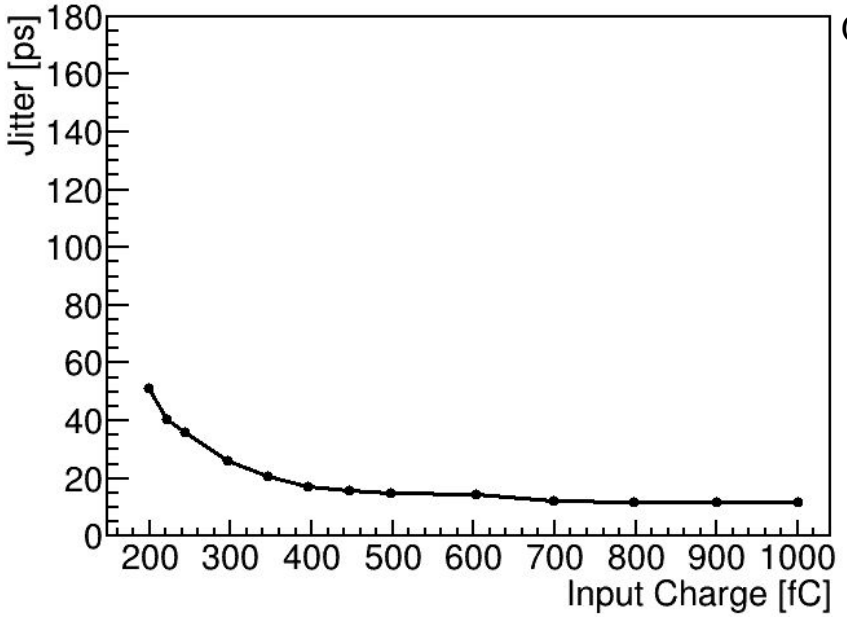


Coincidence Time Resolution with 16-channel Tile detector prototype[2]

[1] Huangshan Chen et al, A dedicated readout ASIC for Time-of-Flight Positron Emission Tomography using Silicon Photomultiplier (SiPM), Proceedings of NSS/MIC 2014, Seattle, 2014, pp. 1-5.
[2] Patrick Eckert, The Mu3e Tile Detector, Doctoral Dissertation, Heidelberg University, 2015

FE Jitter Measurements (Single Channel)

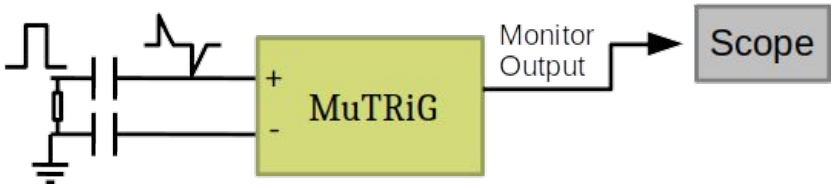


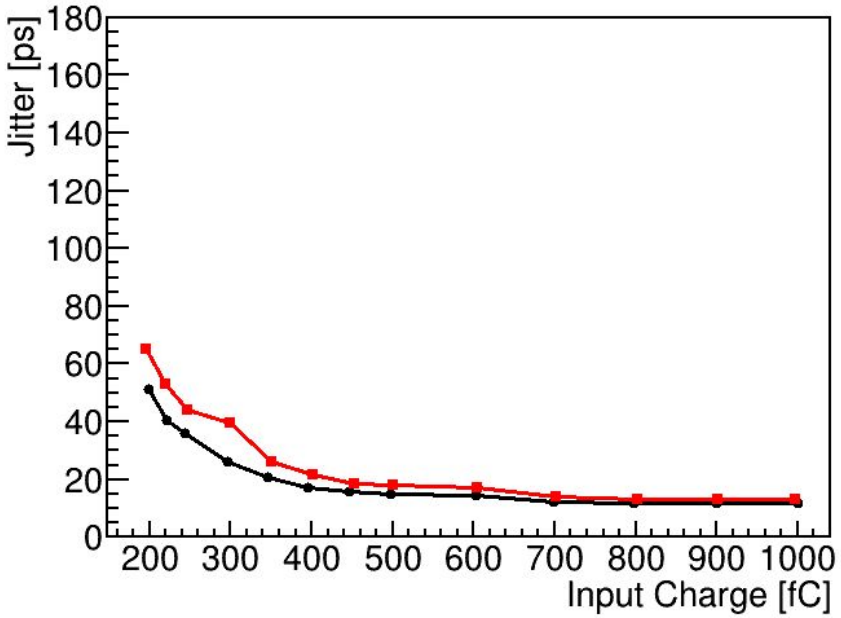


Only FE active

- FE Jitter < 20 ps when input charge > 350 fC (1 p.e.(fiber): 480 fC)

FE Jitter Measurements (Single Channel)

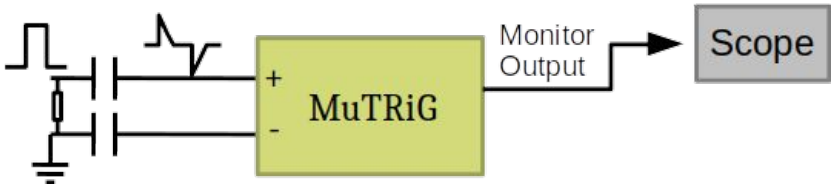


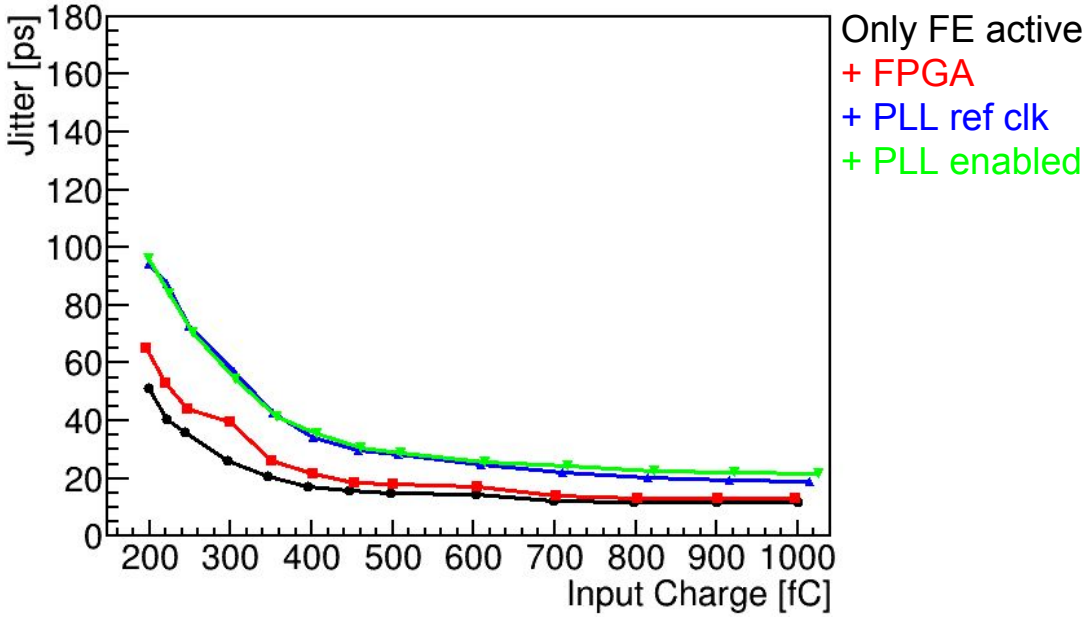


Only FE active
+ FPGA

- FE Jitter < 20 ps when input charge > 350 fC (1 p.e.(fiber): 480 fC)

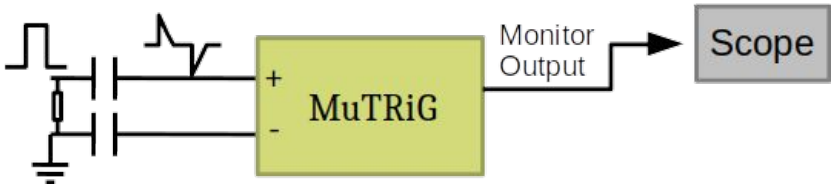
FE Jitter Measurements (Single Channel)

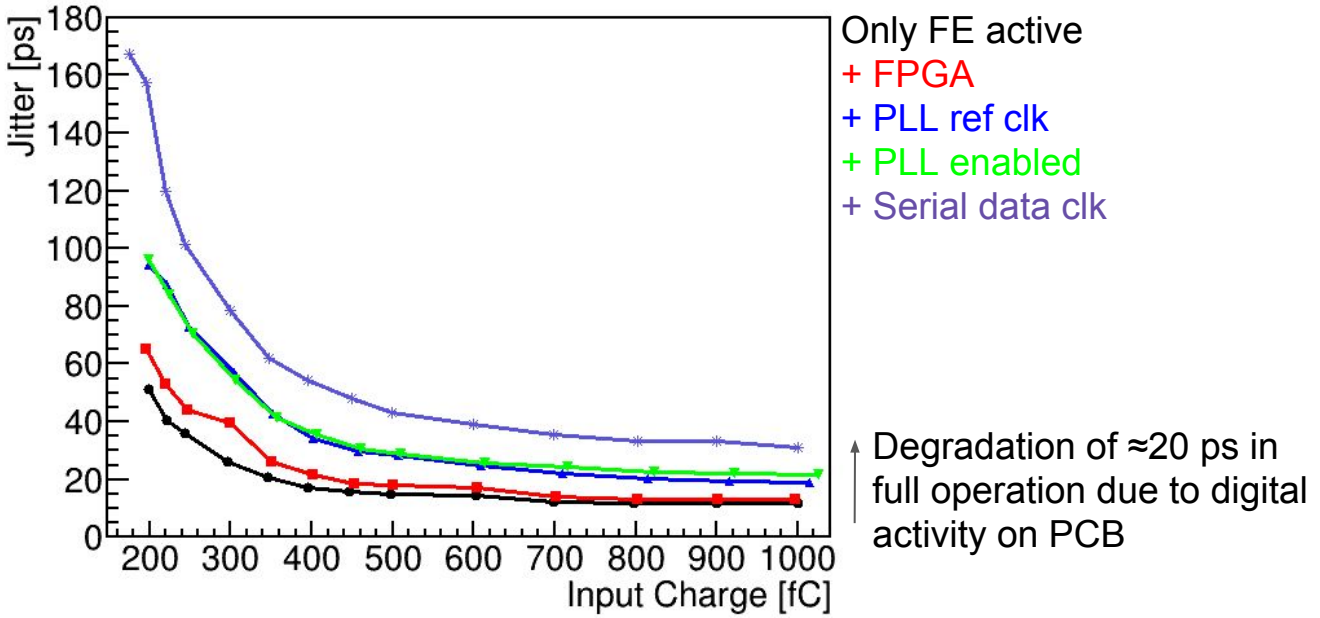




- FE Jitter < 20 ps when input charge > 350 fC (1 p.e.(fiber): 480 fC)
- PCB design problem, need better separation between analog and digital region
- On-Chip PLL activity only slightly affects the jitter performance

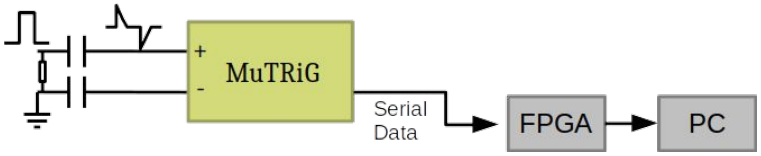
FE Jitter Measurements (Single Channel)

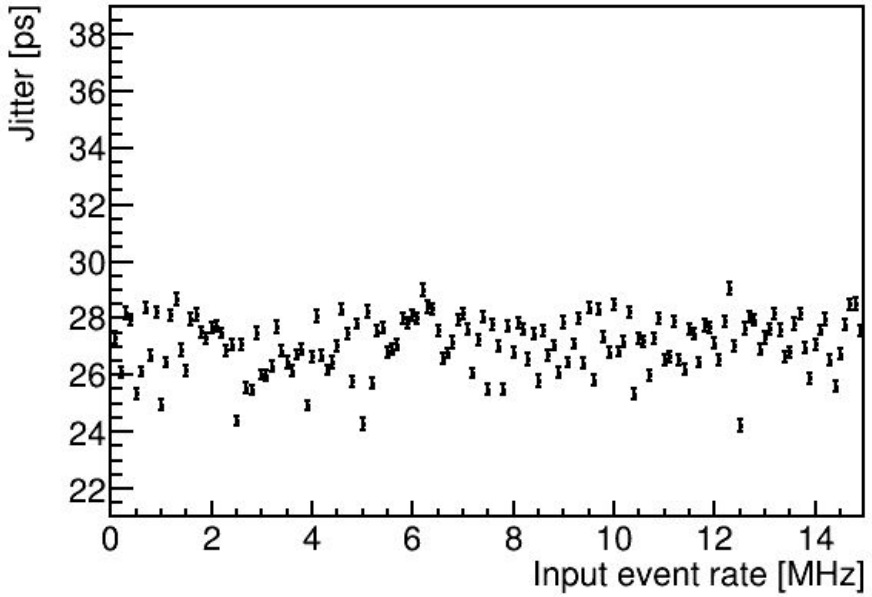




- FE Jitter < 20 ps when input charge > 350 fC (1 p.e.(fiber): 480 fC)
- PCB design problem, need better separation between analog and digital region
- On-Chip PLL activity only slightly affects the jitter performance

Full Chain Jitter Measurements

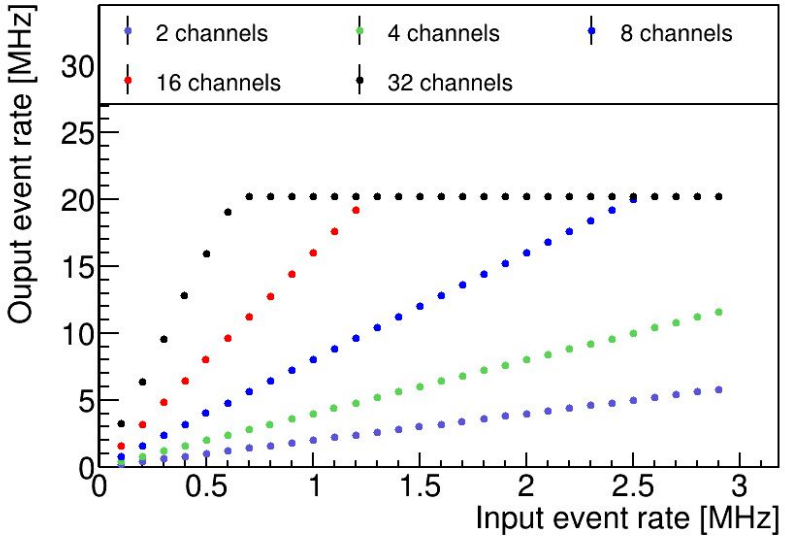




- Single channel: Jitter < 30 ps up to 15MHz input event rate

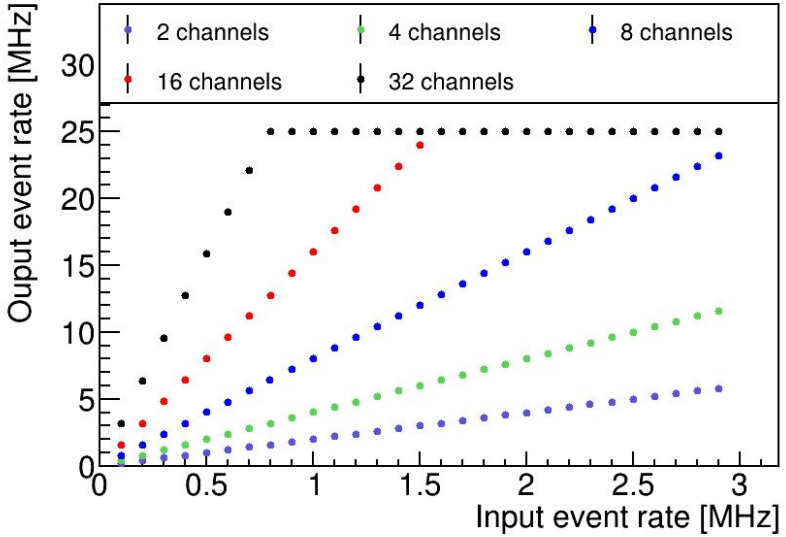
Maximum Event Rate (std / short event structure)

Standard (for tile detector)



- 48 bit/event: both time and energy info.
- Event Rate limit: 20.24 MHz (632 kHz/ch)
- More than sufficient for Mu3e Tile detector (60 kHz/ch)
- Limited by 1.25Gbps serial data link

Short (for fiber detector)

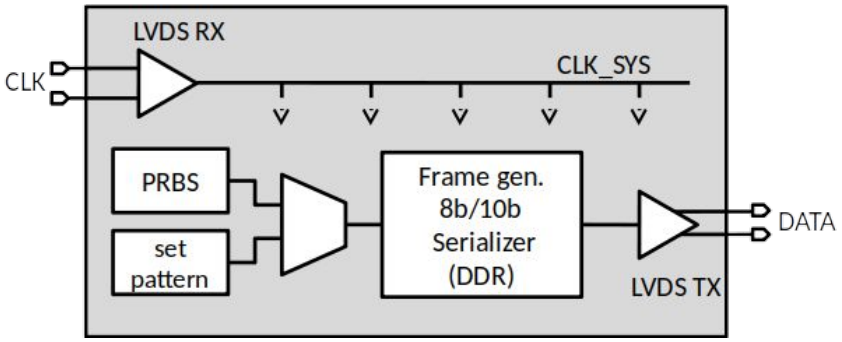


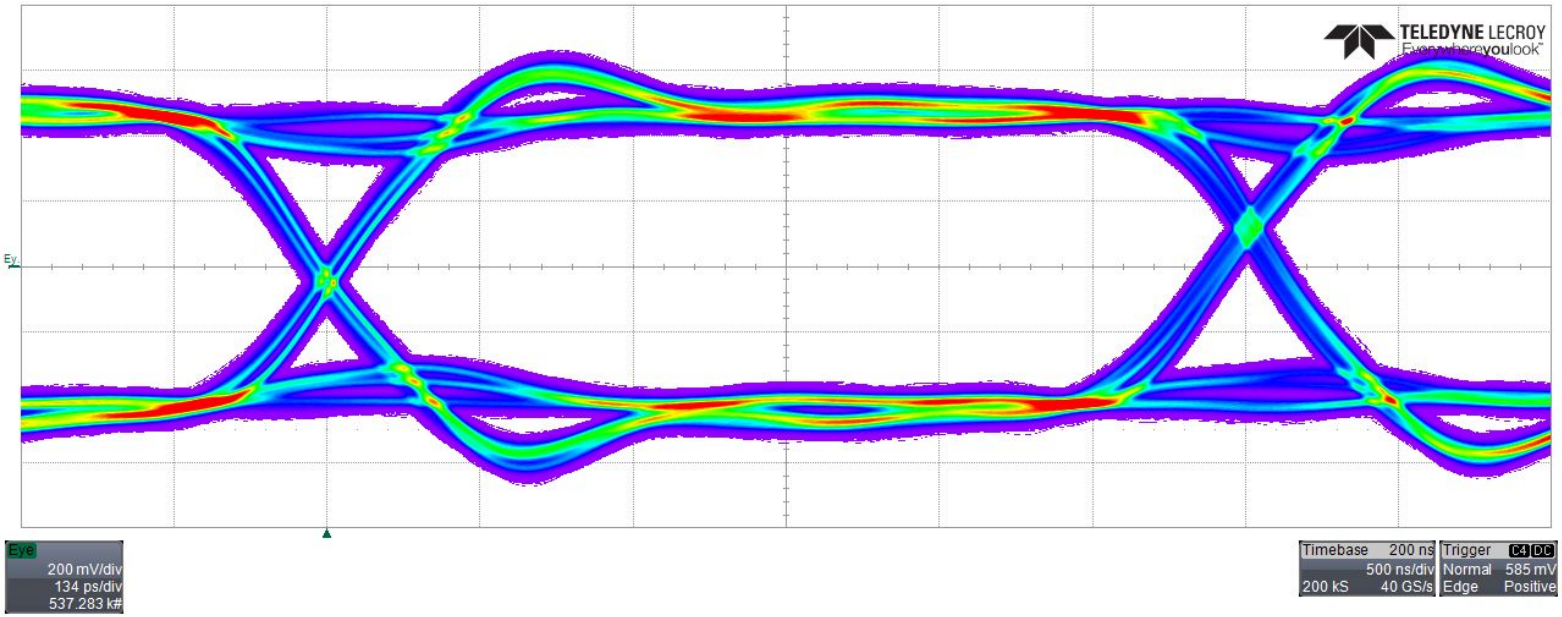
- 27 bit/event: time info. + 1 bit energy info.
- Event rate limit: 25 MHz (781 kHz/ch)
- Not sufficient for Fiber detector (700 kHz/ch - 1 MHz/ch)
- Currently limited by digital part (fixed in next tape-out)

LVDS Serial Data link

Double Data Rate Serializer + Customized LVDS TX cell
An opened eye diagram of PRBS data with 8b/10b encoding at 1.25 Gbps

BER measured with DAQ
BER < 5.90E-15 at 1.25Gbps.





Summary of MuTRiG Measurements

Quantity	Value	Conditions
Front-End Jitter	< 20ps	● Single channel ● Charge injection (> 350fC) ● Event rate: 100kHz
Full-Chain Jitter	< 30ps	● Single channel ● Charge injection (1pC) ● Event rate: up to 15MHz
Maximum Output Event Rate	20.24 MHz (632 kHz/ch) 25 MHz (781 kHz/ch)	● Standard event structure ● Short event structure
Bit Error Rate of Serial Data Link	< 5.90E-15	● @1.25Gbps