MuTRiG: A Silicon Photomultiplier Readout ASIC with High Timing Precision and High Event Rate Capability

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Outline

- Motivation - Mu3e Experiment
- MuTRiG ASIC
- Jitter Measurements
- Maximum Event Rate Measurements
- Serial Data Link Measurements
- Summary
Motivation - Mu3e Experiment

**Goal**
Search for $\mu^+ \rightarrow e^+e^+e^-$ at $10^{-16}$ level
Forbidden in standard model (BR < $10^{-52}$)
Clear sign for new physics

**Challenge**
Observe $1 \times 10^{17}$ muon decay within a reasonable measurement time
Require high event rate, high geometrical acceptance and high efficiency

Suppress background to below a level of $10^{-16}$
Require good momentum, vertex resolution (HV-MAPS) and timing resolution (Tile/Fiber detector, MuTRiG)
Mu3e tile detectors requirements (6272 SiPM channels):
- Timing: 100 ps
- Event rate: 60 kHz/ch

Mu3e fiber detectors requirements (3072 SiPM channels):
- Timing: 500 ps
- Event rate: 700 kHz/ch - 1 MHz/ch
Mu3e Experiment Requirement (Phase I)

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From STiC to MuTRiG

STiCv3 ASIC
- 64-channel mixed-signal SiPM readout ASIC for precise timing applications
  - Fully-differential analog front-end
  - 50 ps time binning TDC
  - On-chip digital circuit for event data processing
  - Transferring data to DAQ over 160 Mbps serial data link (max. event rate: ~40 kHz/ch)

MuTRiG ASIC
- 32 channels successor of STiCv3
- Preserve the timing performance
  - Same Analog FE/TDC as STiCv3
- Increase the event rate capability
  - Gigabit serial data link (1.25 Gbps)
  - Switchable event length
- Add more digital functionalities
Front-End and Trigger Principle

- SiPM bias tuning ($V_{SiPM}$)
Front-End and Trigger Principle

- SiPM bias tuning
- Separate timing and energy threshold tuning
- Energy measurement based on linearized Time-over-Threshold (ToT) method
- Encode arrival time and energy information into two rising edges of the combined signal
Front-End and Trigger Principle

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MuTRiG Chip block diagram

- Gigabit serial data link
- Standard/short event length
- External trigger
- Channel event counter
- CRC for data transmission error detection
- PRBS
Reminder of STiC measurement results

Front-End Jitter measurement\[^{[1]}\]

Coincidence Time Resolution with 16-channel Tile detector prototype\[^{[2]}\]

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FE Jitter Measurements
(Single Channel)

- FE Jitter < 20 ps when input charge > 350 fC (1 p.e.(fiber): 480 fC)
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- On-Chip PLL activity only slightly affects the jitter performance
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Degradation of ≈20 ps in full operation due to digital activity on PCB
Full Chain Jitter Measurements

- Single channel: Jitter < 30 ps up to 15MHz input event rate
Maximum Event Rate (std / short event structure)

- 48 bit/event: both time and energy info.
- Event Rate limit: 20.24 MHz (632 kHz/ch)
- More than sufficient for Mu3e Tile detector (60 kHz/ch)
- Limited by 1.25Gbps serial data link

- 27 bit/event: time info. + 1 bit energy info.
- Event rate limit: 25 MHz (781 kHz/ch)
- Not sufficient for Fiber detector (700 kHz/ch - 1 MHz/ch)
- Currently limited by digital part (fixed in next tape-out)
LVDS Serial Data link

Double Data Rate Serializer + Customized LVDS TX cell
An opened eye diagram of PRBS data with 8b/10b encoding at 1.25 Gbps

BER measured with DAQ
BER < 5.90E-15 at 1.25Gbps.
# Summary of MuTRiG Measurements

<table>
<thead>
<tr>
<th>Quantity</th>
<th>Value</th>
<th>Conditions</th>
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</thead>
<tbody>
<tr>
<td>Front-End Jitter</td>
<td>&lt; 20ps</td>
<td>• Single channel</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Charge injection (&gt; 350fC)</td>
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<tr>
<td></td>
<td></td>
<td>• Event rate: 100kHz</td>
</tr>
<tr>
<td>Full-Chain Jitter</td>
<td>&lt; 30ps</td>
<td>• Single channel</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Charge injection (1pC)</td>
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<tr>
<td></td>
<td></td>
<td>• Event rate: up to 15MHz</td>
</tr>
<tr>
<td>Maximum Output Event Rate</td>
<td>20.24 MHz (632 kHz/ch)</td>
<td>• Standard event structure</td>
</tr>
<tr>
<td></td>
<td>25 MHz (781 kHz/ch)</td>
<td>• Short event structure</td>
</tr>
<tr>
<td>Bit Error Rate of Serial Data Link</td>
<td>&lt; 5.90E-15</td>
<td>• @1.25Gbps</td>
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