Performance and integration studies of a first large scale HV-CMOS prototype

Lennart Huth
Physikalisches Institut Heidelberg

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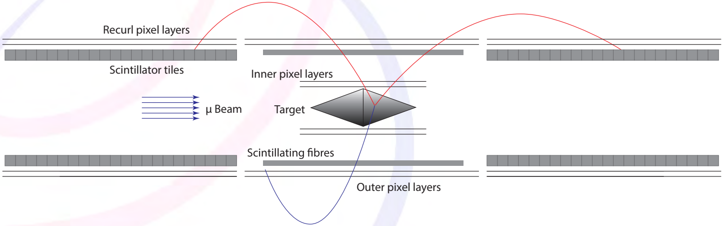
INTERNATIONAL MAX PLANCK RESEARCH SCHOOL
PTFS FOR PRECISION TESTS OF FUNDAMENTAL SYMMETRIES

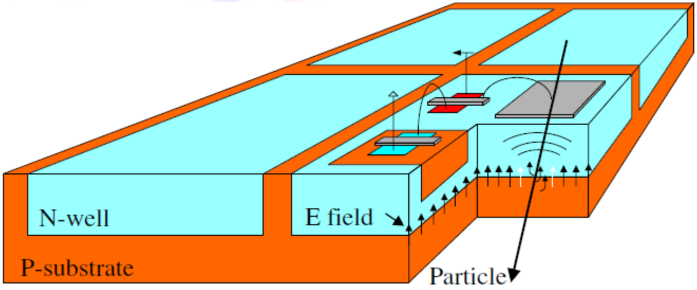
Motivation

- Mu3e searches cLFV
- Final SES target: 1 in 10^{16}
- High rate (10^9 muons/s)
- Low momentum
  $\rightarrow$ Scattering dominates resolution
- Almost everything will be background
  $\rightarrow$ Need novel pixel tracker HV-MAPS



HV-MAPS

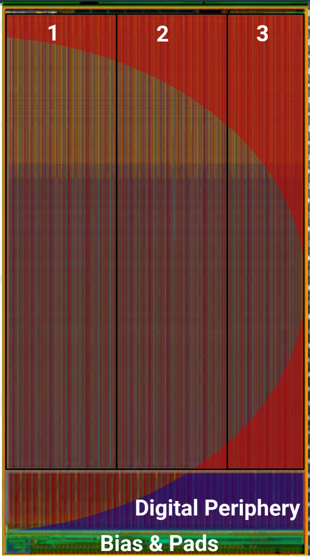
- Monolithic sensor
- p-n-junction
- HV between p-n
- Drift based charge collection
- In-pixel amplification
- Digital partner cell with
  - → Digitization
  - → Time stamping
  - → ToT/charge measure
- RO statemachine and serializer



(I.Peric, P. Fischer et al., NIM A 582 (2007) 876)

MuPix8 in numbers

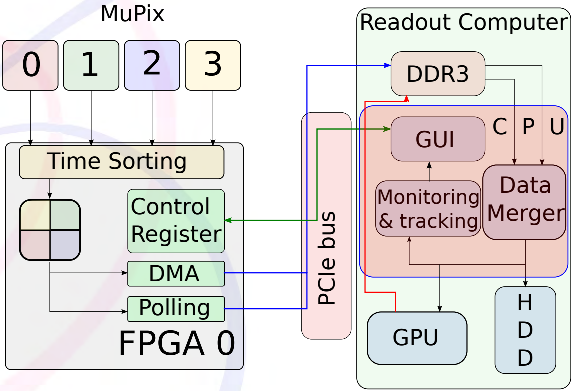
- 128 x 200 pixel
- 80 x 81 μm^2 pixel size
- 4 LVDS links at 1.25 GBit/s
- 2 comparators
- 2/3 bit tuneDACs
- All crucial pads on bottom side
- Pixel masking
- Temperature stable voltage references
- On-chip thresholds
- Temperature diode

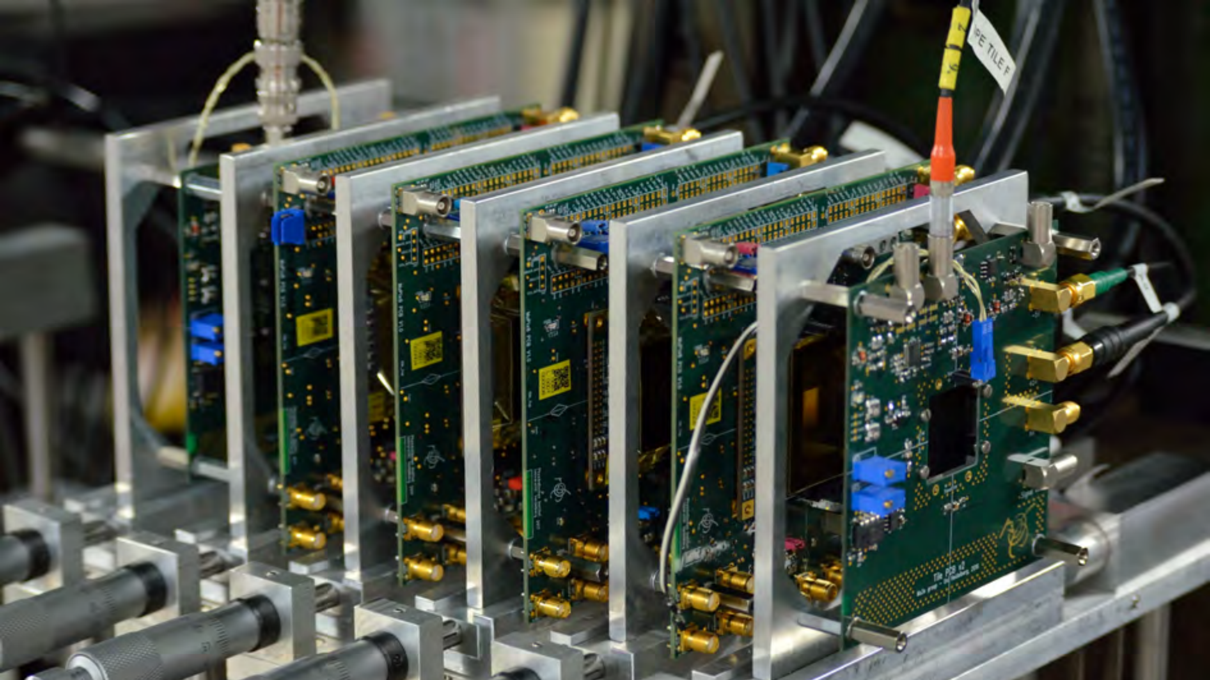


MuPix Telescope

MuPix Telescope

- 4 MuPix8 layers
- 2 tiles for time reference
- On-FPGA time sorting and data buffering optional
- FPGA to steer sensors and receive data
- Data transfer to PC via polling or DMA
- Multi-threaded software DAQ
- Results within 5 mins after data taking
- MuPix/AtlasPix used as DUT
  $\rightarrow$ Only MuPix in this talk

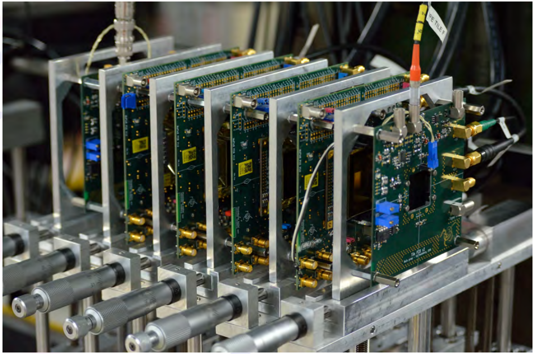



PE TILE F

Test beam measurements
- all results are preliminary!

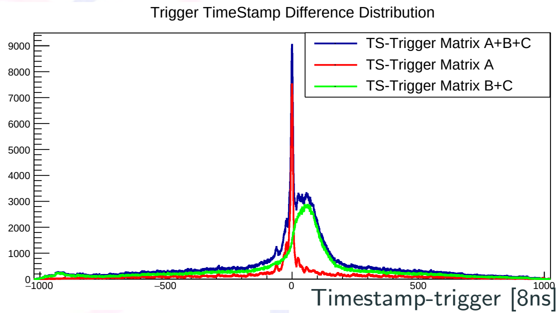
setup and runs

- 2 campaigns at desy
- Telescope setup and mimosa setup in use
- Tested various settings and sensors
- Time resolution, efficiency, noise, clustering and crosstalk
- Data analysis still ongoing



Time resolution

- Matrix A uses the transmission scheme from MuPix7
- Matrix B+C use a new transmission scheme and is not optimized
- Matrix A has significantly better time resolution
- We will focus on Matrix A for the rest of the talk
- Low threshold



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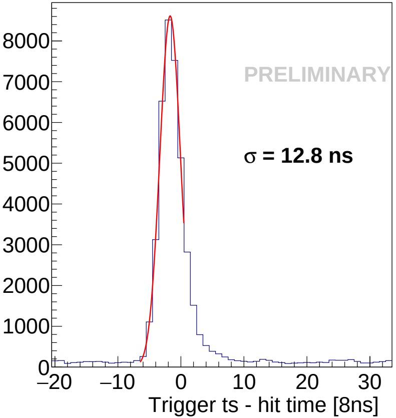

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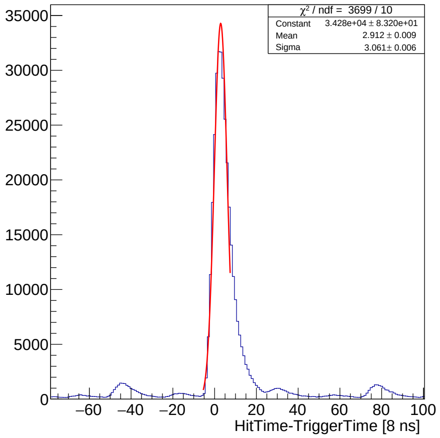
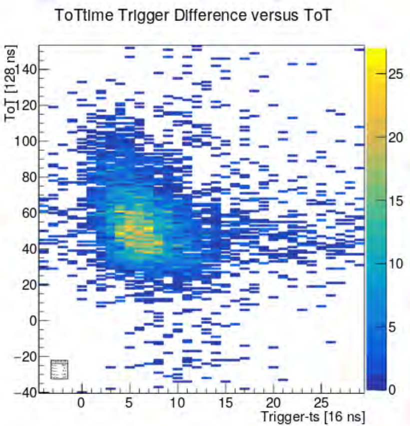
- After reverting a feature on the PCB, which doubled the available current, resolution of 24 ns are observed

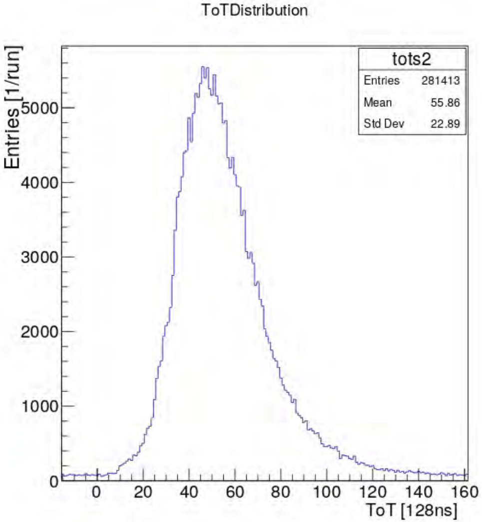


ToT and Timewalk

ToT and timewalk maesurements

ckdivend1=0x1, ckdivend2=0xf

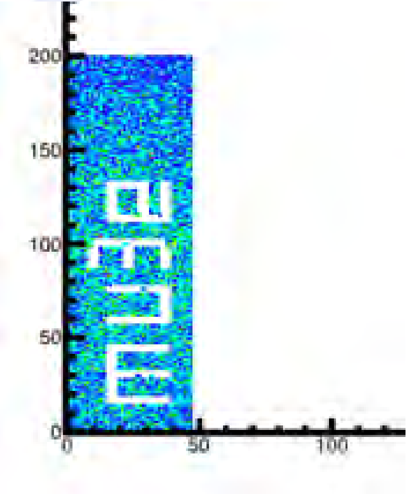




Pixel masking

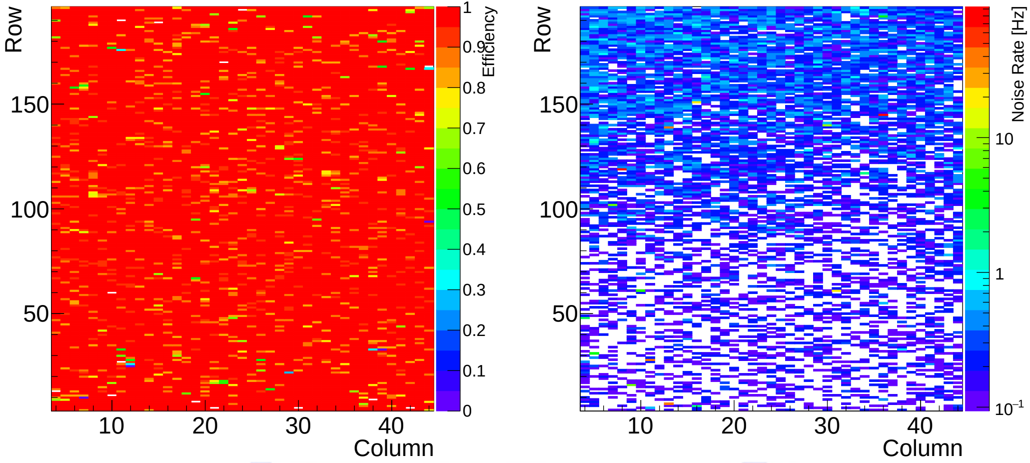
Pixel masking

- 25k pixels
- Some will be really noisy/broken
  → pixel masking
- Tested by drawing a nice logo
- Routine can be used in telescope and single setup
- Voltage level to store masking slightly to high - some pixels are not masked correctly.



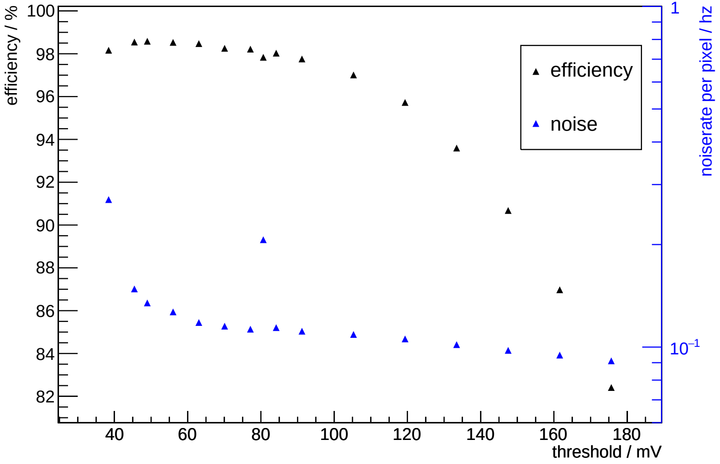
Efficiency and noise

Threshold 45 mV



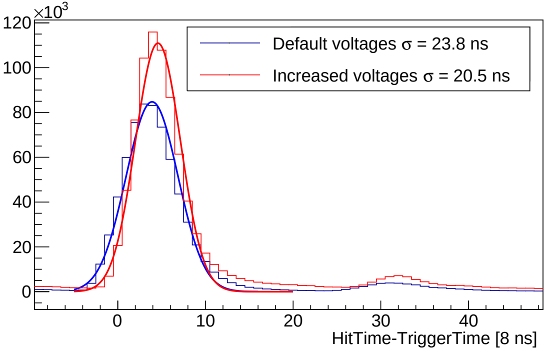
Thresholdscan at -30V

- Essentially noise free (mu3e allows up to 10 Hz/pixel)
- Chip untuned
- Up to 25 pixels ignored in analysis
- 98.5 % efficiency seen
- HV is only -30 V
  → HV can be increased



Increasing Bias Voltages

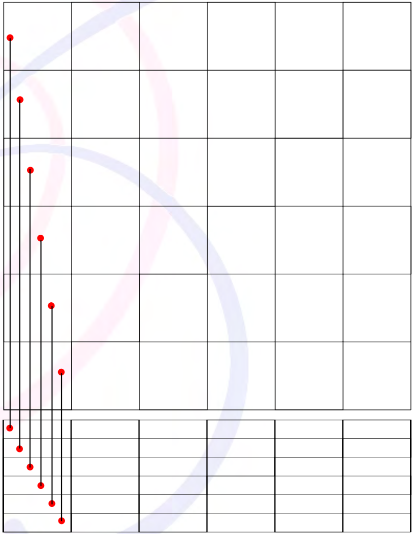
- VDD/VDDA = 1.9 V
- VSSA = 1.1 V
- Efficiency of 99.1%
- Time resolution improves by 15%
- Noise stays unchanged
- Substantial voltage drop over the MuPix8



Crosstalk and clustering

Crosstalk

- Connection lines between active pixel and digital periphery are crosstalk effected
- Crosstalk can be calculated by looking at differences in vertical and horizontal cluster sizes (pixels are squared)
- Double and triple cluster in 1d indicate crosstalk
- Line crosstalk only in vertical direction
  $\rightarrow$ 11.8 % for a threshold of 45 mV



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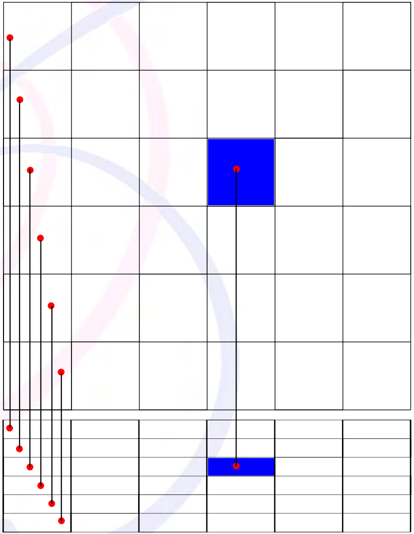

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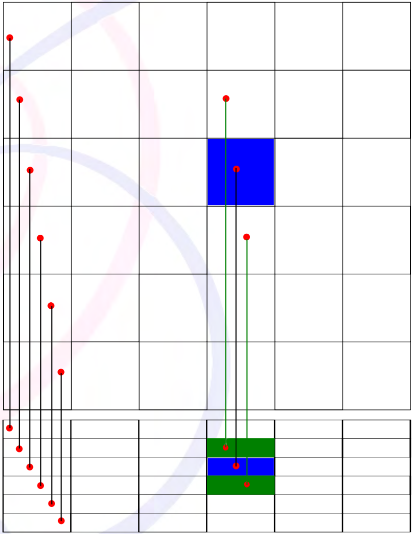

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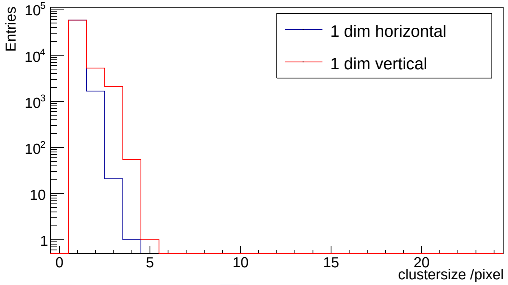
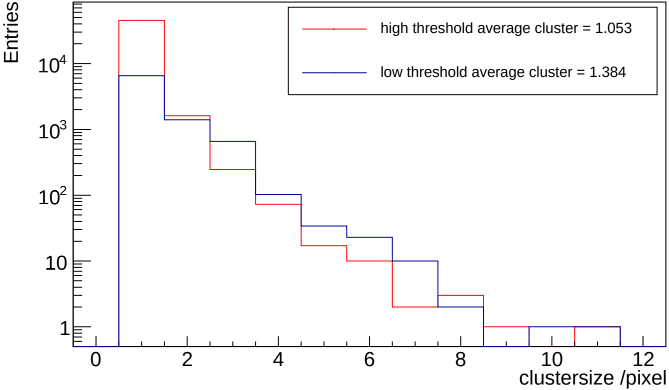


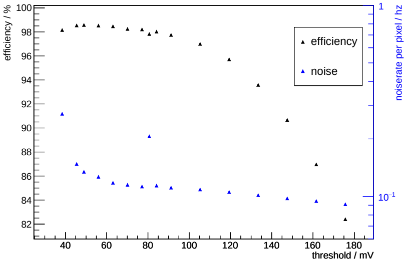
Clustering

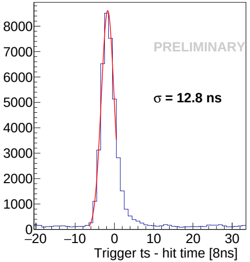
- First studies → very preliminary
- Only clusters with matched hits are counted
- Cluster size 180 mV threshold: 1.053
- Cluster size 45 mV threshold: 1.384
- Cluster sizes are effected by crosstalk



Summary and Outlook

- MuPix8 telescope in operation and functional
- Time resolution of 12.8 ns (20 ns low power settings)
- Efficiencies above 98% at low noise (99.1% for increased supply voltages)
- No timewalk observed at operational thresholds
- Crosstalk and clustering seen, but seems to be smaller than expected - average clustersize < 1.4
- Increasing VDDA, VDD and VSSA by 100mV each improves performance
- Injection tests and lab studies in preparation/ongoing

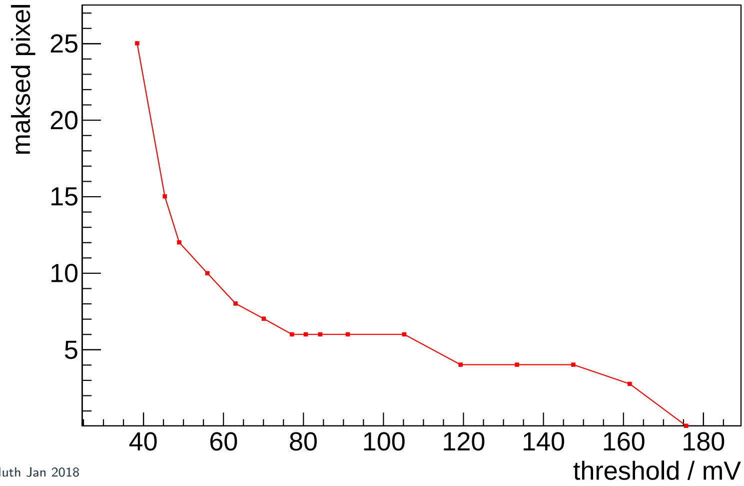




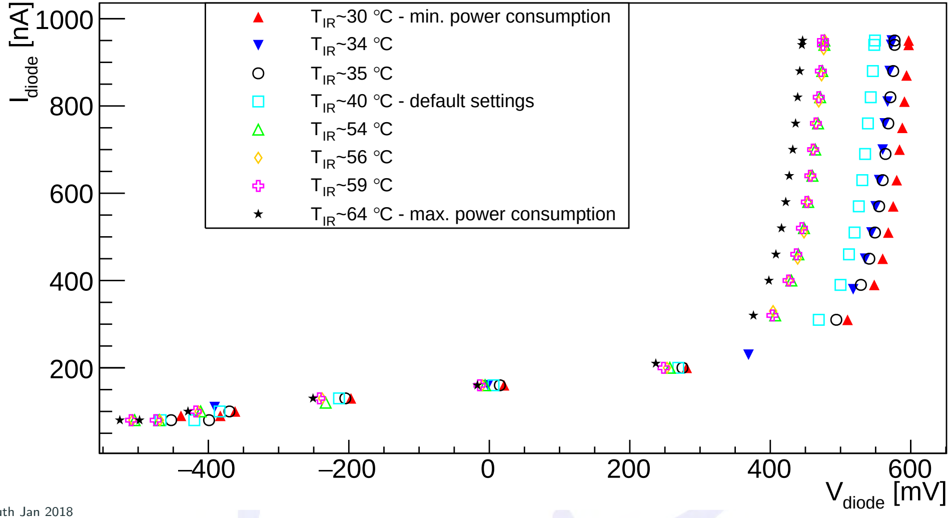
BACKUP

Masked pixels

Pixels with a factor 10 more rate above the average and at least 2 Hz rate are masked



Temperature diode



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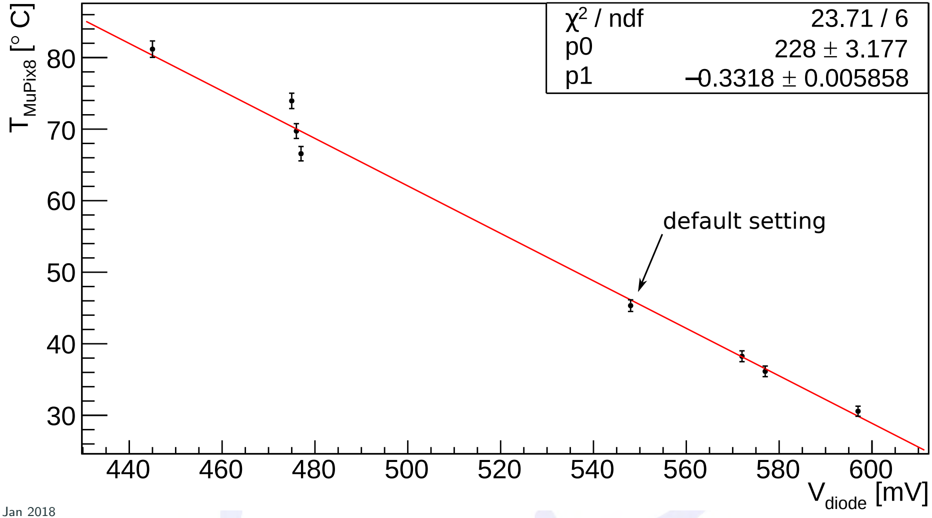
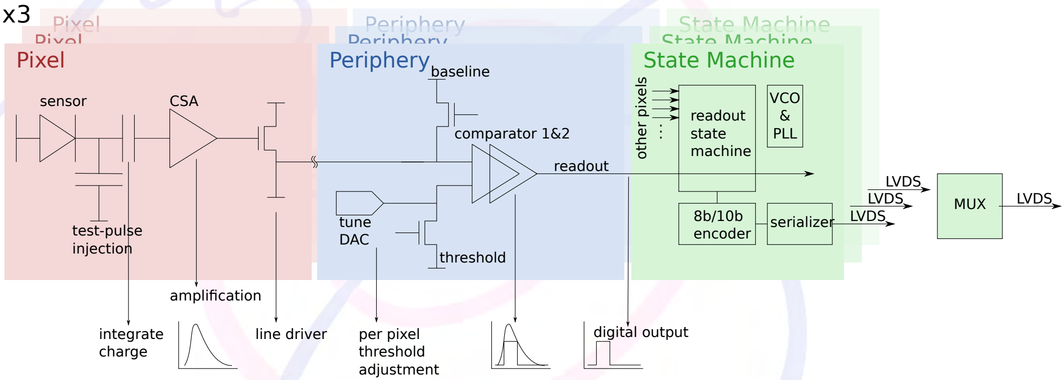


MuPix8 readout



auxiliary

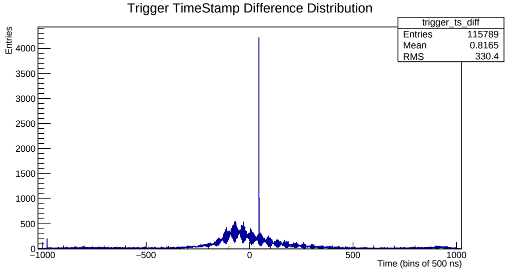
Frequency tests

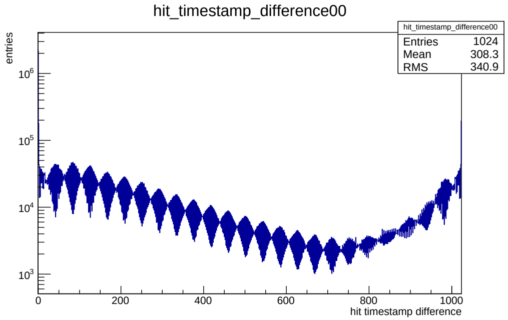
- Setup allows to use a reference frequency (w PLL) or external clock (w/o PLL)
- Tested with 10 MHz external clock: looks as if threshold can be lowered further than running at full speed (125 MHz reference $\rightarrow$ factor 62.5 faster!)
- Will be investigated using telescope

- Side note: Checked data quality of MuPix telescope @ 1.25 Gb/s: no bit errors observed for all channels: BER $< 10^{-}14$

Frequency tests - 10 MHz external clock commissioning

- Bin size 500 ns
- Commissioning of single MuPix setup with slow external clock (10 MHz)
- Top: tile-MuPix correlation
- Bottom: time stamp difference between two consecutive MuPix hits





DAC Scans at VDD/A = 1.9 V & VSSA = 1.1 V

efficiency [%]	noise [kHz/chip]	VNPix	VnFbPix	VNOutPix
99.1	6.4 kHz	0x18	0x10	0x12
99.0	5.6 kHz	0x12	0x10	0x12
98.9	4.1 kHz	0x15	0x10	0x12
98.4	2.1 kHz	0x1B	0x10	0x12
96.8	1.5 kHz	0x1E	0x10	0x12
98.7	2 kHz	0x18	0x13	0x12
98.7	1.9 kHz	0x18	0x16	0x12
98.6	7.3 kHz	0x18	0x10	0x6
98.8	1.9 kHz	0x18	0x10	0x9
98.8	2.0 kHz	0x18	0x10	0xC
98.8	2.2 kHz	0x18	0x10	0xF

Default DACs

VNRegCasc: 20
VDel: 16
VPComp: 5
VPDAC: 0
BLResDig: 10
VPDelDclMux: 6
VNDelDclMux: 12
VPDelDcl: 6
VNDelDcl: 12
VPDelPreEmp: 6
VNDelPreEmp: 12
VPDcl: 24
VNDcl: 12
VNLVDS: 63
VNLVDSDel: 0

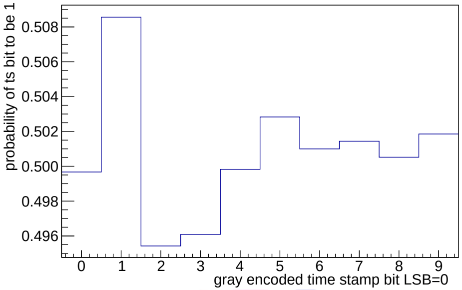
Bandgap1/2_on: 0
Biasblock1/2_on: 5
VPVCO: 10
VNVCO: 10
slowdownend: 0
timerend: 3
BLResPix: 5
VNPix: 20
VNFBPix: 10
VNFollPix: 10
VNPix2: 0
VNBiasPix: 0
VPLoadPix: 5
VNOutPix: 16
VPFoll: 10
VNDACPix: 0

maxcycend: 63
VPPump: 20
resetckdivend: 3
SelectTest: 0
SelectTestOut: 0
DisableHitbus: 0
sendcounter: 0
Linkselect: 0
Termination: 0
AlwaysEnable: 1
ThHigh: 336
ThLow: 293
ThPix: 463
BLPix: 463 (800mV)
BLDig: 256 (500mV)

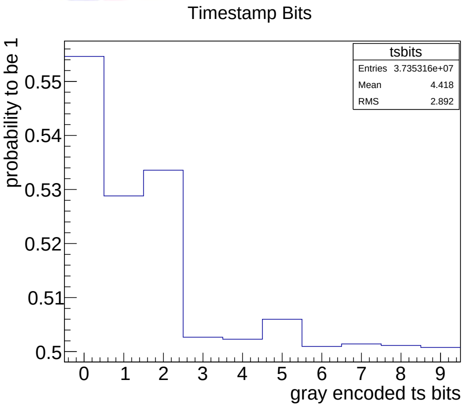
tsphase: 0
ckdivend2: 7
ckdivend: 0
VPRegCasc: 20
VPRamp: 0
VPBiasReg: 30
VNBiasReg: 30
enable2threshold: 0
enableADC: 0
Invert: 0
SelEx: 0
SelSlow: 0
EnablePLL: 1
Readout_reset_n: 1
Serializer_reset_n: 1
Aurora_reset_n: 1

Lazy bits

VDD/A 1.9 V & VSSA 1 V



VDD/A 1.8 V & VSSA 1.1 V



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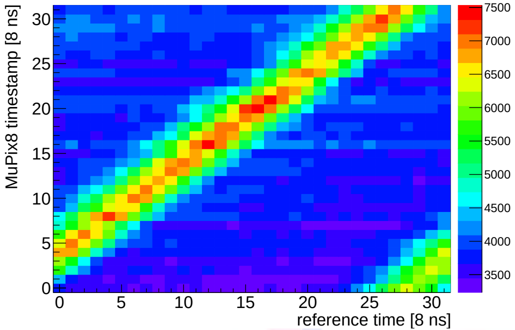

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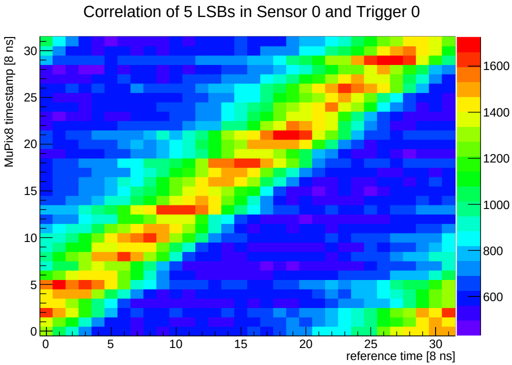

Column and row dependence of the time resolution