Radiation Tolerance of HV-CMOS Sensors

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Overview

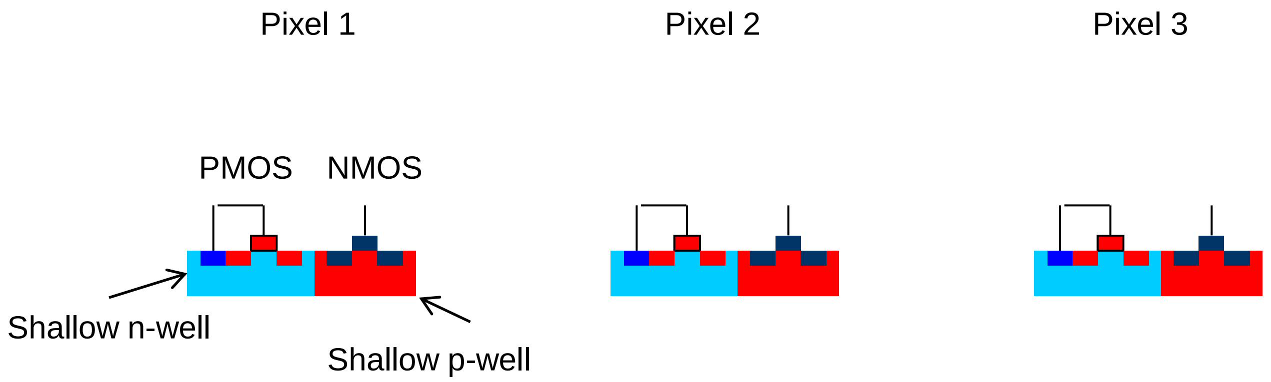
- High-voltage CMOS pixel sensors – introduction
- Results of irradiations with neutrons, protons and x-rays

High-voltage CMOS pixel detectors

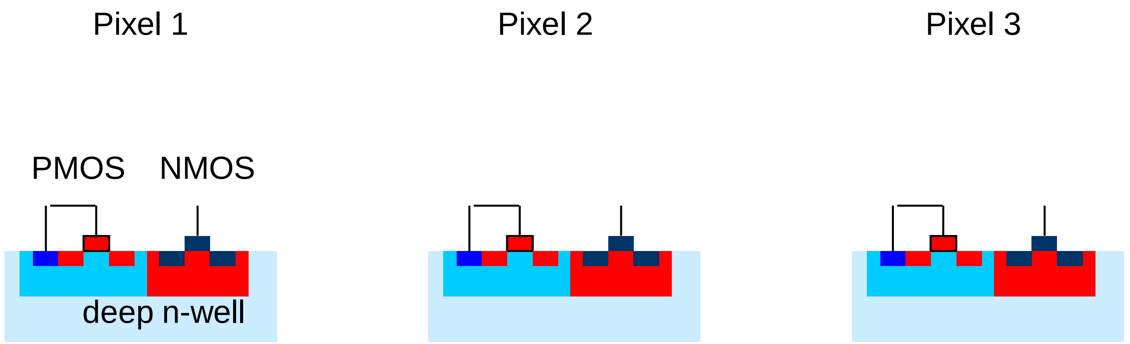
or “smart diode arrays” or “HV-MAPS”

The structure

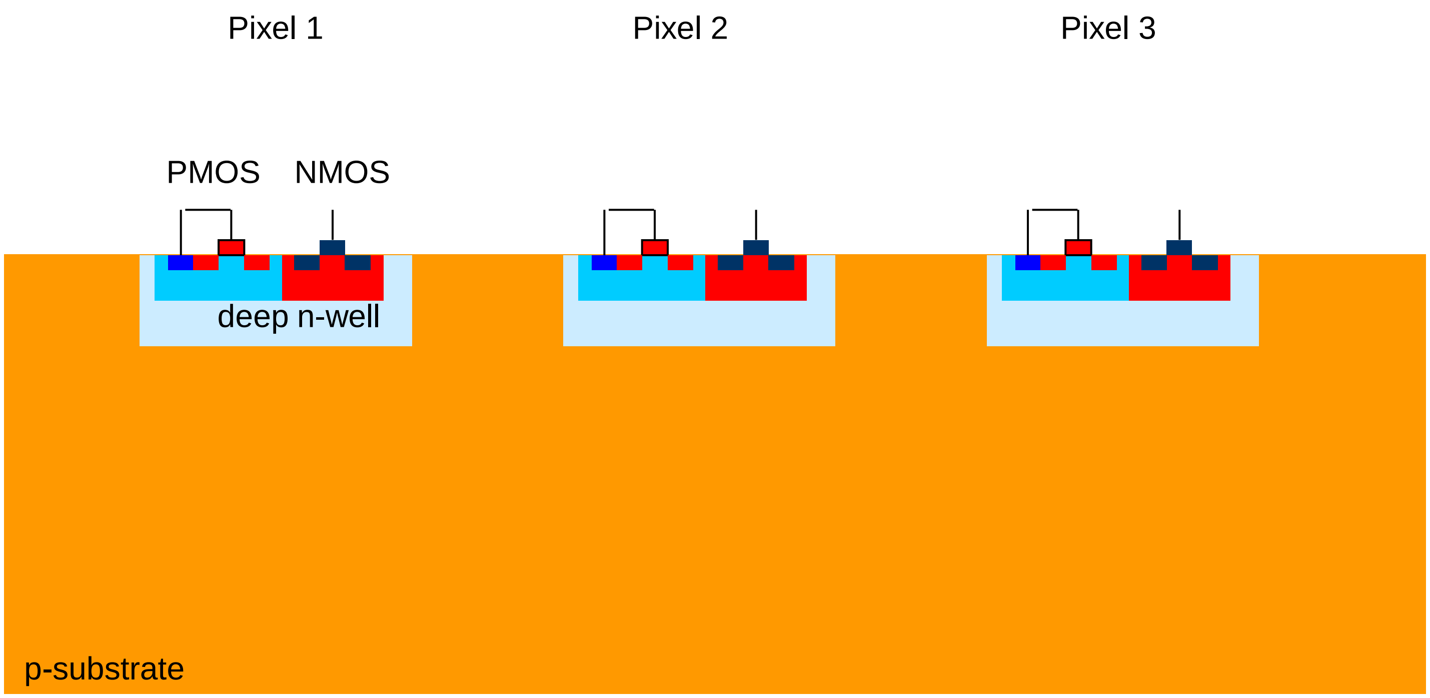
- Monolithic active pixel sensor.
- Pixel electronics based on CMOS.
- Implemented in commercial technologies.
- PMOS and NMOS transistors are placed inside the shallow n- and p-wells.



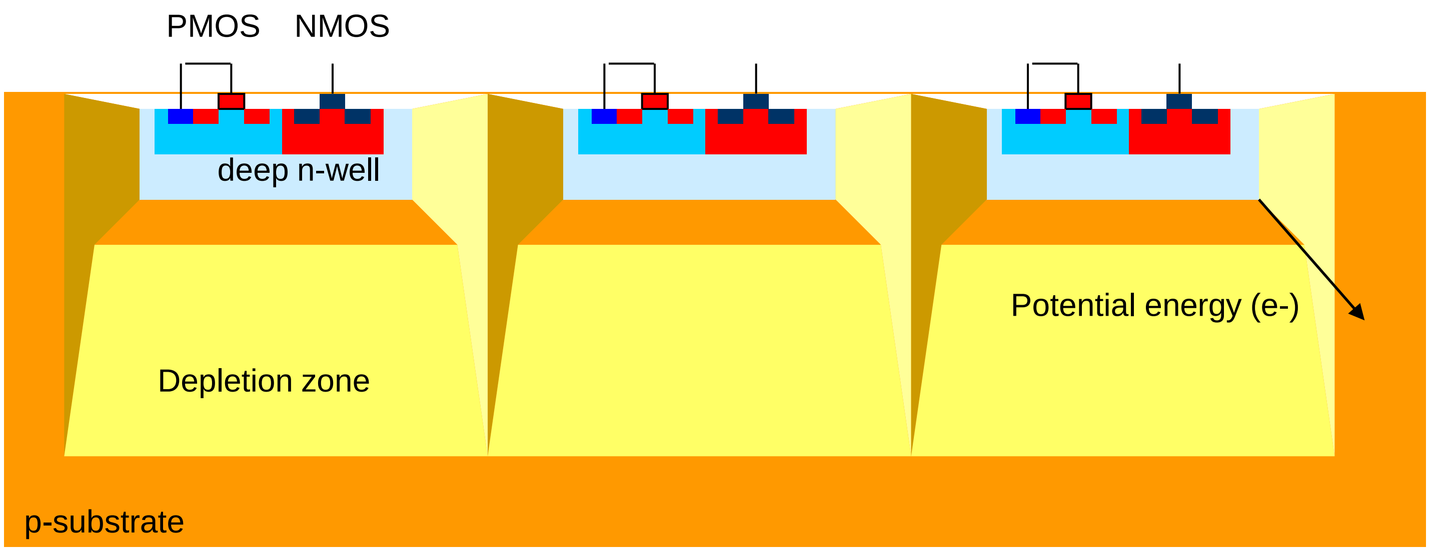
- A deep n-well surrounds the electronics of every pixel.



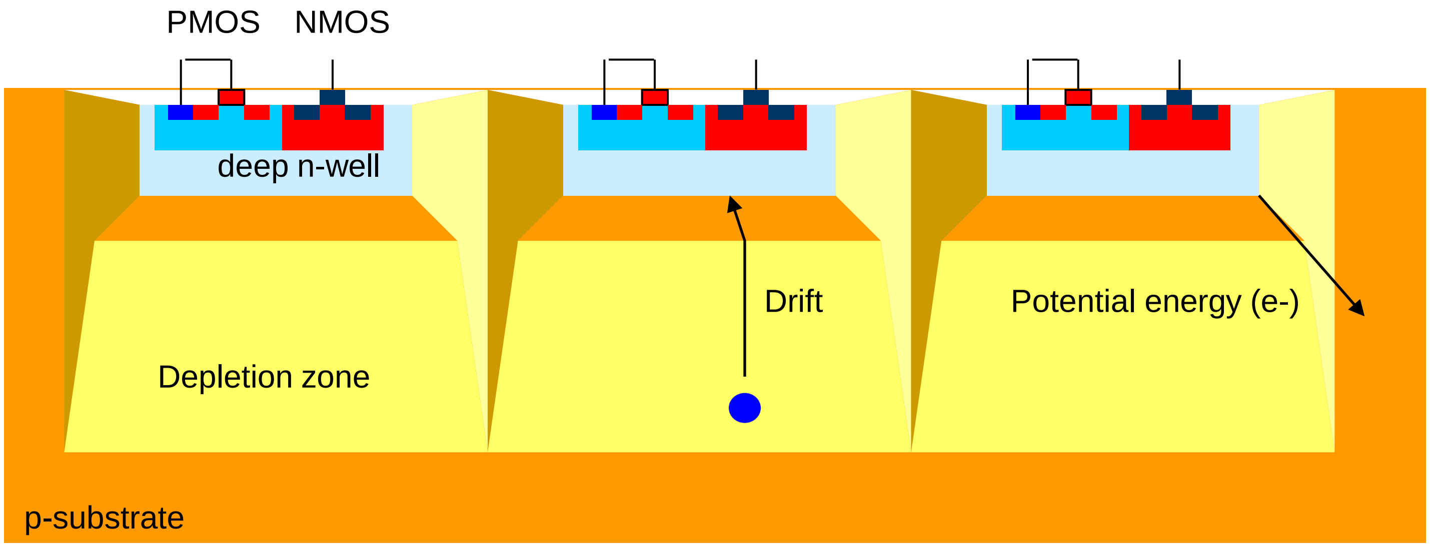
- The deep n-wells isolate the pixel electronics from the p-type substrate.



- The substrate can be biased low without damaging the transistors.
- In this way the depletion zones in the volume around the n-wells are formed.
- => Potential minima for electrons

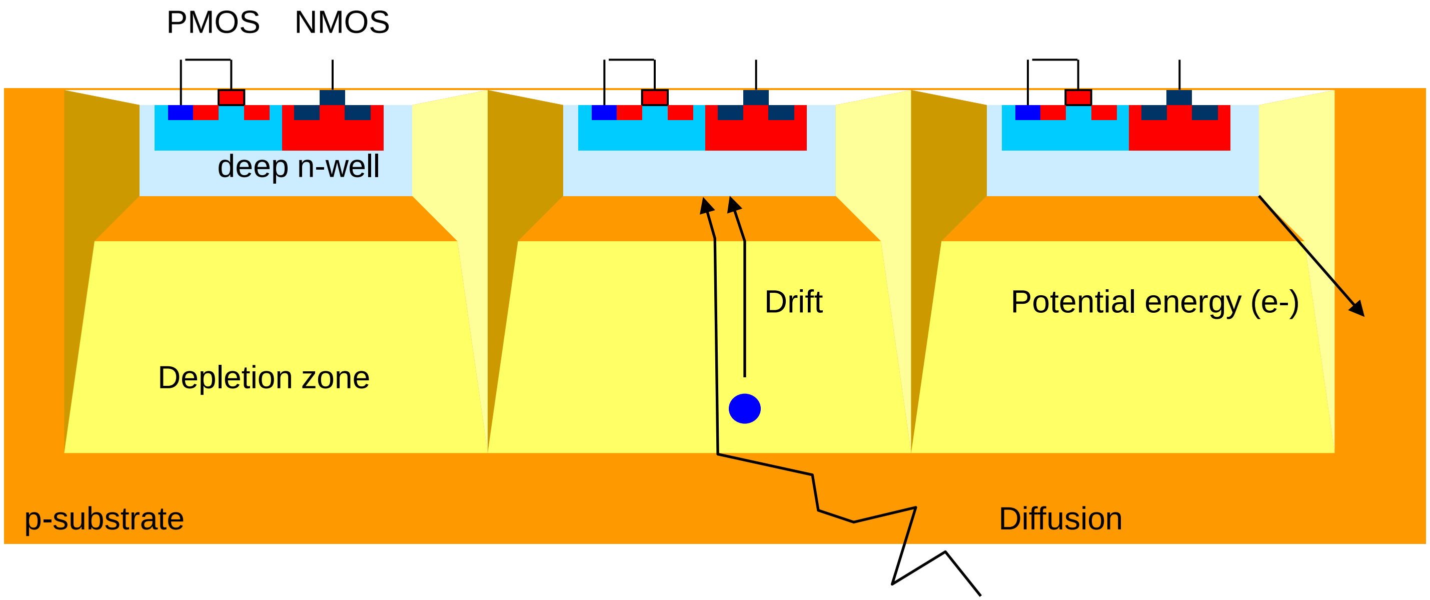


- Charge collection occurs by drift. (main part of the signal)

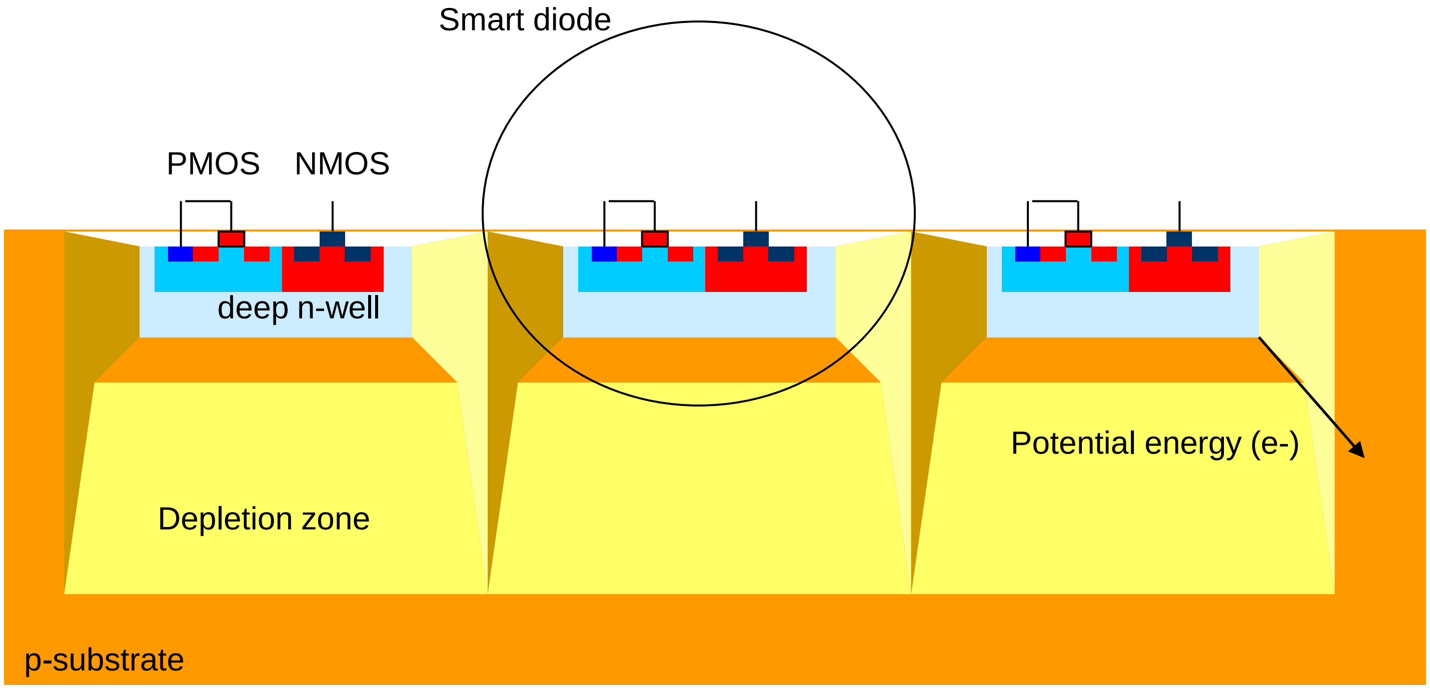


HV CMOS detectors

- Charge collection occurs by drift. (main part of the signal)
- Additional charge collection by diffusion.

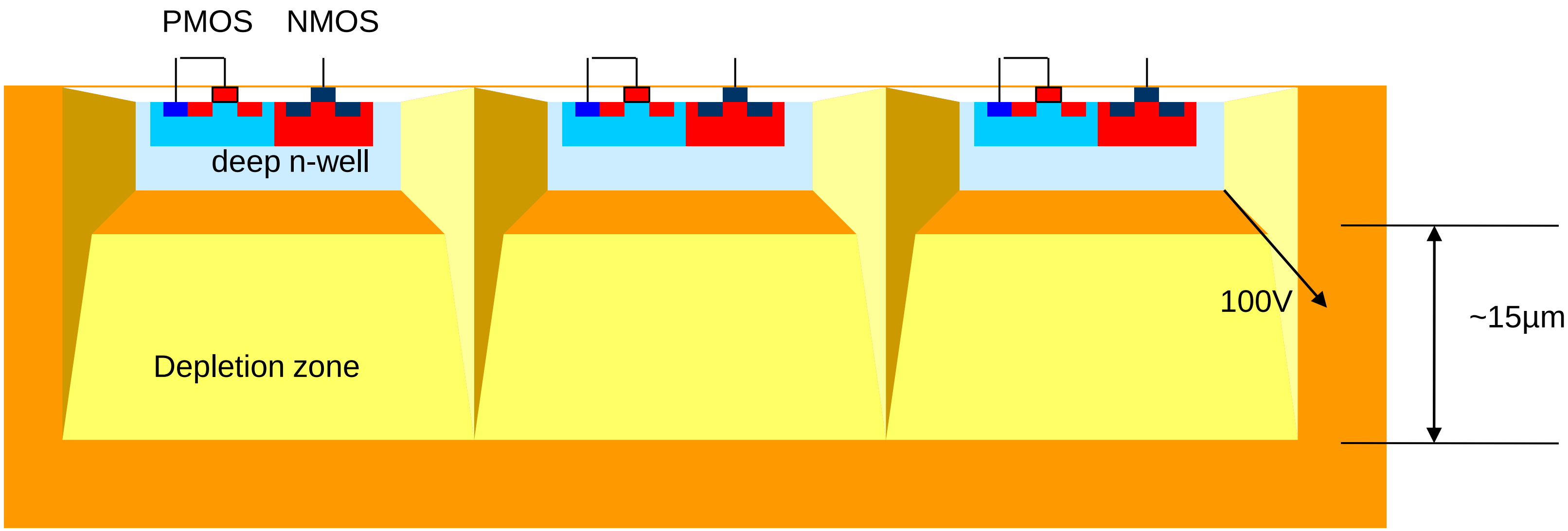


- HVCMOS sensors can be implemented in *any CMOS technology* that has a deep-n-well surrounding low voltage p-wells. (We have successfully used TSMC 65nm: 2.5 μm pixels.)
- We expect the best results in high-voltage technologies:
- These technologies have deeper n-wells and the substrates of higher resistances than the LV CMOS.



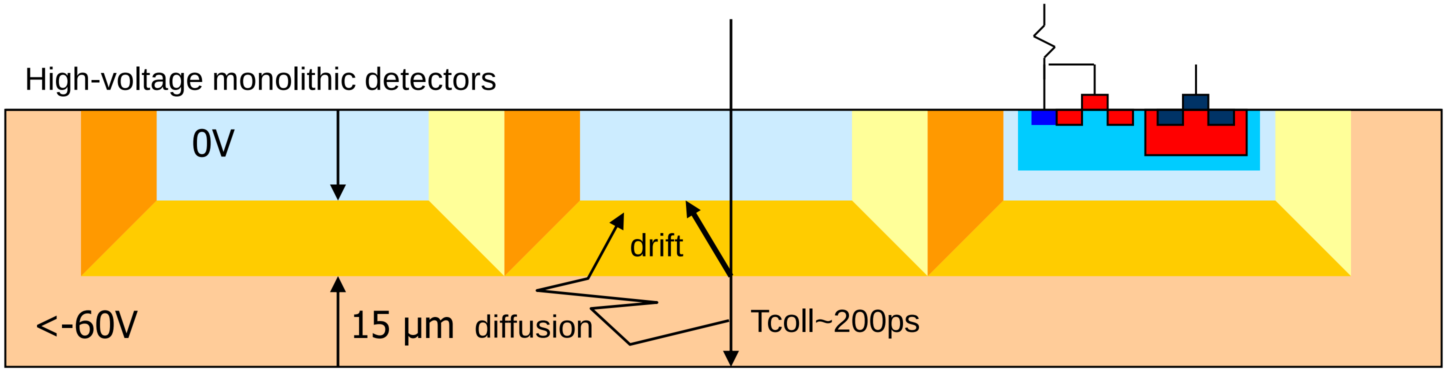
HV CMOS detectors

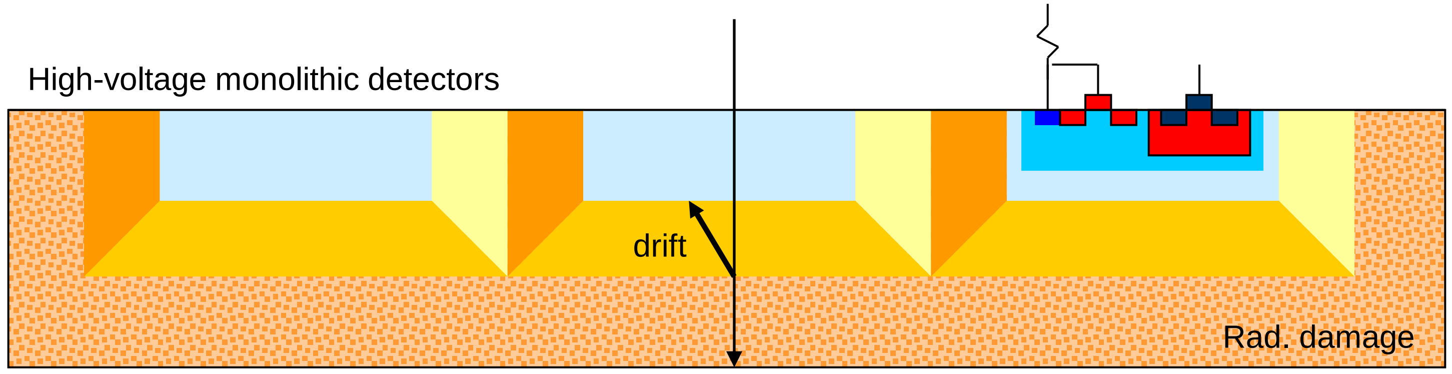
- Example AMS 350nm HVCMOS: Typical reverse bias voltage is 60-100 V and the depleted region depth ~15 μm.
- 20 Ωcm substrate resistance -> acceptor density ~ 10^{15} cm^{-3}.
- E-field: 100V/15μm or 67 kV/cm or 6.7 V/μm.



Radiation tolerance

High-voltage monolithic detectors




High-voltage monolithic detectors
drift
Rad. damage

Project results

Project history

2006

„Proof of principle“ phase

350nm AMS HV technology

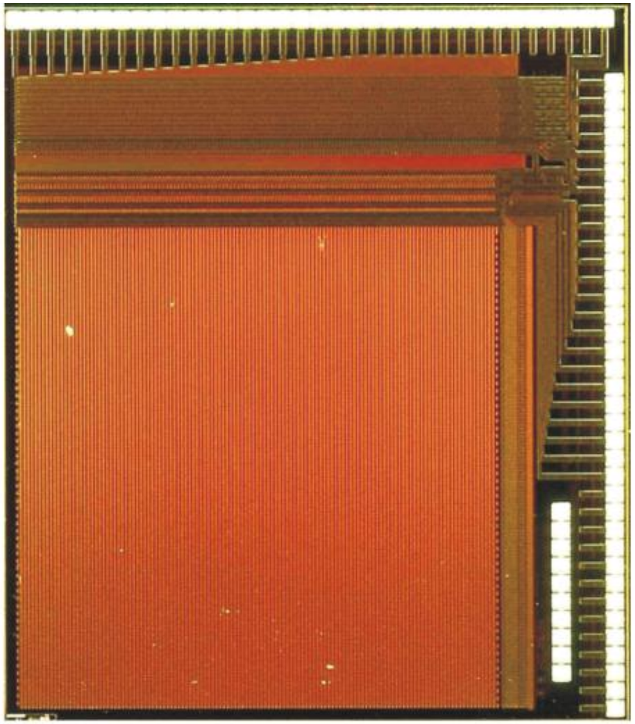
1) Simple charge integrating pixels with pulsed reset and rolling shutter RO.
(Possible applications: ILC, transmission electron microscopy, etc.)

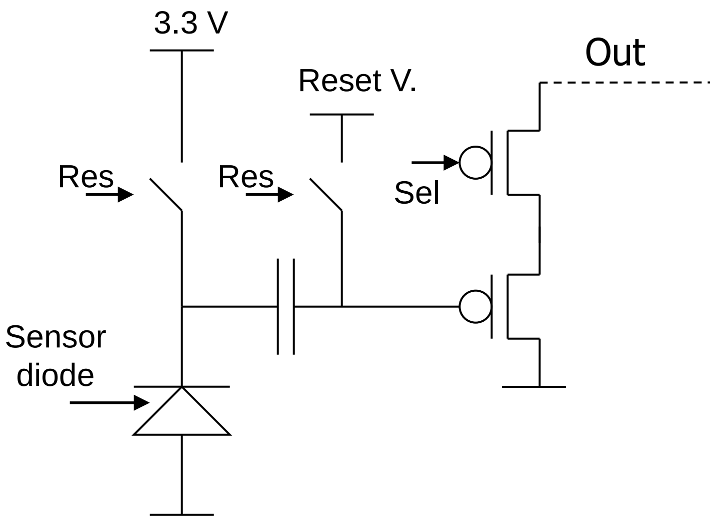
2) Pixels with complex CMOS-based pixel electronics that detect particle signals.
(Possible applications: CLIC, LHC, CBM, etc.)

3) Capacitively coupled pixel detectors (CCPDs) based on a pixel sensor implemented as a smart diode array
.

First publication: I. Peric, “A novel pixelated monolithic particle detector implemented in high-voltage CMOS technology” Nucl. Instr. Meth. A 582, 876 - 885 (2007)

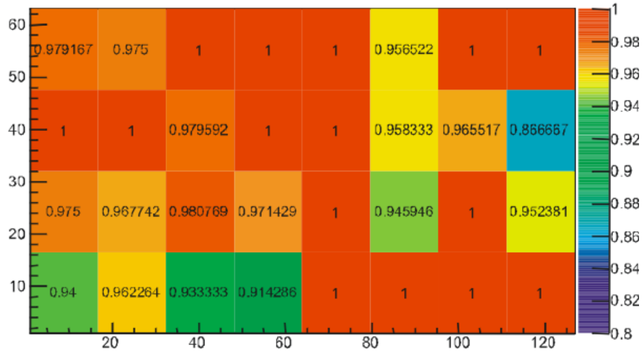
Charge integrating pixel detector



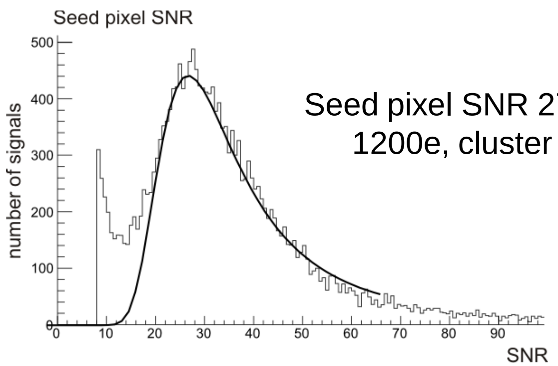


HVPixelM:
21x21 µm pixel size
128 x 128 pixel matrix

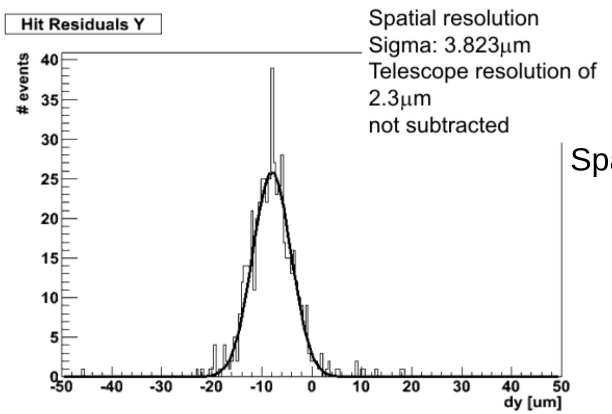
Test-beam results: HVPixelM



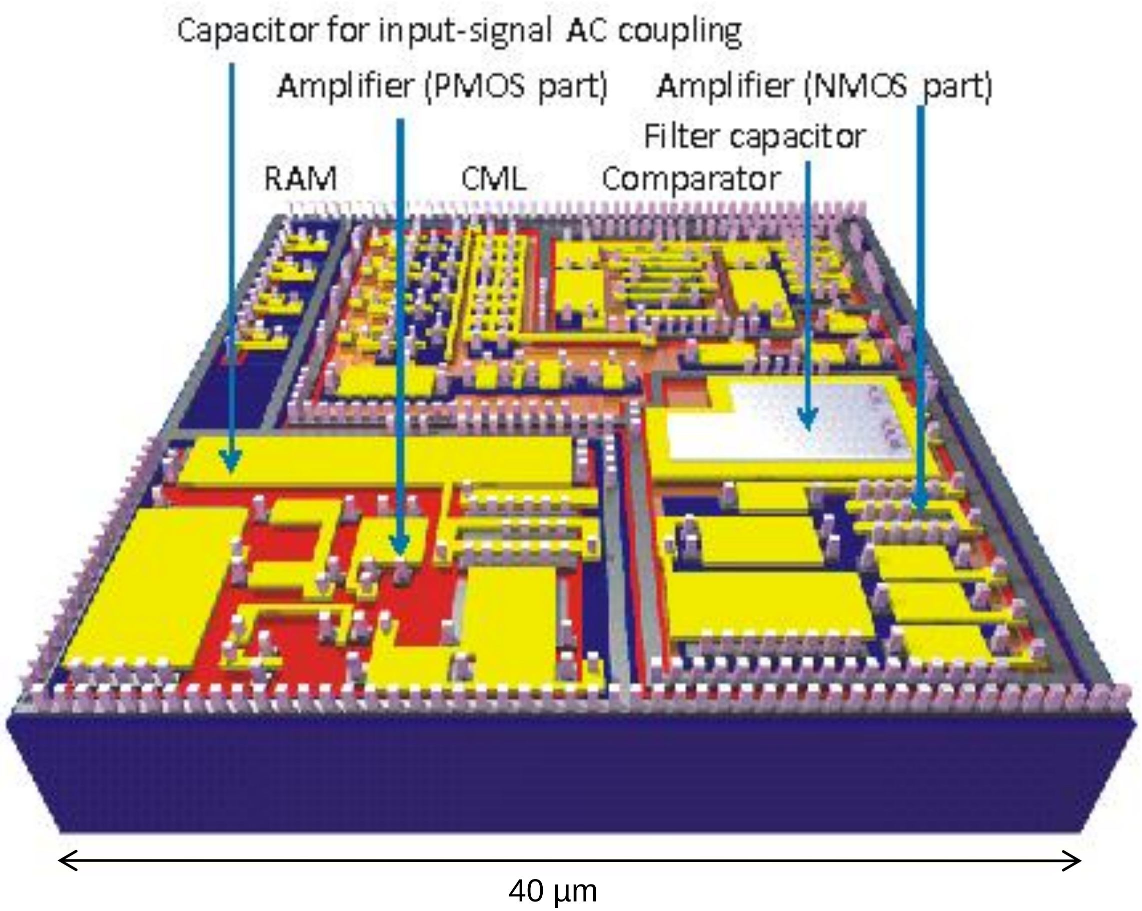
Efficiency at TB: ~98% (probably due to rolling shutter effects – one row out of 64 is in reset state.



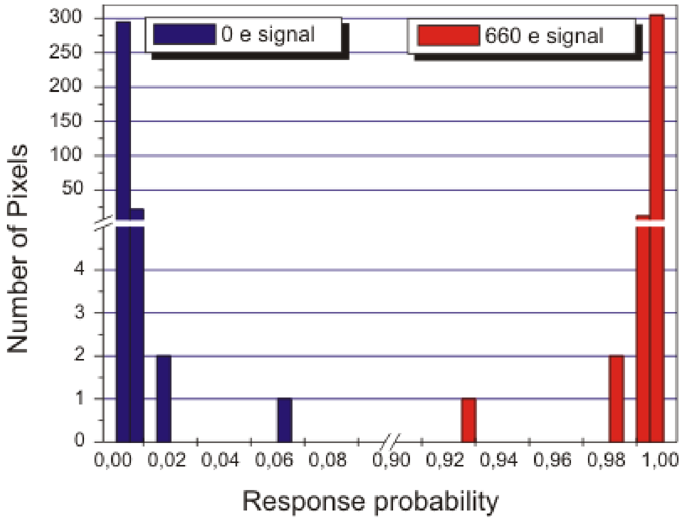
Seed pixel SNR 27, seed signal 1200e, cluster 2000e

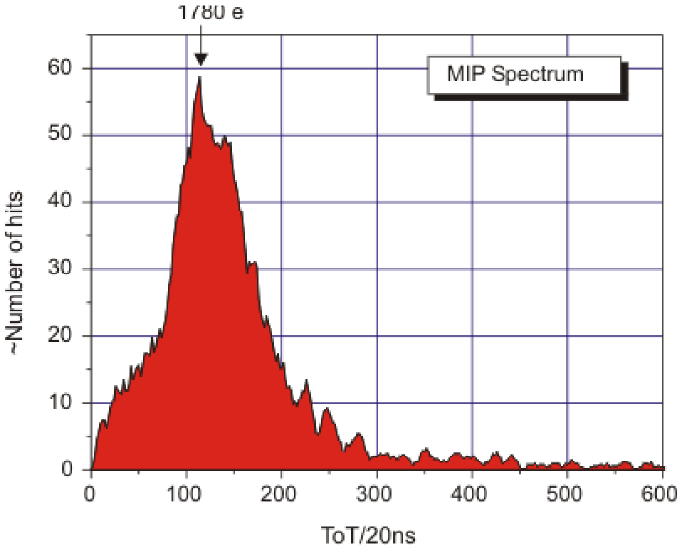


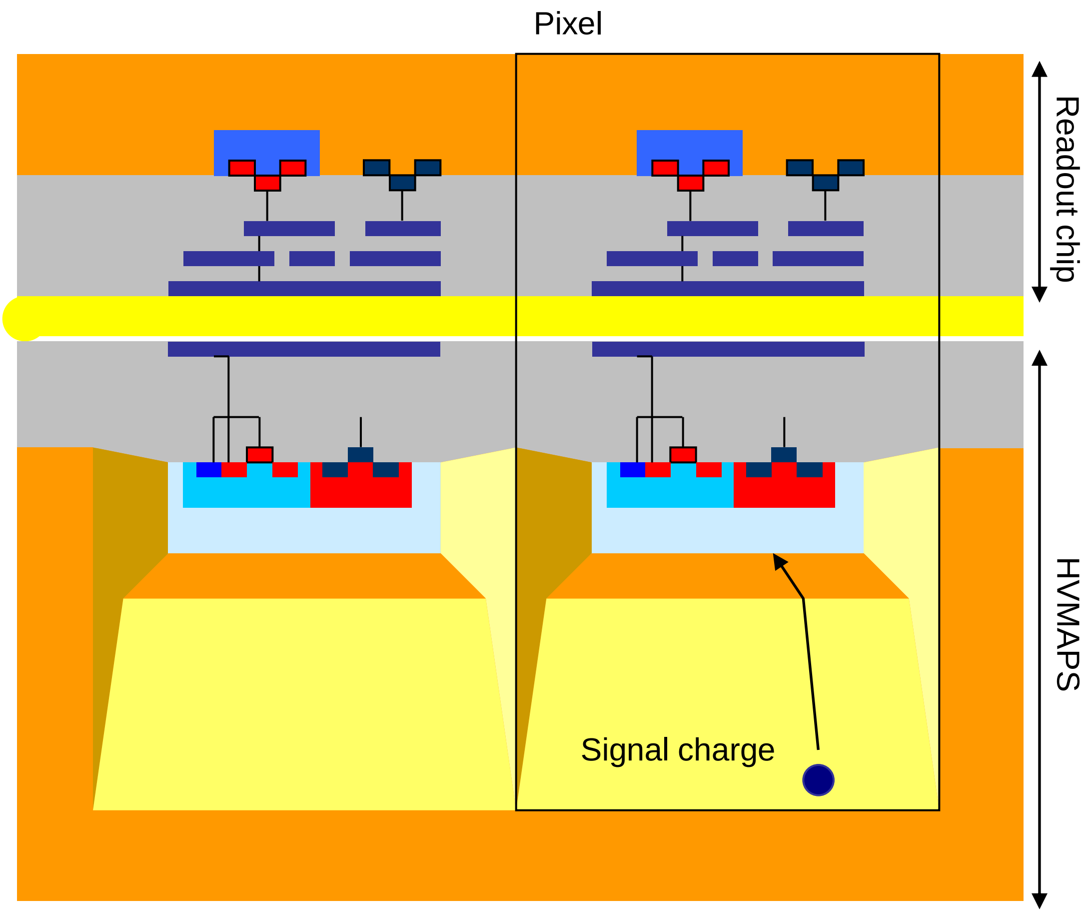
Spatial resolution 3-3.8µm

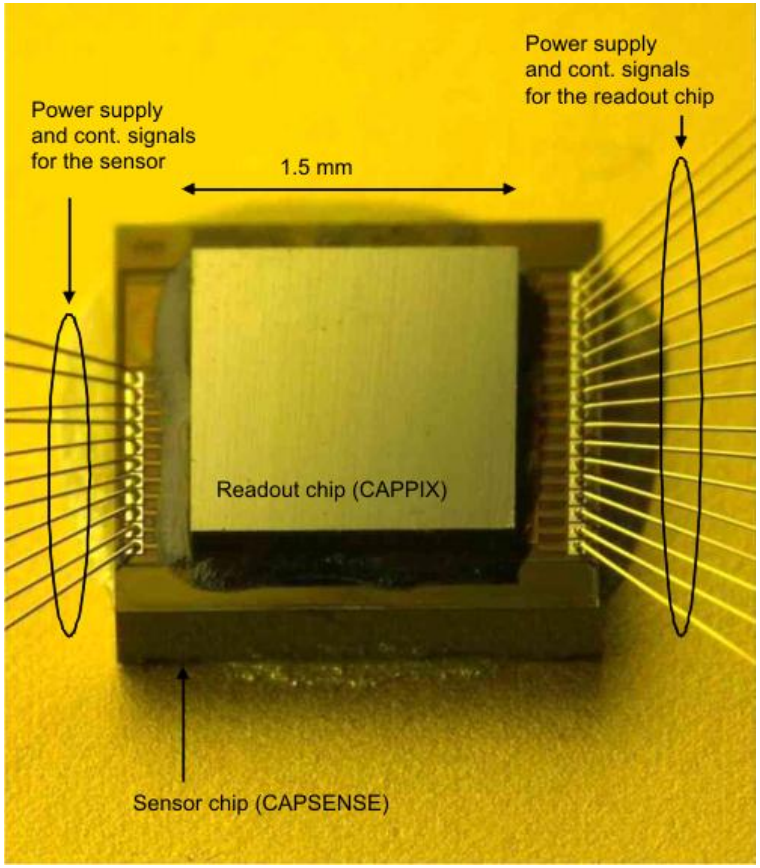

Capacitor for input-signal AC coupling
Amplifier (PMOS part)
Amplifier (NMOS part)
Filter capacitor
RAM
CML
Comparator
40 µm

- Left: Response probability of the entire pixel matrix for 660e test pulse and the noise occupancy.
- Right: MIP spectrum measured at SPS (CERN).

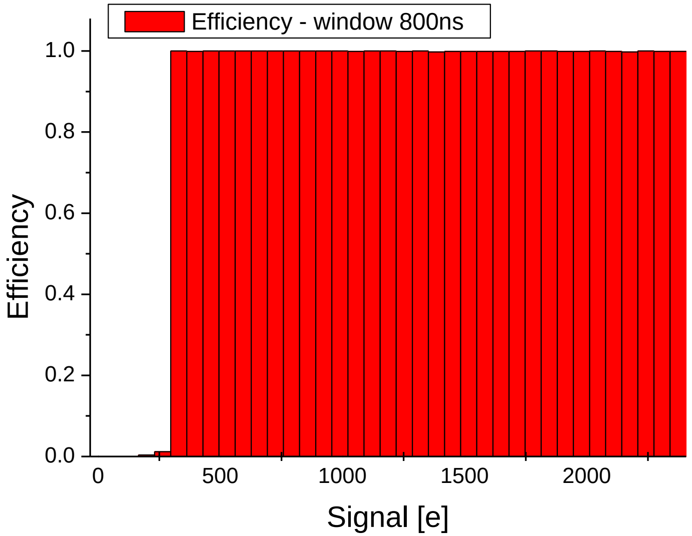





Pixel
Readout chip
HVMAPS
Signal charge



Pixel matrix efficiency:
Detection of signals > 350e possible
MIP signal ~ 1800 e



CAPPIX/CAPSENSE edgeless CCPD
50x50 µm pixel size
Noise 30-40e
Time resolution 300ns
MIP SNR 45-60

New projects

65nm UMCLV technology

2006

„Proof of principle“ phase

350nm AMS HV technology

A 180nm HV technology

Applications:

1) ATLAS and CLIC
Smart sensors readout by pixel- and strip – readout chips.

2) Mu3e experiment at PSI
Monolithic pixel detector

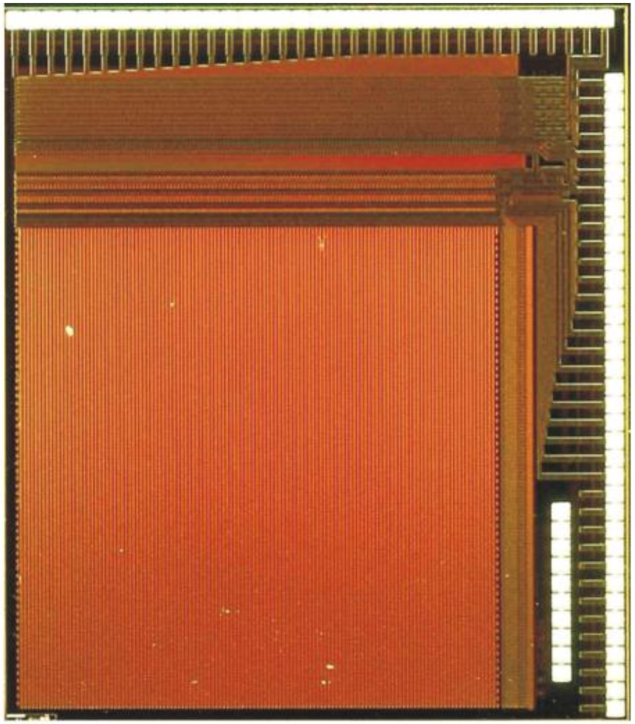
3) Transmission electron microscopy
integrating pixels with pulsed reset and rolling shutter RO – in-pixel CDS

Irradiations

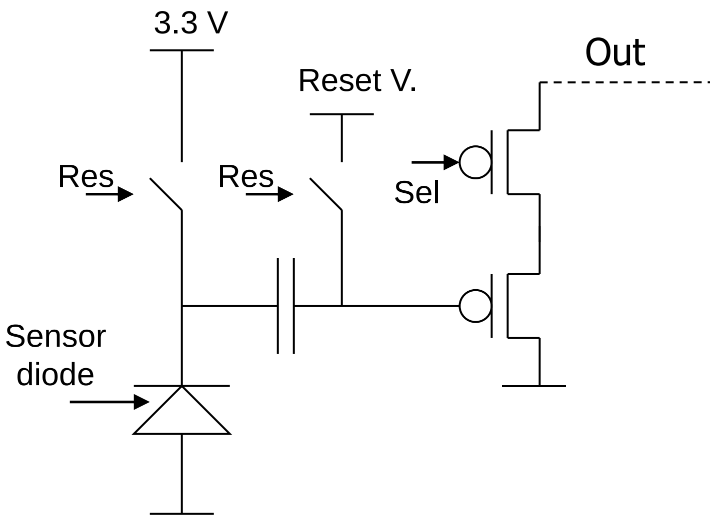
Neutron irradiation at the research-reactor in Munich

10^{14} n_{eq}/cm^2

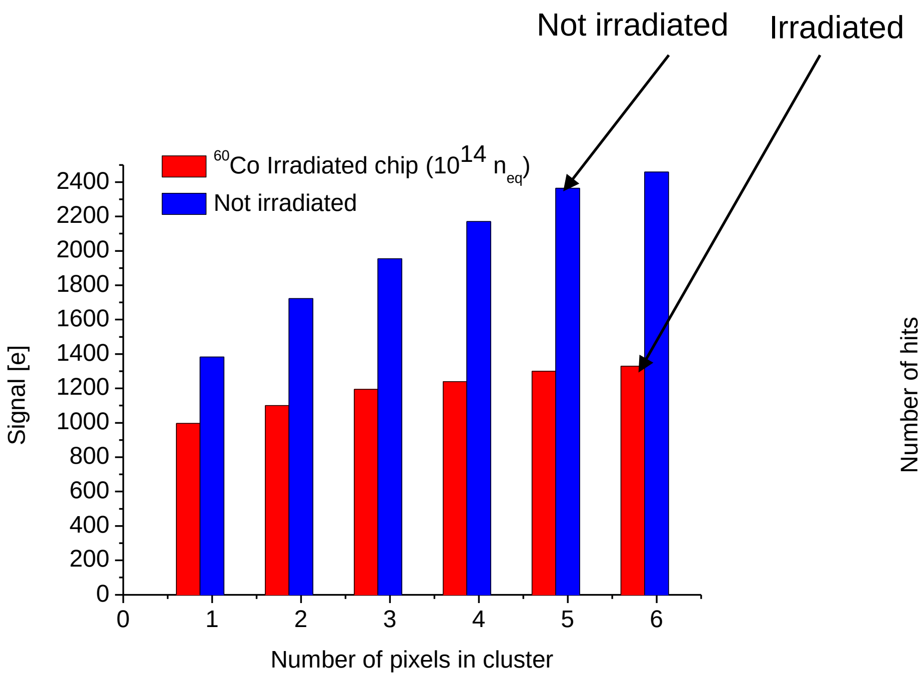
Irradiated device: HVPixelM

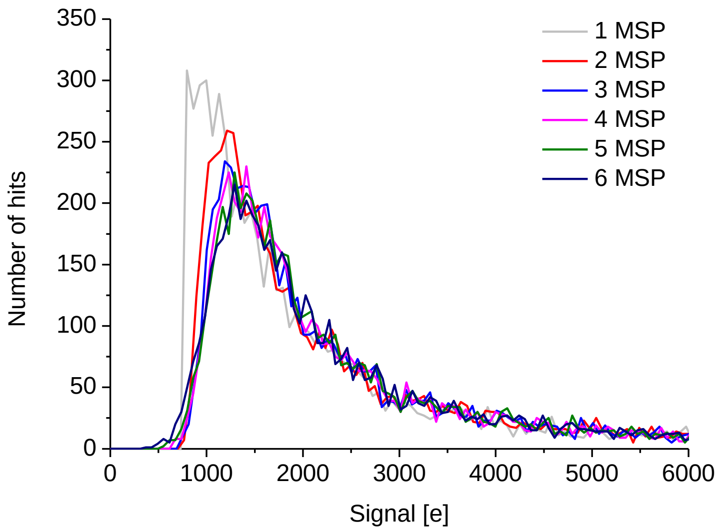


HVPixelM:
21x21 µm pixel size



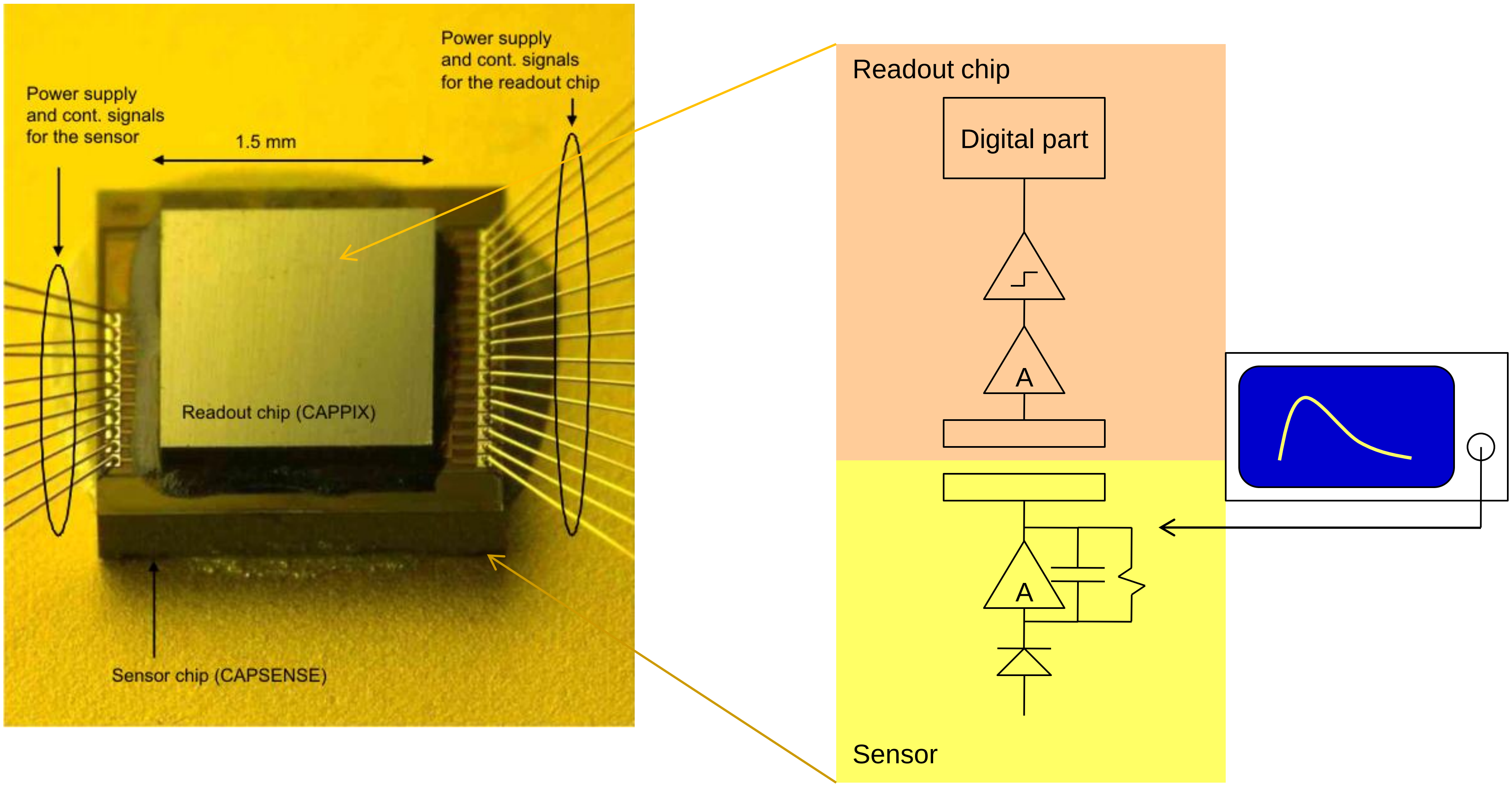
Increase of the detector leakage current from 350fA (room T) to 130pA (0C) per pixel
=> 30 μA / cm^2 at 0C
Seed pixel signal decrease from 1300e to 1000e.
The measurement has been performed at 0C.





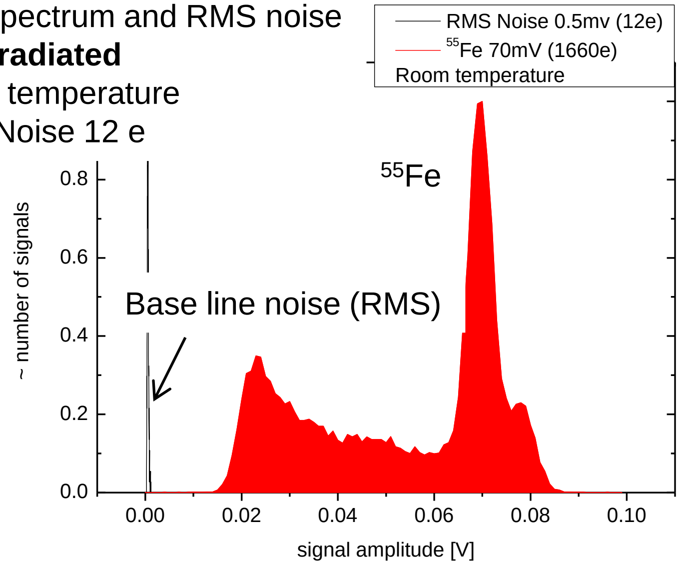
Proton irradiation at KIT (Karlsruhe)
$10^{15}\ n_{eq}/cm^2$

Irradiated device: CCPD2

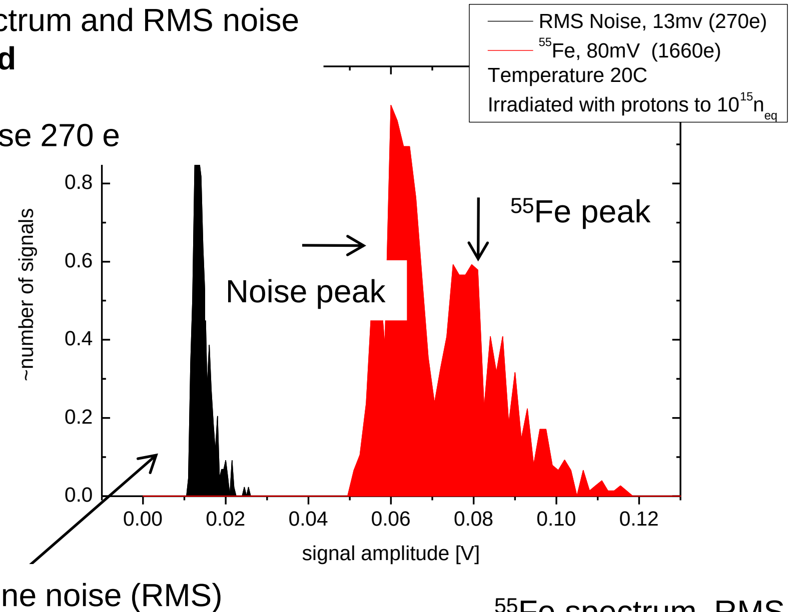


CAPPIX/CAPSENSE edgeless CCPD
50x50 µm pixel size

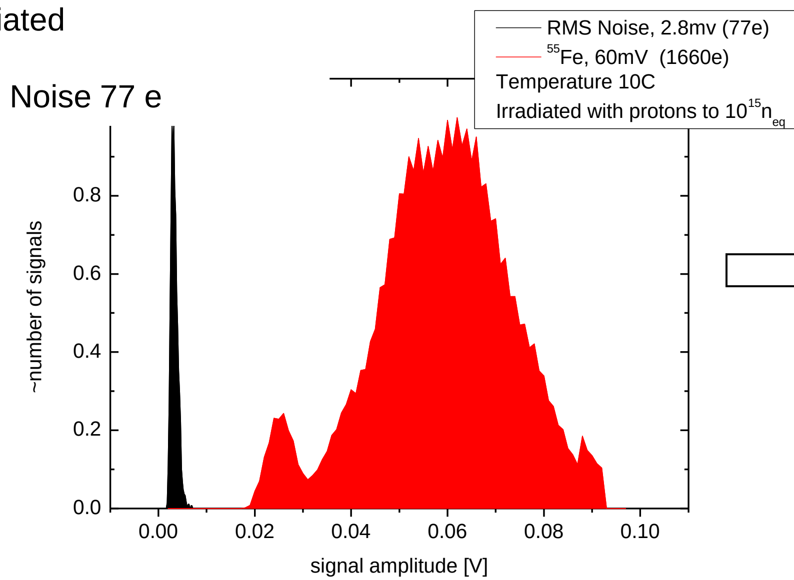
^{55}Fe spectrum and RMS noise
Not irradiated
Room temperature
RMS Noise 12 e



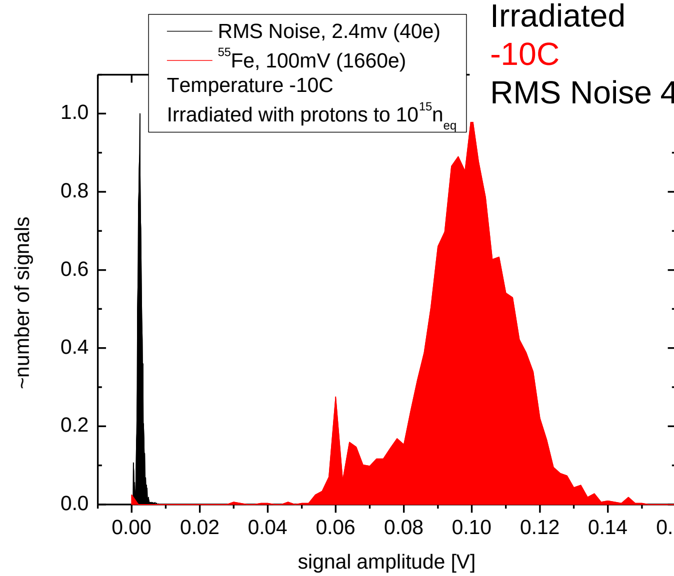
^{55}Fe spectrum and RMS noise
Irradiated
20C
RMS Noise 270 e

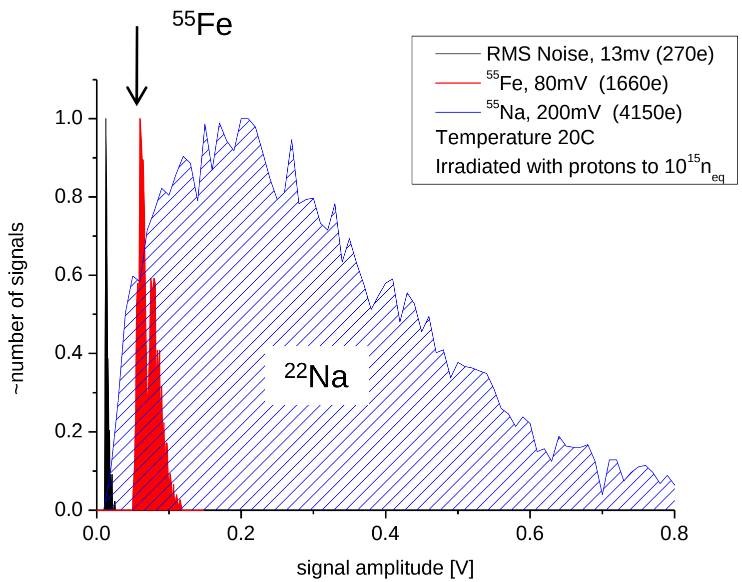


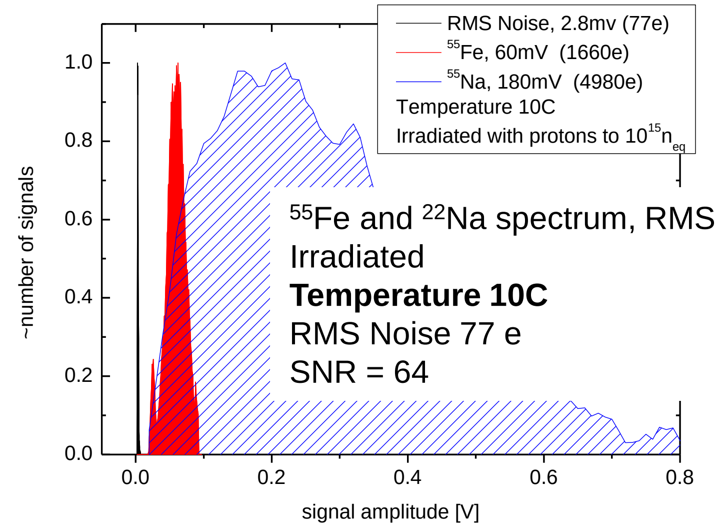
^{55}Fe spectrum, RMS noise
Irradiated
10C
RMS Noise 77 e



^{55}Fe spectrum, RMS noise
Irradiated
-10C
RMS Noise 40 e

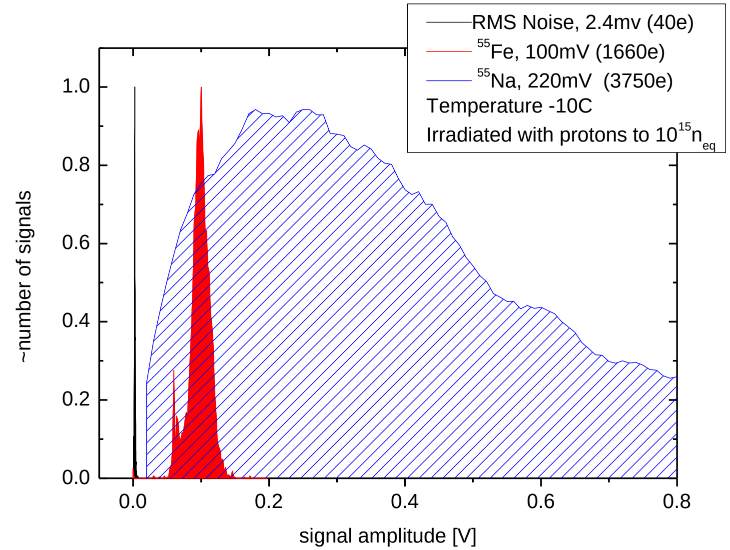




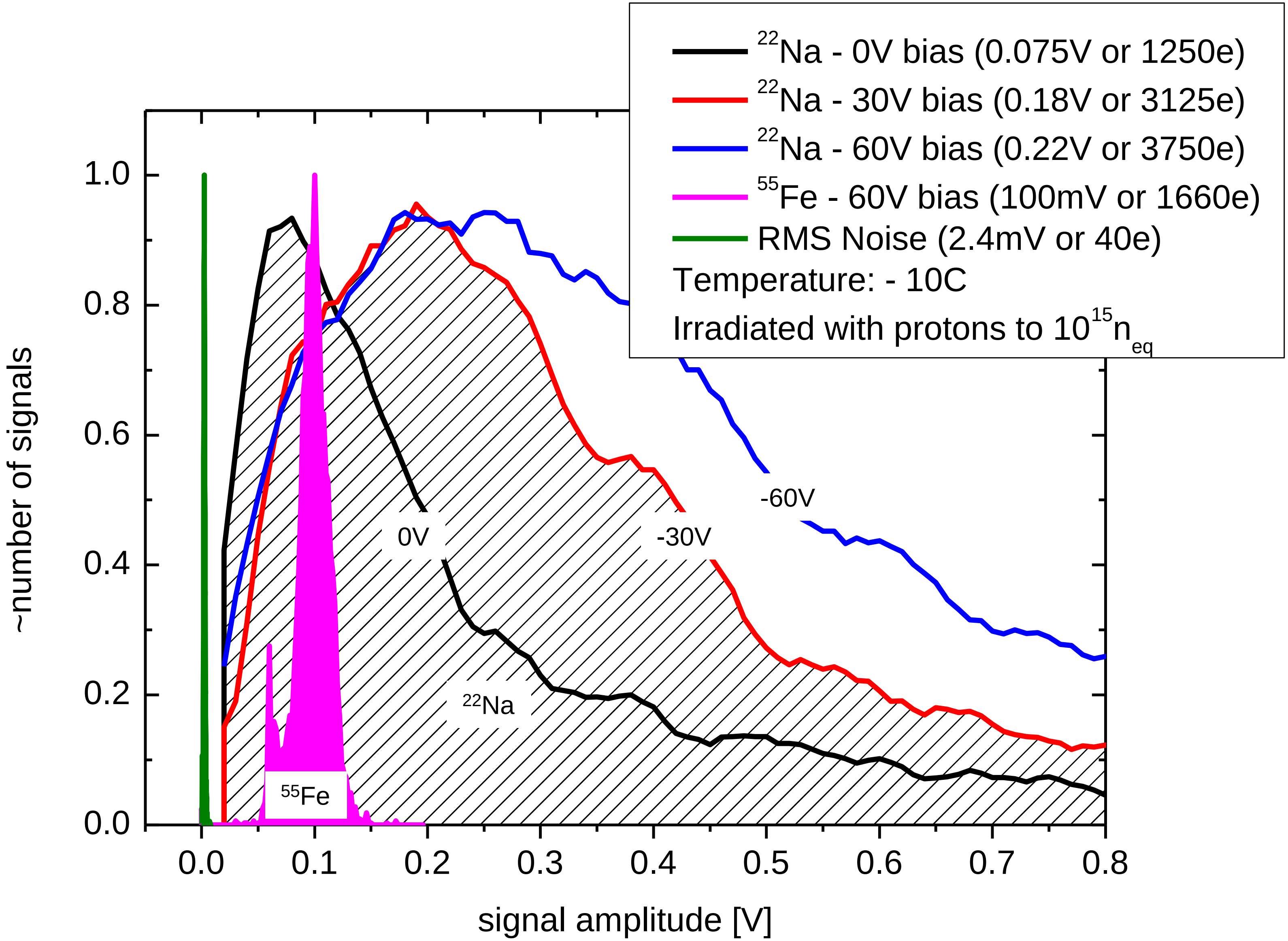


^{55}Fe and ^{22}Na spectrum, RMS noise
Irradiated
Temperature 10C
RMS Noise 77 e
SNR = 64

^{55}Fe and ^{22}Na spectrum, RMS noise
Irradiated
Temperature 20C
RMS Noise 270 e
SNR = 15



^{55}Fe and ^{22}Na spectrum, RMS noise
Irradiated
Temperature -10C
RMS Noise 40 e
SNR = 93

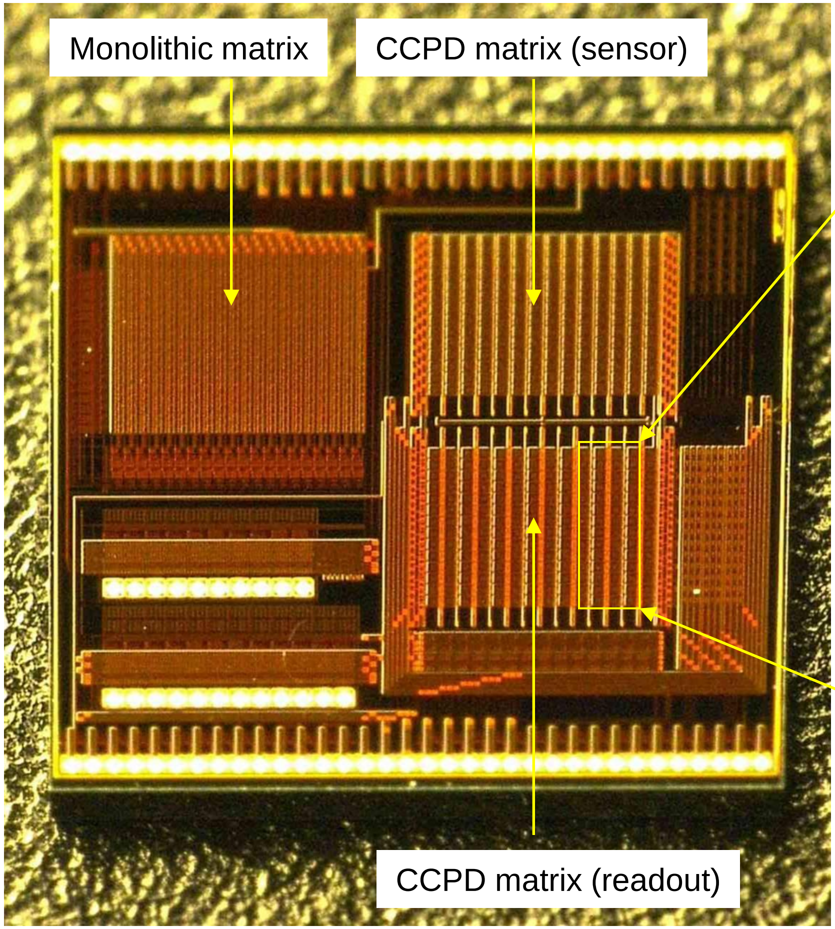


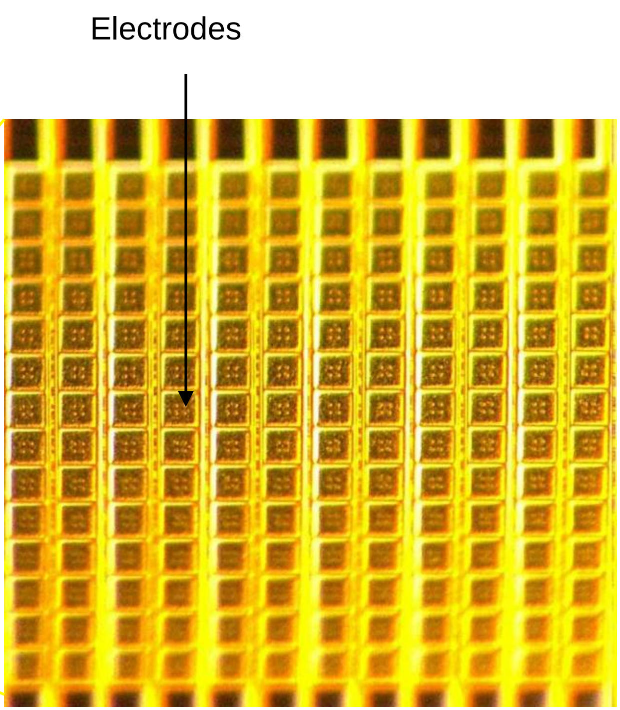
22Na - 0V bias (0.075V or 1250e)
22Na - 30V bias (0.18V or 3125e)
22Na - 60V bias (0.22V or 3750e)
55Fe - 60V bias (100mV or 1660e)
RMS Noise (2.4mV or 40e)
Temperature: - 10C
Irradiated with protons to 10^15 n_eq
~number of signals
signal amplitude [V]
0.0
0.2
0.4
0.6
0.8
1.0
0.0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0V
-30V
-60V
22Na
55Fe

X-Ray irradiation at KIT

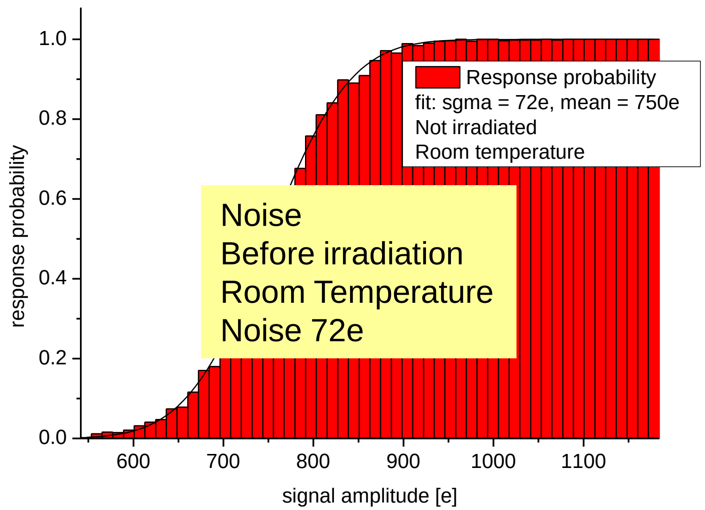
50 MRad

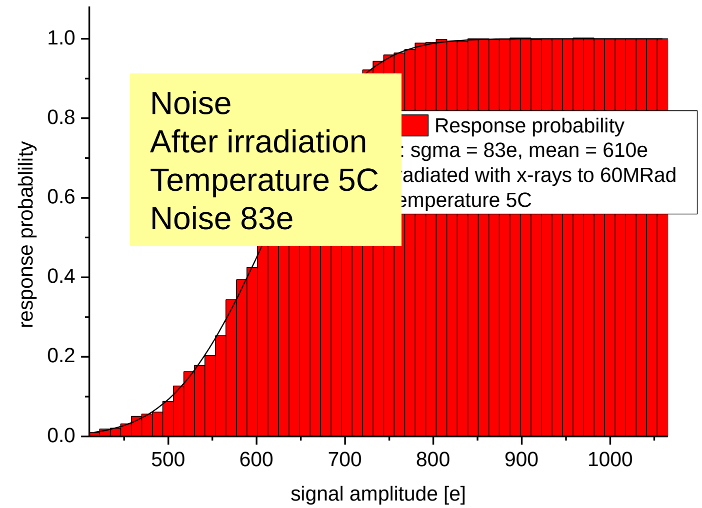
Irradiated device: CCPD1



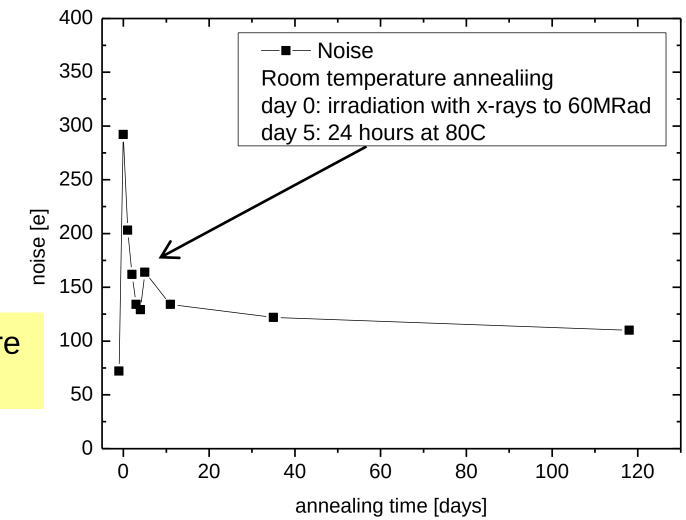


Irradiation with x-rays (50 MRad)





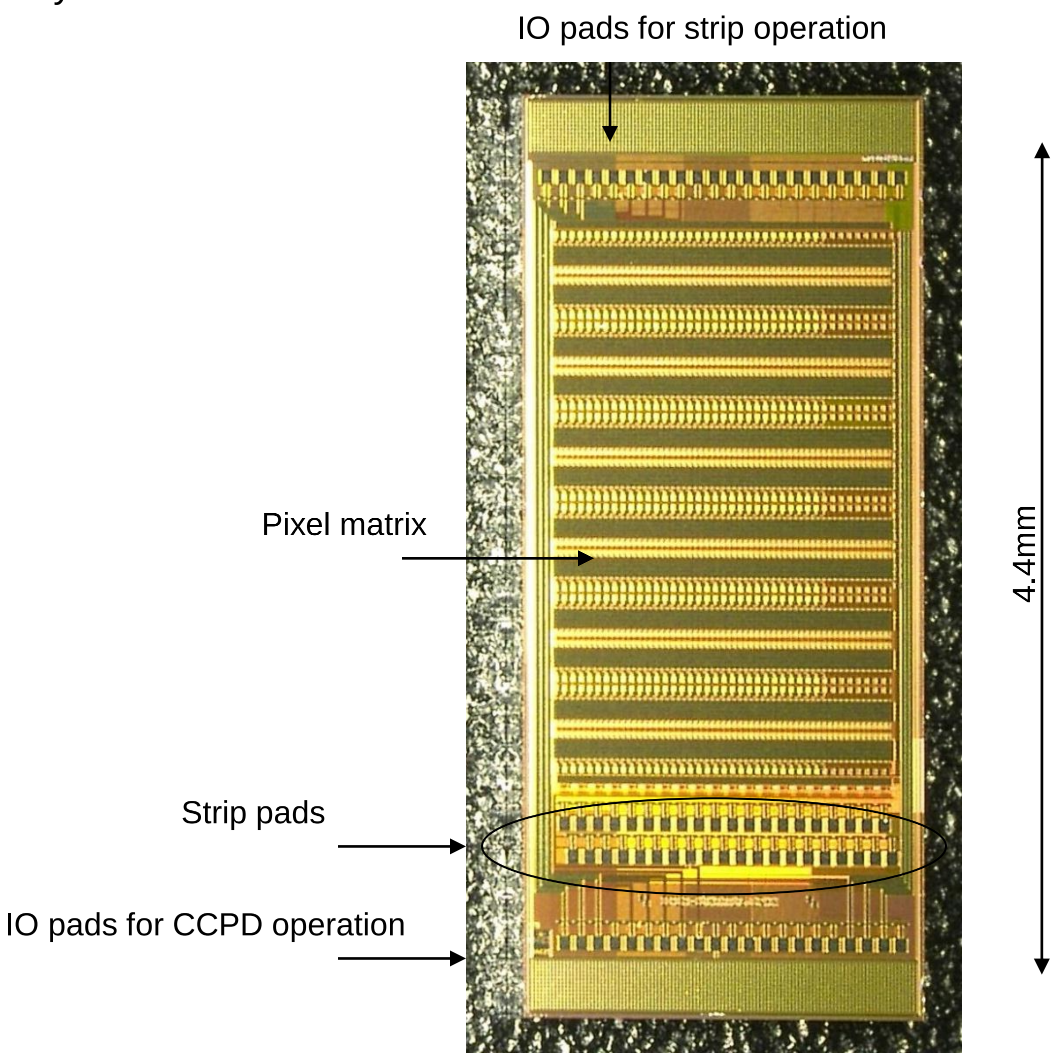
Noise at room Temperature
Vs. annealing time

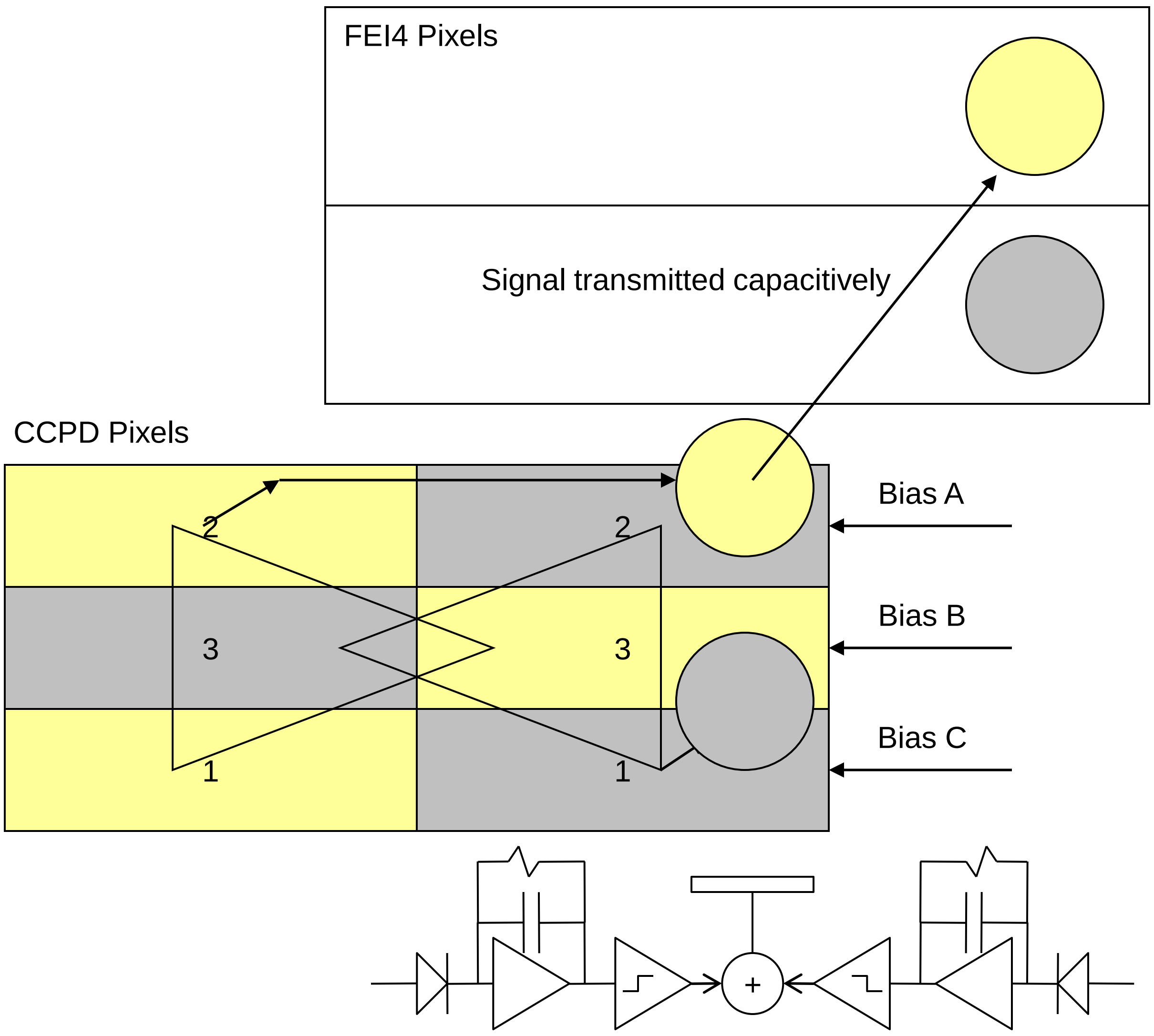


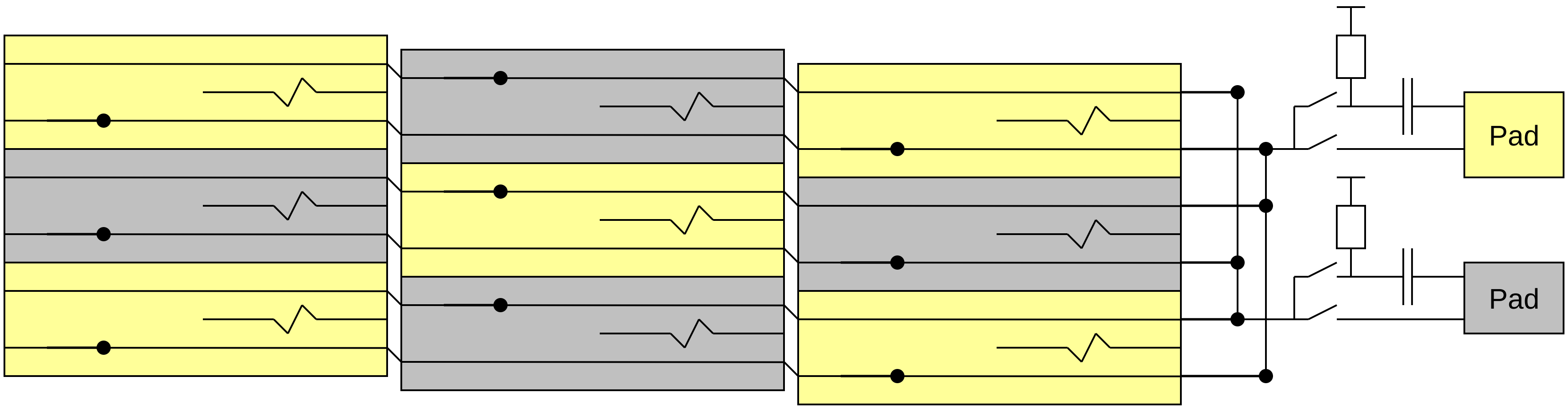
Irradiation at PS (CERN)

Irradiated device: HV2FEI4

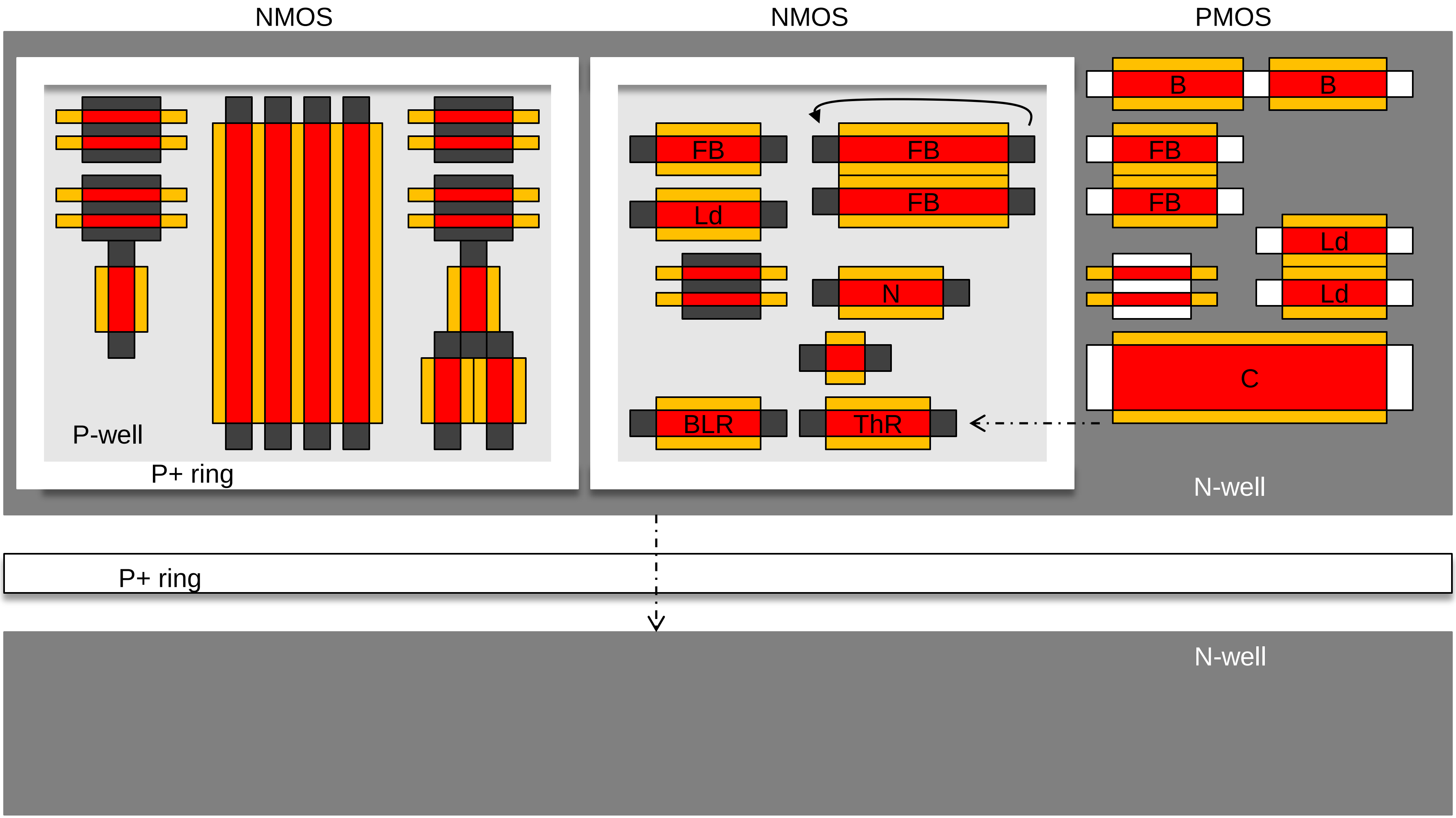
- Pixel matrix: 60x24 pixels (readout by 20 x 12 FEI4 pixels)
- Pixel size 33 μm x 125 μm.

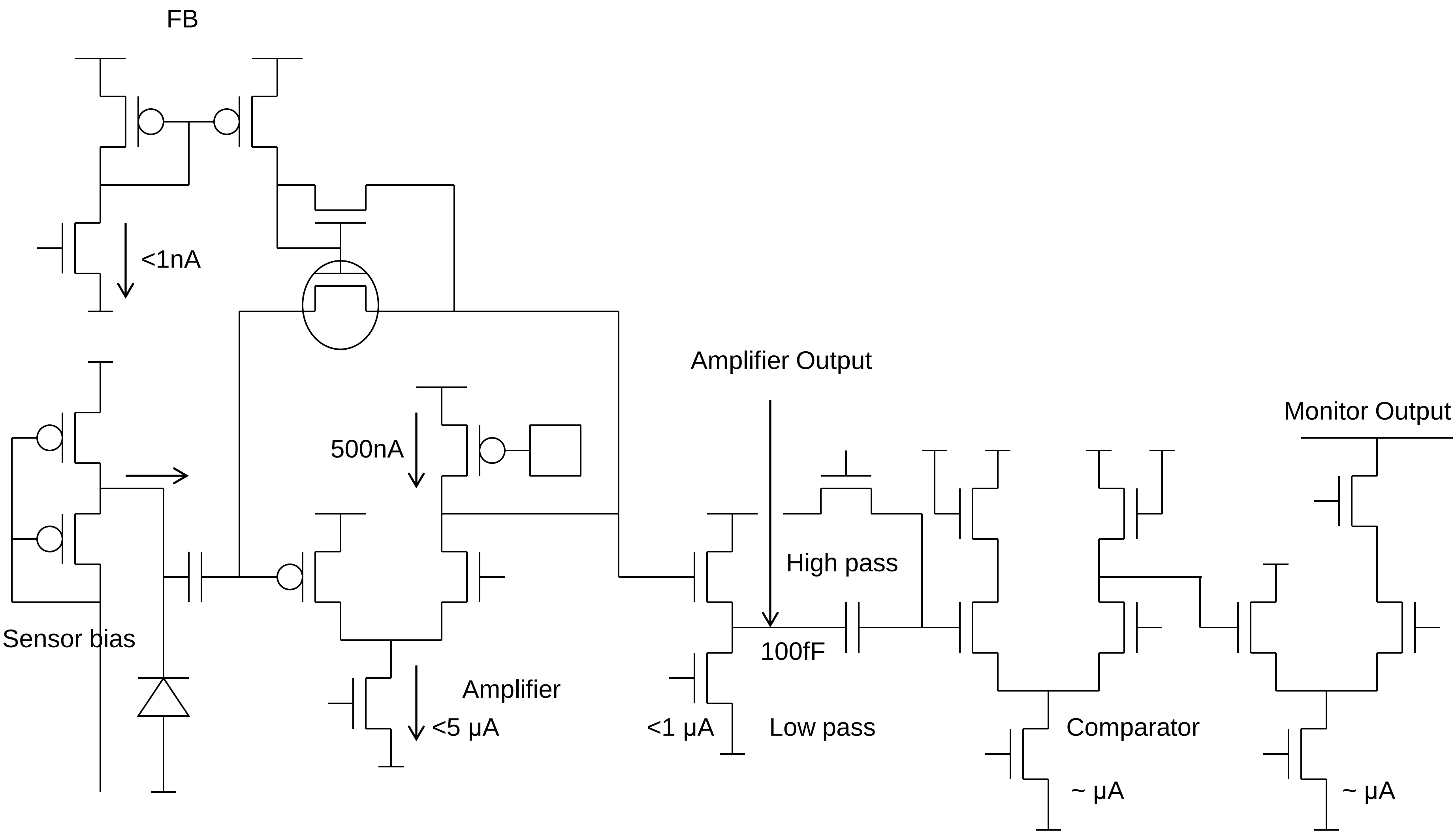



FEI4 Pixels
Signal transmitted capacitively
CCPD Pixels
2
2
3
3
1
1
Bias A
Bias B
Bias C
+

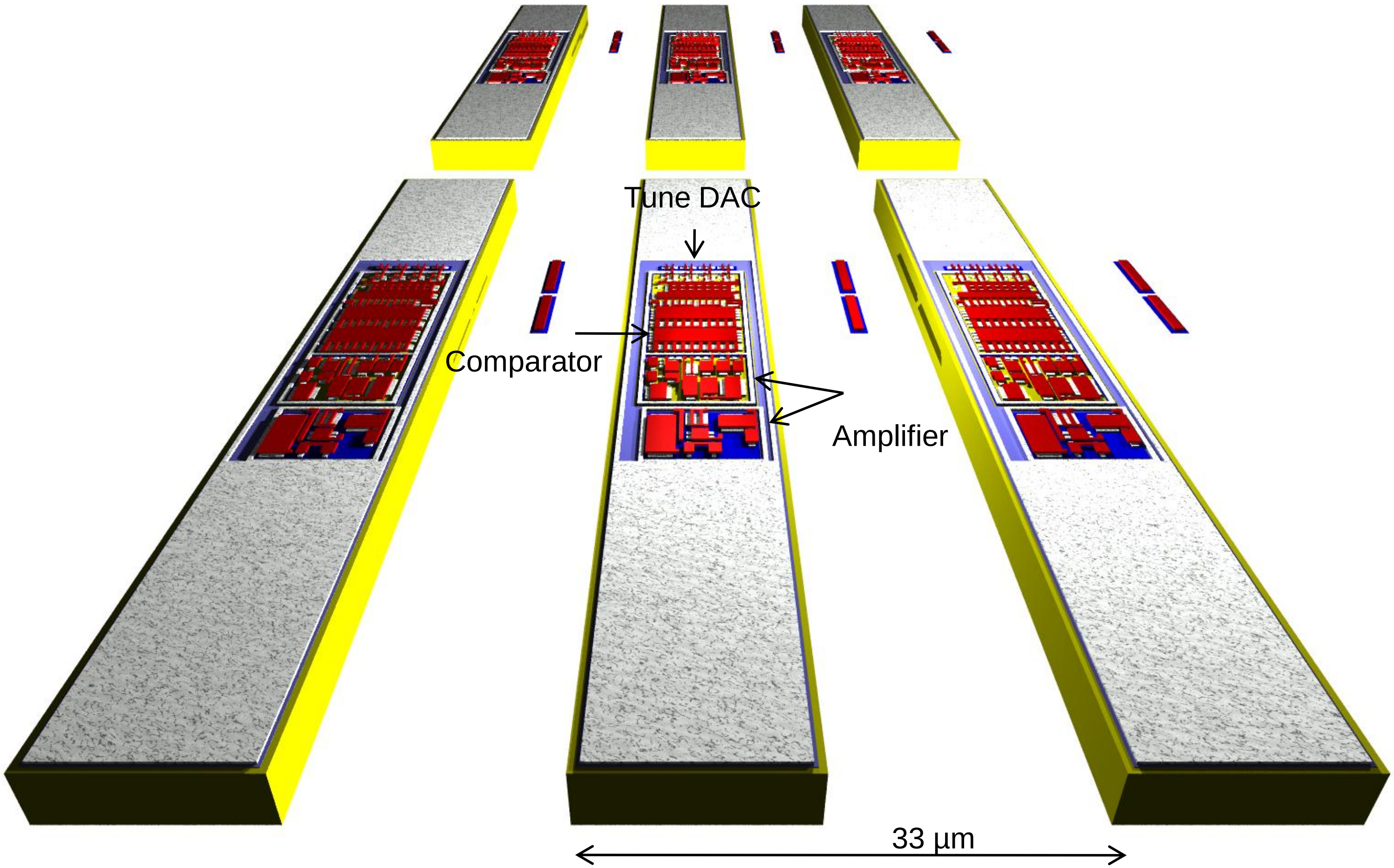

Pad
Pad

Pixel electronics - layout



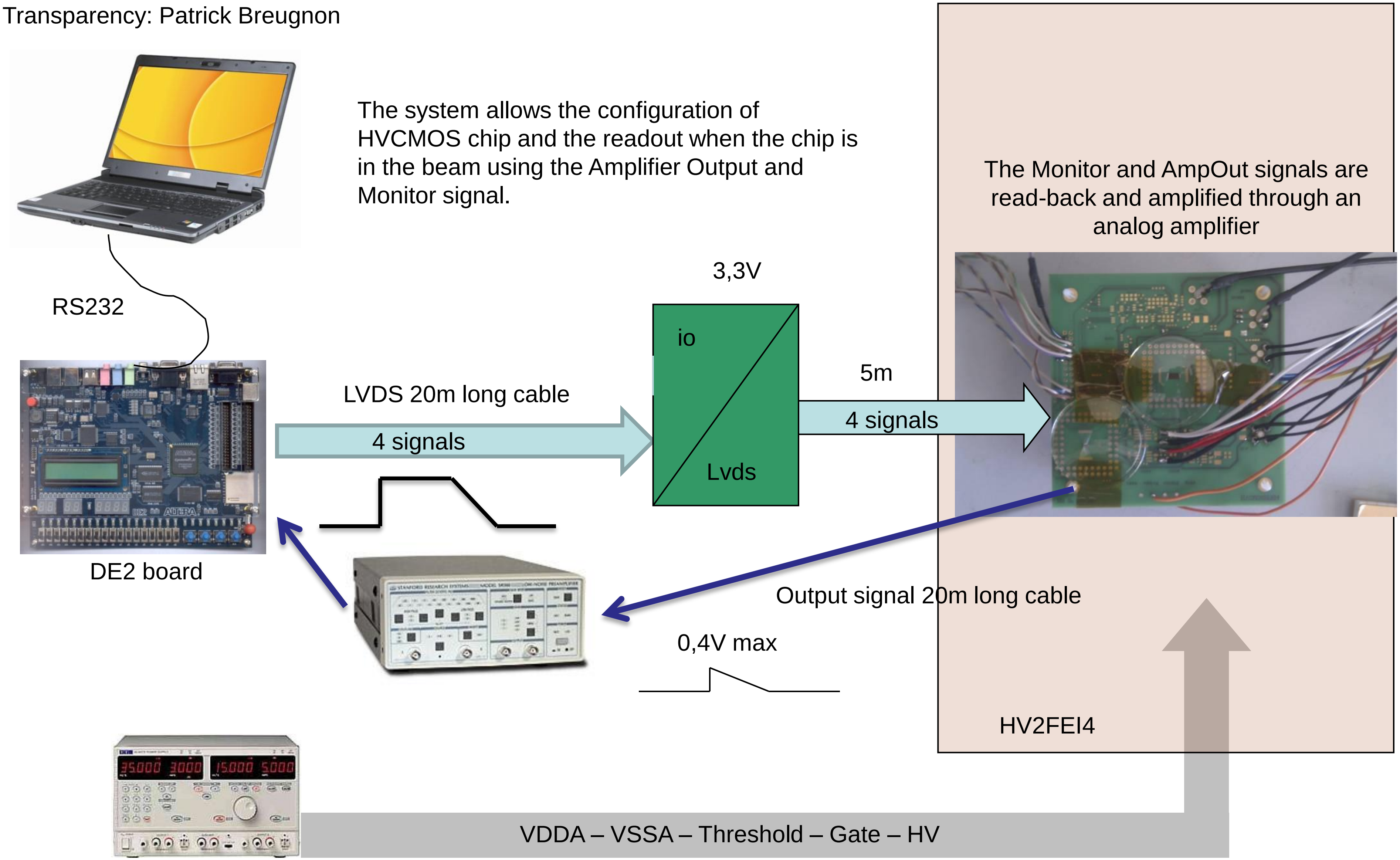

FB
<1nA
500nA
Amplifier Output
Monitor Output
High pass
100fF
Sensor bias
Amplifier
<5 μA
<1 μA
Low pass
Comparator
~ μA
~ μA

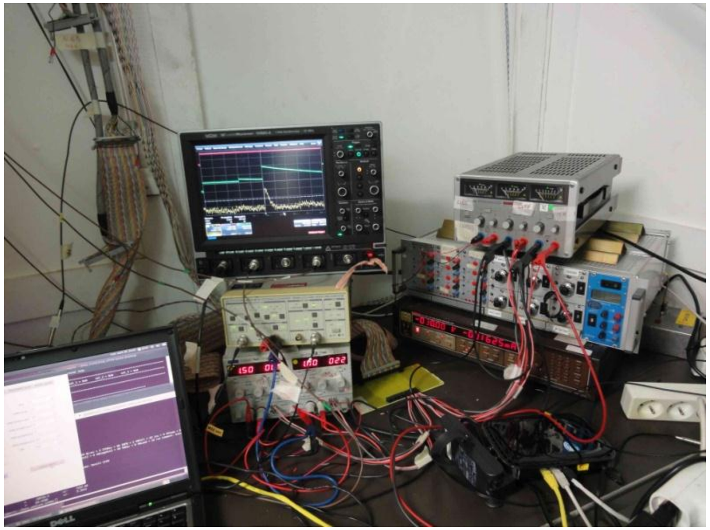
6 pixels – layout

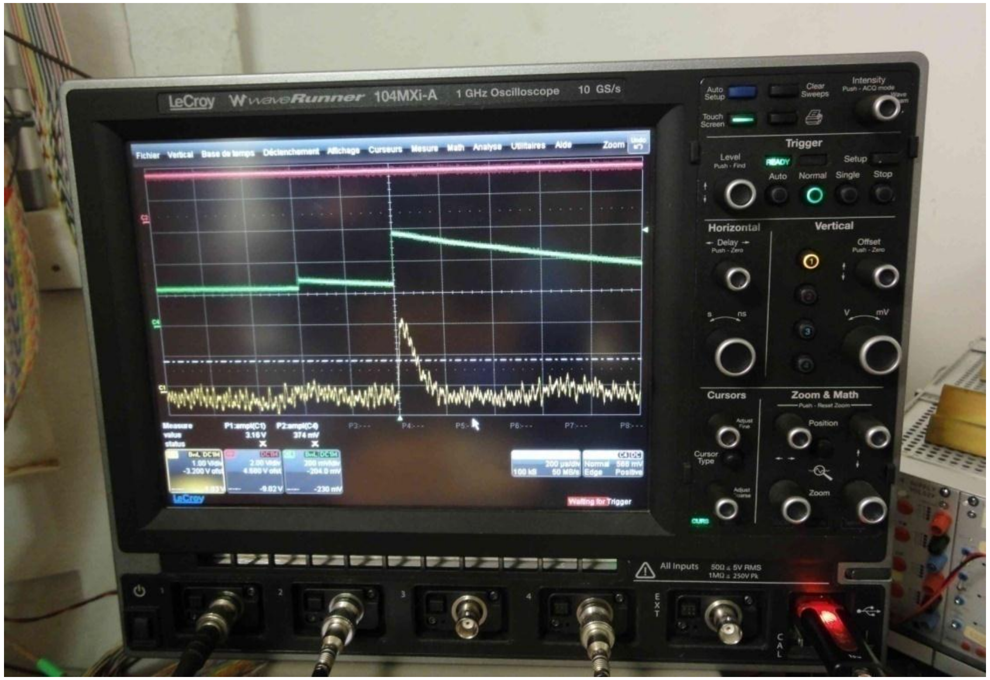


Transparency: Patrick Breugnon

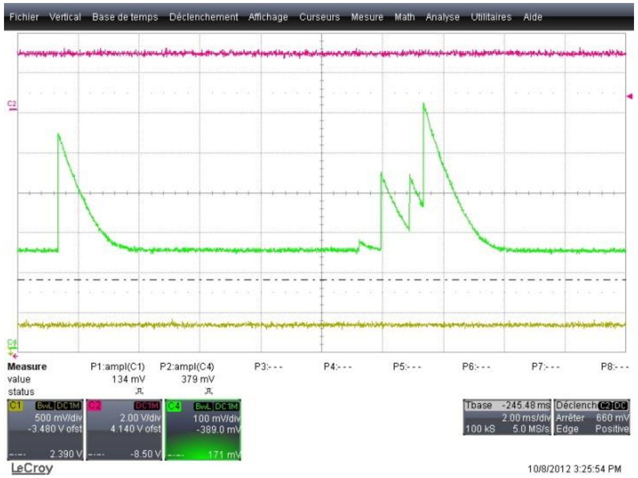
The system allows the configuration of HVCMOS chip and the readout when the chip is in the beam using the Amplifier Output and Monitor signal.

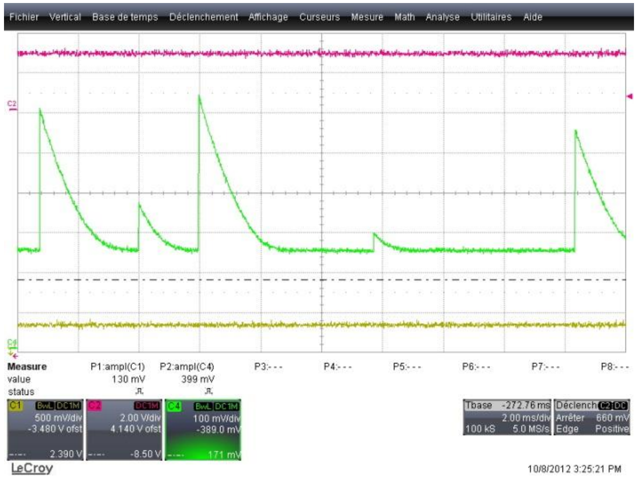




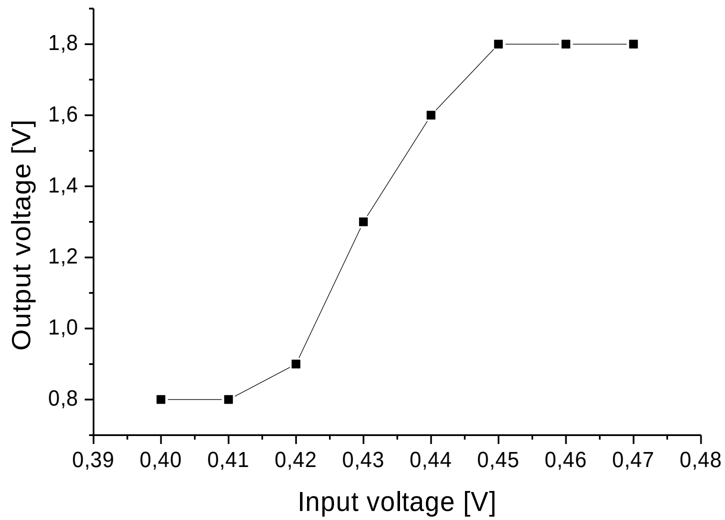

LeCroy
WaveRunner 104MXi-A
1 GHz Oscilloscope
10 GS/s
Trigger
Horizontal
Vertical
Cursors
Zoom & Math

Results after 380 MRad and ~ 8 x 10^{15} n_{eq}/cm^2



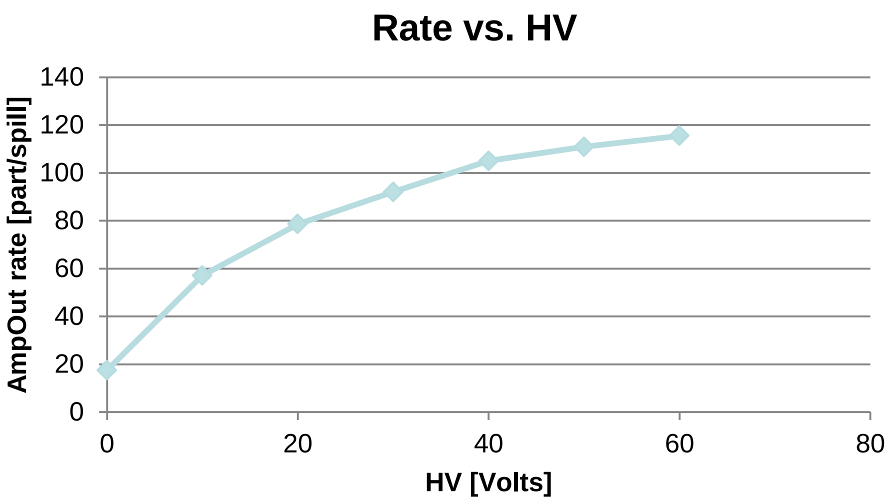


The chip works, particles are measured when the chip is in the beam: Output of the amplifier

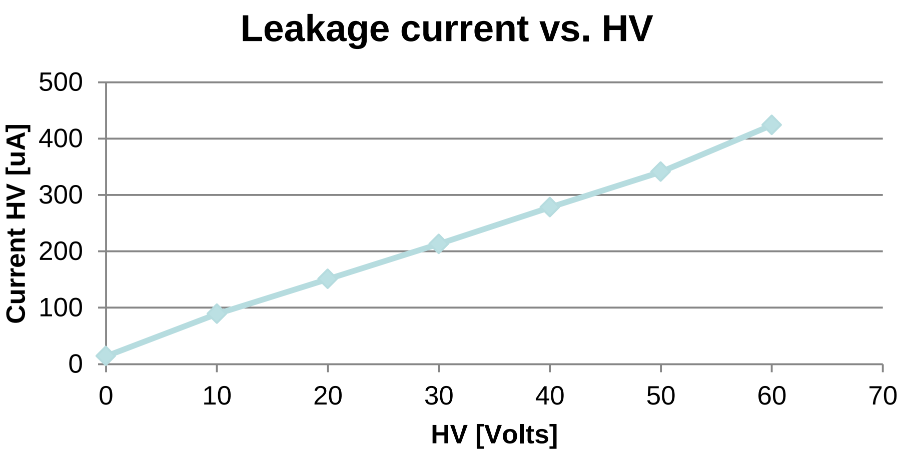


Comparator characteristics.

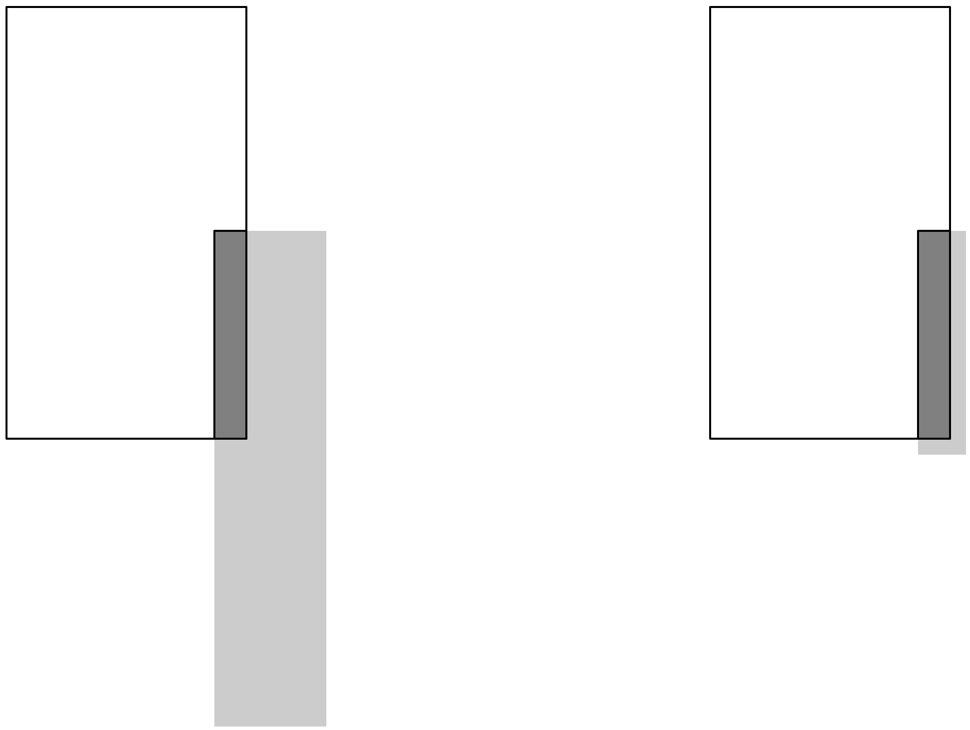
Results after 144 MRad



The rate of detected particles depends on the high voltage bias.
T: Superposition of two effects:
Positive effect: The increase of HV bias leads to an increase of the depleted region depth => better detection efficiency.
Negative effect: The increase of the leakage current leads to a signal loss.

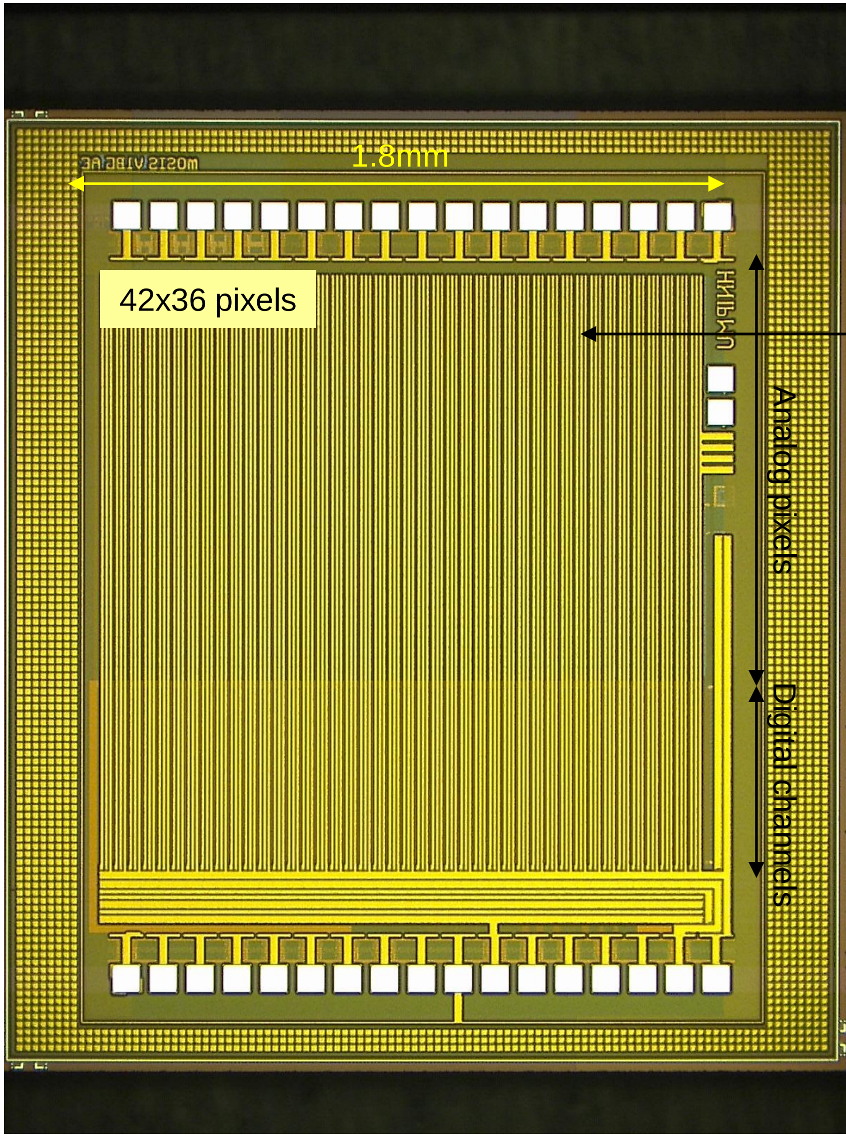


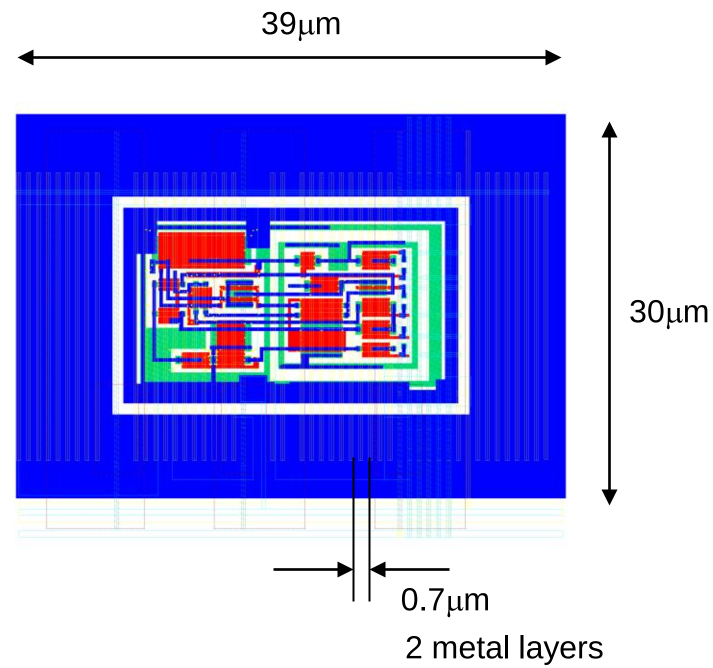
Measured HV (leakage) current dependence on the high voltage bias.
T: Leakage current depends on the volume of the depleted region.
Linear size of the depleted layer depends as *square root* of the bias voltage but…
The cylindrical depleted layer volume depends *linearly* on bias voltage.



Charge multiplication effect

Test device: Mu3e test-chip

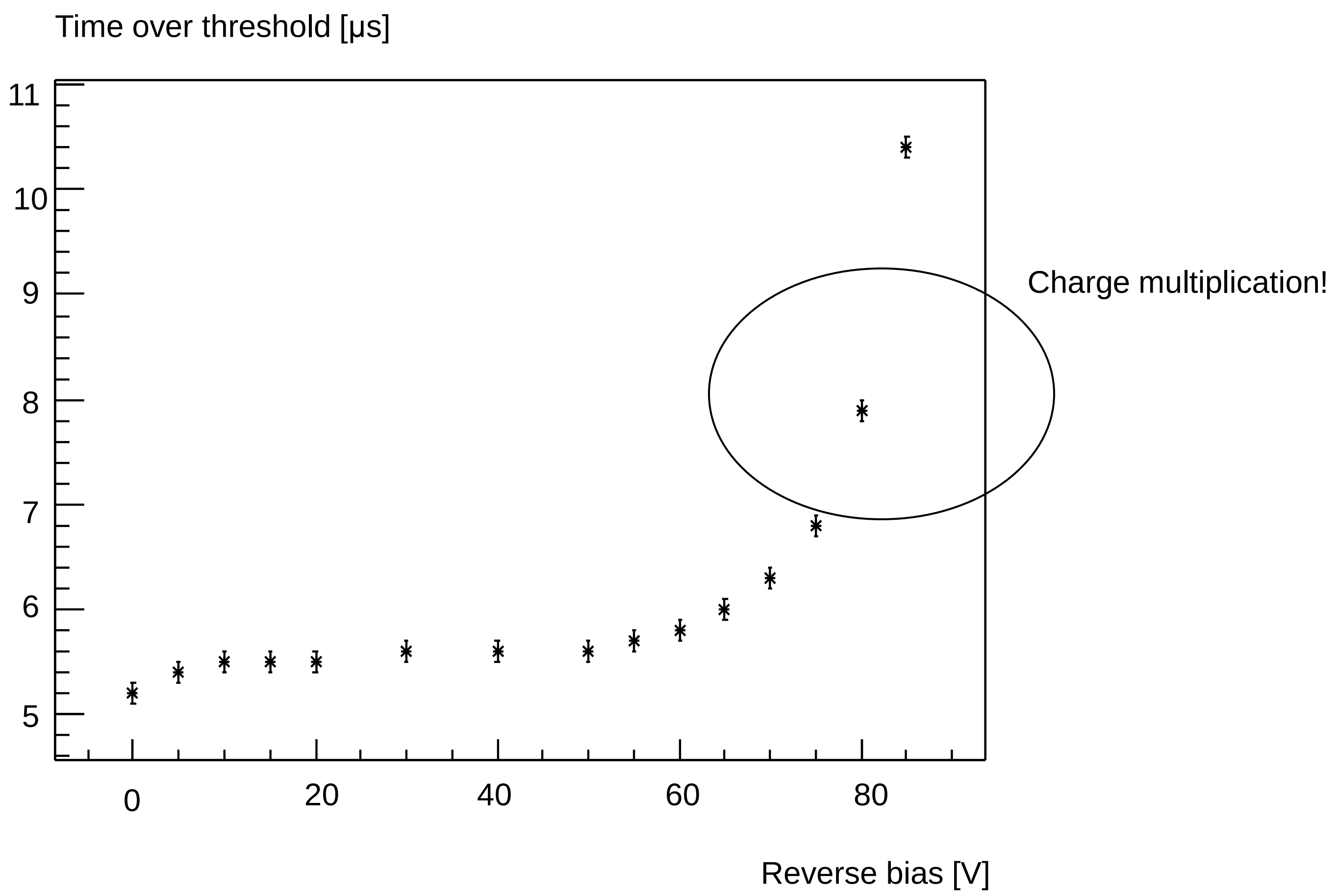




Analog pixel layout

Pixel size 39x30 micrometers.
Separated digital and analog block.
Signal amplitude can be measured as ToT.

- LED – light pulses have been detected.
- Signal amplitude has been measured as the time over threshold.
- From 60V reverse bias, the time over threshold increases exponentially. (about 2x increase)



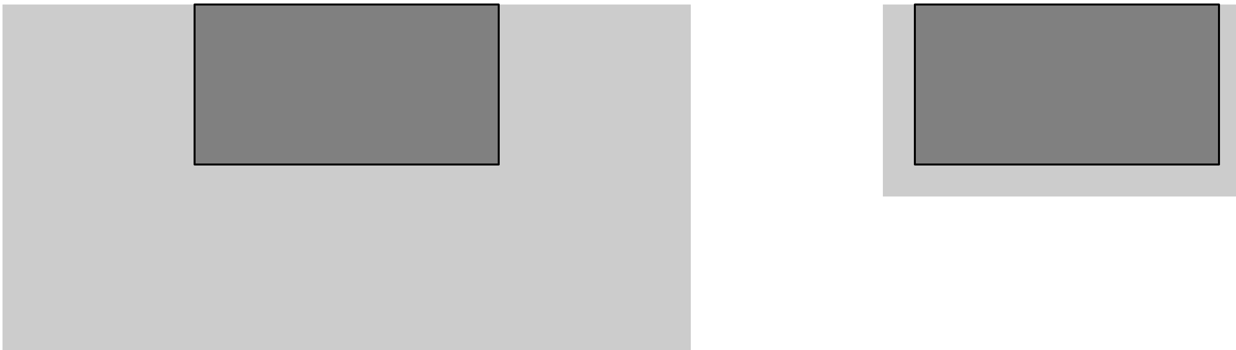
Conclusions

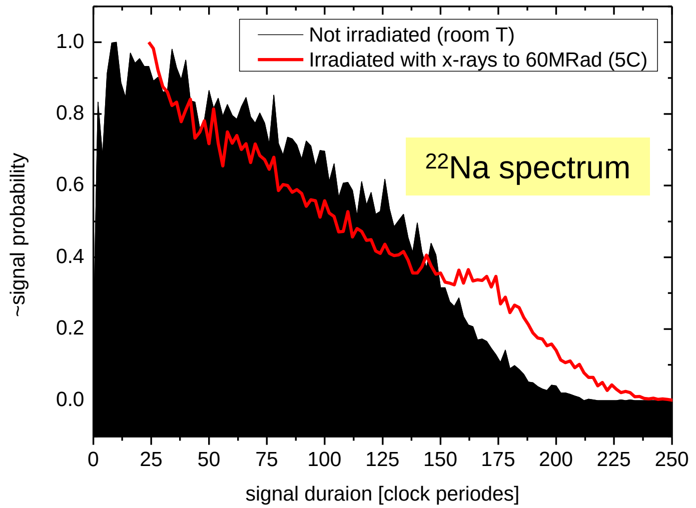
- HVCMOS is an active pixel technology with the charge collection based on drift.
- Thanks to the use of commercial processes, the production of relatively low-cost (1.5 k€/12' wafer), large area detectors is possible.
- We have irradiated test HVCMOS sensors wit neutrons (10^{14} n_{eq}) (Munich), protons (10^{15} n_{eq} and 8×10^{15} n_{eq} - 380 MRad) (KIT and PS), and x-rays (50MRad) (KIT).
- Two main effects are observed:
- 1) Reduction of the secondary signal part that is collected by diffusion.
- 2) Increase of leakage current.
- Good SNR can be achieved after irradiation if the sensors are cooled to ~ 0C.
- Charge multiplication factor can further increase SNR.
- Although we still do not understand all effects, the HVCMOS sensors seem to have a high radiation tolerance.

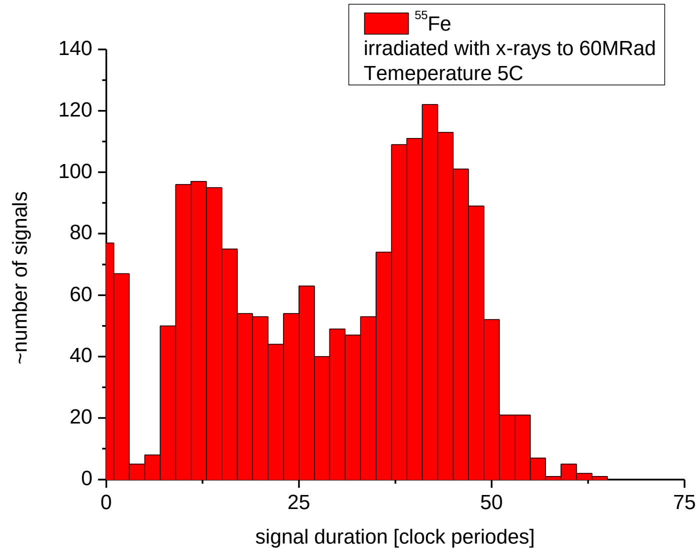
Thank you

Backup Slides

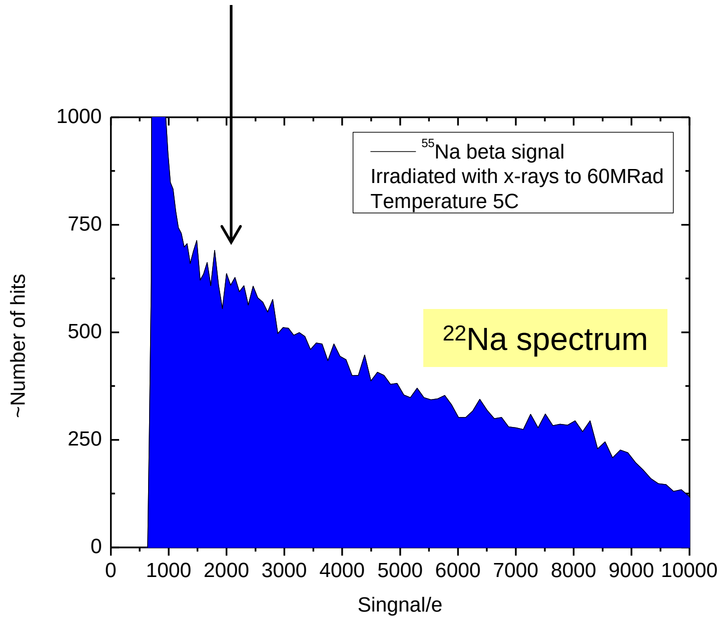
Decrease of counting rate





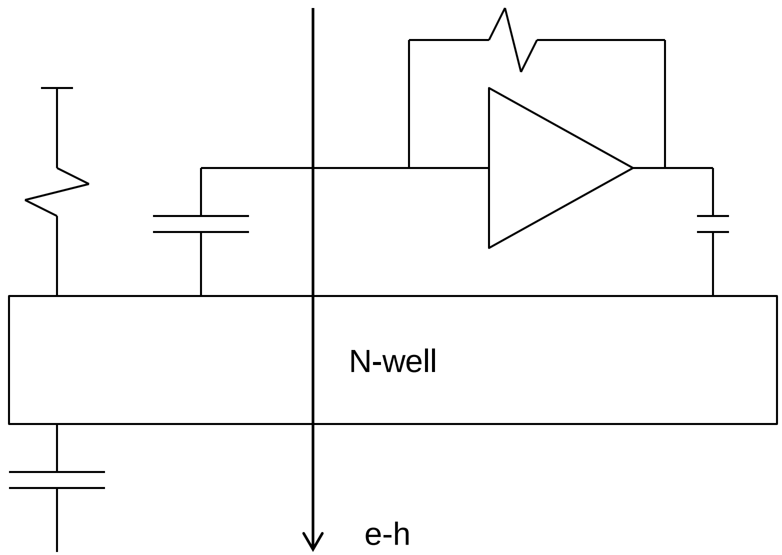


22Fe spectrum

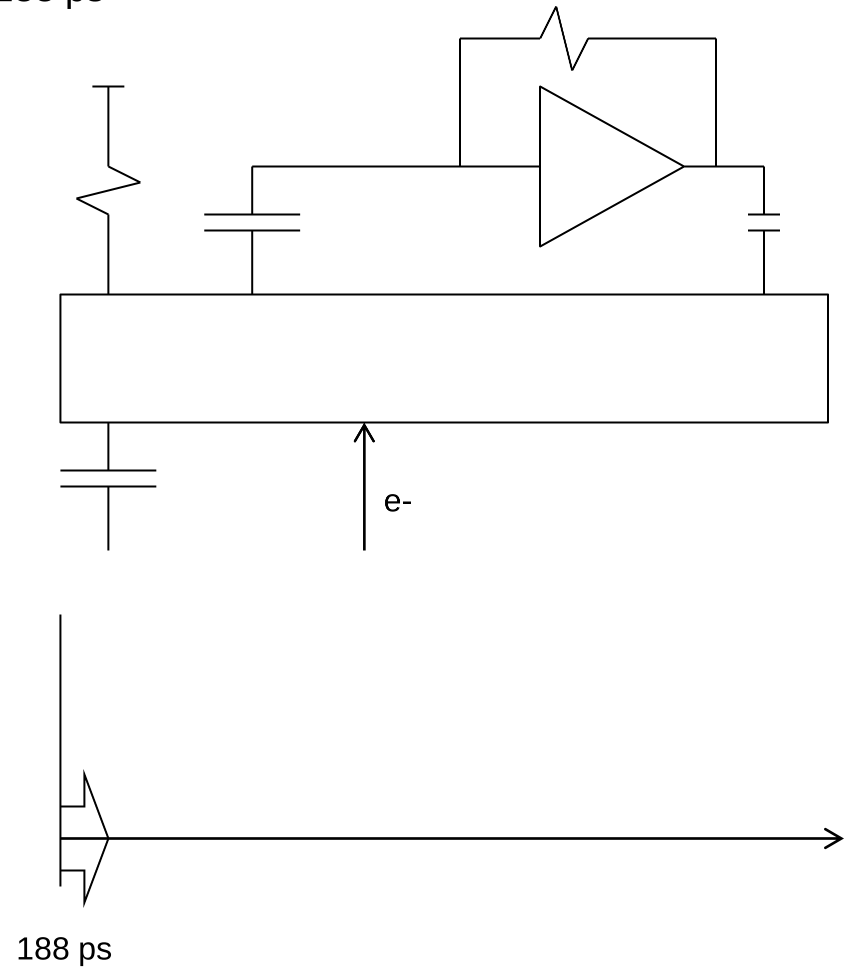


Signal-generation and amplification

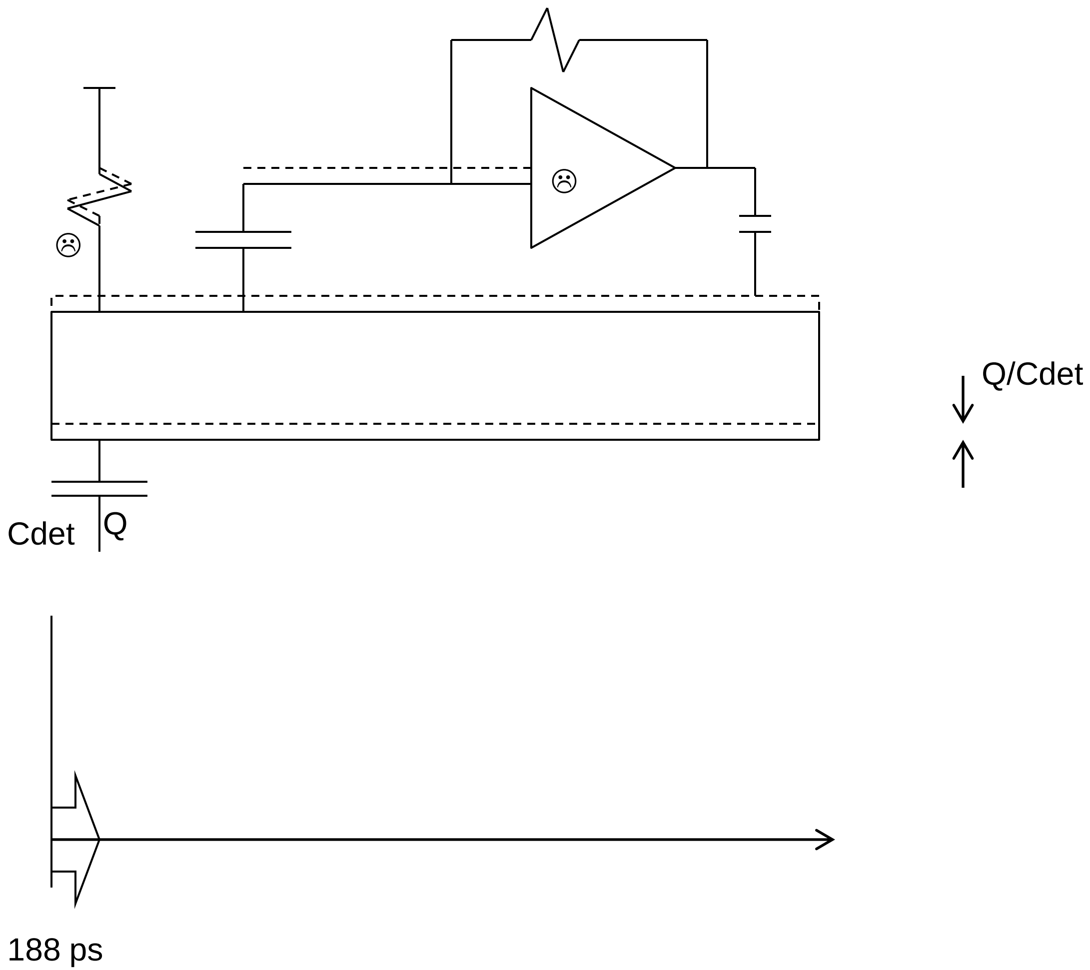
- Particle hit



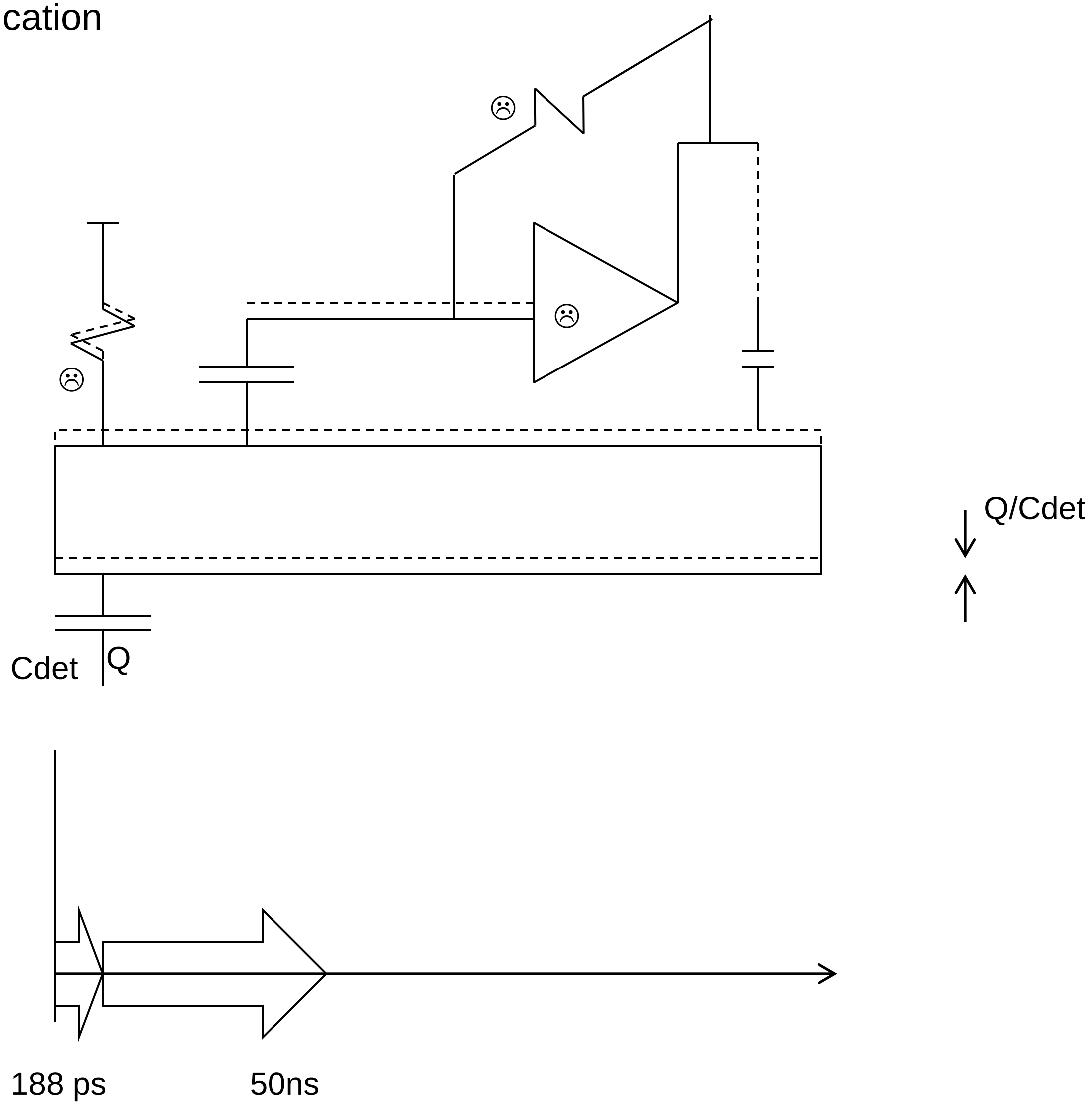
- Charge collection
- Assume: V_{sat} = 8 x 10^4 m/s
- T_{col} = 188 ps



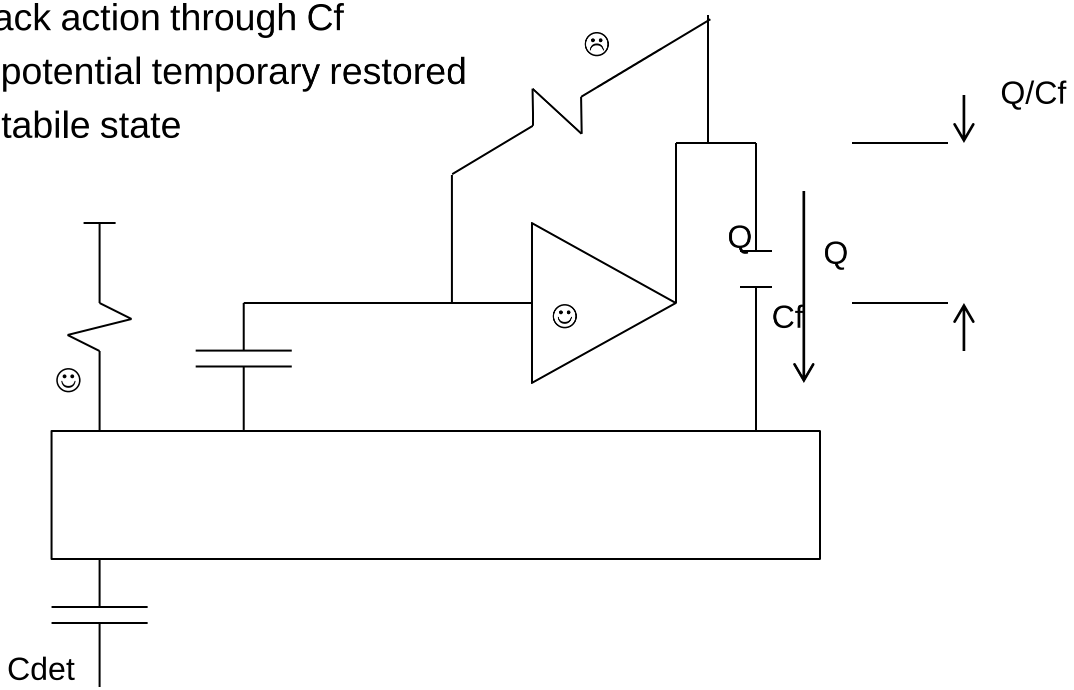
- Voltage drop in the n-well

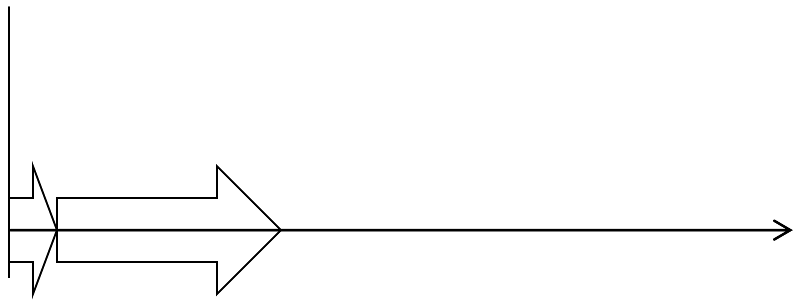


- Amplification

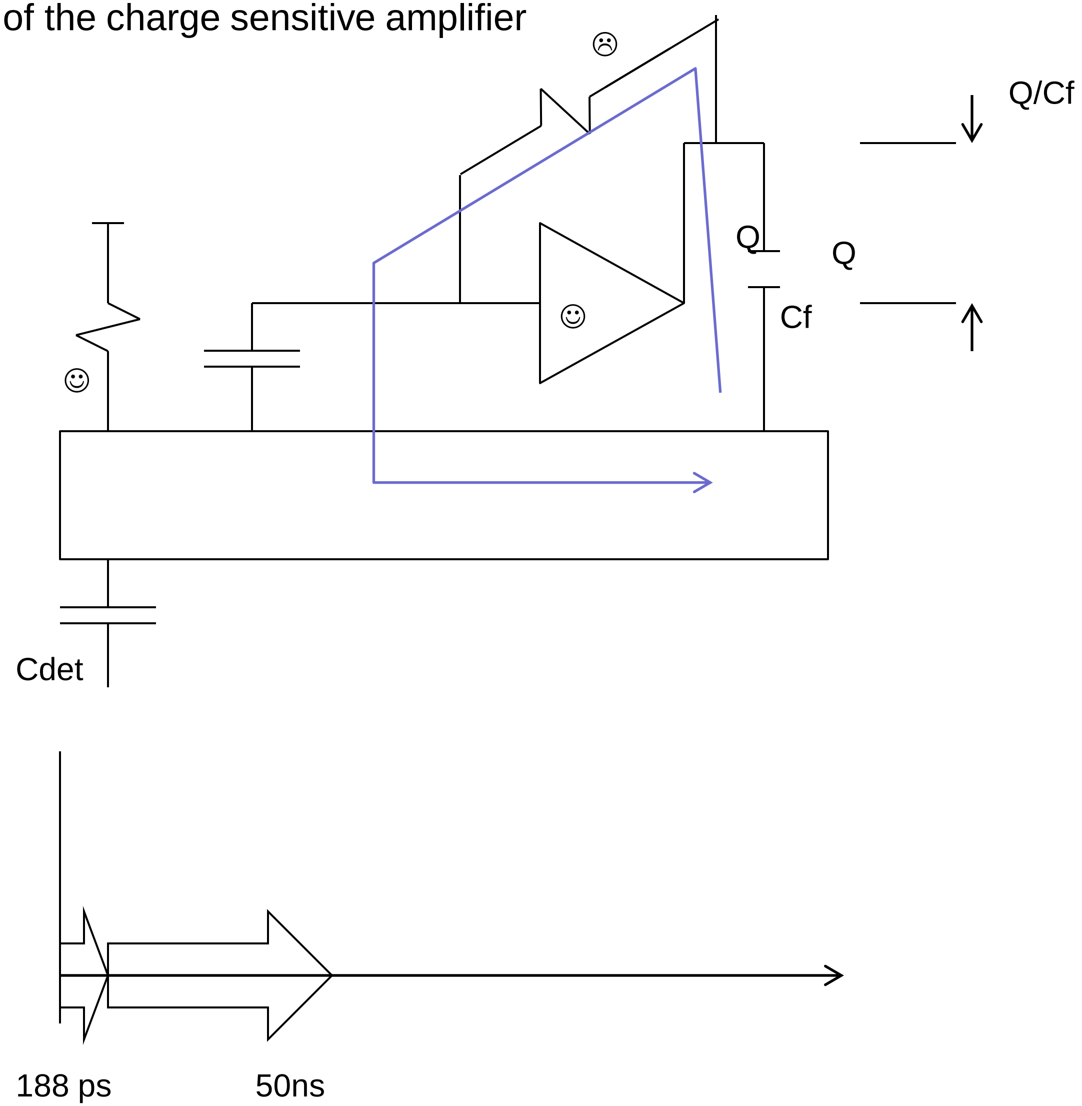


- Feedback action through Cf
- N-well potential temporary restored
- Meta-stabile state



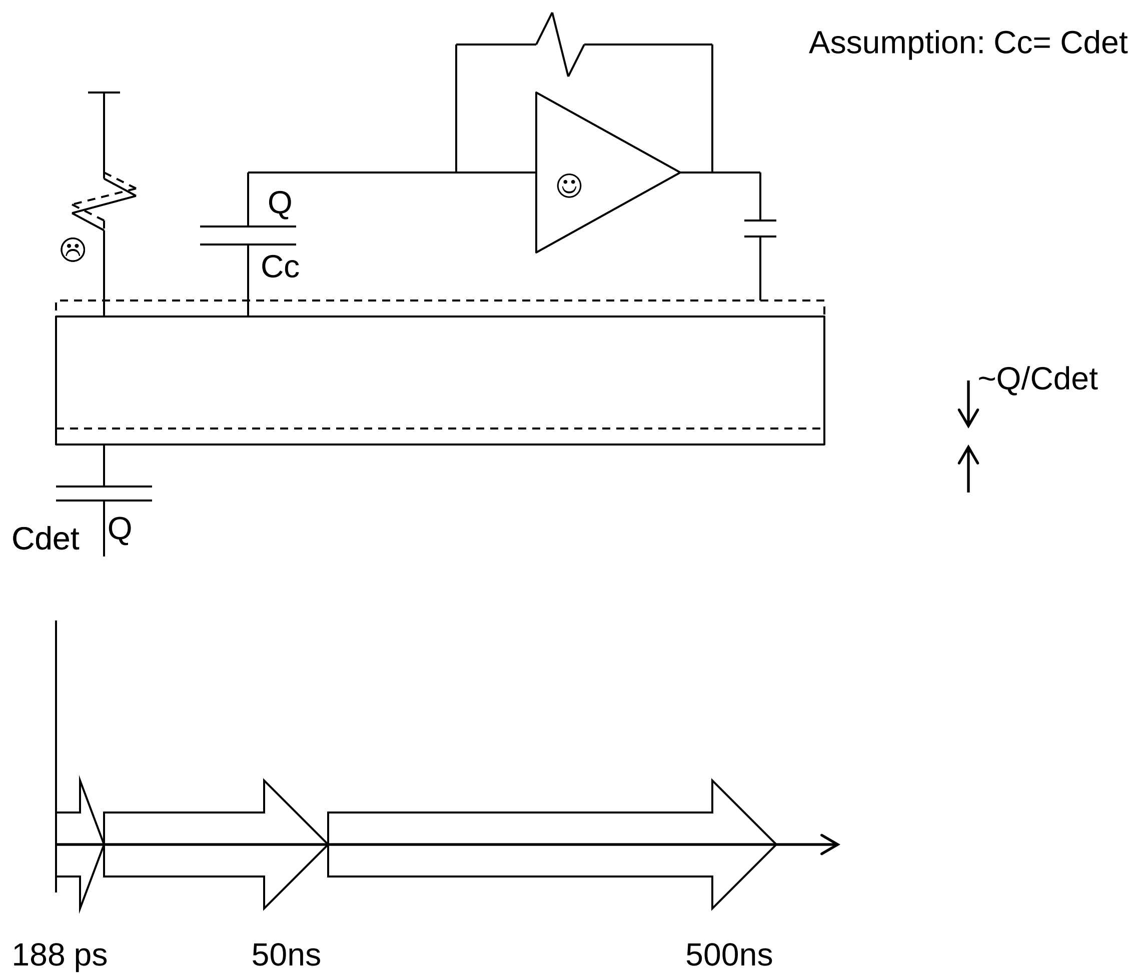


- Reset of the charge sensitive amplifier

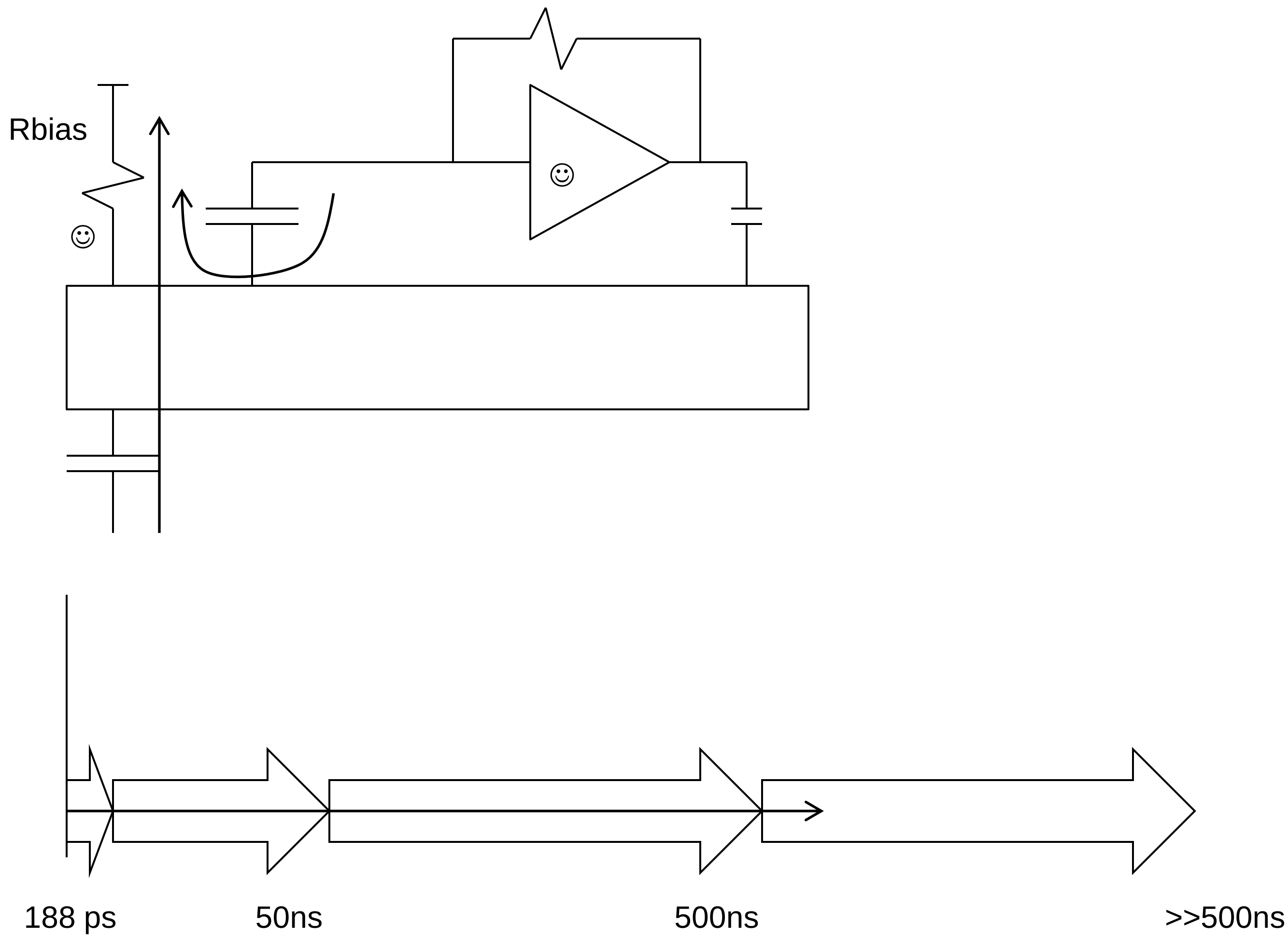


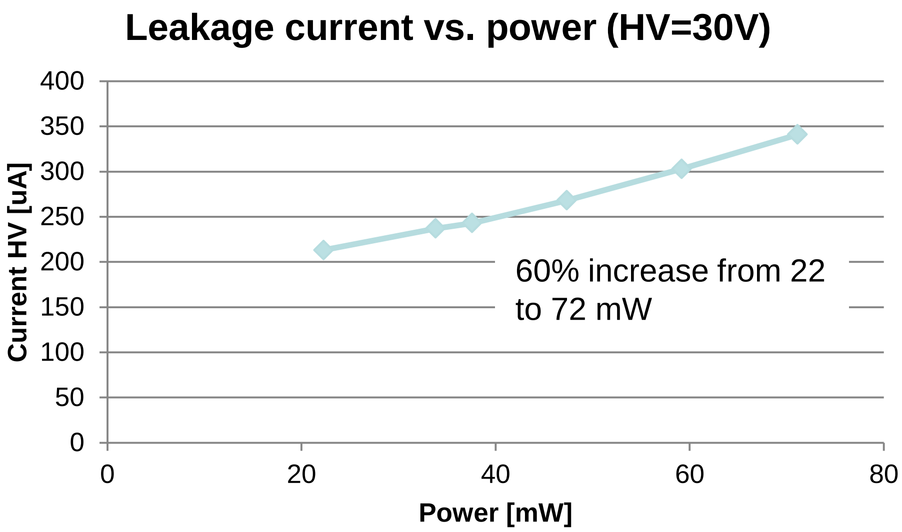
HV CMOS detectors

- Reset of the charge sensitive amplifier accomplished:
- N-well again negative!

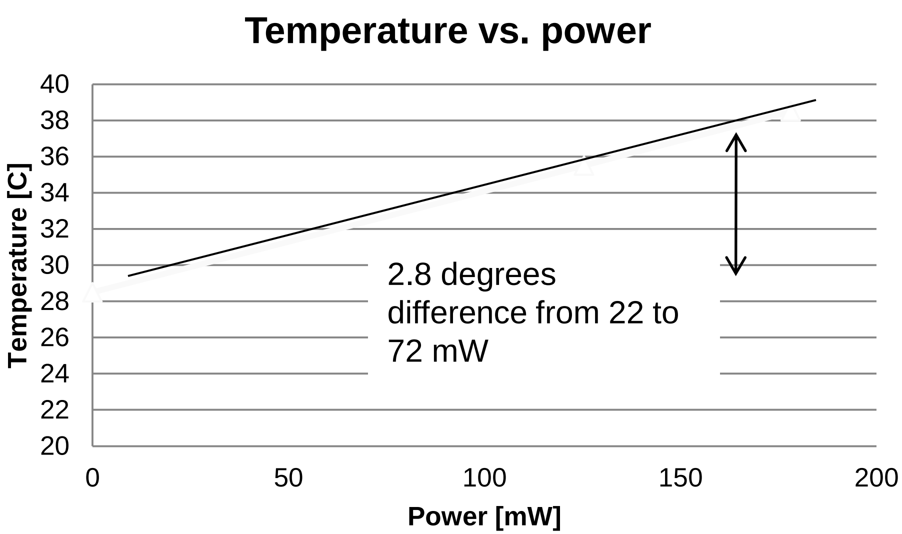


- Initial voltage across the n-well and the coupling capacitance restored by R_{bias}



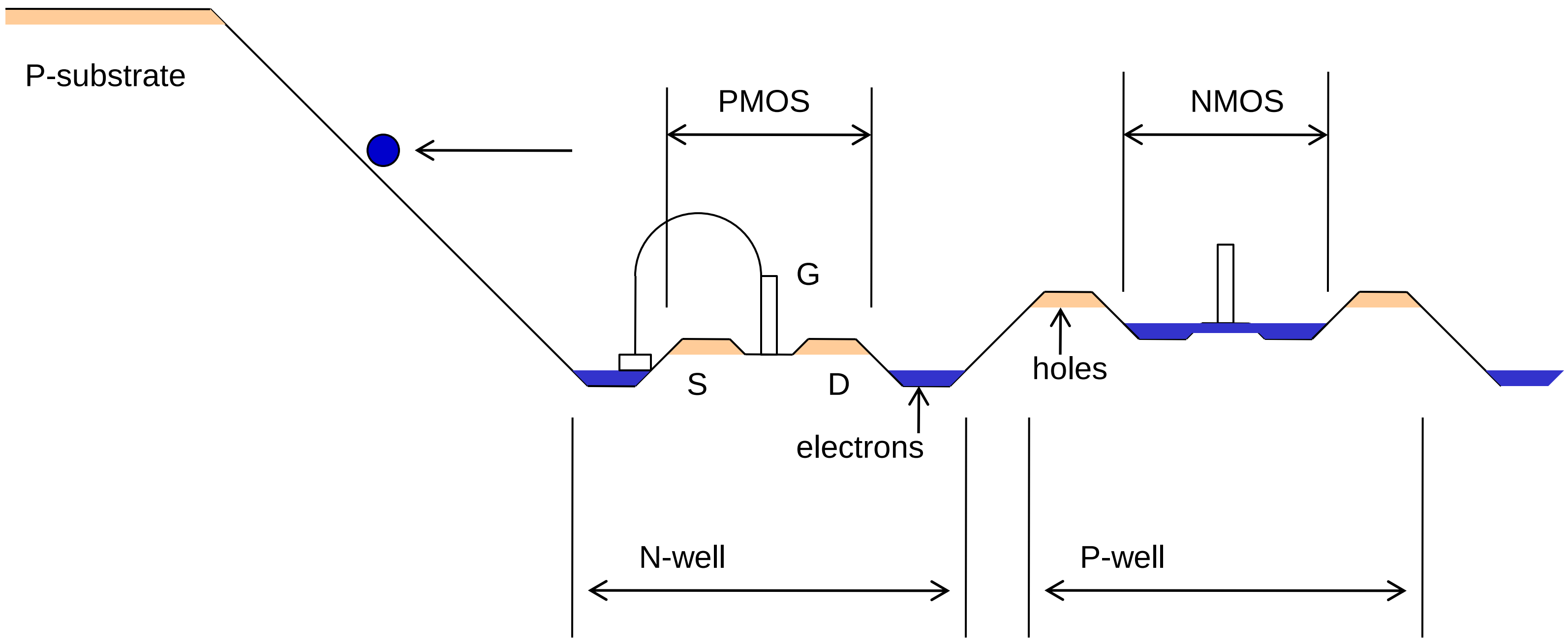


Measured HV current dependence on the analog power.
T: Increase of the analog power leads to a temperature increase.
The temperature increase leads to the diode leakage increase.



Measured temperature dependence on the analog power.
Check: About 2.8 degrees temperature increase leads to 60% leakage increase,

- Collected charge causes a voltage change in the n-well.
- This signal is sensed by the amplifier – placed in the n-well.



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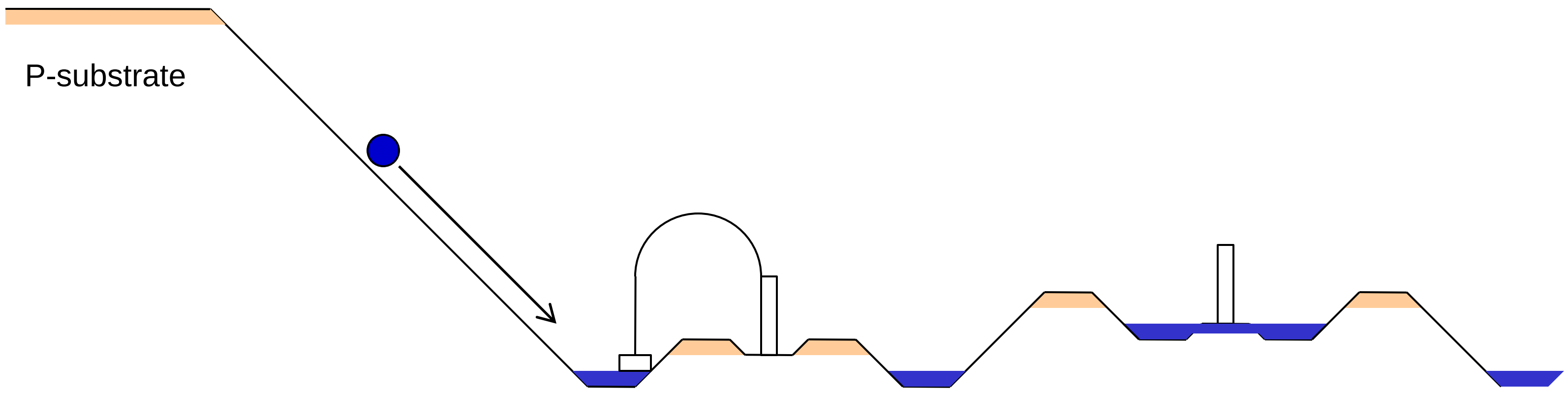

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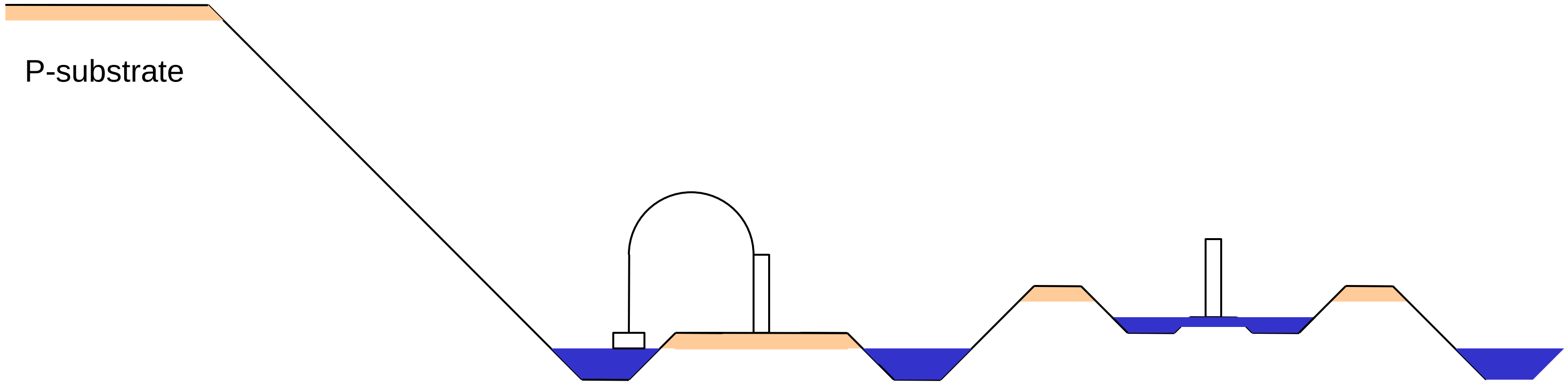


Experimental results - overview

HVPixel1 – **CMOS in-pixel electronics with hit detection**
Binary RO
Pixel size 55x55µm
Noise 60e
MIP seed pixel signal 1800 e
Time resolution 200ns

Capacitive coupled hybrid detector

CCPD2 -**capacitive coupled pixel detector**
Pixel size 50x50µm
Noise 30-40e
Time resolution 300ns
MIP SNR 45-60

Irradiations of test pixels
60MRad – MIP SNR 22 at 10C (CCPD1)
$10^{15}n_{eq}$ MIP SNR 50 at 10C (CCPD2)

HV2FEI4 chip
CCPD for ATLAS pixel detector
Readout with FEI4 chip
Reduced pixel size: 33x125µm
RO type: capacitive and strip like
Noise: ~80e (stand alone test, preliminary)

Monolithic detector – continuous readout with time measurement

MuPixel –
Monolithic pixel sensor for Mu3e experiment at PSI
Charge sensitive amplifier in pixels
Hit detection, zero suppression and time measurement at chip periphery
Pixel size: 39x30 µm (test chip)
(80 x 80 µm required later)
MIP seed signal 1500e (expected)
Noise: ~40 e (measured)
Time resolution < 40ns
Power consumption 7.5µW/pixel

Monolithic detector - frame readout

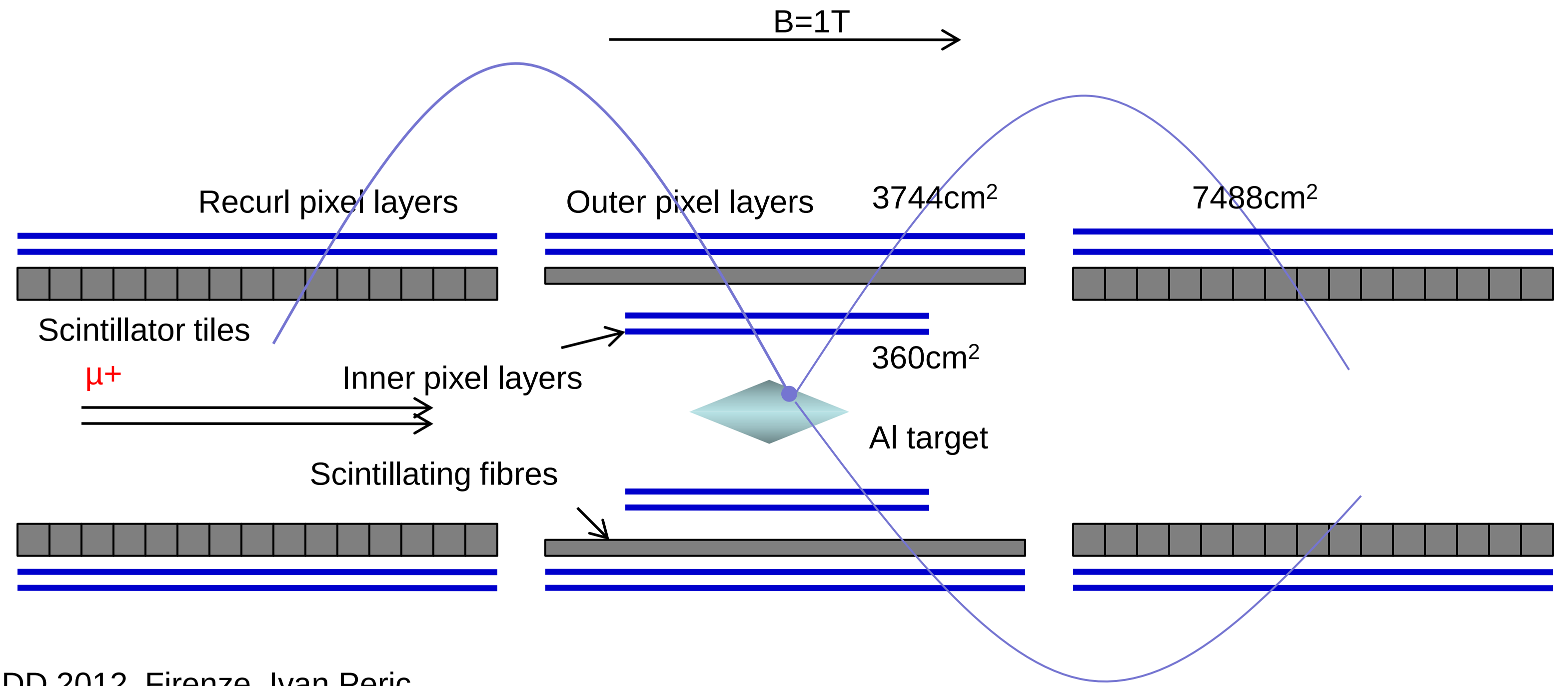
PM2 chip - frame mode readout
Pixel size 21x21µm
4 PMOS pixel electronics
128 on-chip ADCs
Noise: 21e (lab) - 44e (test beam)
MIP signal - cluster: 2000e/seed: 1200e
Test beam: **Detection efficiency >98%**
Seed Pixel SNR ~ 27
Cluster signal/seed pixel noise ~ 47
Spatial resolution ~ 3 µm

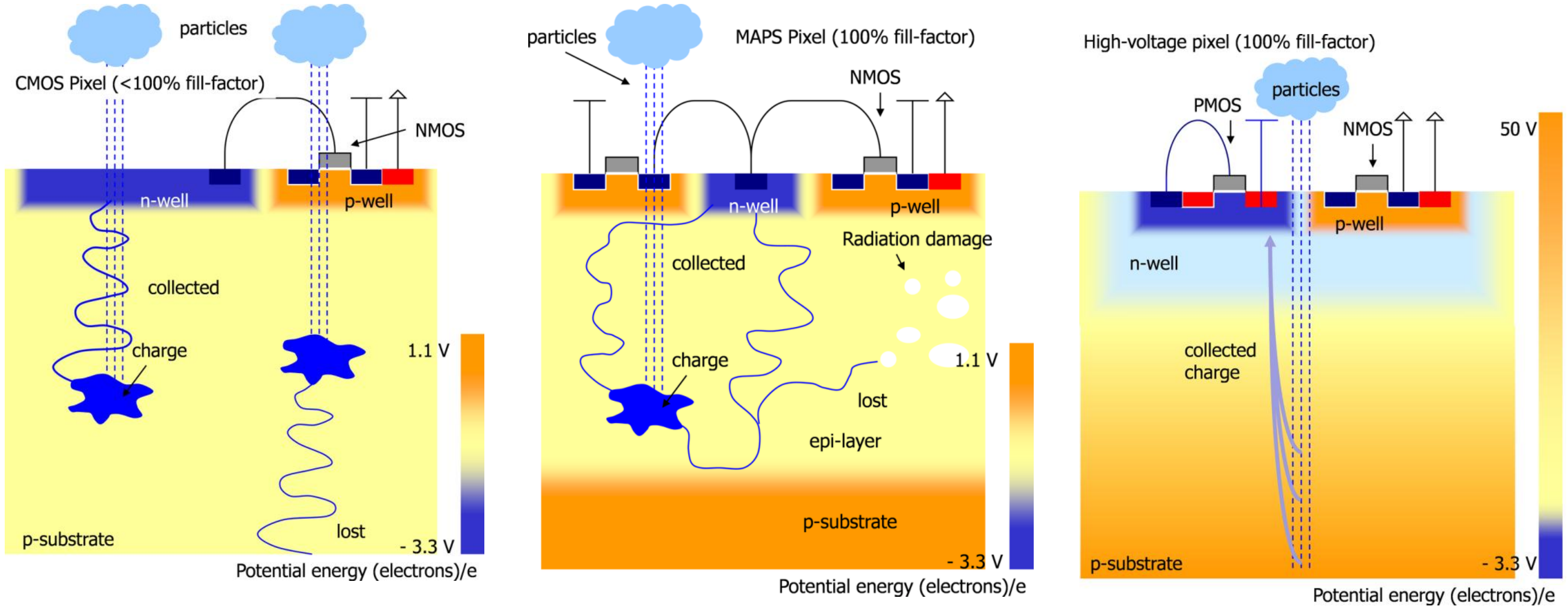
HPixel - frame mode readout
In-pixel CMOS electronics with CDS
128 on-chip ADCs
Pixel size 25x25 µm
Noise:60-100e (preliminary)
MIP signal - cluster: 2100e/seed: 1000e (expected)

SDS - frame mode readout
Pixel size 2.5x2.5 µm
4 PMOS electronics
Noise: 20e (preliminary)
MIP signal (~1000e - estimation)

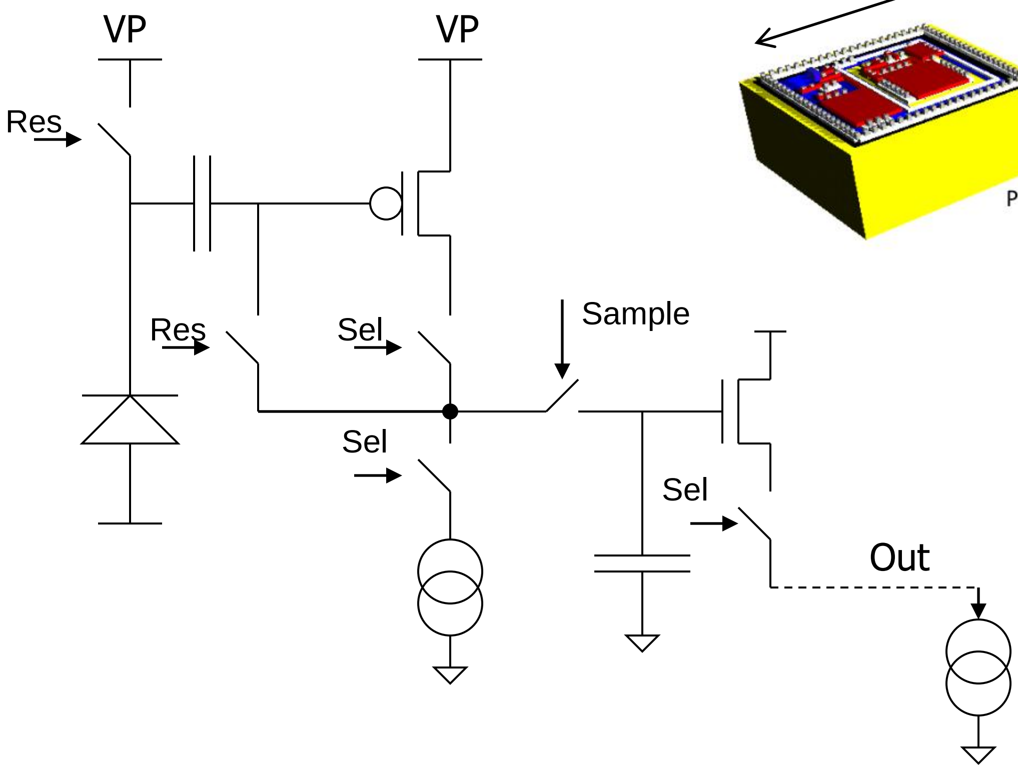
1. Technology 350nm HV – substrate 20 Ωcm uniform
2. Technology 180nm HV – substrate 10 Ωcm uniform
3. Technology 65nm LV – substrate 10 Ωcm/10 µm epi

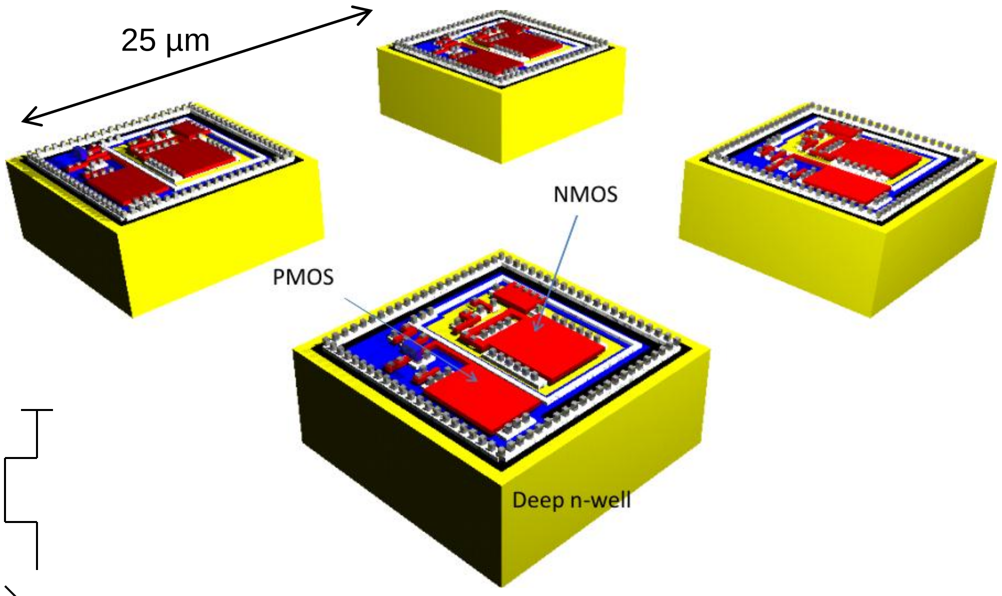
- Proposed: four layers of pixels ~ 80x80μm^2 size – HV CMOS monolithic detectors
- Time stamping with < 100ns resolution required to reduce the number of tracks in an image.
- Sensors should be thinned to ~50 μm
- Triggerless readout
- Power ~ 200mW/cm^2 cooling with helium
- Total area: 1.9 m^2
- 275 M pixels
- 100 wafers (if 100% yield)




particles
CMOS Pixel (<100% fill-factor)
NMOS
n-well
p-well
collected
charge
1.1 V
lost
p-substrate
- 3.3 V
Potential energy (electrons)/e
particles
MAPS Pixel (100% fill-factor)
NMOS
n-well
p-well
Radiation damage
collected
charge
1.1 V
lost
epi-layer
p-substrate
- 3.3 V
Potential energy (electrons)/e
High-voltage pixel (100% fill-factor)
particles
PMOS
NMOS
50 V
p-well
n-well
collected
charge
p-substrate
- 3.3 V
Potential energy (electrons)/e

- Correlated double-sampling (CDS) is implemented in the pixels using CMOS electronics. The pixel output signals are digitized by 128 on-chip ADCs.
- The readout electronic has been optimized for a fast readout and a low power consumption.





A pixel with CMOS-based electronics