HV-CMOS

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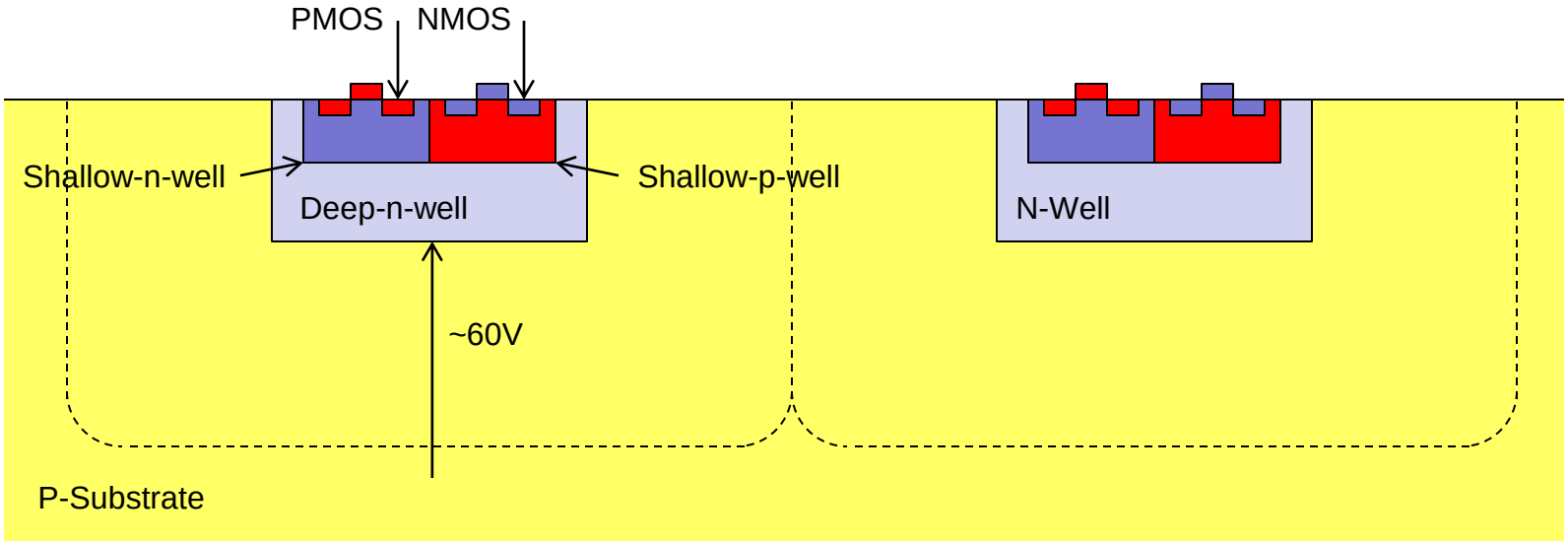
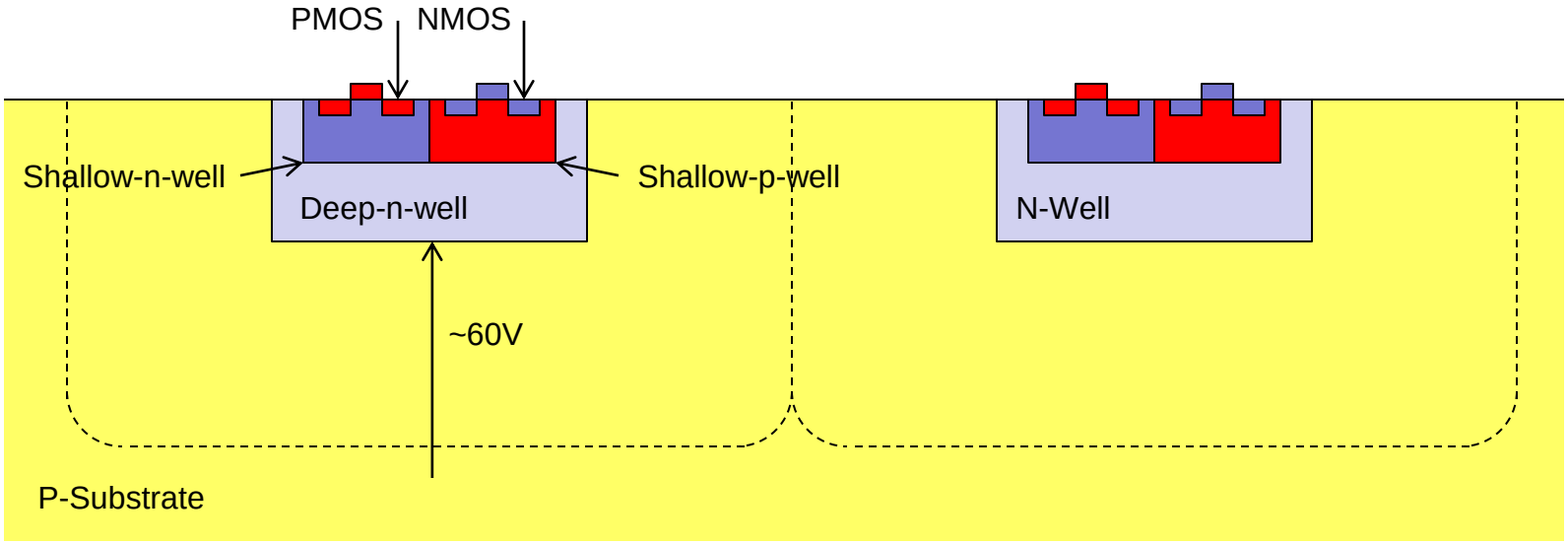
for ATLAS and CLIC HVCMOS R&D and Mu3e Collaborations

- Ideas:
- Use the standard (HV)CMOS technologies to implement particle detectors
- Use a high voltage to deplete the sensor volume – charge collection by drift
- The standard implementation: CMOS electronics inside the deep n-well-collecting electrode
- “Smart diode”
- Partial depletion from the top, no backside electrode needed

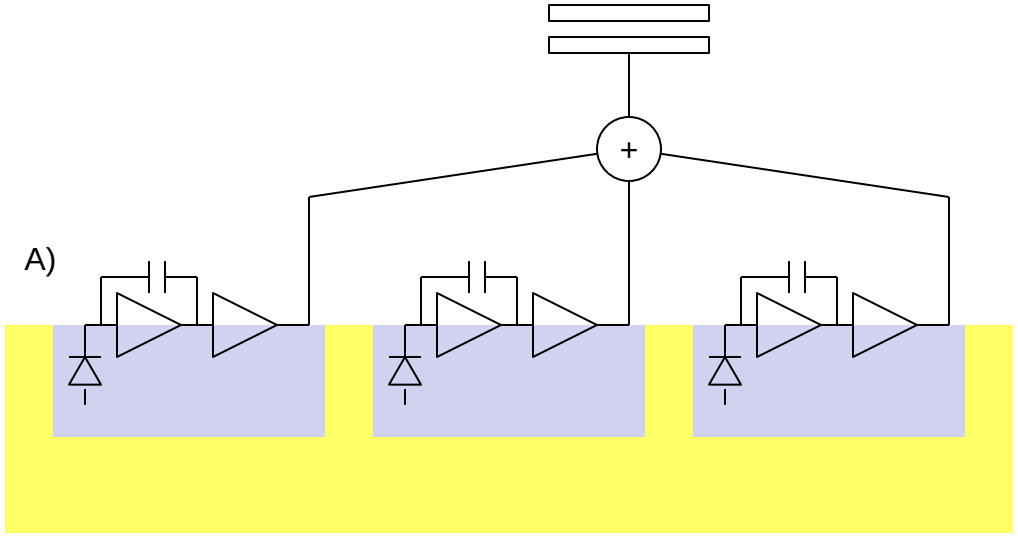


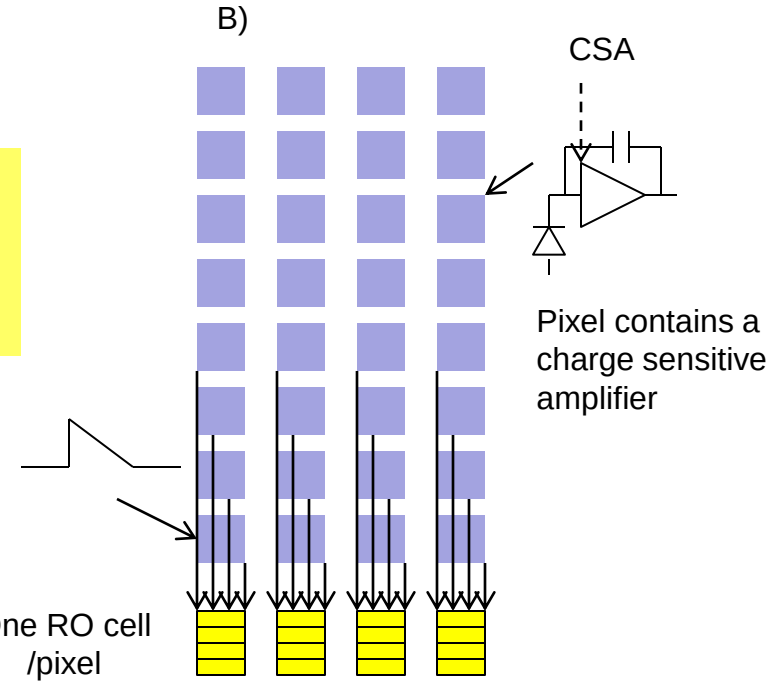
- Some drawbacks:
- The standard substrates are relatively low resistive (~20 Ωcm)
- The depleted region is up to ~15 µm thick – MIP signals are relatively weak ~ 1800 e
- The collection electrode is, at the same time, the PMOS bulk – there is a strong capacitive crosstalk from PMOS transistors to the detector input.
- General drawback of monolithic sensors: Complex in-pixel electronics leads to increased detector capacitance or to decreased electrode-/pixel-size ratio



HVCMOS detector types

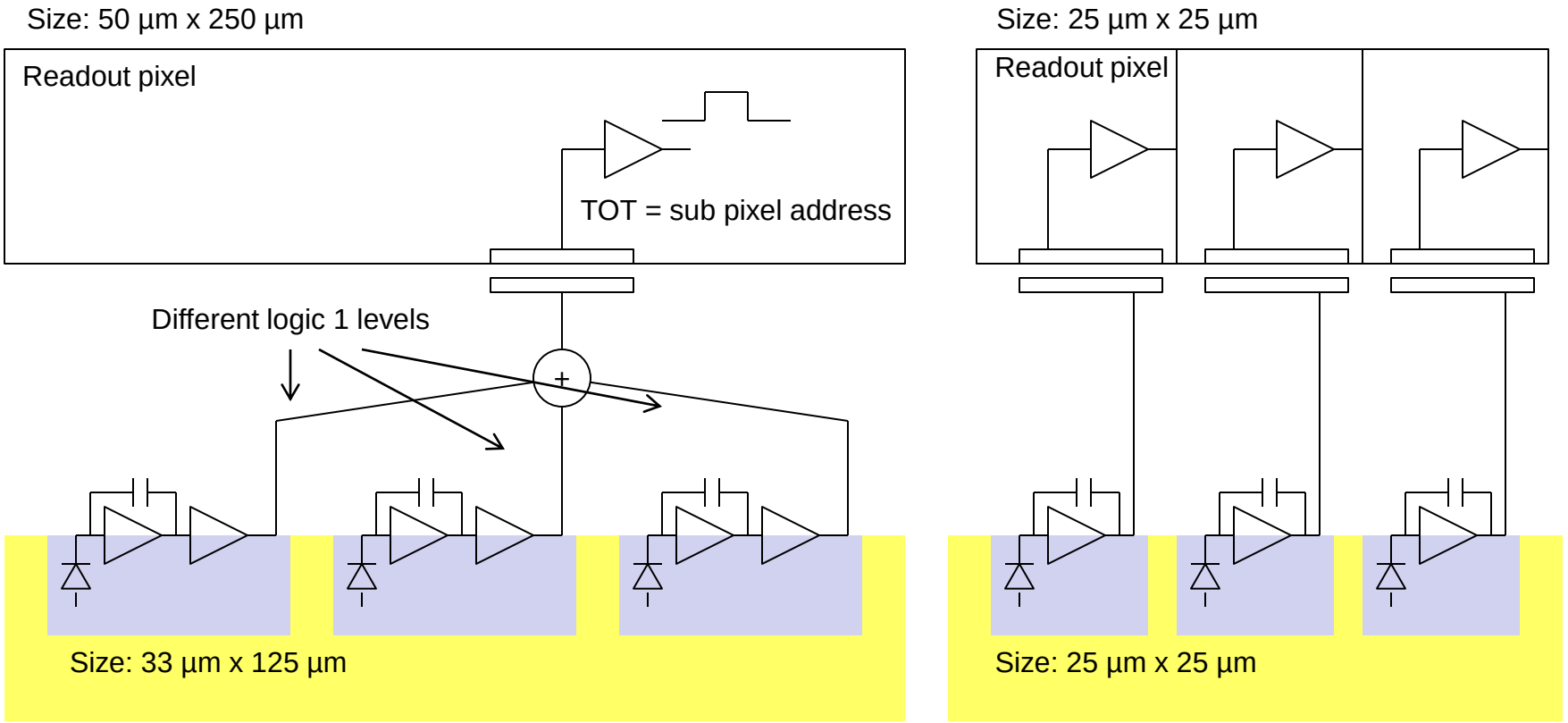
- We investigate two detector structures:
- A) Hybrid detector with a “smart” HVCMOS sensor and the capacitive signal transmission to the readout ASIC (capacitively coupled pixel sensor - CCPD)
- B) Monolithic pixel detector with digital signal processing on the chip periphery





HVCMOS detector types

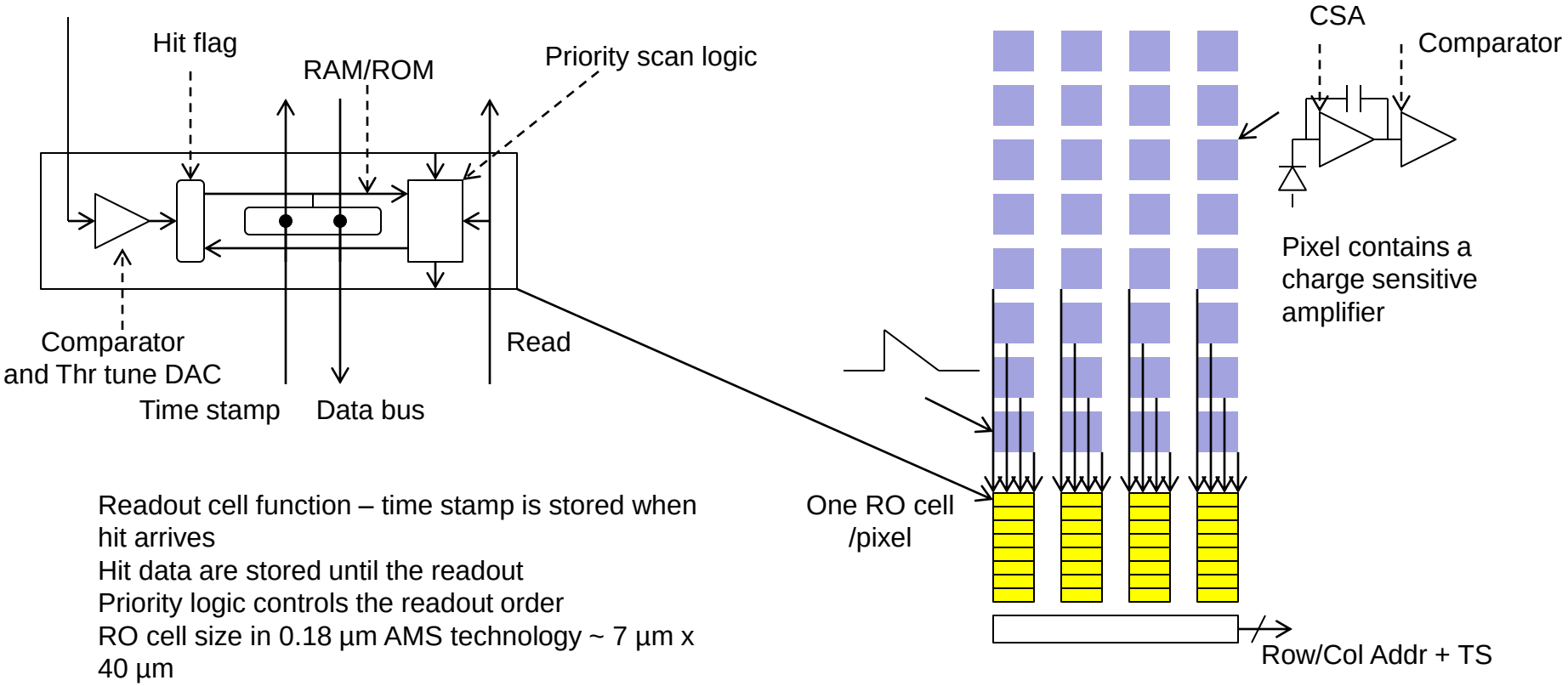
- CCPD
- ATLAS-pixel “style”: the digital outputs of three pixels are multiplexed to one pixel readout cell
- HVCMOS pixel contains an amplifier and a comparator
- CLIC “style”: every HVCMOS pixel has its own readout cell
- HVCMOS pixel contains only an amplifier



Monolithic HVCMOS pixel sensor for Mu3e experiment

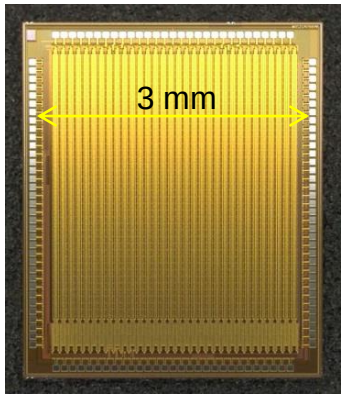
Monolithic HVCMOS pixel sensor for Mu3e experiment

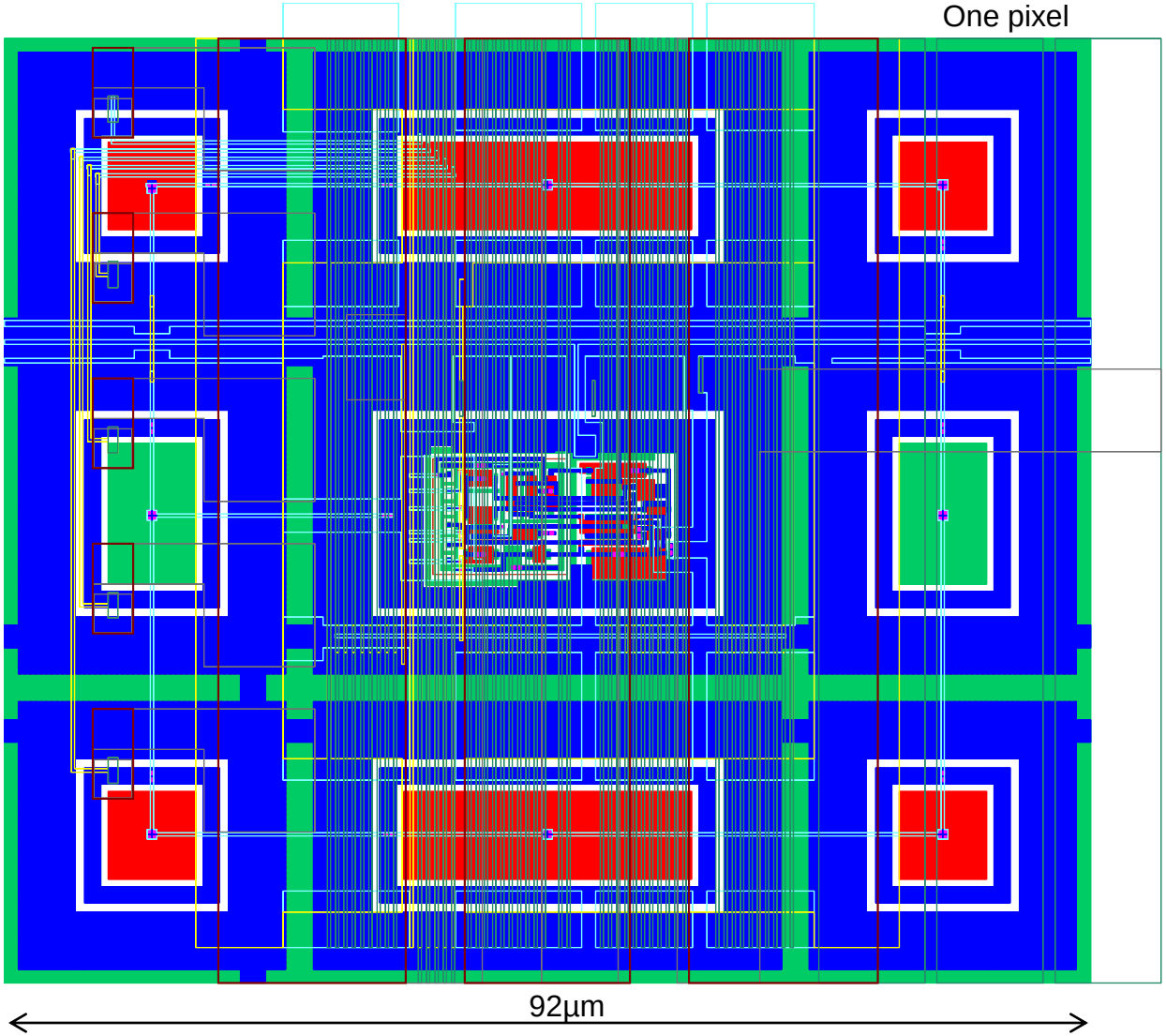
Concept: Every pixel has its own readout cell, placed on the chip periphery

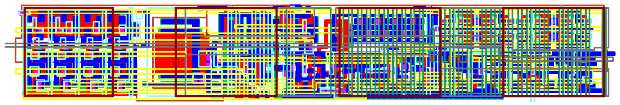


Readout cell function – time stamp is stored when hit arrives
Hit data are stored until the readout
Priority logic controls the readout order
RO cell size in 0.18 µm AMS technology ~ 7 µm x 40 µm
(with comparator and threshold-tune DAC)

Monolithic HVCMOS pixel sensor for Mu3e experiment

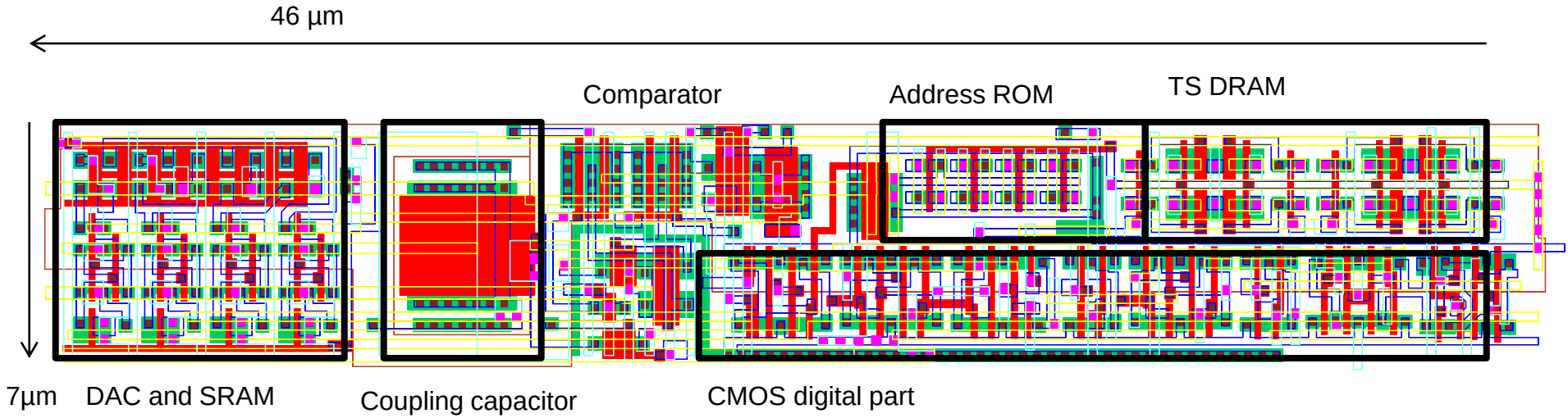






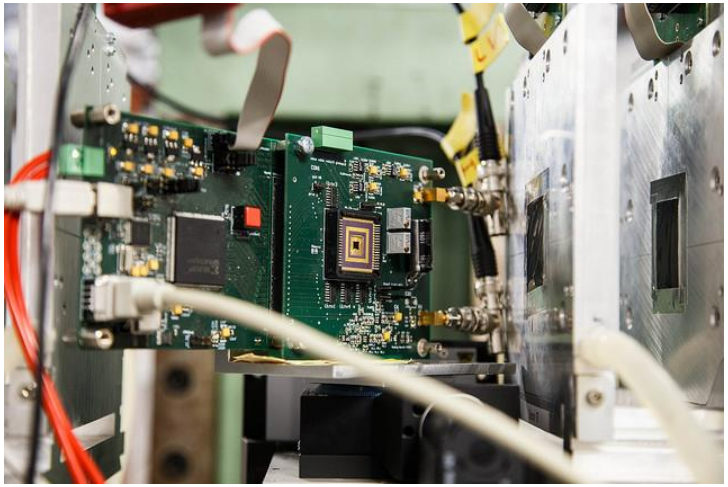
Readout cell

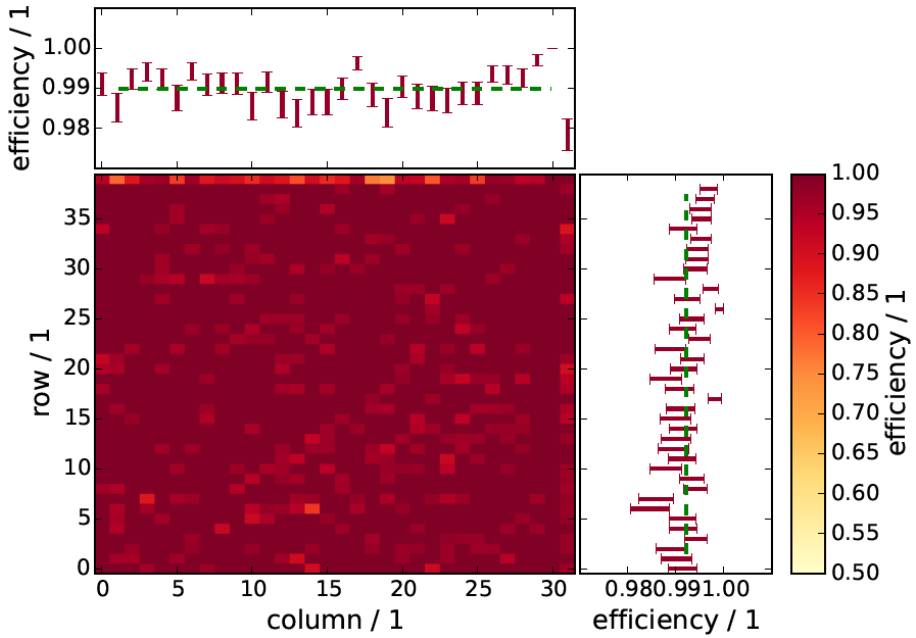
MuPixel (readout-cell)

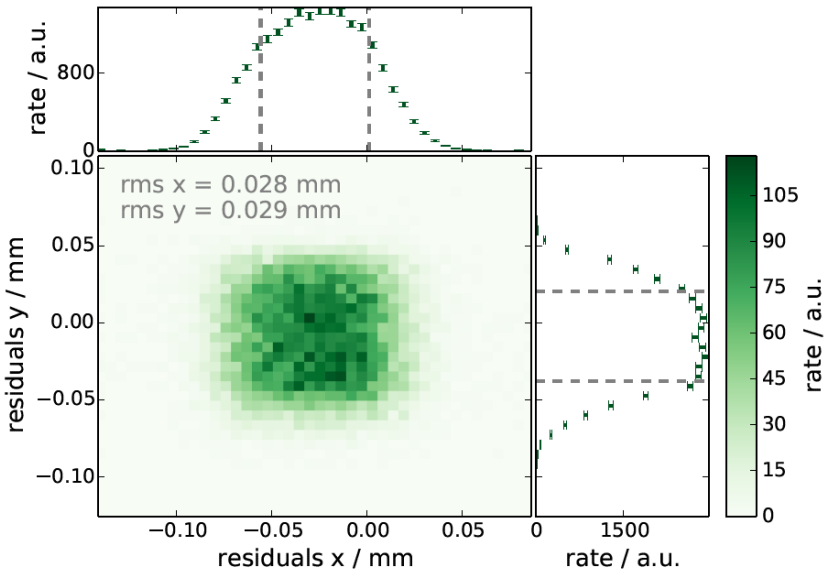


MuPixel test beam

- Test-beam measurement February 2014 DESY
- Performed by our colleagues from Institute for Physics in Heidelberg
- Result analysis: Moritz Kiehn, Niklaus Berger, et al.







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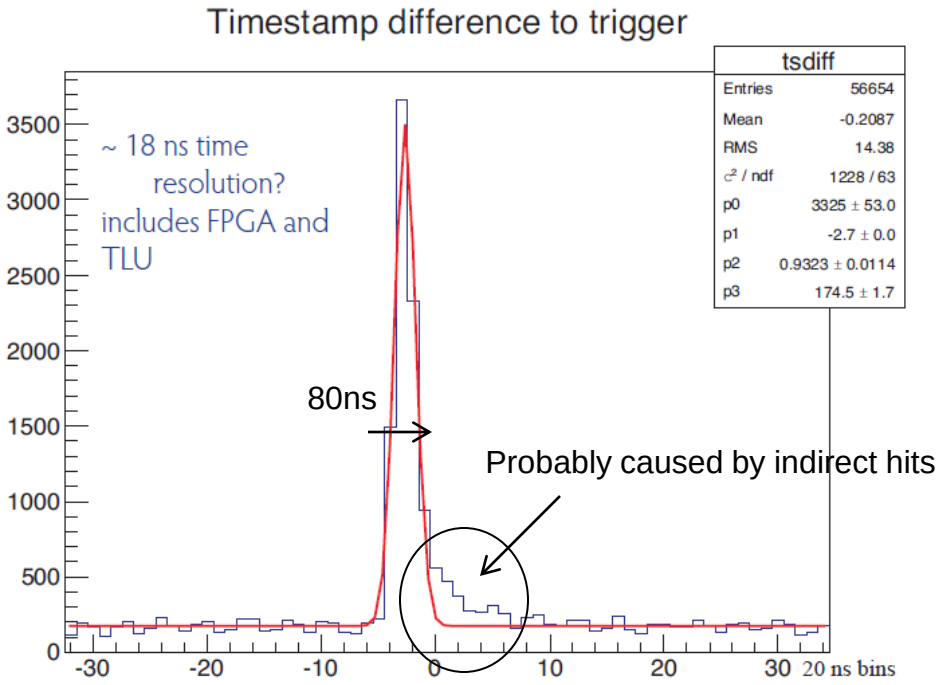
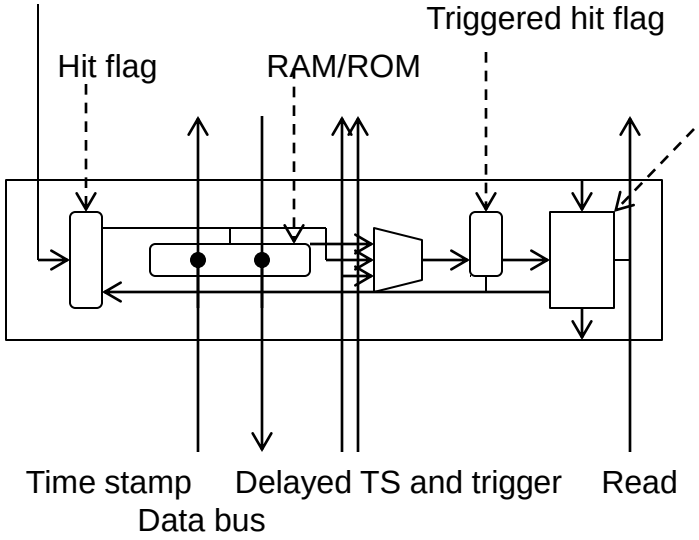
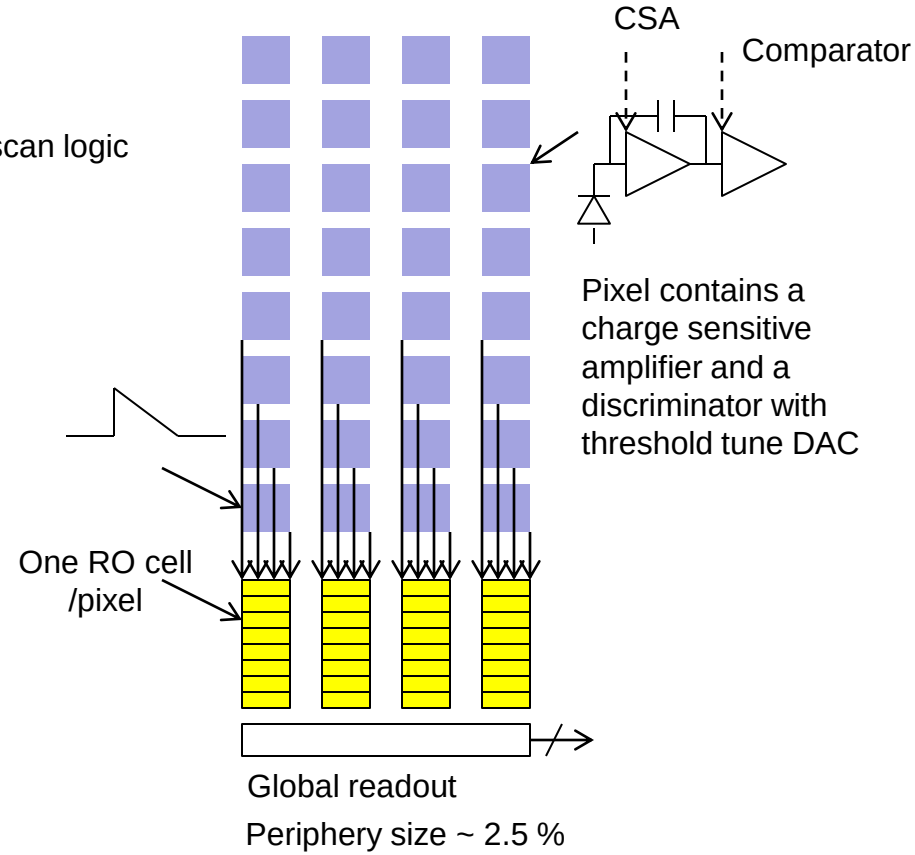


Periphery area estimation for triggered readout

Concept: Every pixel has its own readout cell, placed on the chip periphery



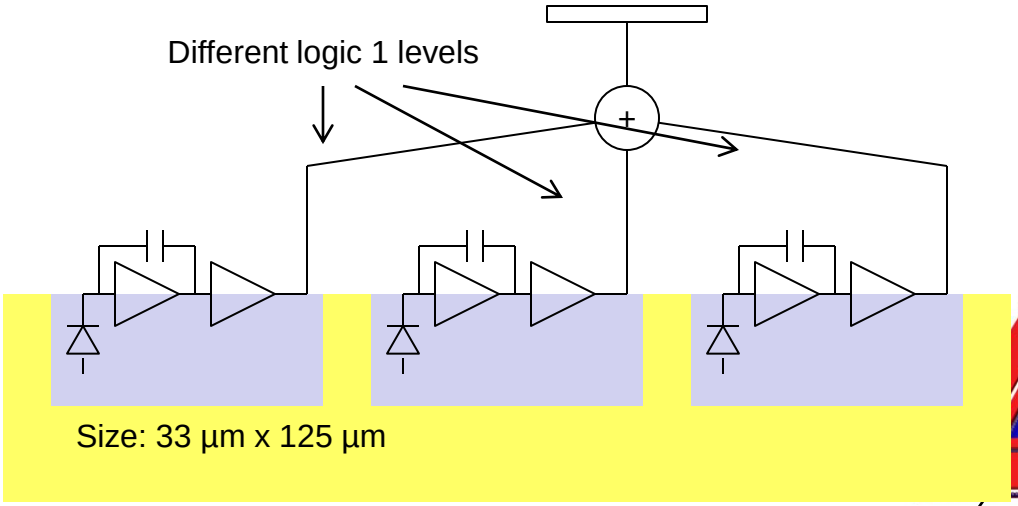


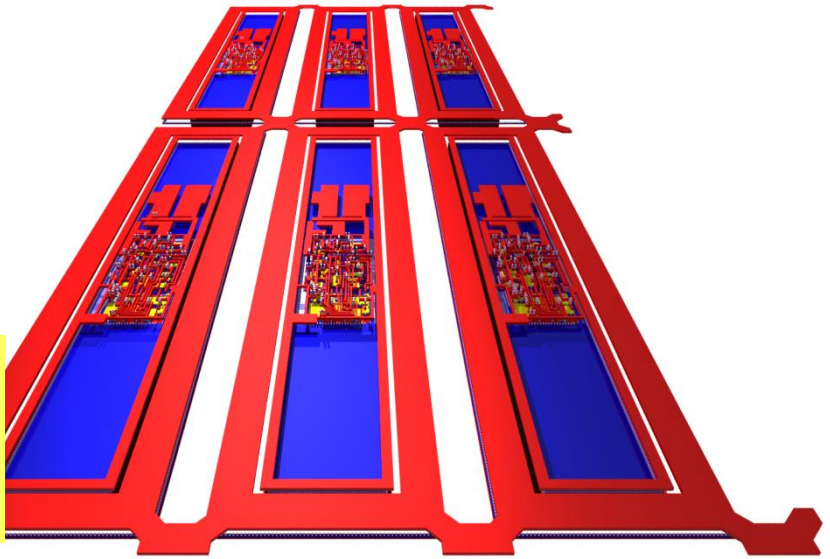
Readout cell function – time stamp is stored when hit arrives
The stored time stamp is compared with the current time stamp
If trigger arrives with the correct latency, the triggered hit flag is set
Priority logic controls the readout order
Estimated cell size in 0.18 µm AMS technology without comparator ~ 7 µm x 50 µm
Example: Pixel size 50 µm x 250 µm
Chip size: ~ 2 cm x 2 cm
Number of pixels: 400 x 80
Size of periphery without comparator:
2 cm x 560 µm (~ 2.5%)

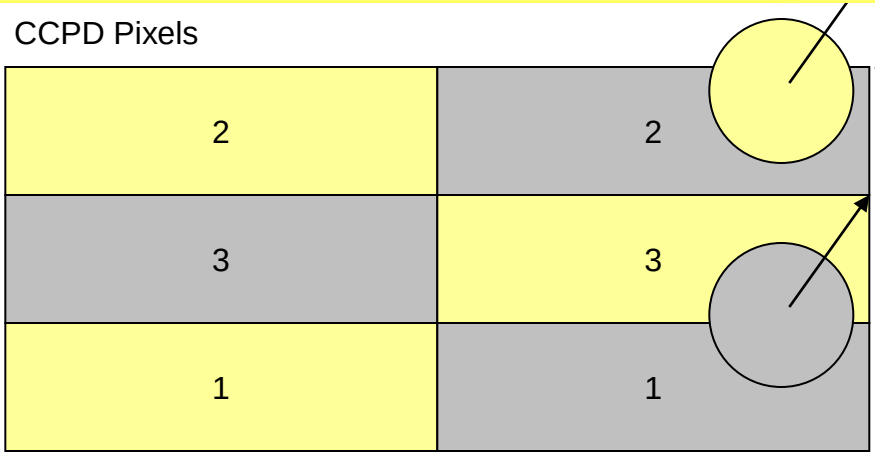
HVCMOS pixel sensor for ATLAS

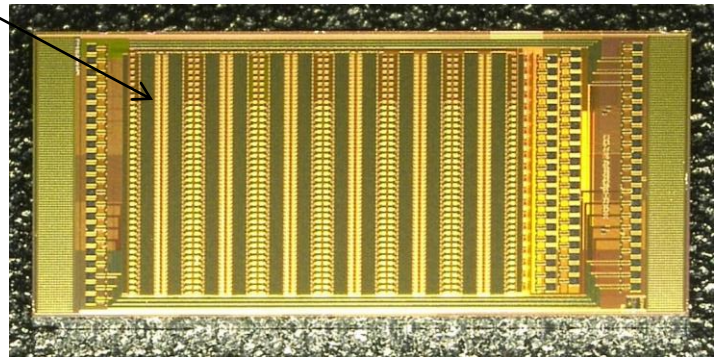
CCPD detector (HV2FEI4)

- The digital outputs of three pixels are multiplexed to one pixel readout cell

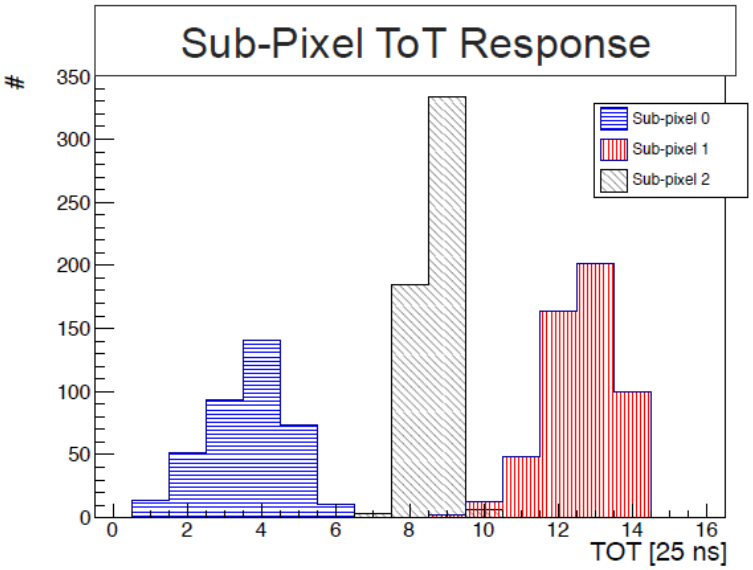


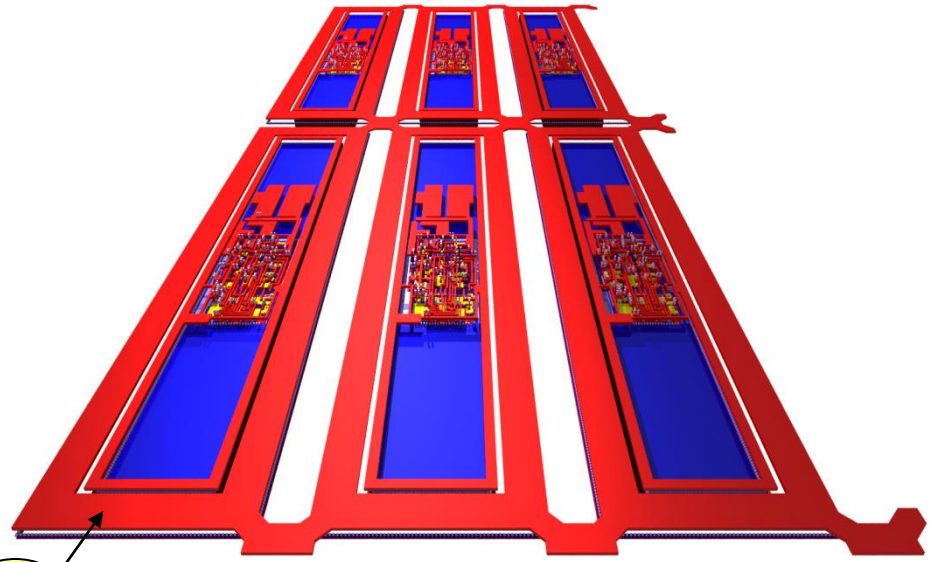




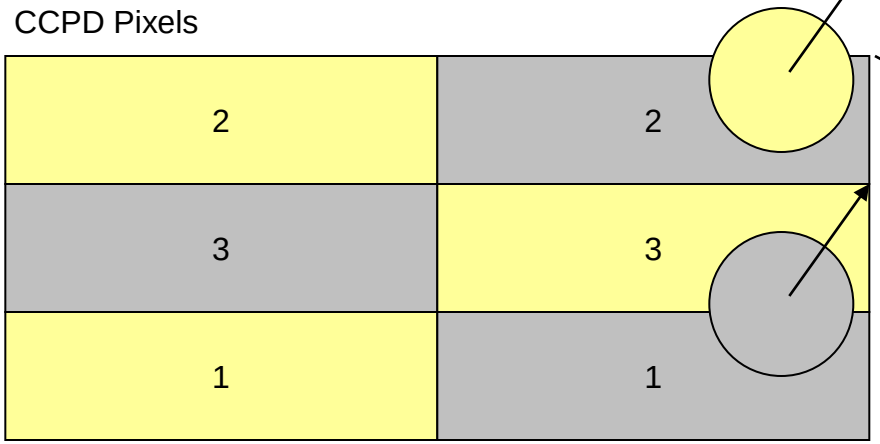


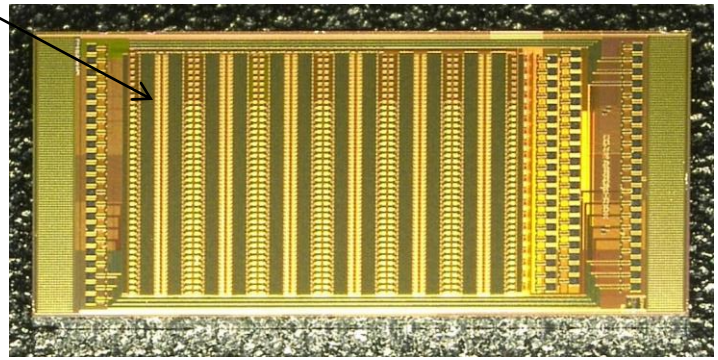
- “Sub-pixel resolution” by measuring of time over threshold (measurement: Malte Backhaus)





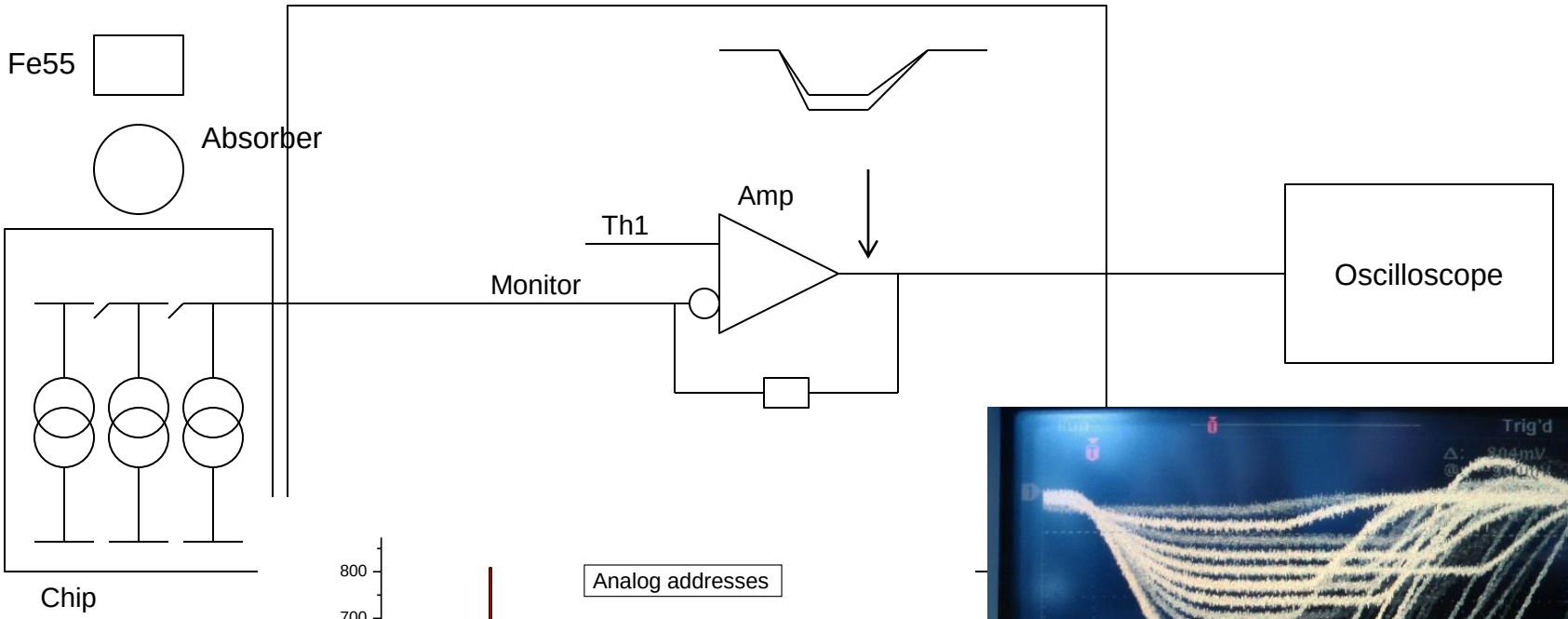
CCPD Pixels

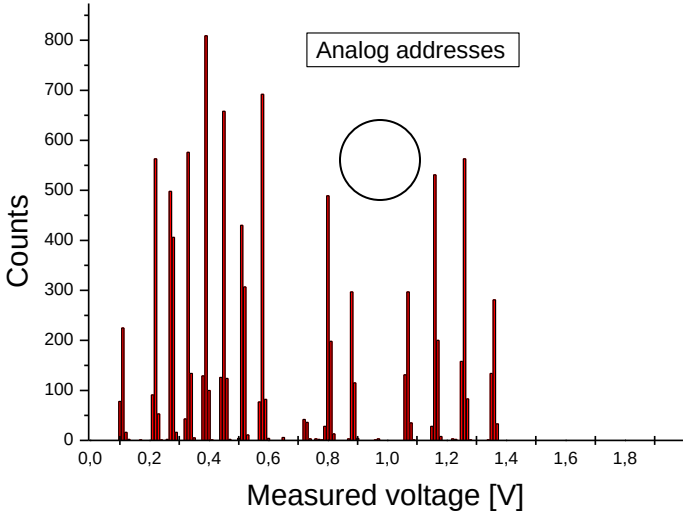


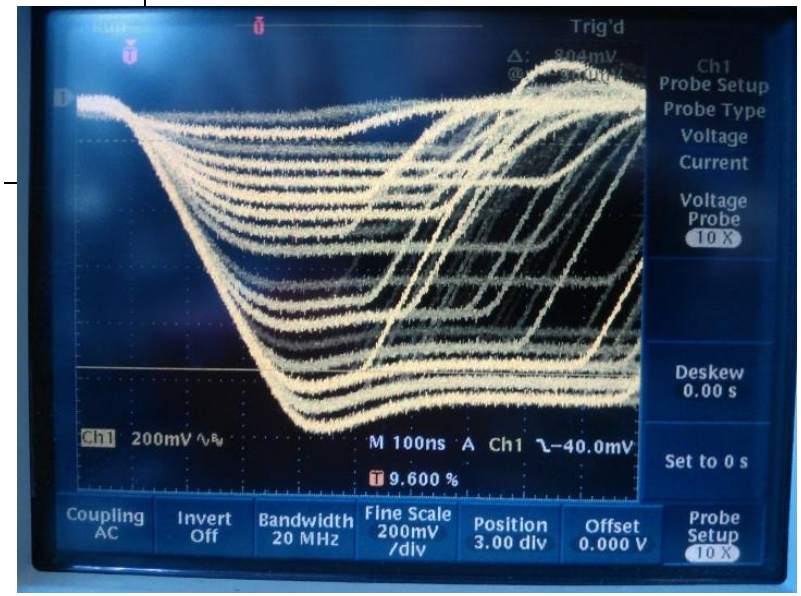


HV2FEI4: segmented strip measurements

- Analog encoding of pixels positions in the case of the segmented strip readout

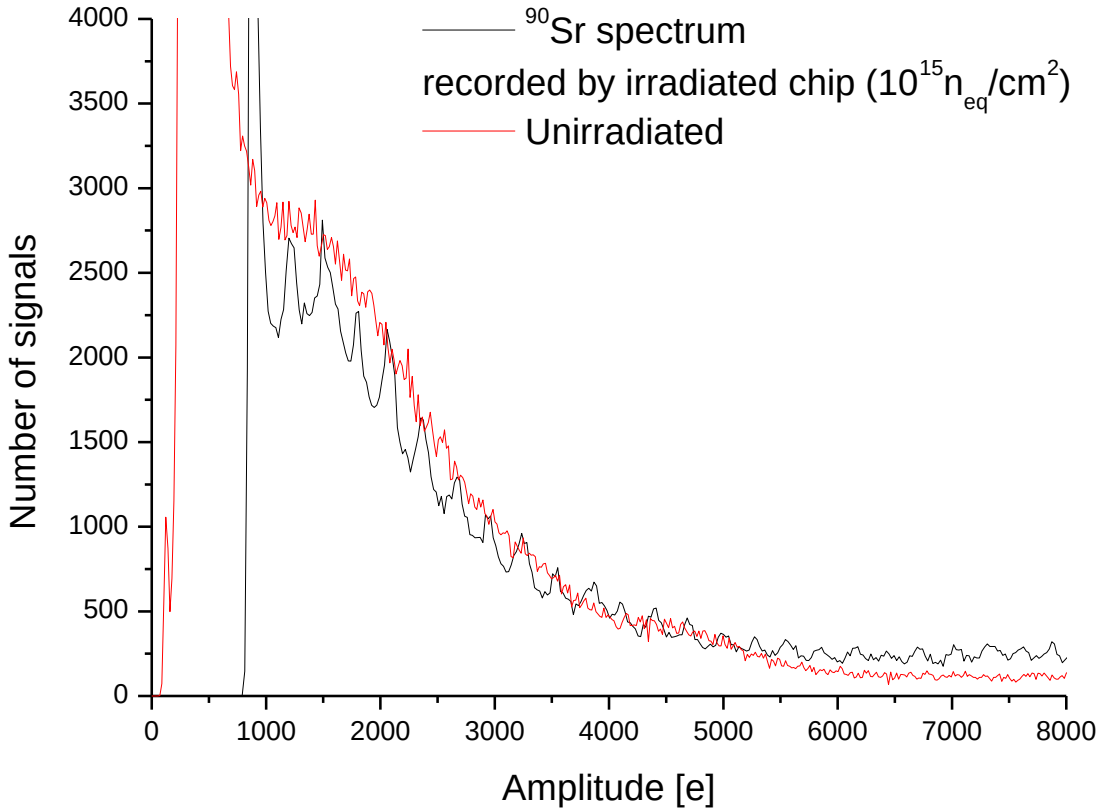






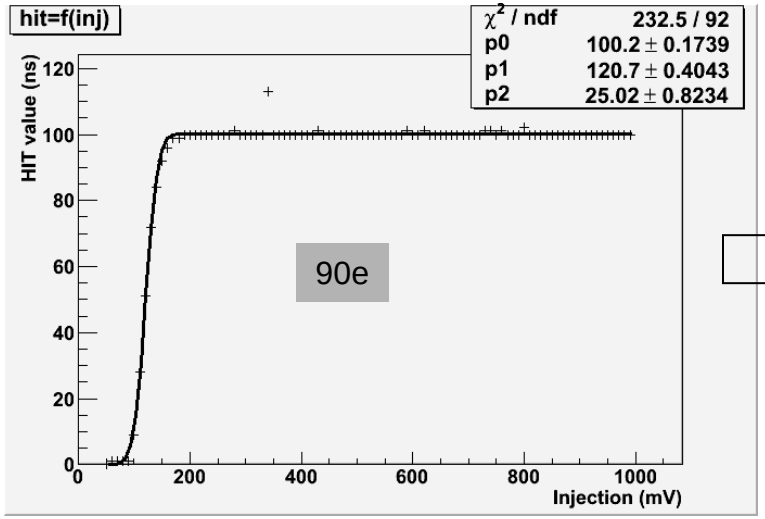
HV2FEI4: neutron irradiation 10^{15} n_{eq}/cm_2

- No evidence of signal decrease after 10^{15} n_{eq}/cm_2

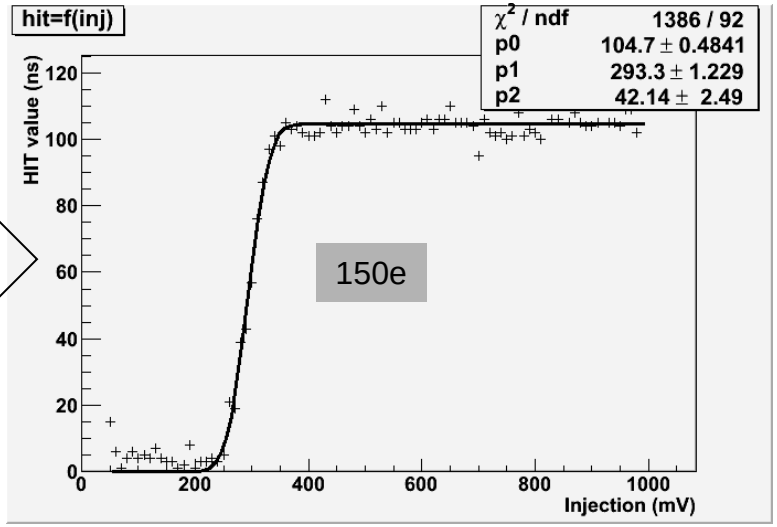


HV2FEI4: x-ray irradiation to 862 Mrad

- A detector has been irradiated to 862 Mrad with x-rays. (chips on during the irradiation, 2 hours of annealing at 70C after each 100Mrad)

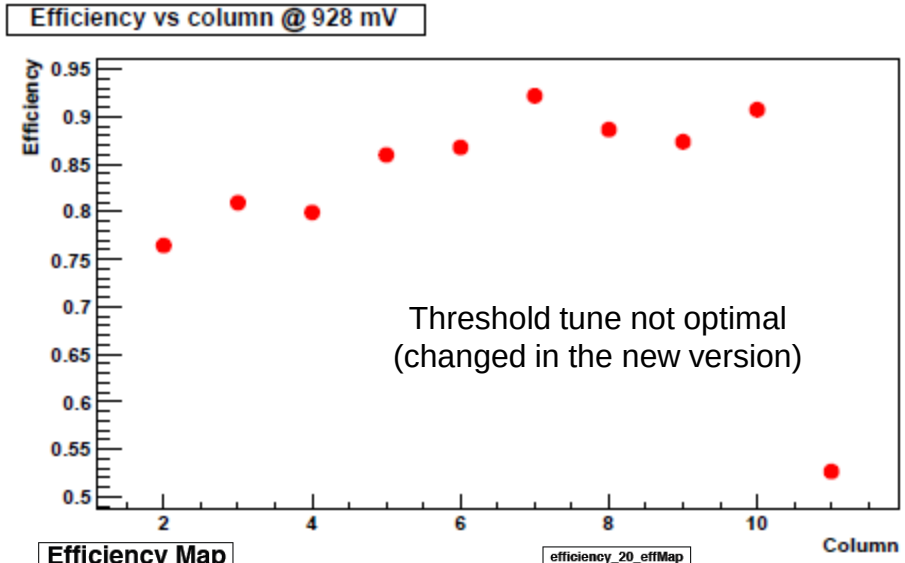


862 Mrad

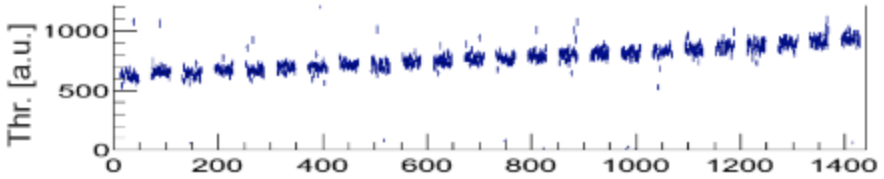


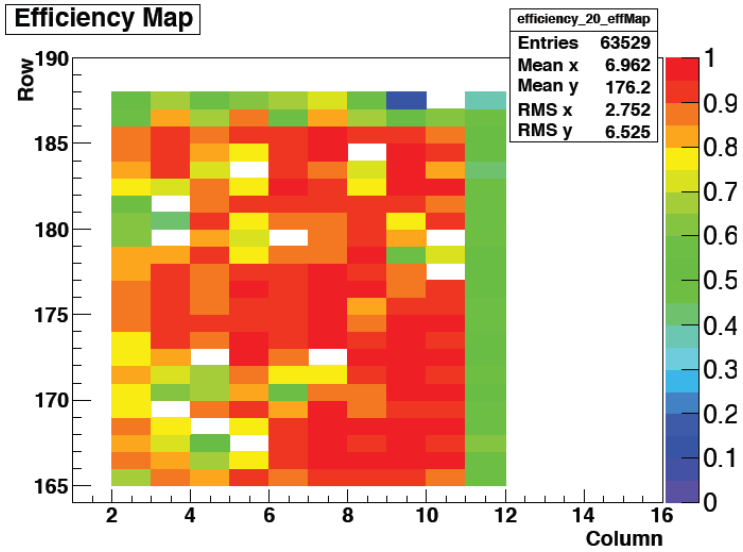
HV2FEI4: test beam

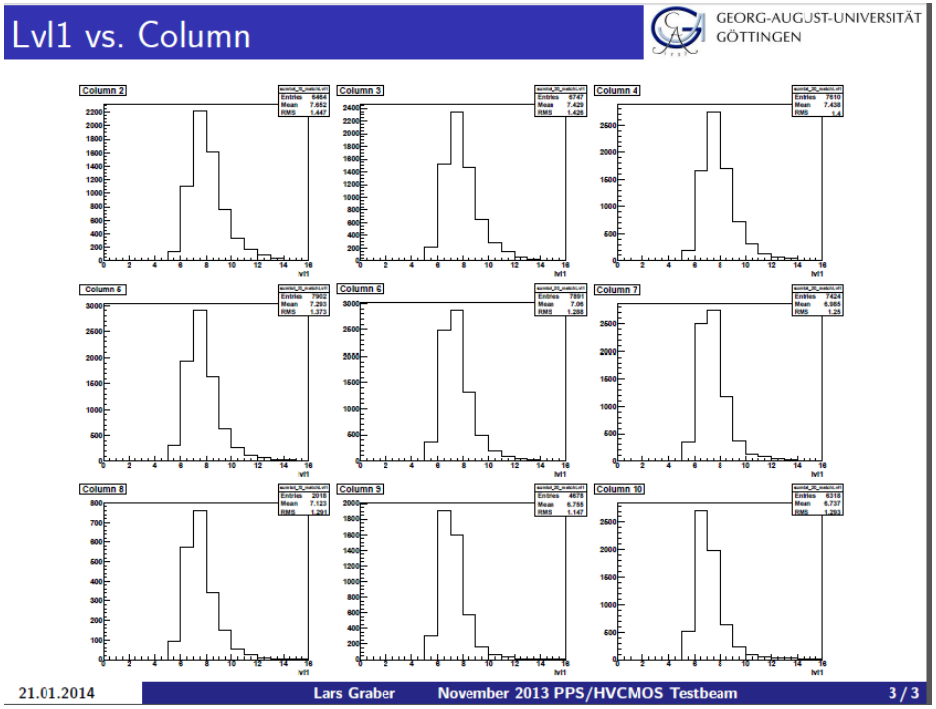
- Test beam DESY, analysis: Lars Graber, et al.



Threshold tune not optimal
(changed in the new version)







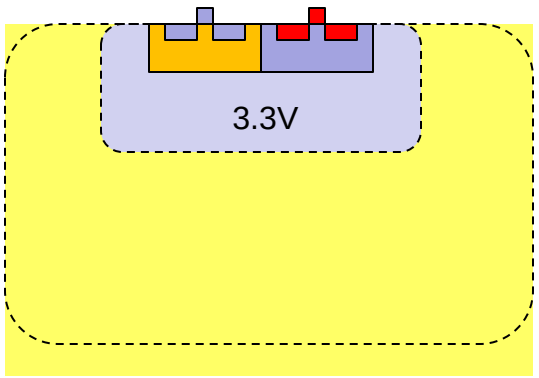
Further steps

- We need to improve time walk
- We need to improve SNR of CCPDs for ATLAS, especially after irradiation
- Three strategies:
- 1) optimize present design
- 2) invent more clever electronics
- 3) improve the detector structure and technology

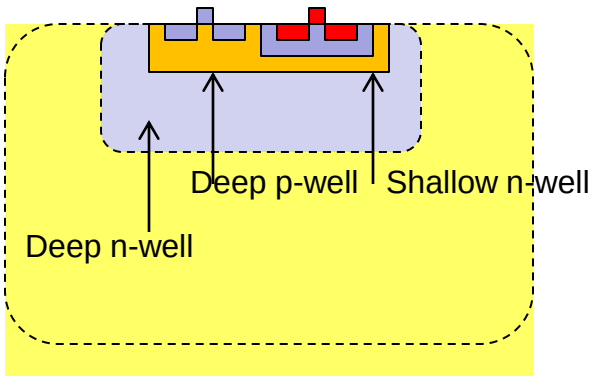
Detector structure improvements

Isolated PMOS

- Detector structure improvements:
- Isolated PMOS
- Eliminates PMOS to sensor crosstalk, allows more freedom when pixel electronics is designed



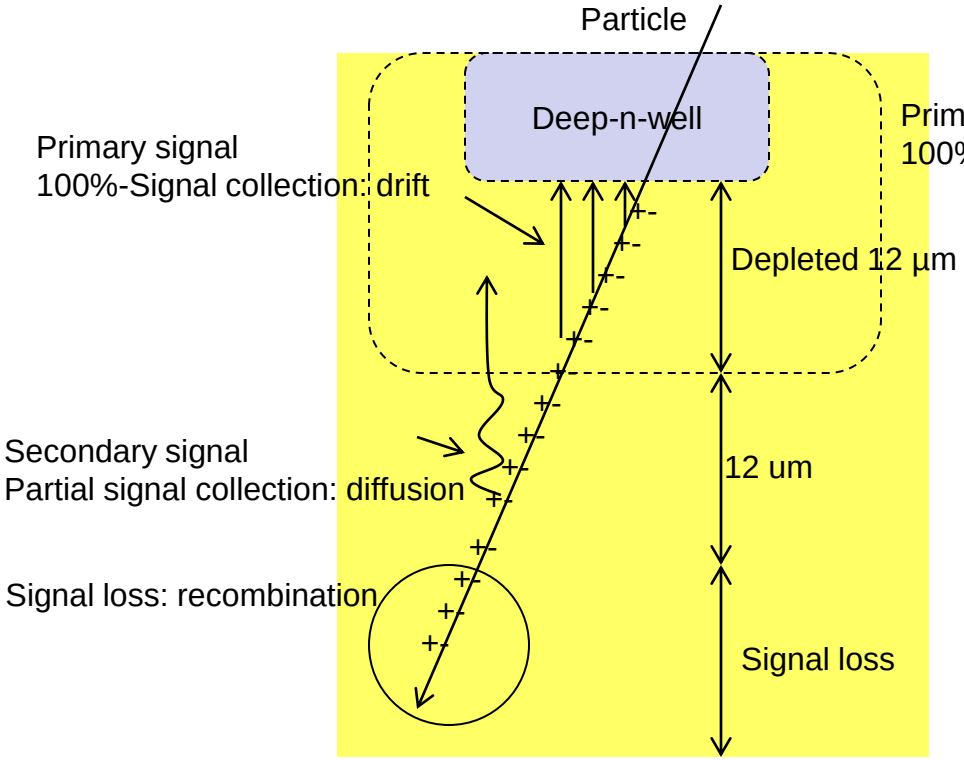
Improvement:



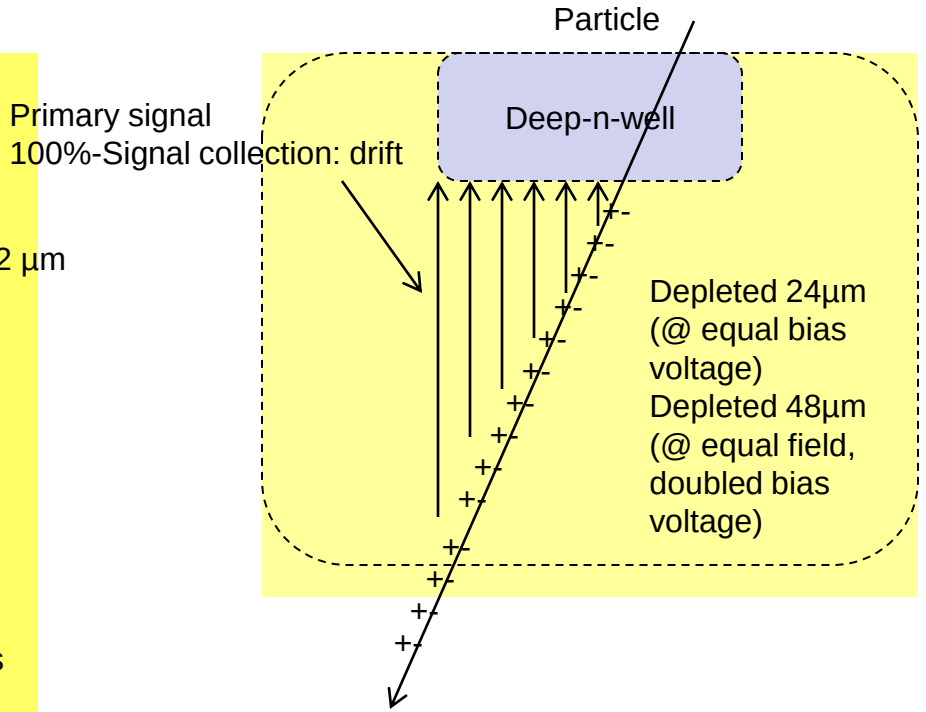
High resistive substrates

- Detector structure improvements:
- High resistive substrates

Uniformly doped substrate 20 Ω cm
Signal 1800e (50%-50% drift-diffusion)



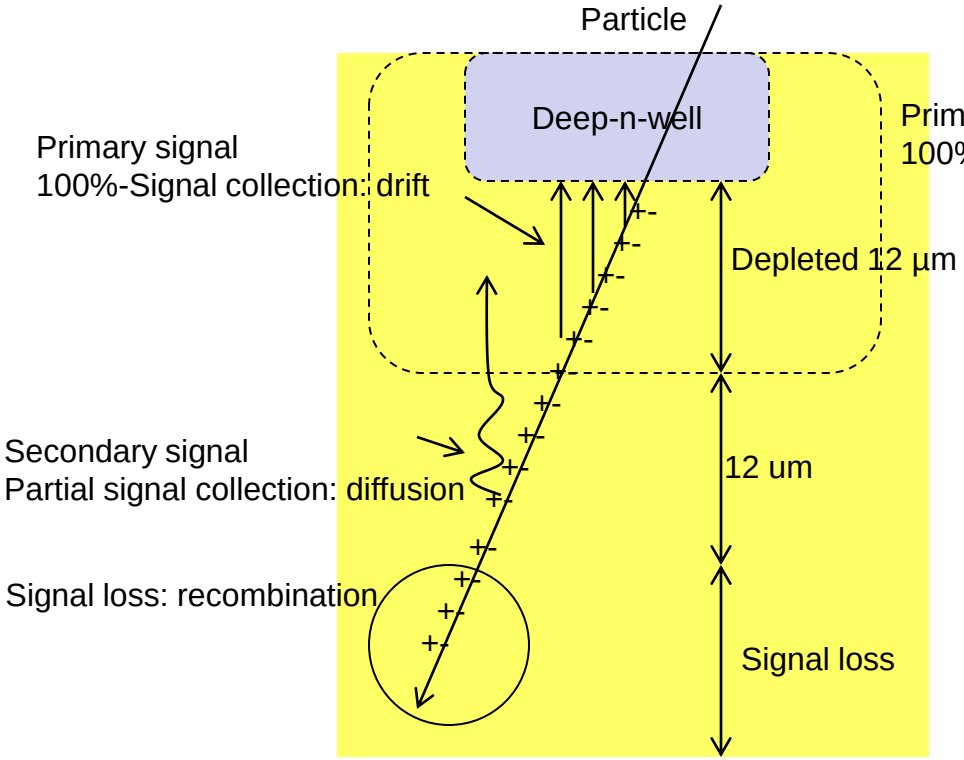
Uniformly doped substrate 80 Ω cm
Signal: ~ 2700e-4500e (estimation)



High resistive substrates

- Detector structure improvements:
- High resistive substrates
- **These improvements are possible within AMS- and LFoundry processes**

Uniformly doped substrate 20 Ω cm
Signal 1800e (50%-50% drift-diffusion)



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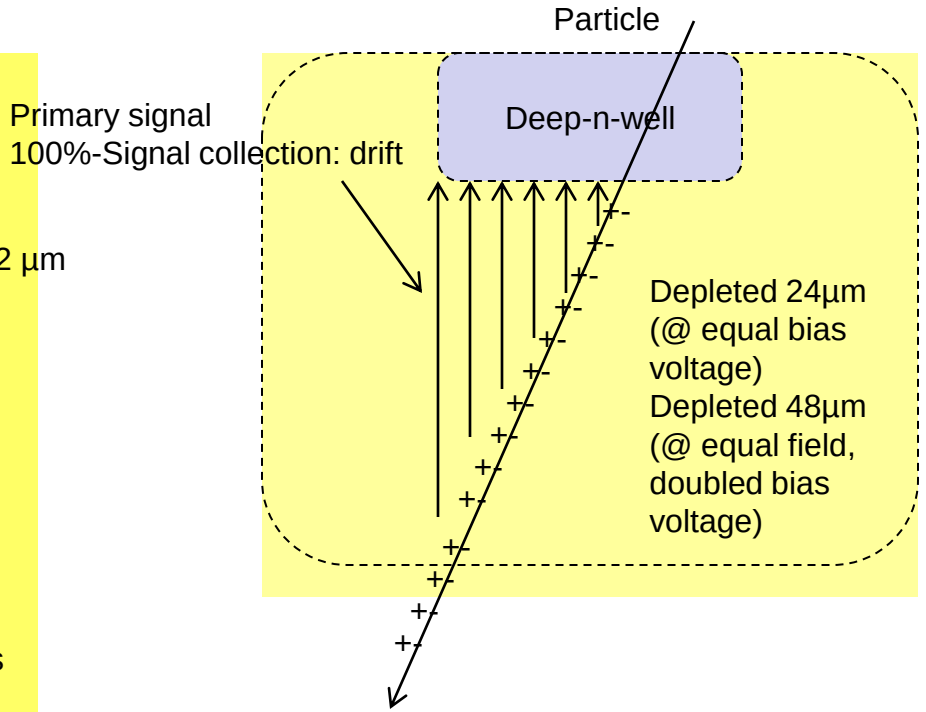
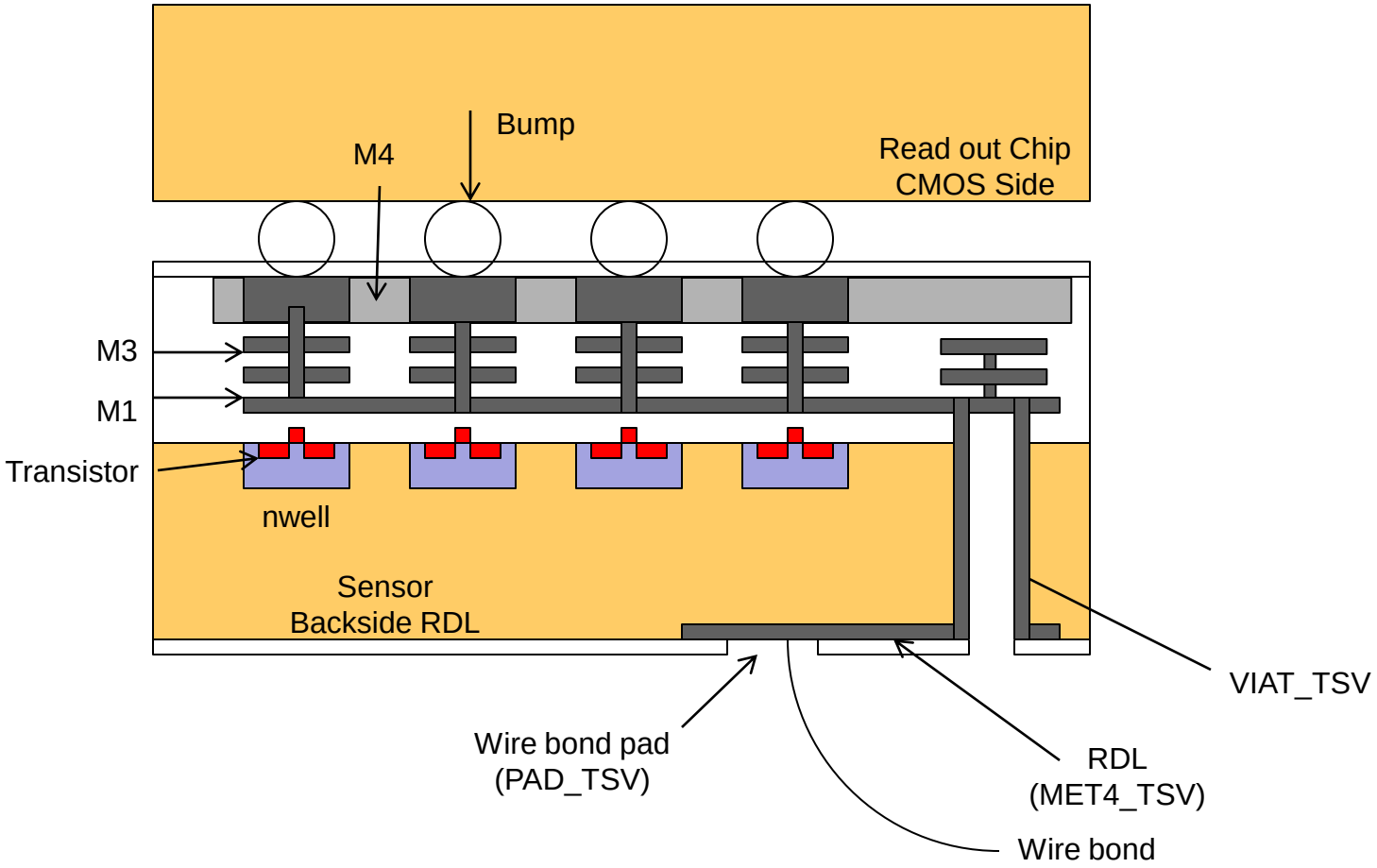


AMS TSV process

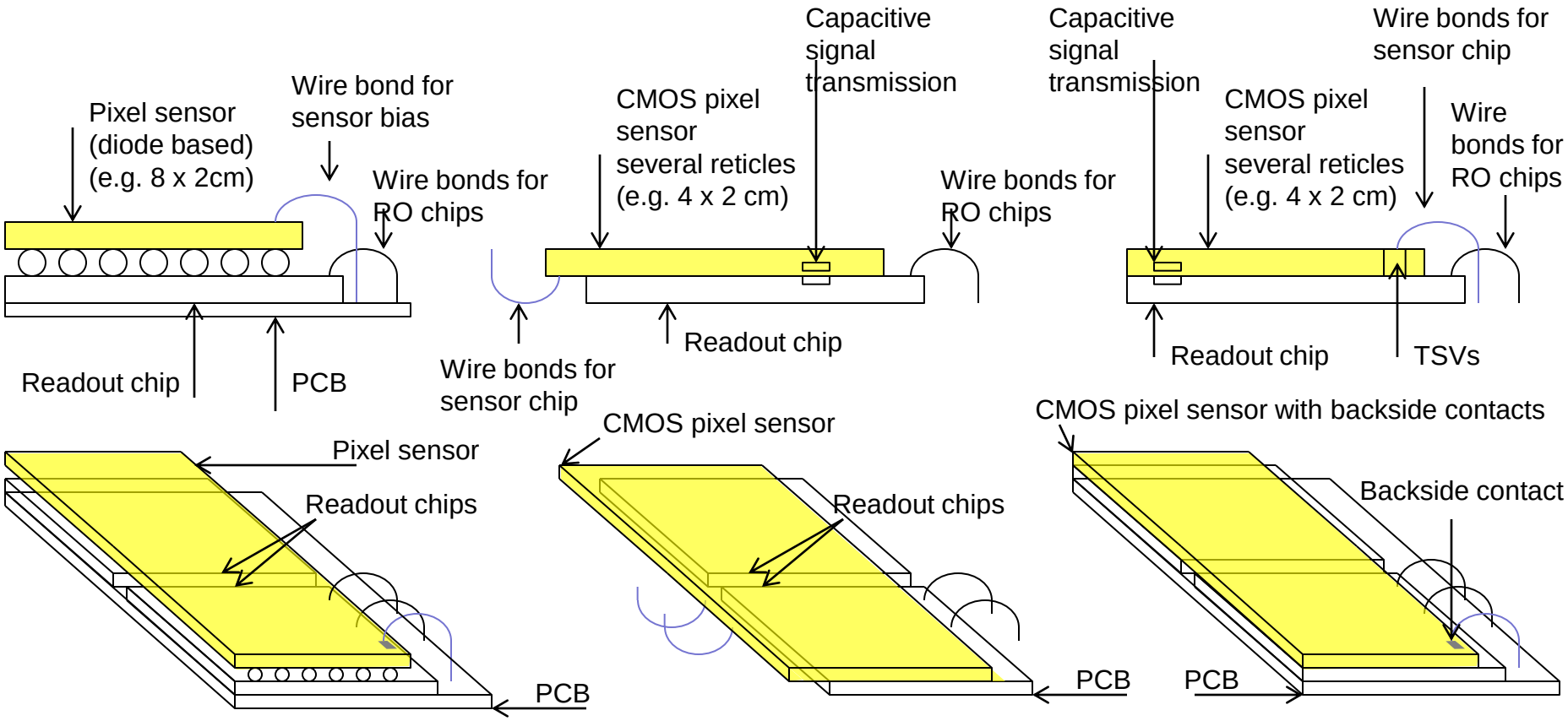
TSV – bask side RDL

- AMS offers through silicon vias and wafer bonding (so far only for H35, from end of 2015 for H18 as well)
- Backside redistribution layer and backside pads are possible
- TSV pitch 260 µm
- Very important for the module construction



Pixel detectors

…



Detector as it is done now:
Diode based pixel sensor bump-bonded to readout ASICs

Present development:
CMOS pixel sensor capacitively coupled to readout ASICs

With TSVs
CMOS pixel sensor with backside contacts capacitively coupled to readout ASICs

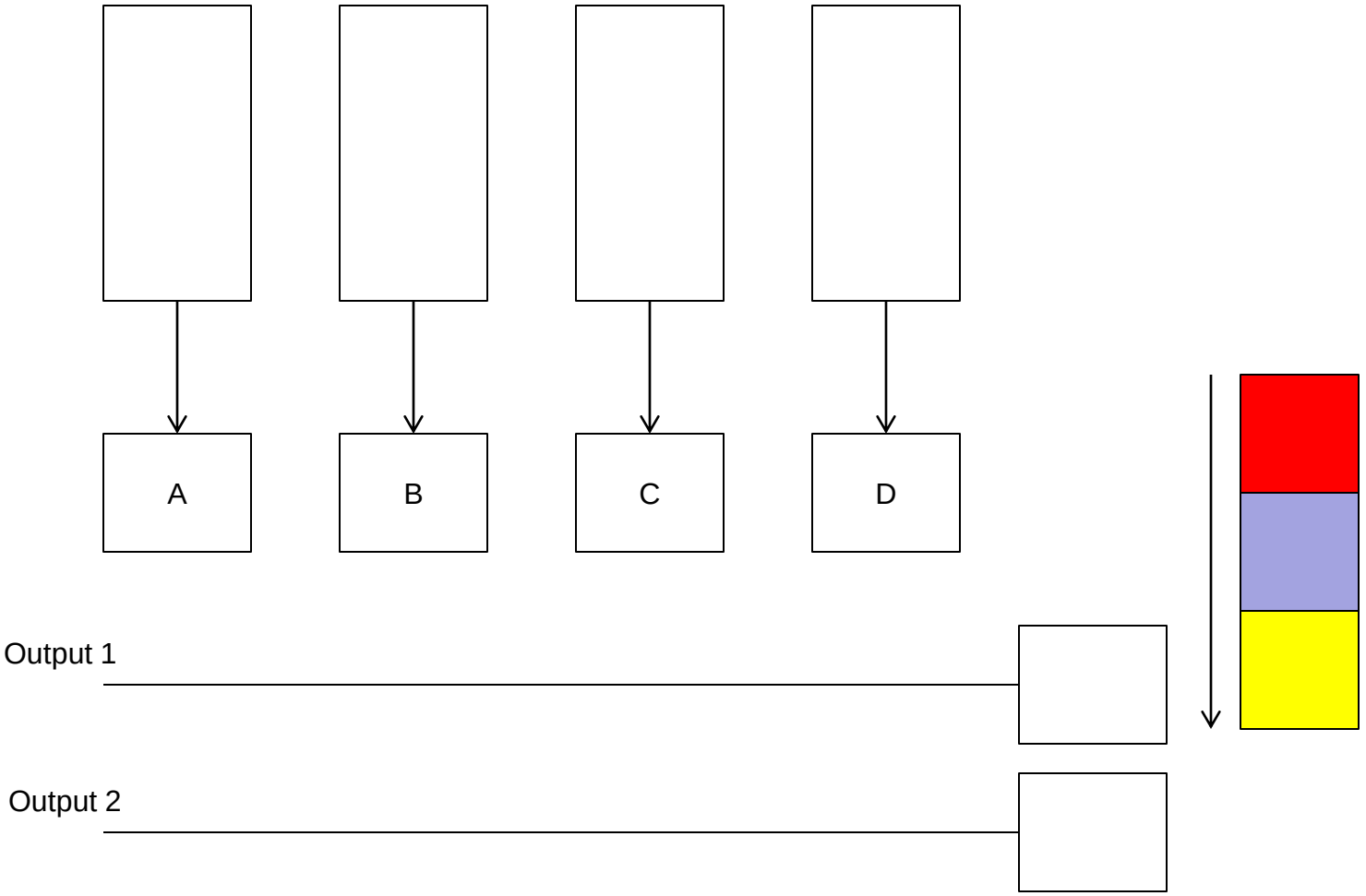
Summary

- Collaborations have been formed with the goals to develop HVCMOS sensors for ATLAS- and Mu3e experiments, as well for CLIC
- The Mu3e prototype detector (technology AMS 0.18 µm H18) (design Heidelberg) is a fully monolithic sensor with untriggered time-stamp based readout
- Detection efficiency of >99% has been measured in a beam test, time resolution (time walk) is ~ 70 ns.
- The ATLAS prototypes in AMS 0.18 µm (H18) (design HD) and GF 0.13 µm (design CPPM, HD) technologies are capacitively coupled smart sensors that can be readout using FE-I4 chip
- Irradiations and test beam measurements have been performed on the H18 chip
- The H18-chip is operational after 880 MRad and 10^{16} n_{eq}/cm^2
- A test beam measurement has been performed with the test-setups which are still not optimized and in development stage – the threshold uniformity was poor
- The uniradiated H18-detector had a detection efficiency of >90% in the regions with lower threshold

Summary

- We need to improve the time walk and the detection efficiency
- Three approaches:
- 1) Optimization of the present design
- 2) Use of low-pass filter and the time-walk compensation circuit
- 3) Detector structure improvements (isolated PMOS) and the use of substrates of higher resistivity
- Chip producers AMS and LFoundry allow such “extra features” within their processes
- AMS additionally offers through silicon vias and wafer bonding (so far only for H35, from end of 2015 also for H18 process)
- We are also investigating the use of HVCMOS sensors (segmented strips) for the ATLAS strip layers
- Constant delay lossy multiplexing can be used – every hit is transmitted to one of n outputs with a constant delay of ~60 ns.
- Hit loss occurs only if there are more than n simultaneous hits within one bunch crossing

Segmented strip detector with lossy constant-delay-multiplexing



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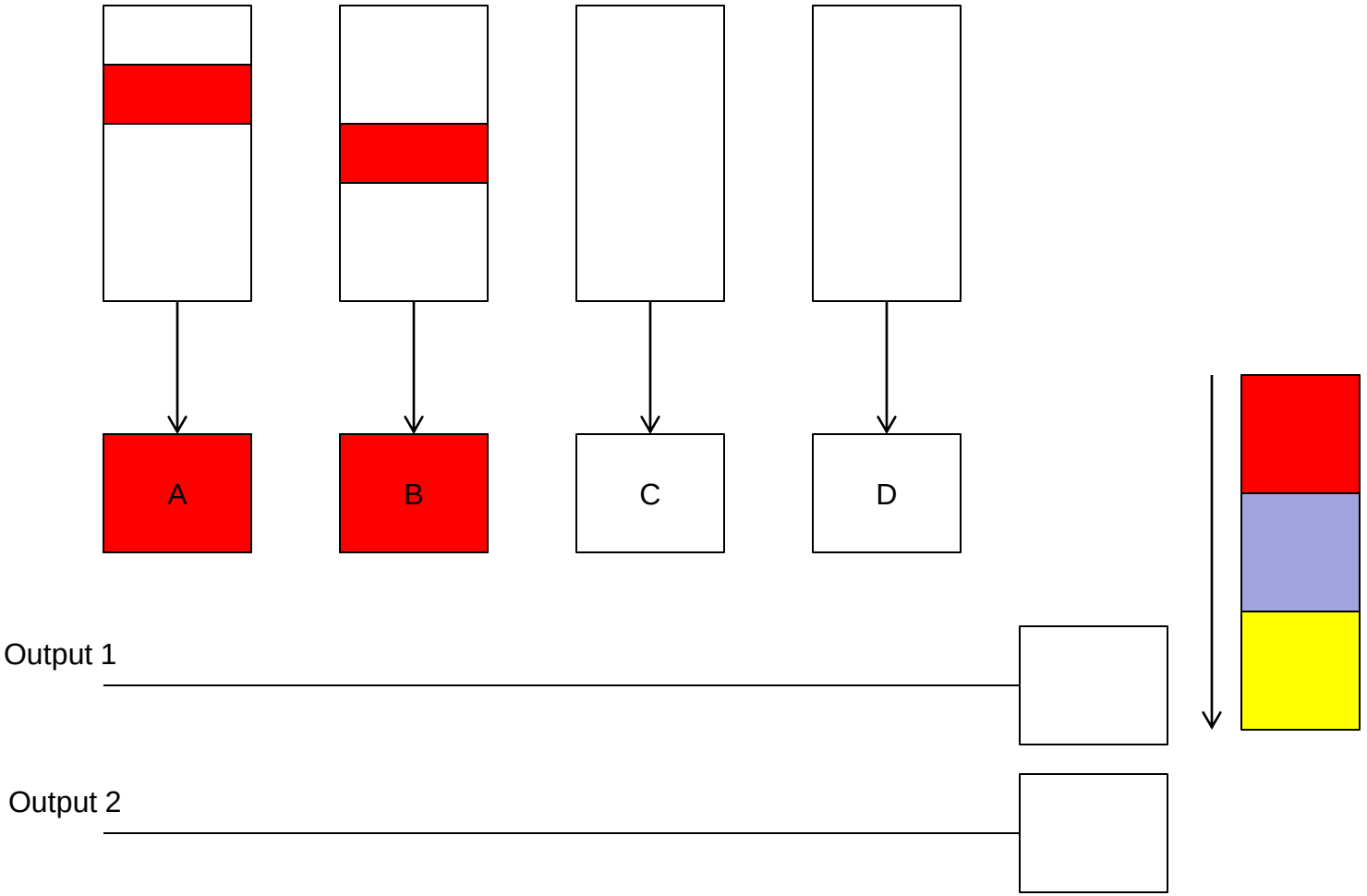
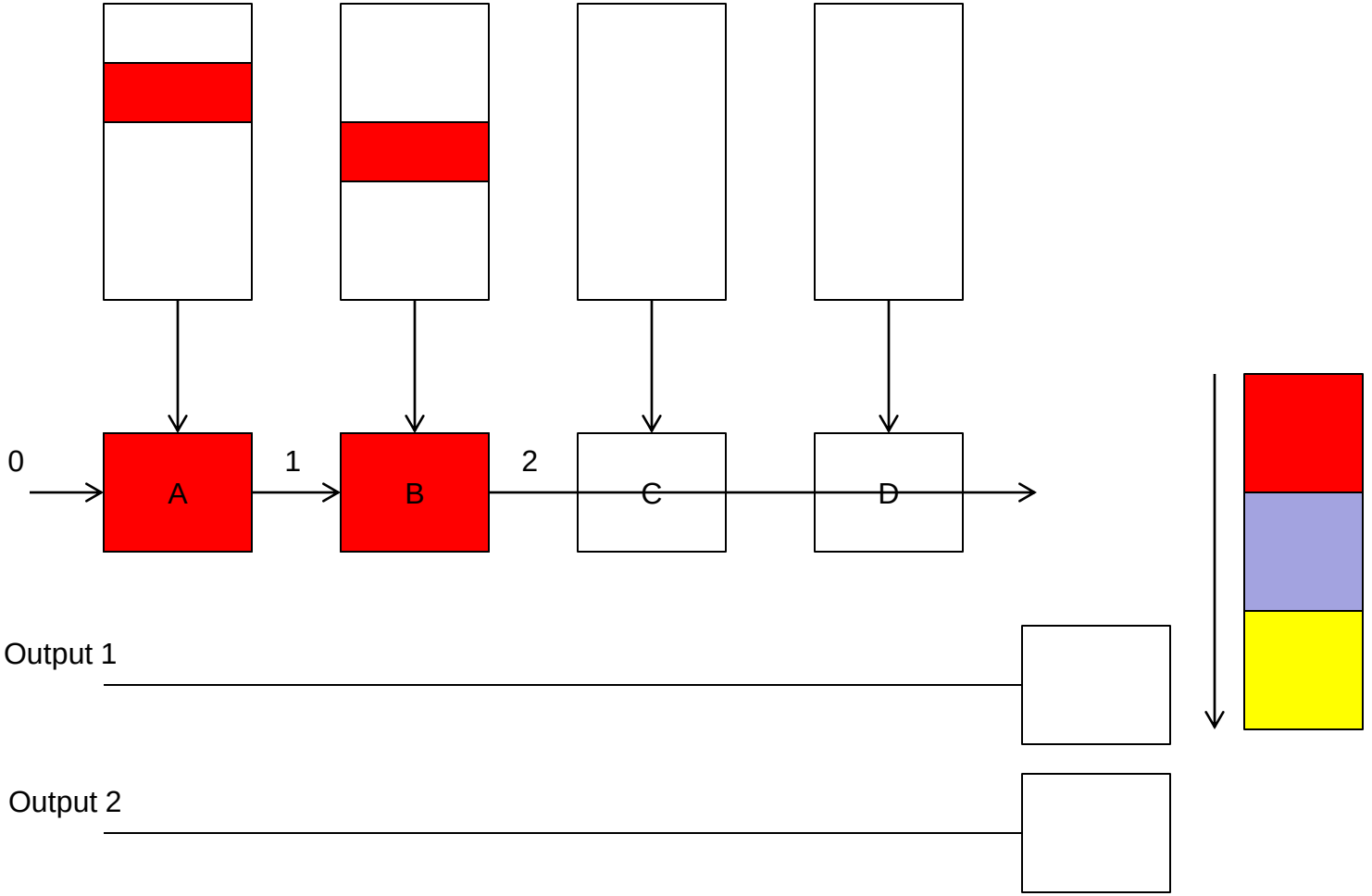
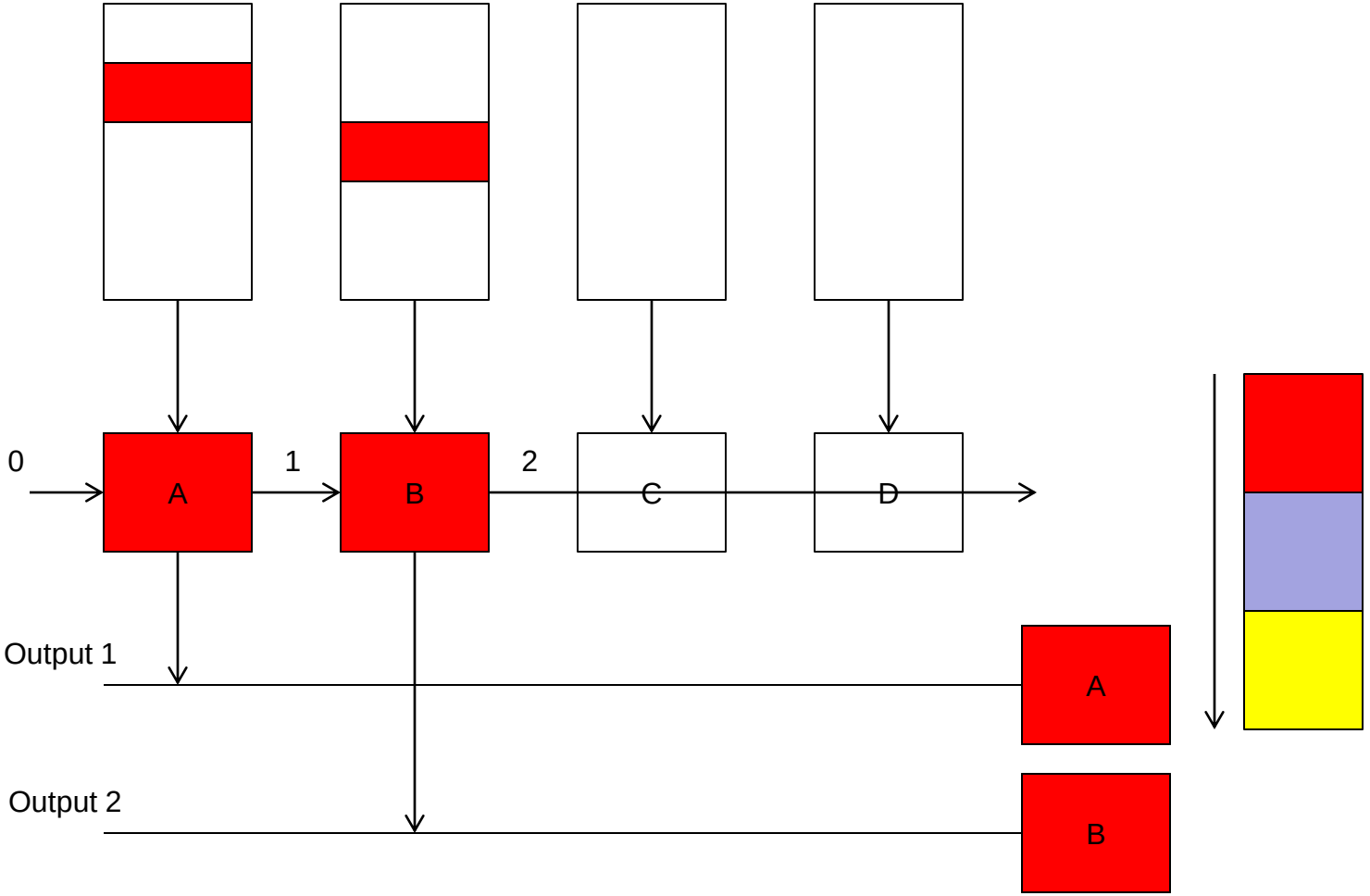


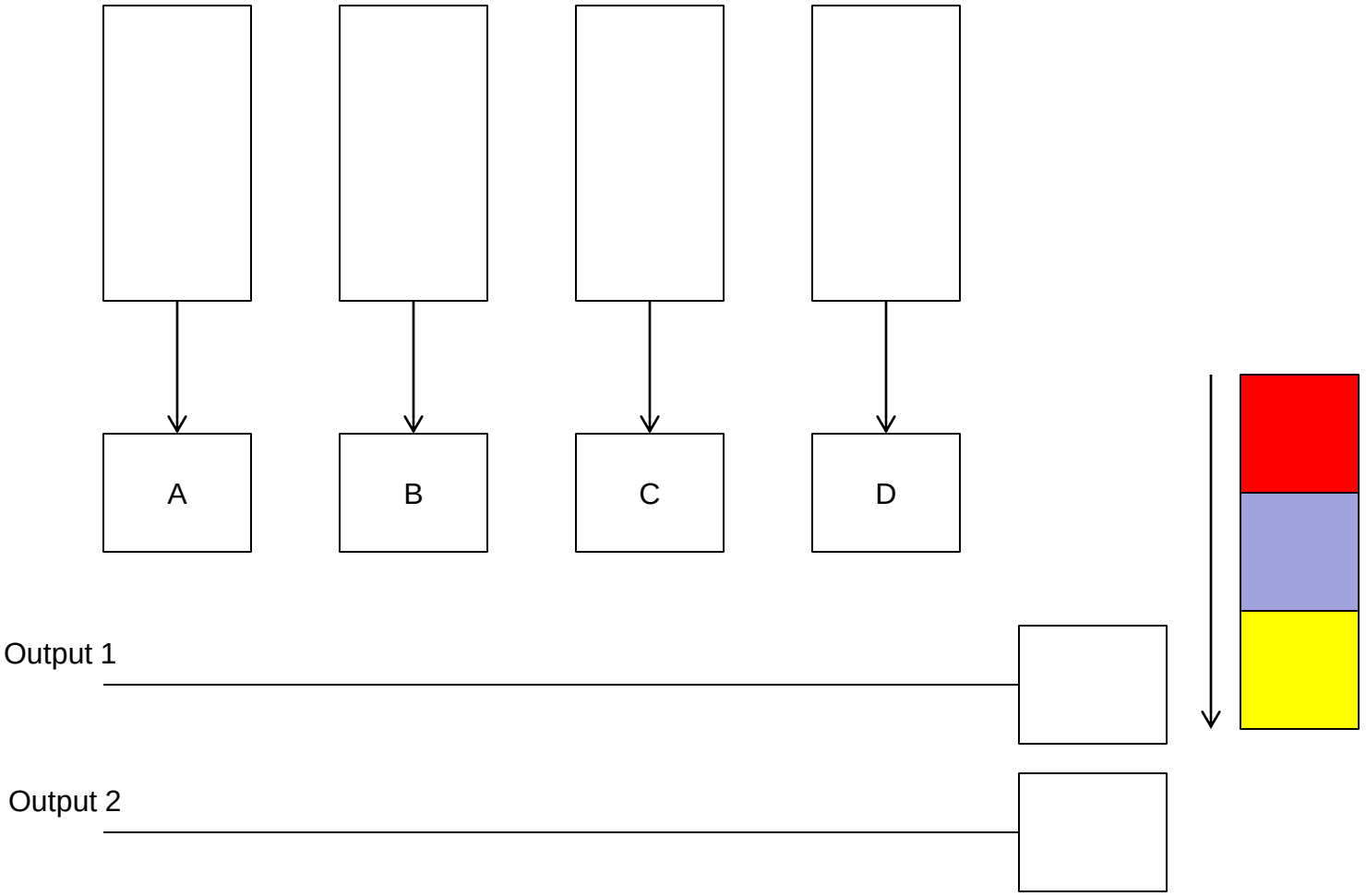
Segmented strip detector with lossy constant-delay-multiplexing



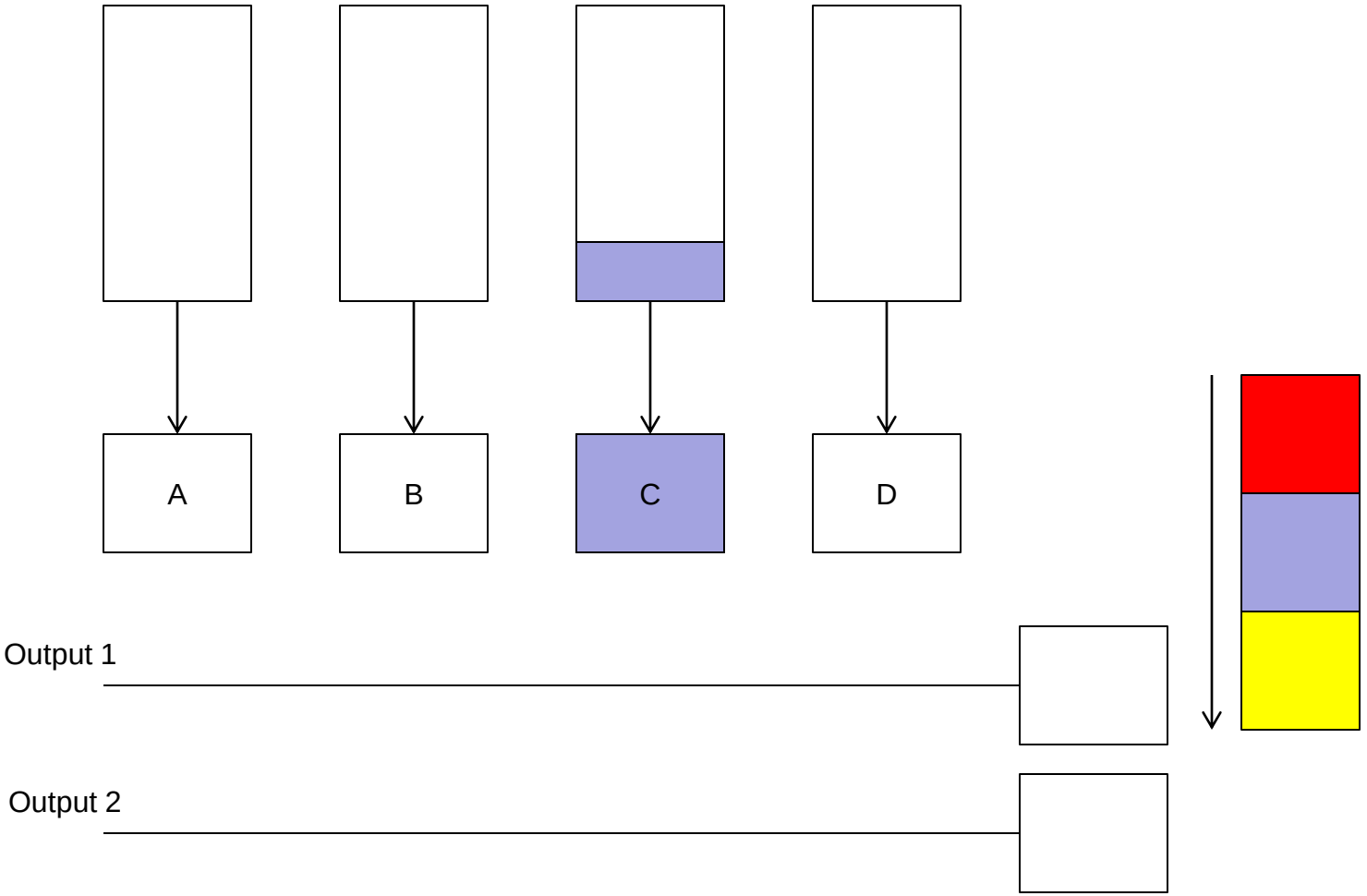
Segmented strip detector with lossy constant-delay-multiplexing



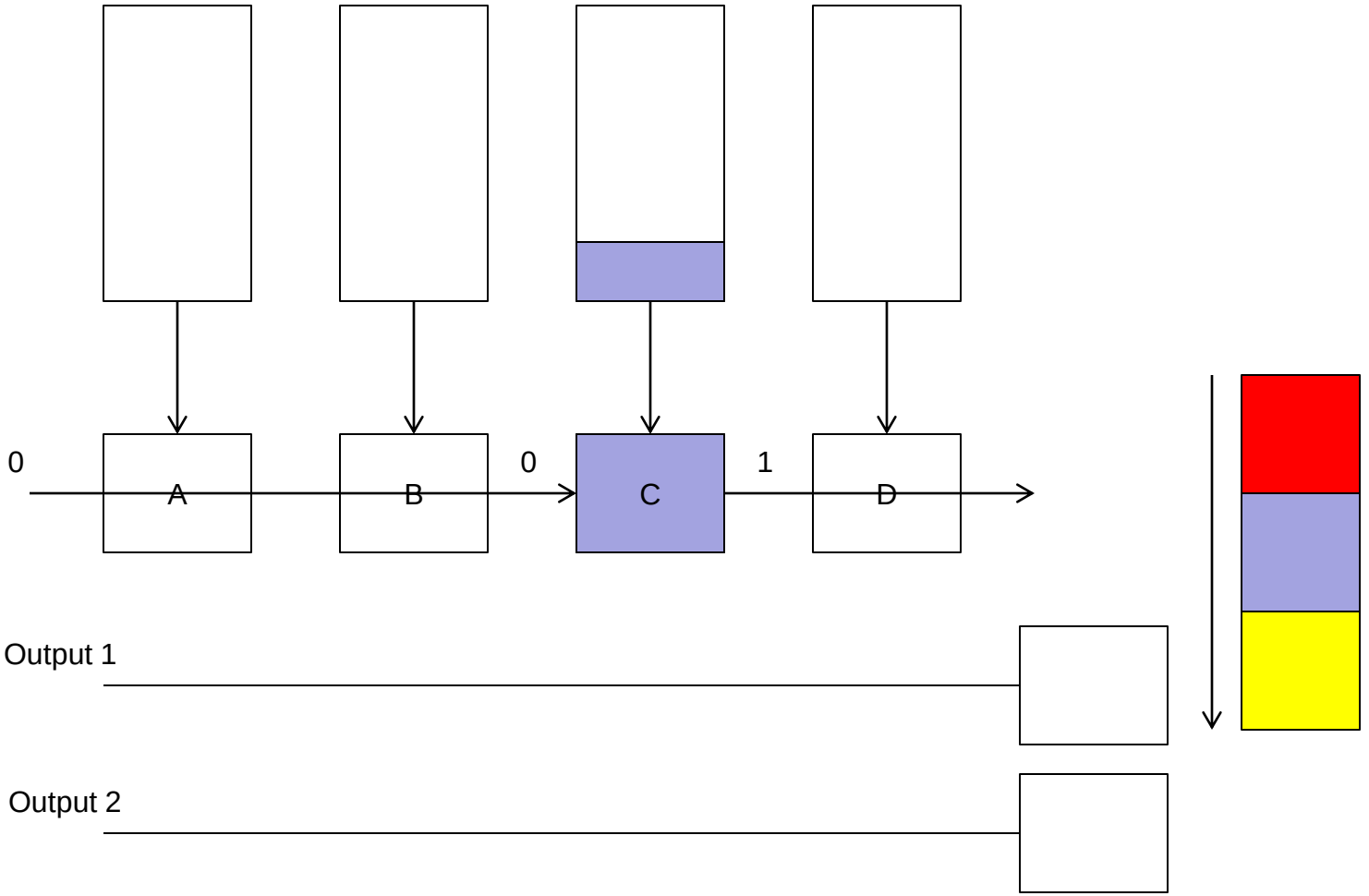
Segmented strip detector with lossy constant-delay-multiplexing



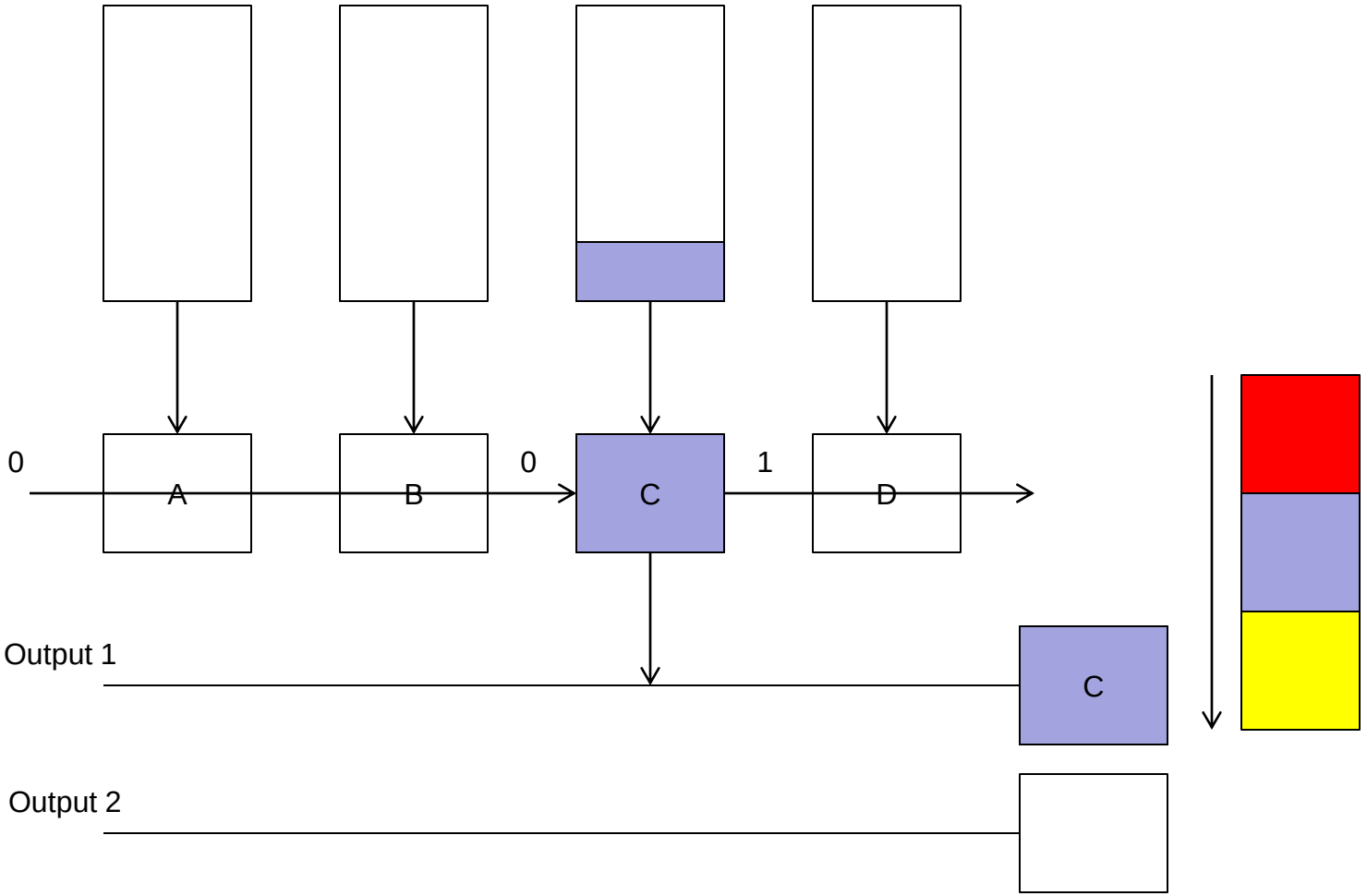
Segmented strip detector with lossy constant-delay-multiplexing



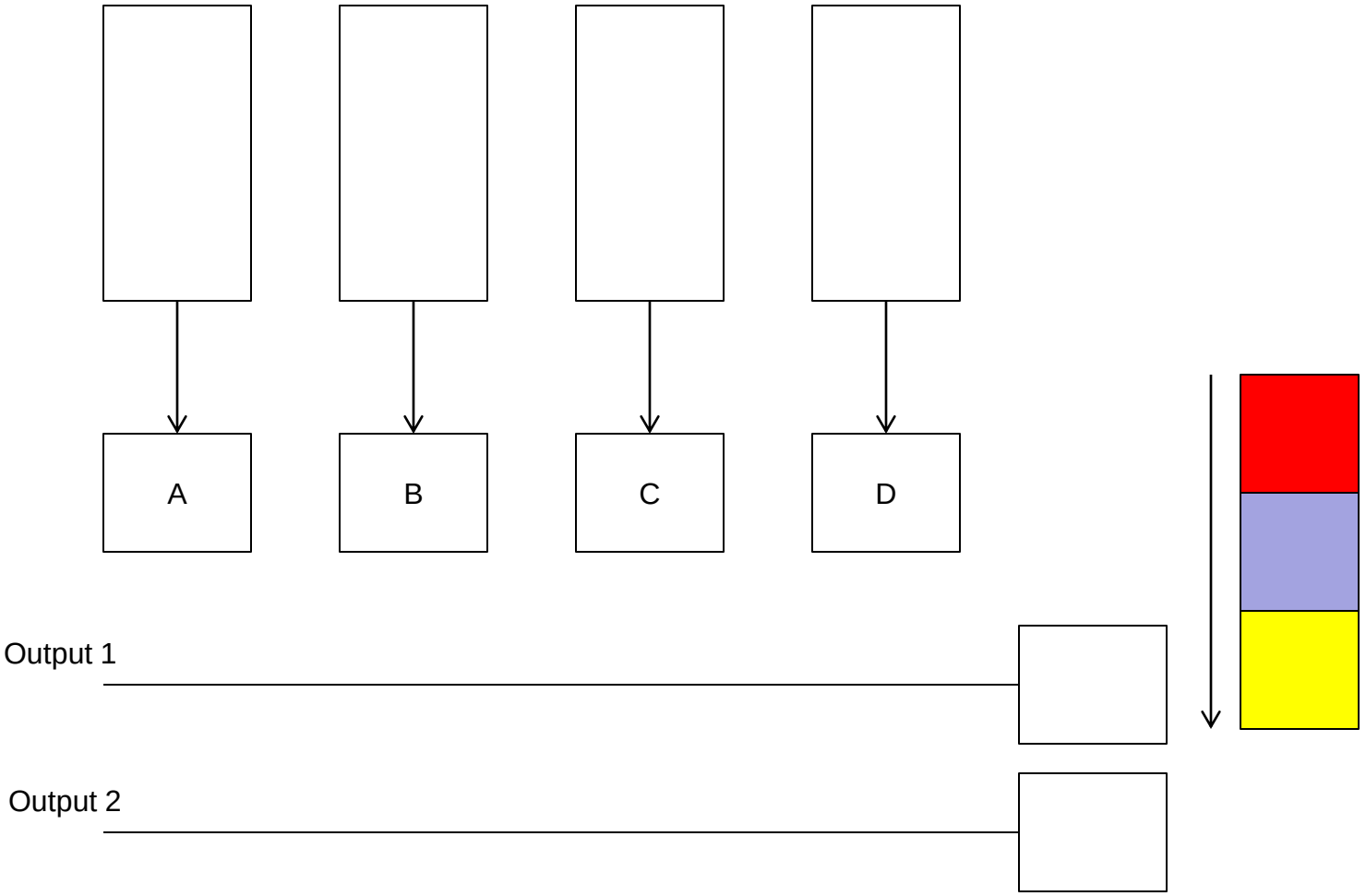
Segmented strip detector with lossy constant-delay-multiplexing



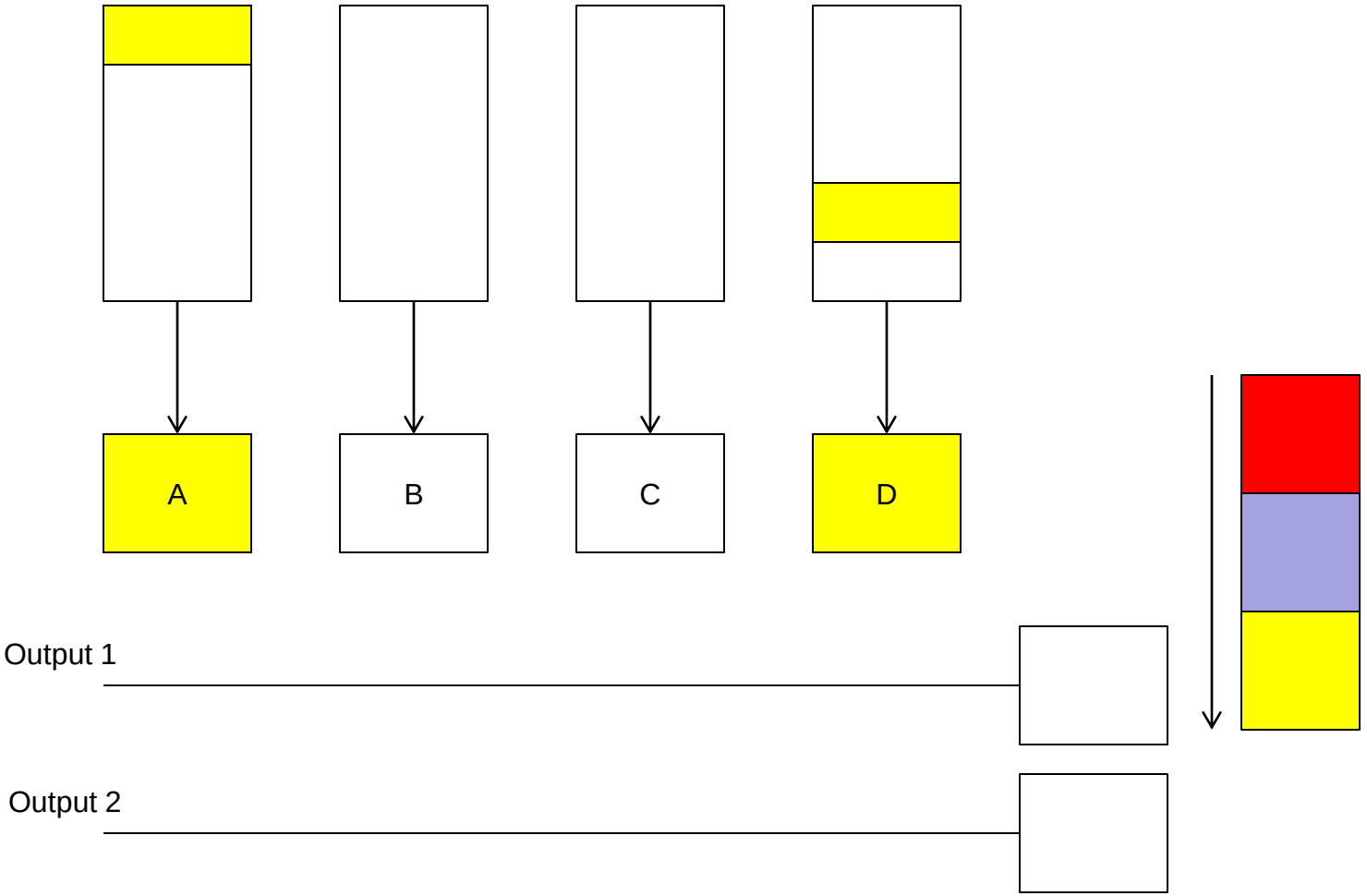
Segmented strip detector with lossy constant-delay-multiplexing



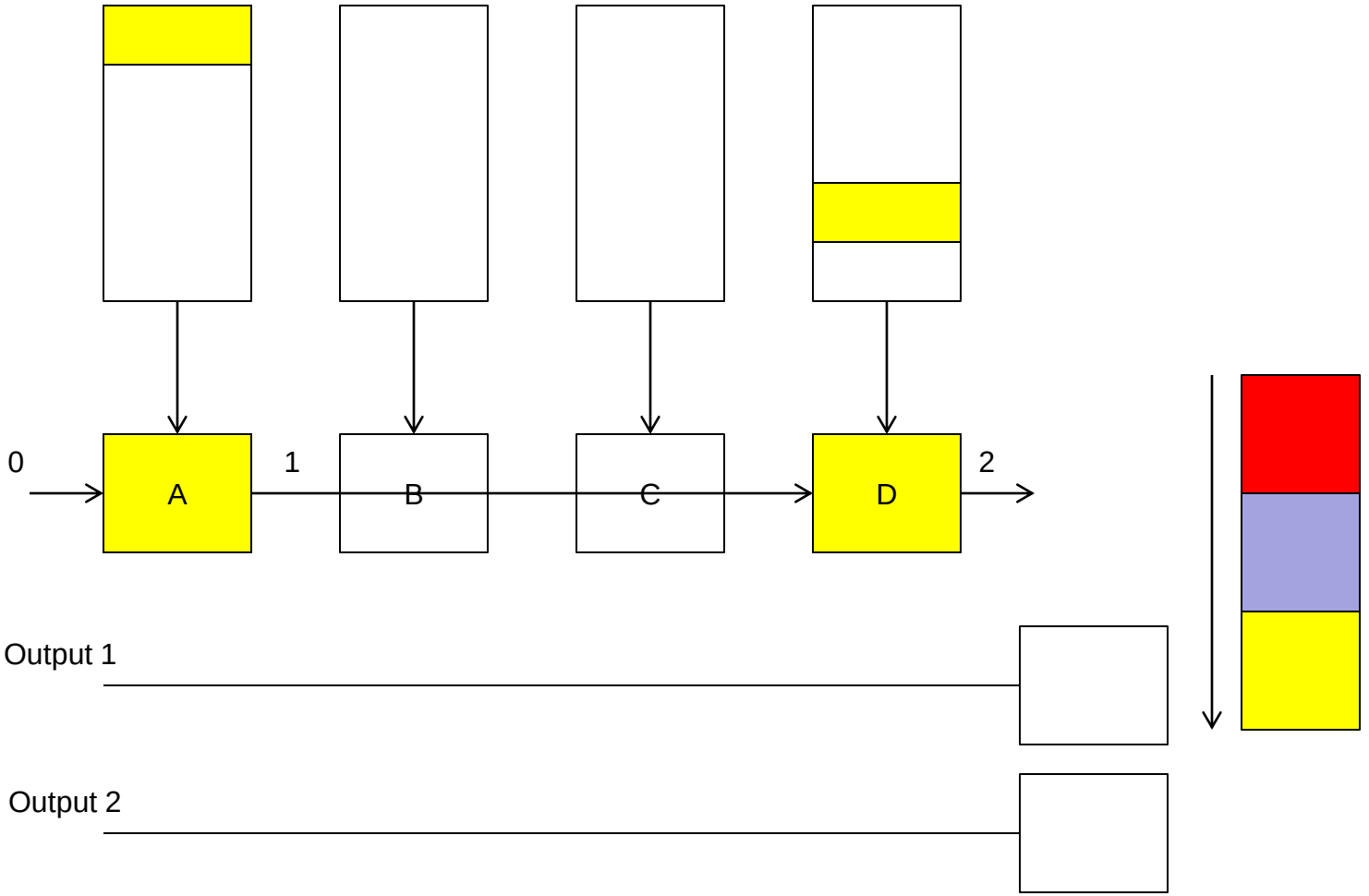
Segmented strip detector with lossy constant-delay-multiplexing



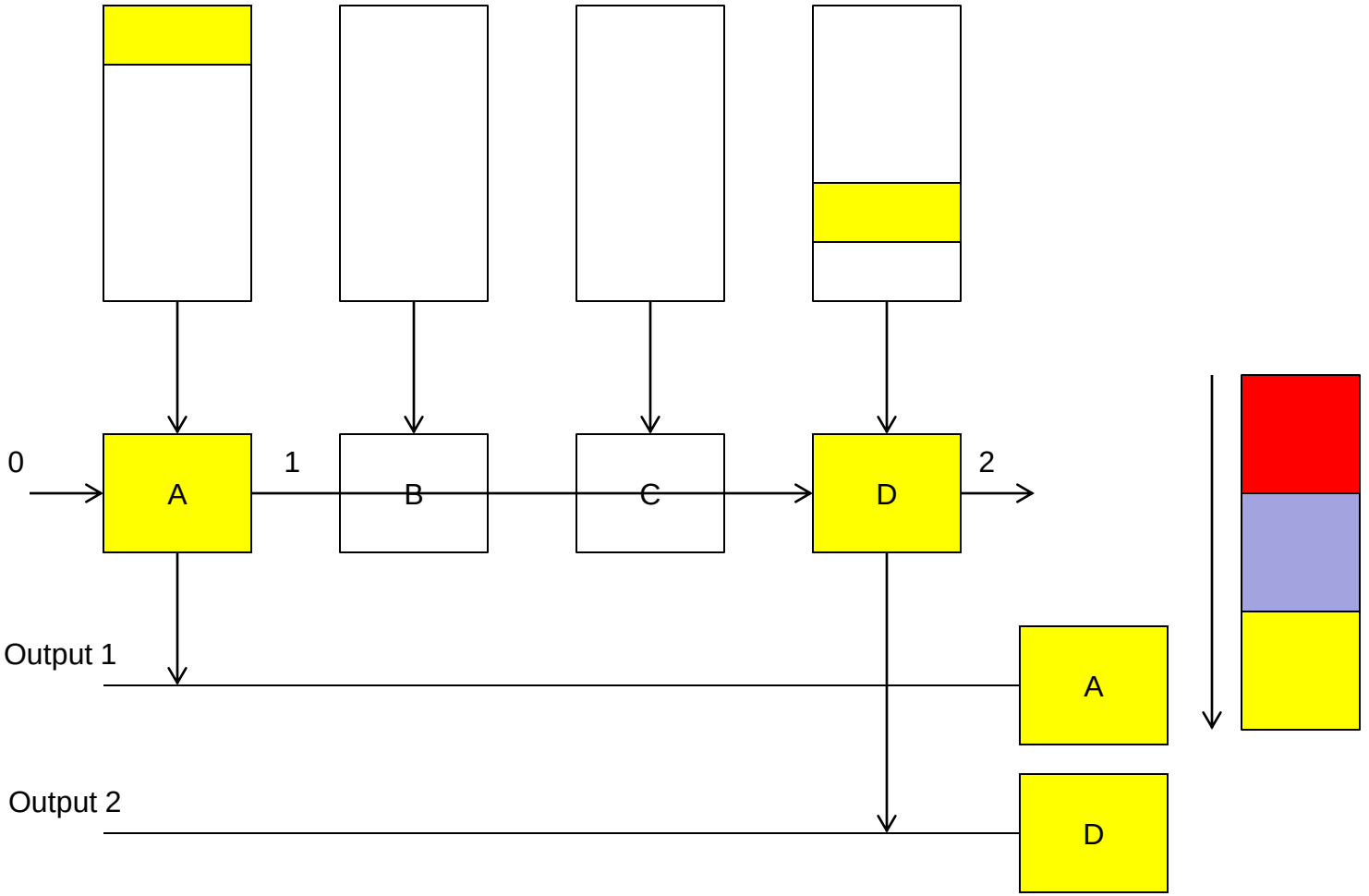
Segmented strip detector with lossy constant-delay-multiplexing



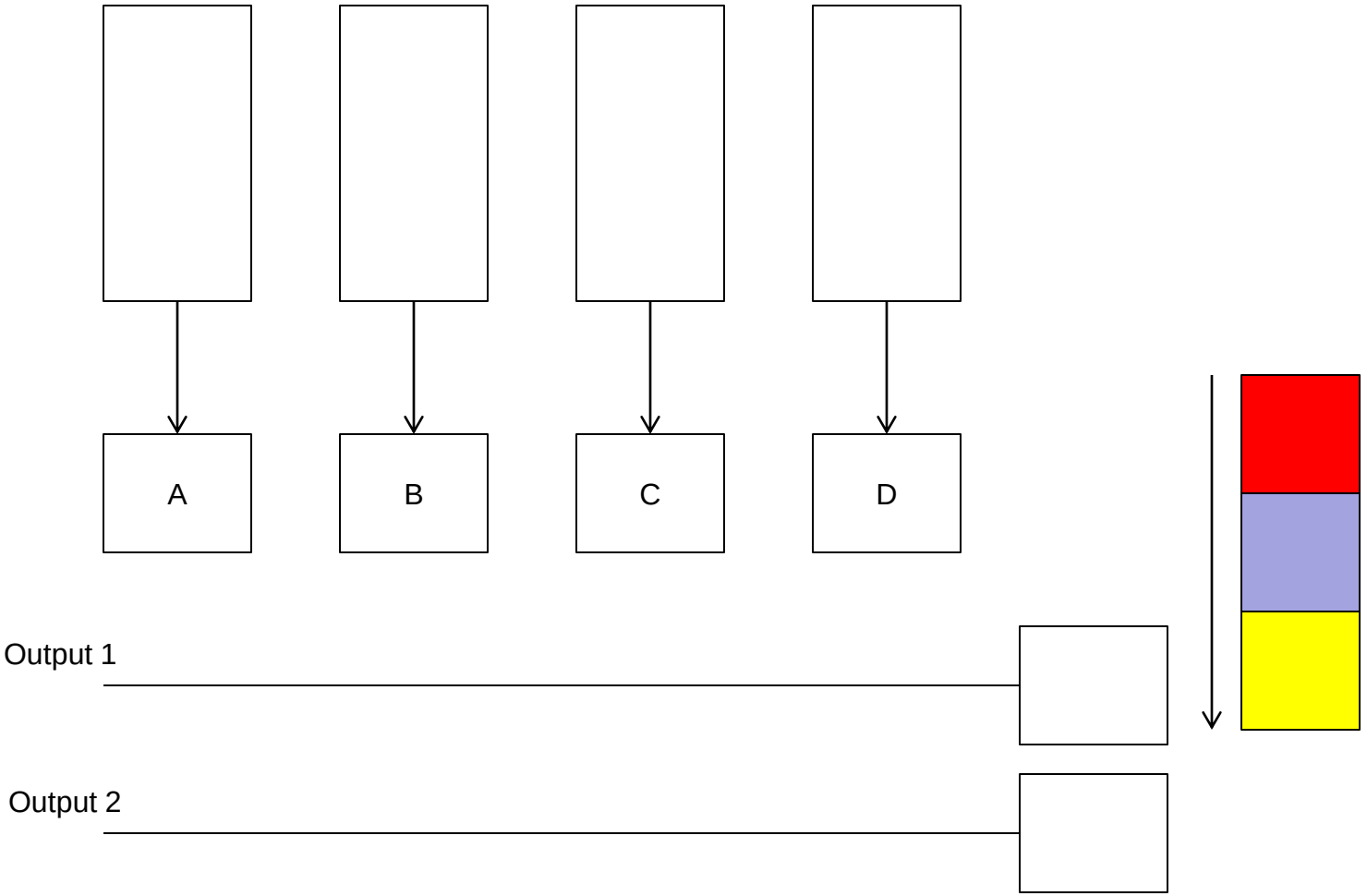
Segmented strip detector with lossy constant-delay-multiplexing



Segmented strip detector with lossy constant-delay-multiplexing



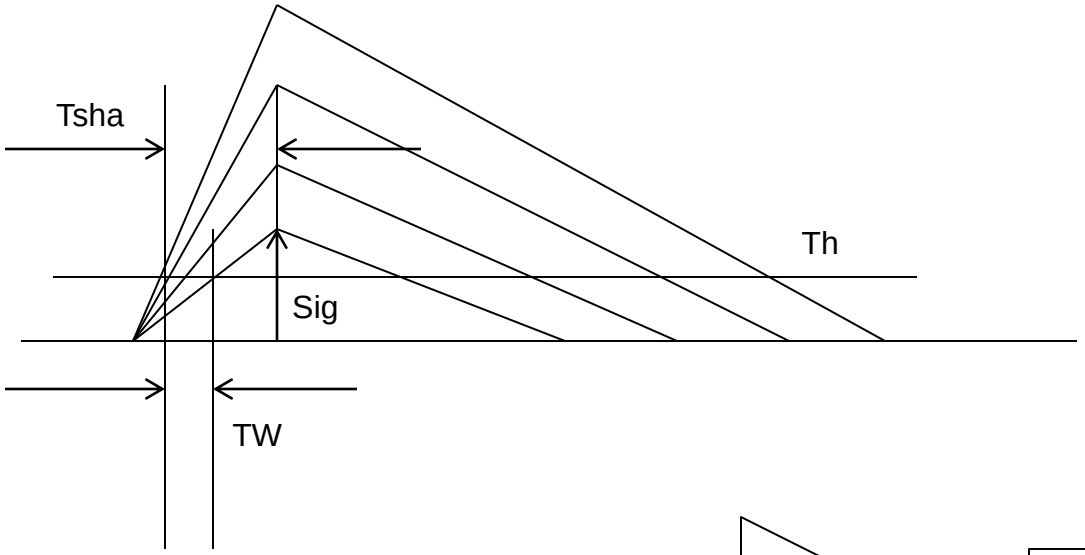
Segmented strip detector with lossy constant-delay-multiplexing

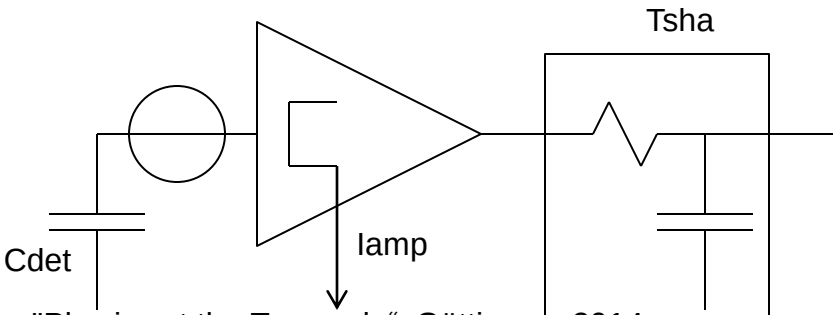


Time Walk Compensation

Time Walk Compensation

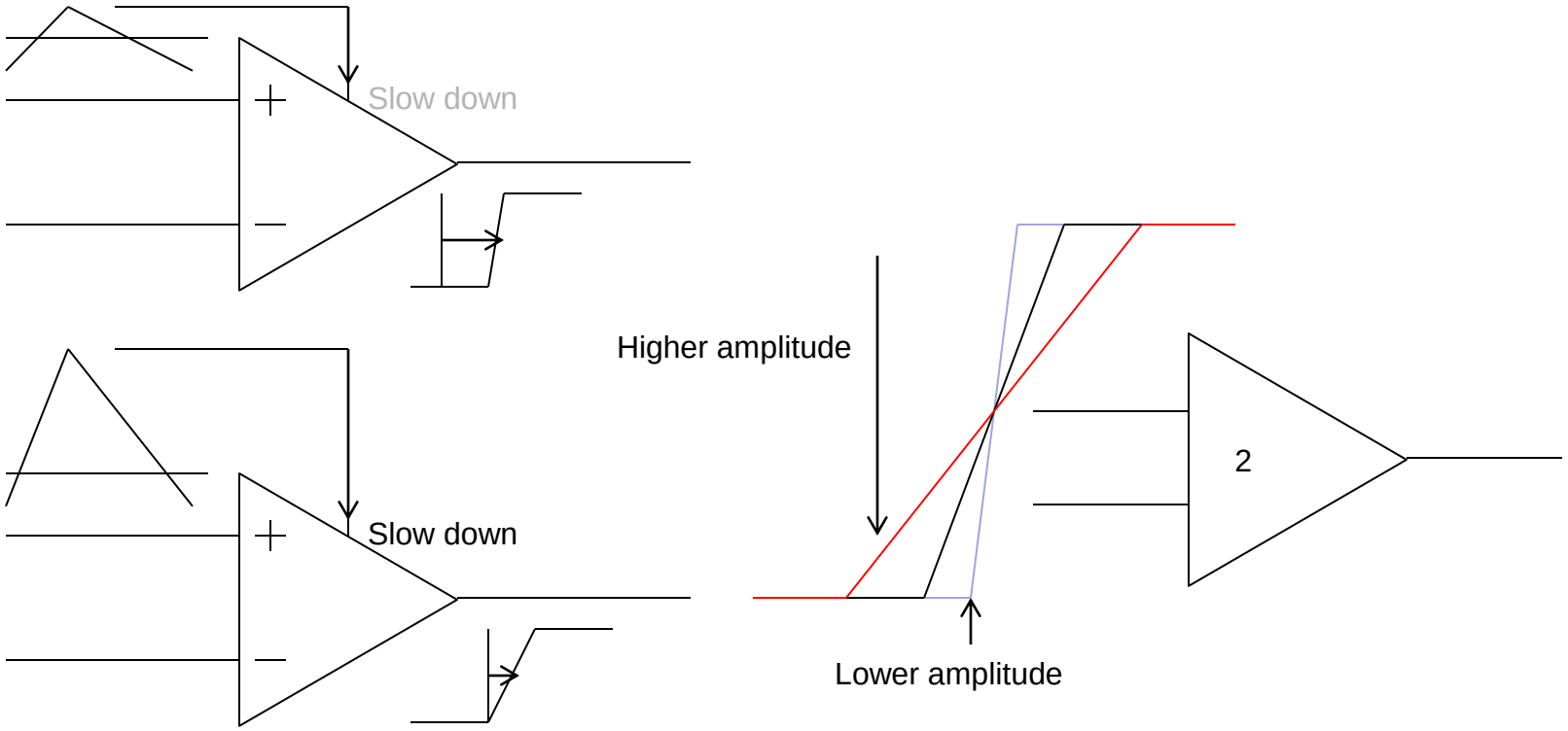
- The idea: Adding of low-pass filter decreases the noise without increasing the power consumption
- => Better SNR, lower threshold
- However: a slow output signal leads to a time-walk
- Time walk is caused 1) by the fluctuations of the input signal and 2) by the low and signal-dependent response speed of the electronics
- Can we compensate for time walk, without decreasing the shaping time constants?





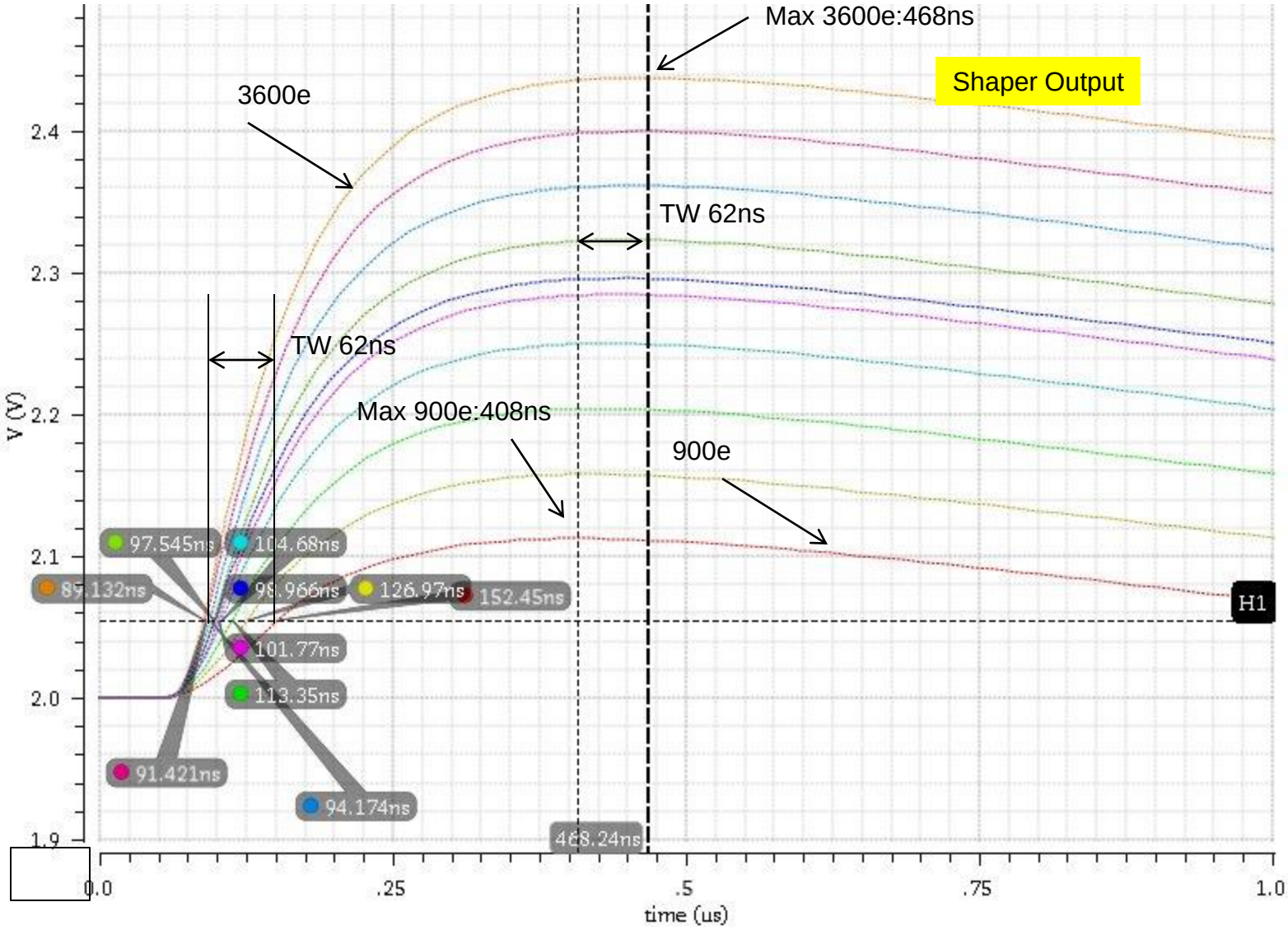
Time Walk Compensation

- Imagine a comparator which has the output zero-to-one transition speed, that depends on the input signal “overdrive”
- High amplitude signal – faster threshold crossing but slower 0-1 transition
- Low amplitude signal – slower threshold crossing but faster 0-1 transition
- Result: the threshold-crossing- and the transition time skews compensate each other
- Second comparator generates time-walk free signal



Time Walk Compensation – AMS 350 nm

- Noise=8.8mV, Thr=55mV, Bias current=10µA, Pixel size = 50x250µm, Ifoll=10, amplifier power **200mW/cm²**



Time Walk Compensation – AMS 350 nm

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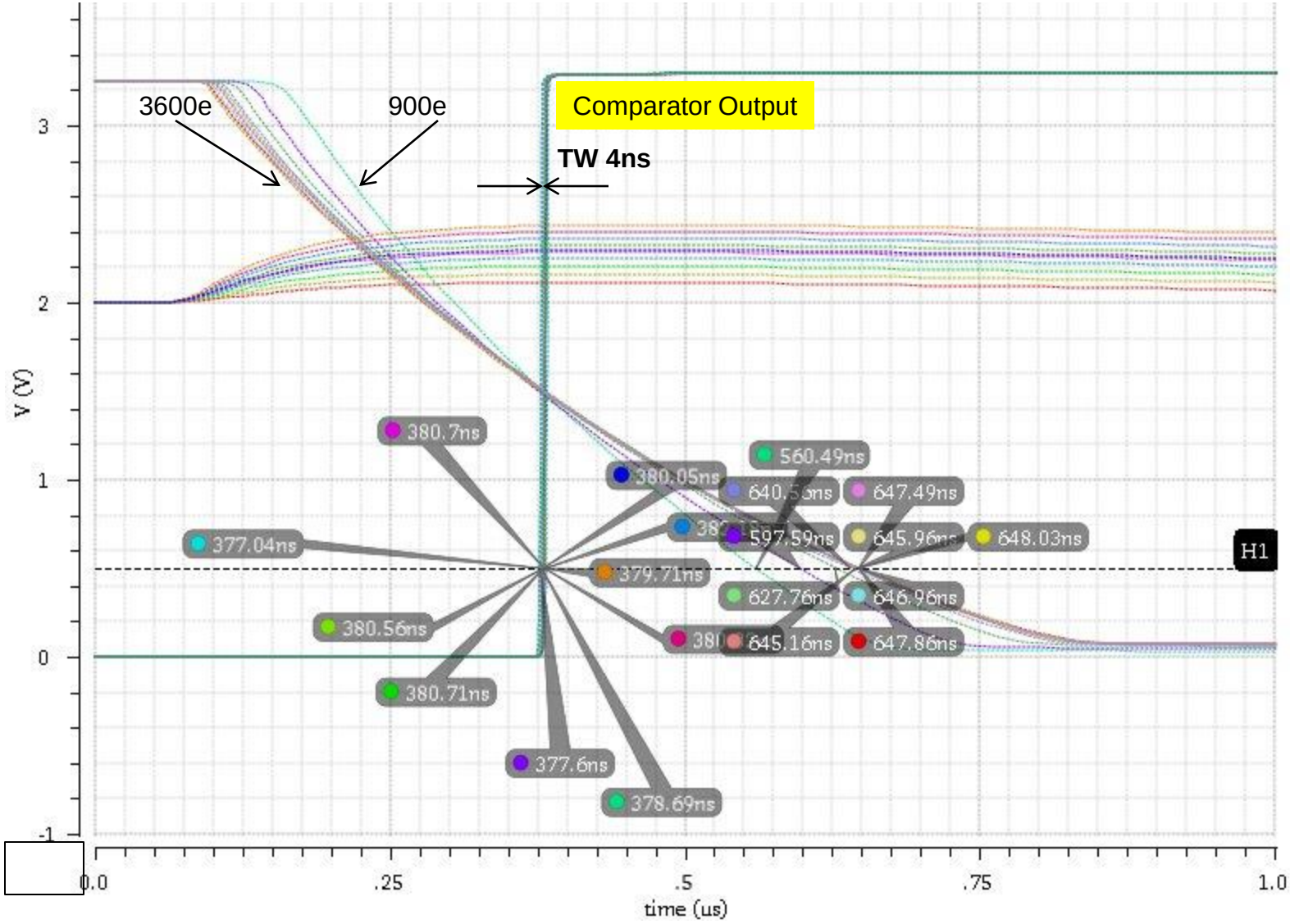
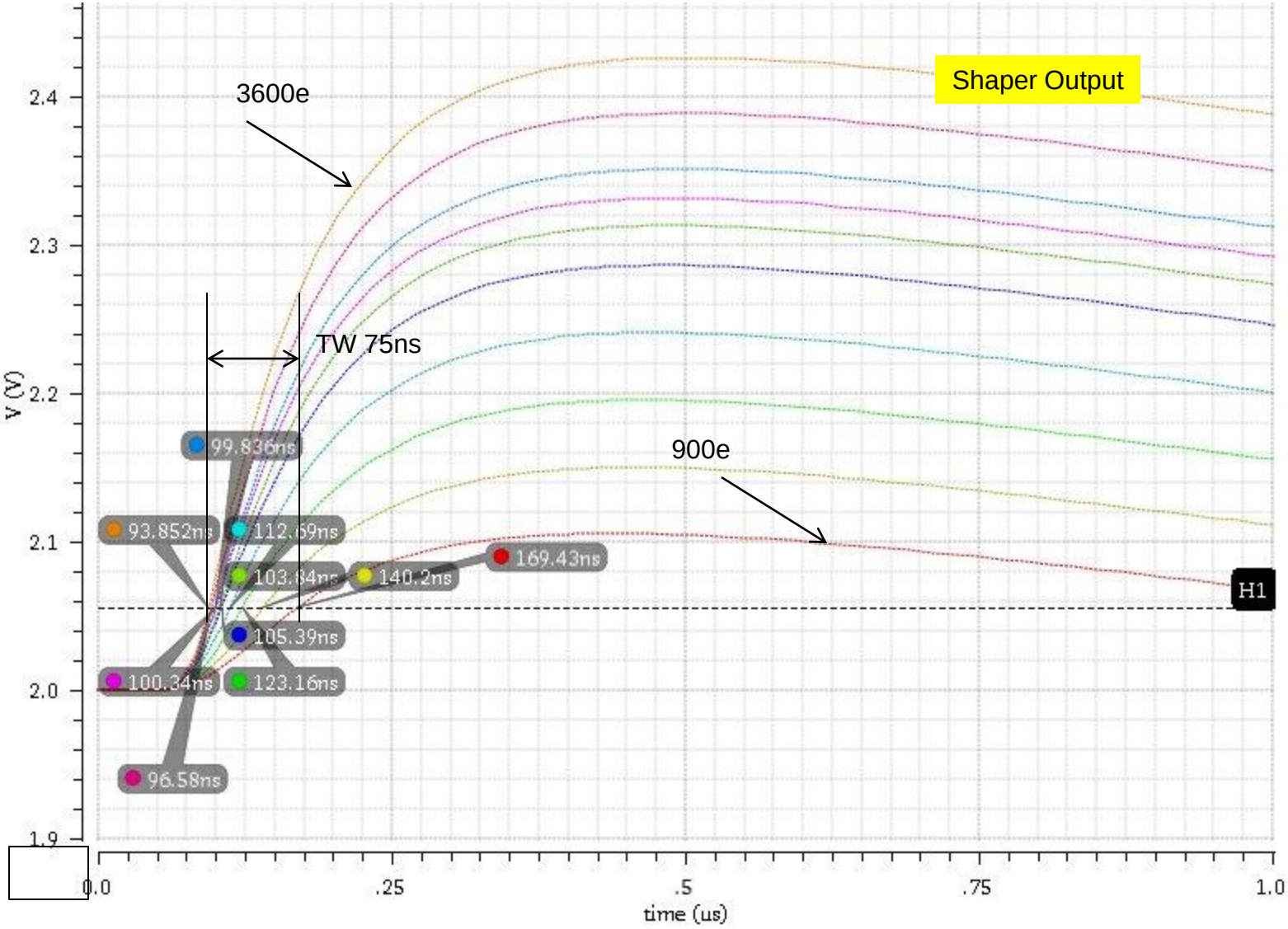


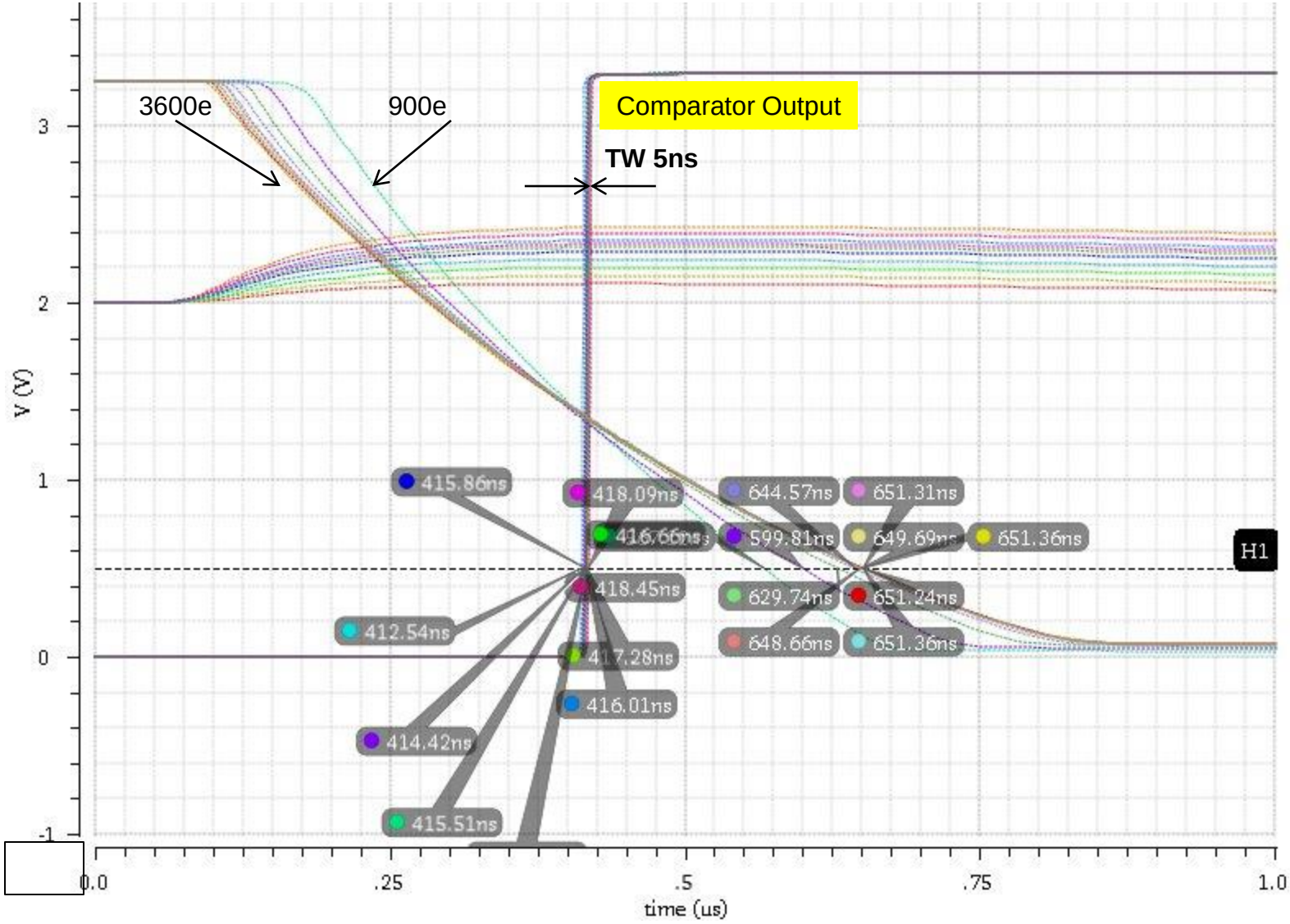
Time Walk Compensation

- Noise=8.0mV, Thr=55mV, Bias current=10µA, Pixel size = 50x500µm, Ifoll=7, amplifier power **100mW/cm²**



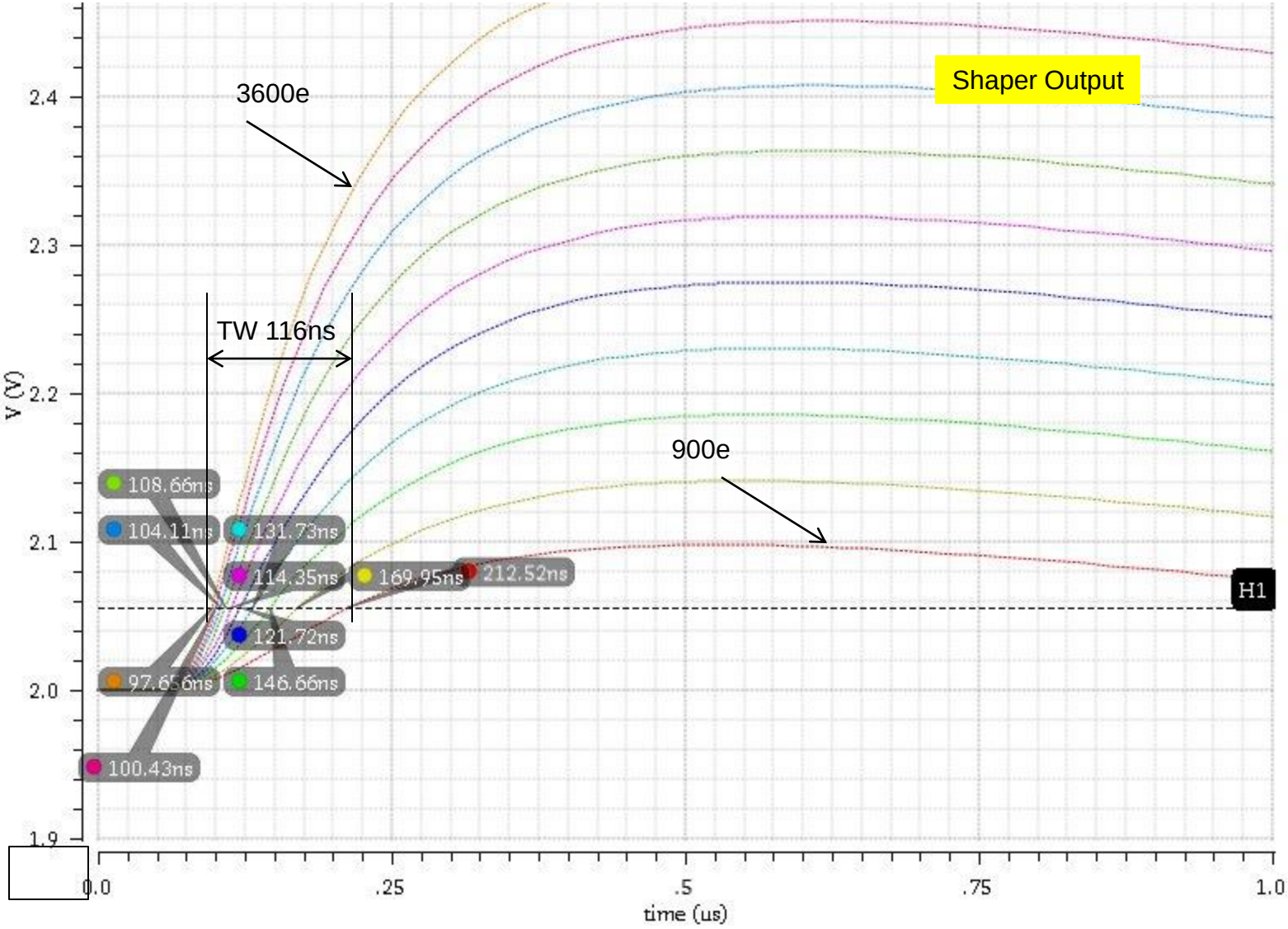
Time Walk Compensation

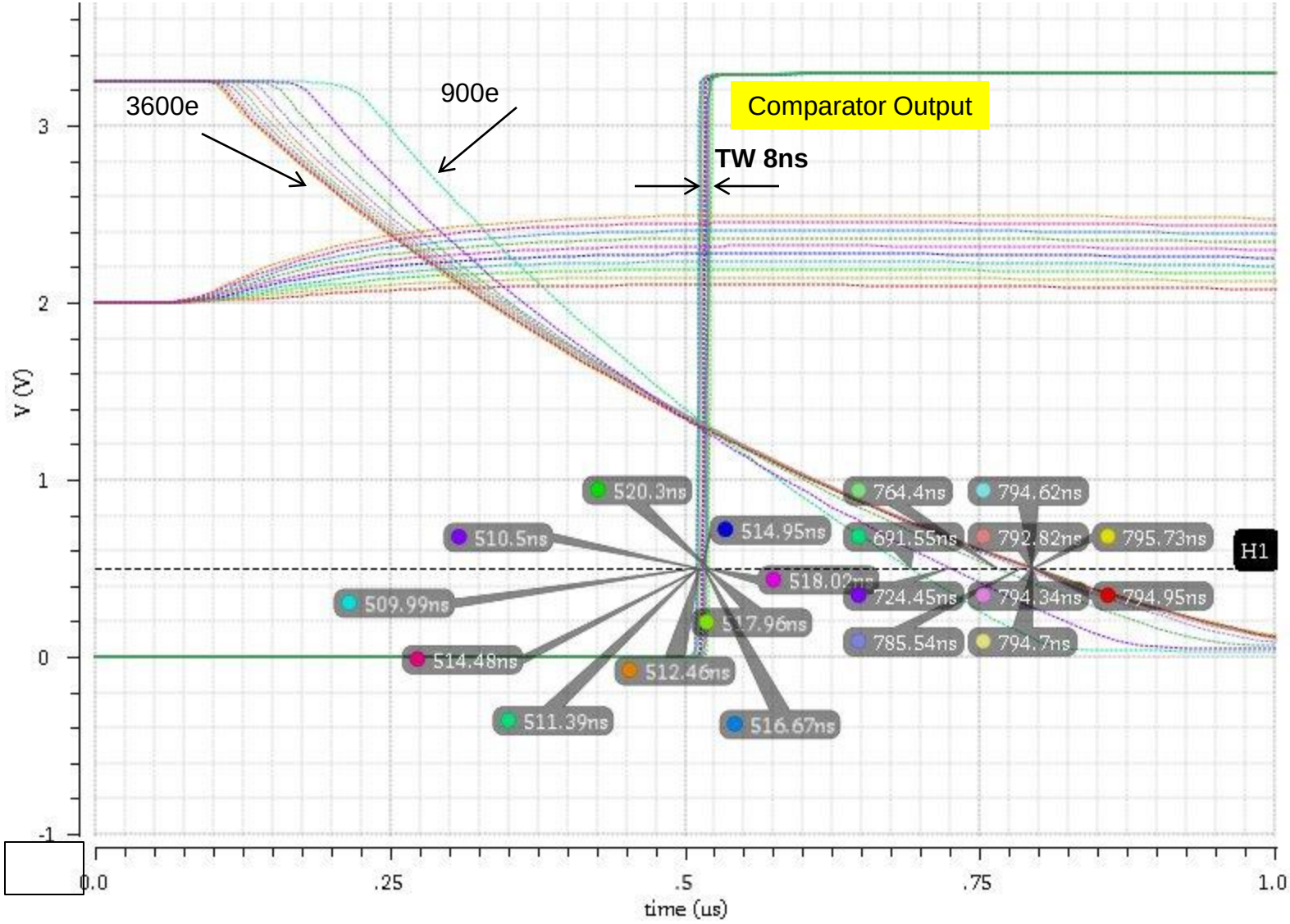
- Noise=8.0mV, Thr=55mV, Bias current=10µA, Pixel size = 50x500µm, Ifoll=7, amplifier power **100mW/cm²**



Time Walk Compensation

- Noise=7.9mV, Thr=55mV, Bias current=5µA, Pixel size = 50x500µm, Ifoll=5, amplifier power **50mW/cm²**



Time Walk Compensation

- Noise=7.9mV, Thr=55mV, Bias current=5µA, Pixel size = 50x500µm, Ifoll=5, amplifier power **50mW/cm²**