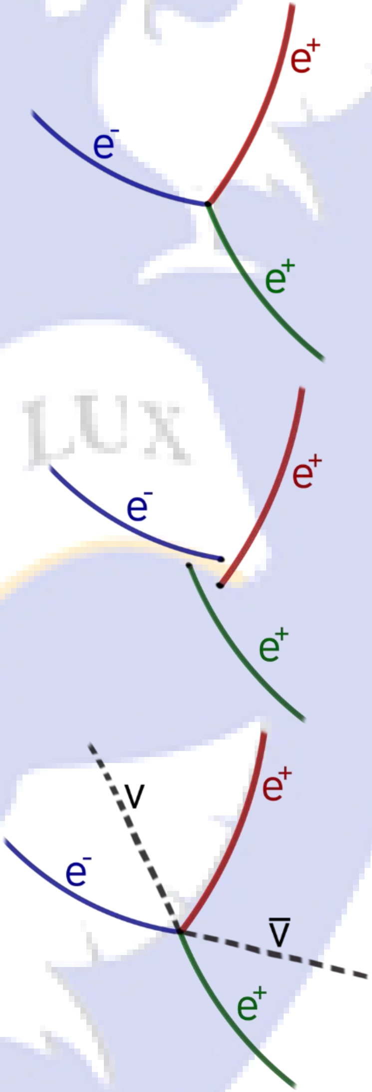
UNIVERSITY OF
LIVERPOOL

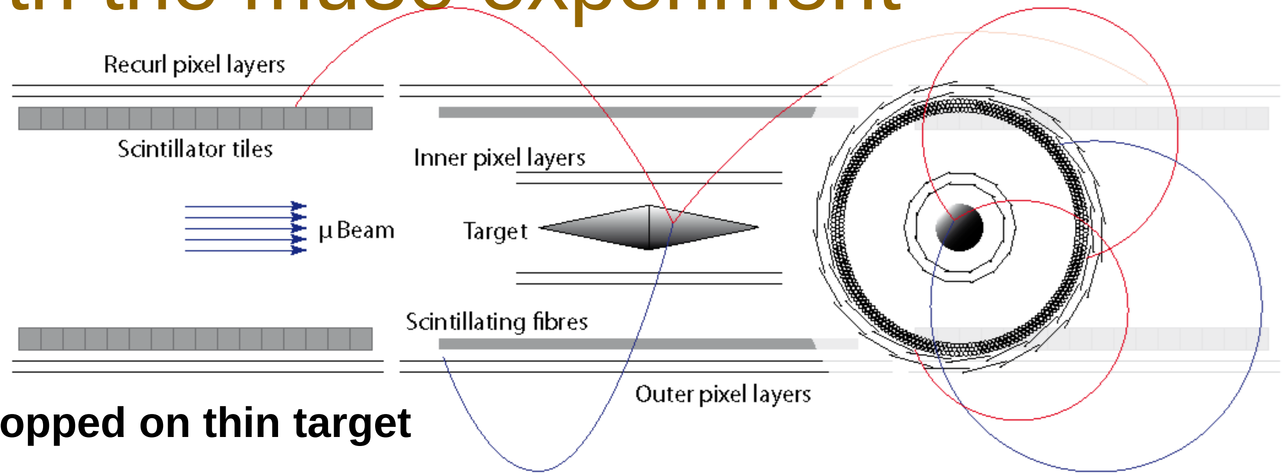
Mu3 MuPix Tracker: mechanics and assembly

A member of the Russell Group

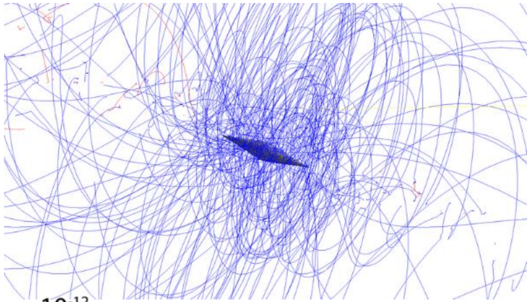
Science & Technology
Facilities Council

$\mu^+ \to e^+ e^+ e^-$ with the mu3e experiment

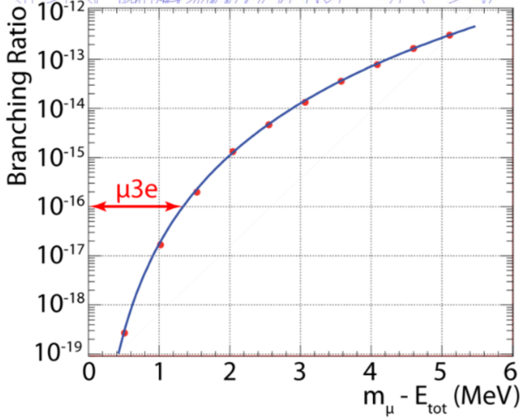




Muons stopped on thin target



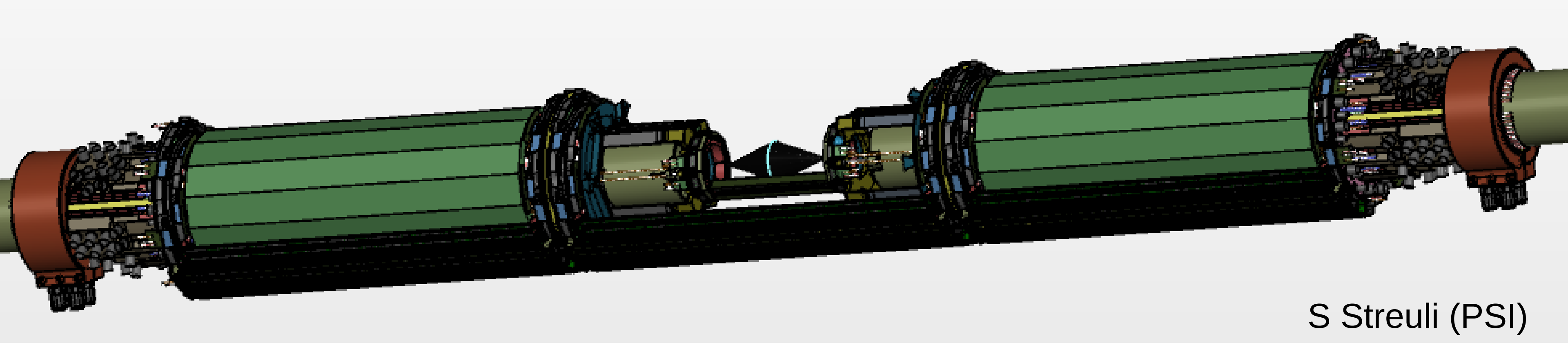
Combinatoric backgrounds:
DC beam & Larger target
Timing resolution: Scintillator fibres (1 ns) and Scintillator tiles (100 ps)
Pixel tracker also needs to be fast (~10ns)
Vertex resolution: Pixel tracker (200 μm)



Michel decays with internal conversion:
$\mu^+ \to e^+ e^+ e^- \nu\nu$
Good momentum resolution:
Thin detectors and re-curling tracker concept
Pixel tracker (0.5 MeV)

The full detector (1)

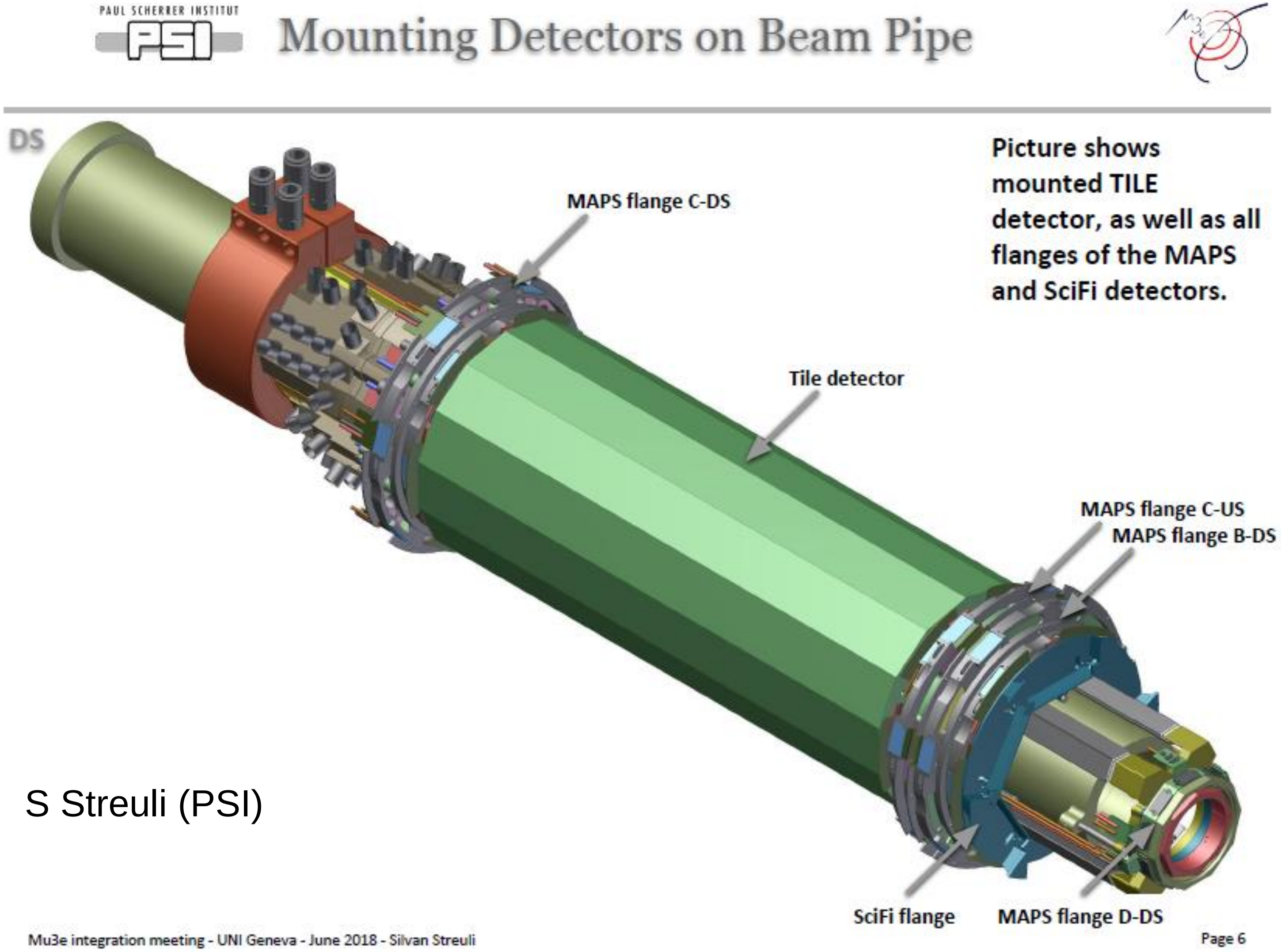
Full mechanical design of Mu3e detector to go inside the solenoid.



S Streuli (PSI)

The full detector (2)

Model for the service routing



PAUL SCHERRER INSTITUT

Mounting Detectors on Beam Pipe

Picture shows mounted TILE detector, as well as all flanges of the MAPS and SciFi detectors.

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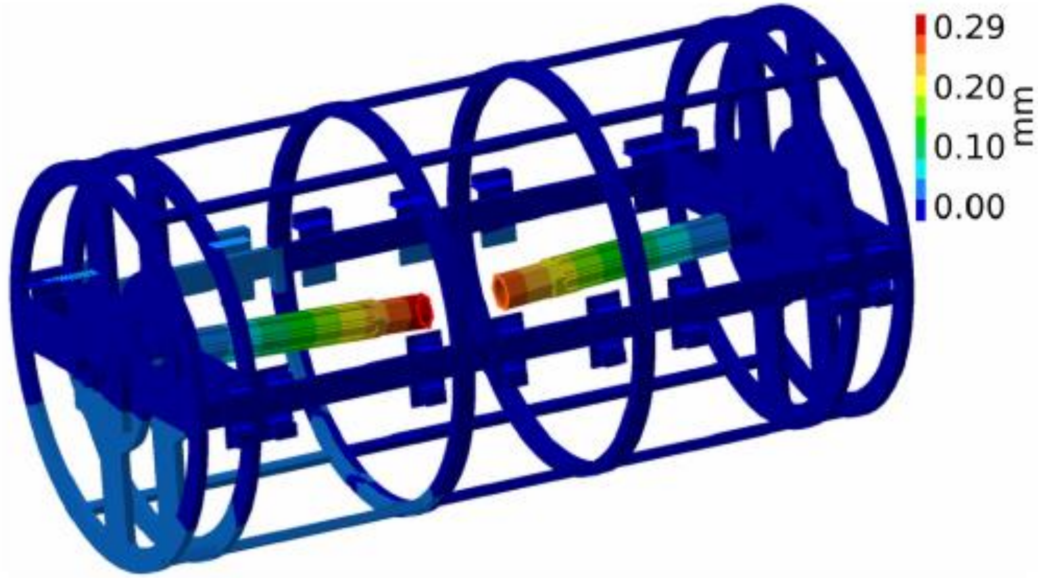
S Streuli (PSI)

The full detector (1)

Up-stream and down stream beam-pipes must be very stable.
Supported from one side only from double wheel structure

Experimental cage

F Meier (Heidelberg)



Ring material: Vetronite

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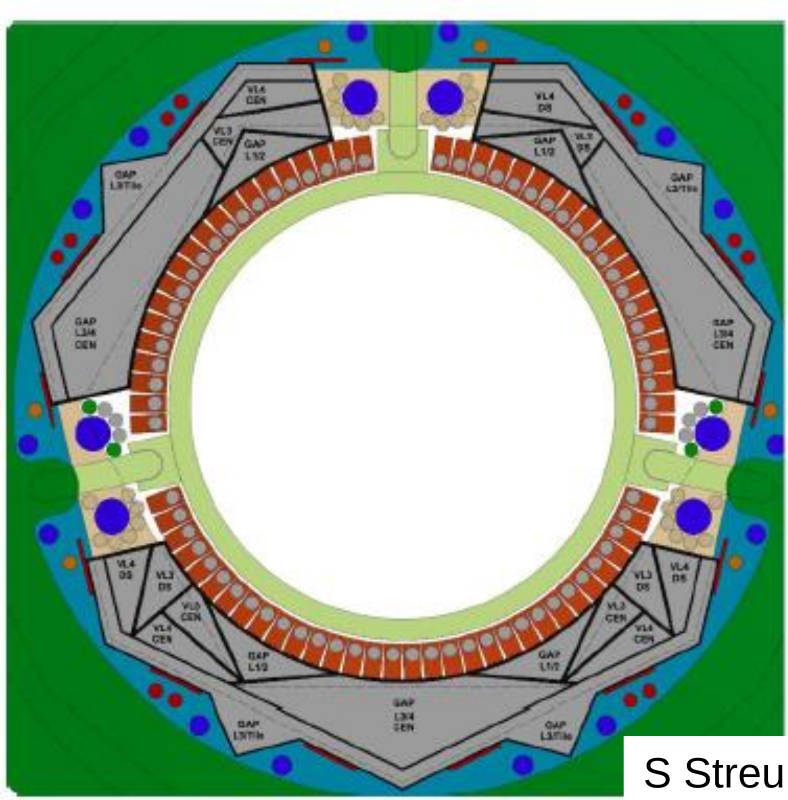
The full detector (2)

Model for service routing

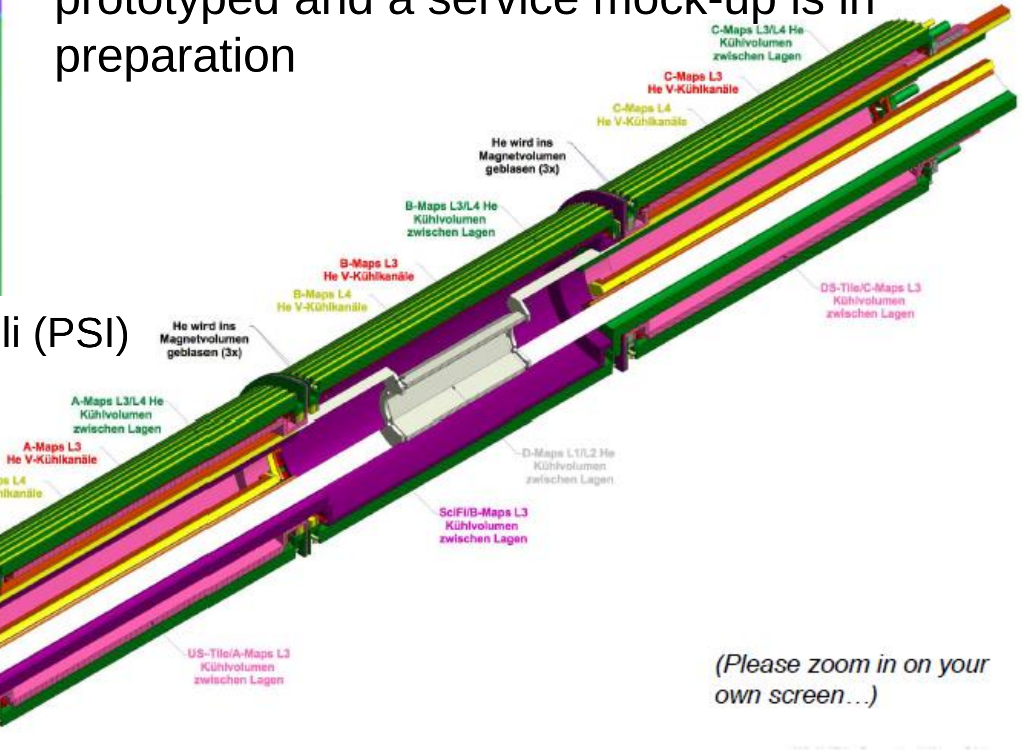


S Streuli (PSI)

All service run between beam-pipe and tile detector

- thin wall Helium ducts
- water cooled copper power bars
- various electrical services

Various components are being prototyped and a service mock-up is in preparation



(Please zoom in on your own screen…)

MuPix Tracker: Some technology choices

Performance requirement dictate the need for a fast, low mass and high resolution detector.

MuPix8 on test board

HV-CMOS sensors (AMS H18 → TSI 180 nm)

- Monolithic pixels with good timing resolution
- and spatial resolution: pixel size 80x80 micron^2
- can be thinned to 50 micron (or less)

So far a 10x20 mm^2 near production ready chip (MuPix8) was successfully demonstrated in the lab in in test beams.

Due to difficulties accessing AMS process now moving to TSI 180nm (both derived from same IBM process). First MPW results indicate TSI chip (MuPix7) performs identically to AMS version.

First construction compatible ~20x23 mm^2 chip (MuPix-10) to be will be submitted to TSI early 2019.

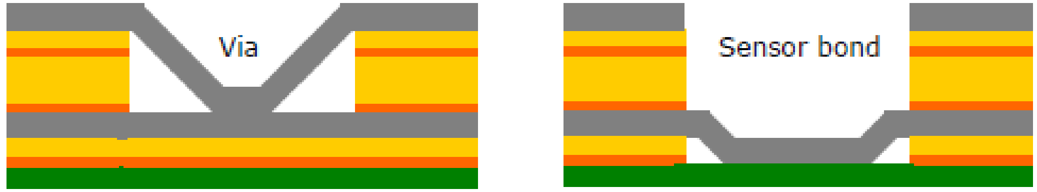
Aluminium-Kapton flex circuits

- Sensors are glued to 2 layer Aluminium-Kapton flex circuit
- electrical connection are made using Single point Tape automated bonding (SP-TAB)

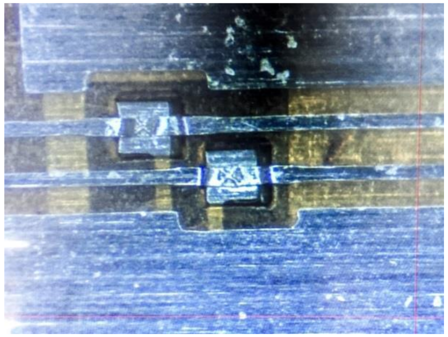
Thin Al-kapton tapes and Single Point Tape Automated Bonding - SPTAB

MAPS sensors are glued to 2 layer Aluminium-Kapton flex circuits (LTU) and connected using SPTAB bonding.

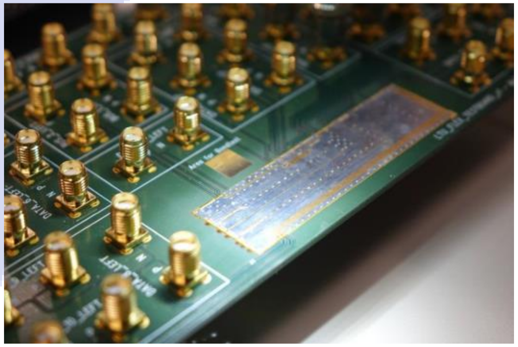
SP-TAB: kapton is etched away leaving an exposed aluminium trace that can be bonded with a wedge bonder to make a bond or via. The bonding can be done on standard wire-bonding machine using a dedicated wedge tool.



Schematic of SPTAB via or bond

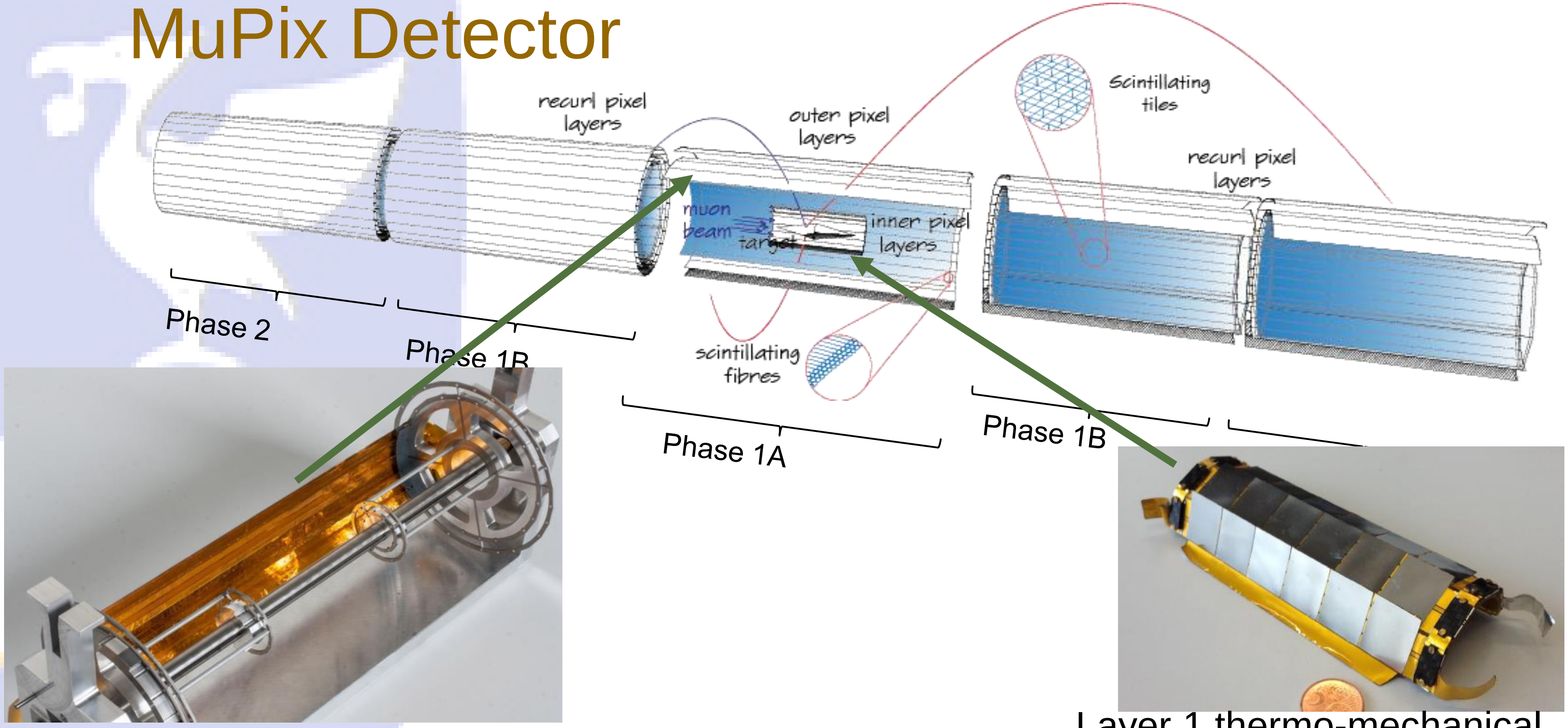


Picture of 2 SPTAB bonds



PCB with prototype flex circuit

MuPix Detector



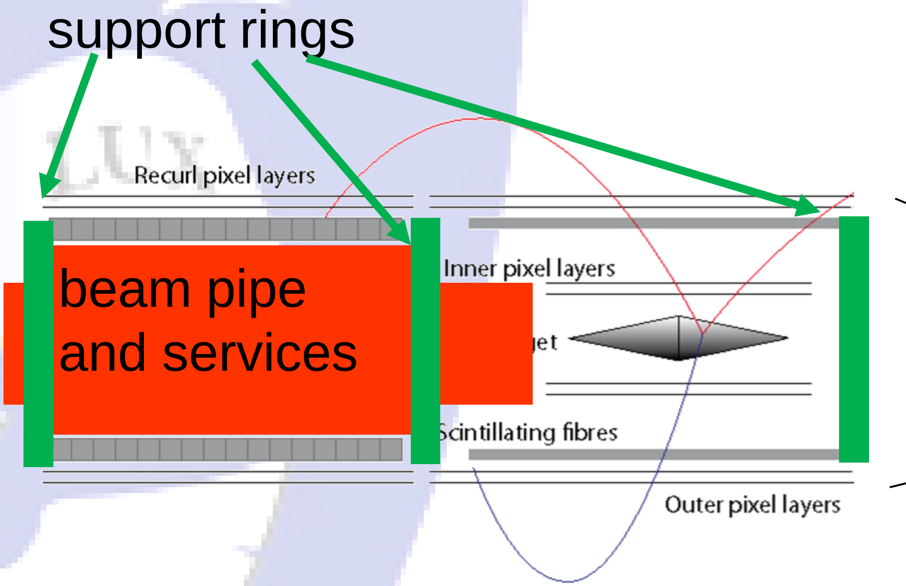
Layer 3 early prototype in assembly frame with 50µm glass “chips”

Layer 1 thermo-mechanical prototype

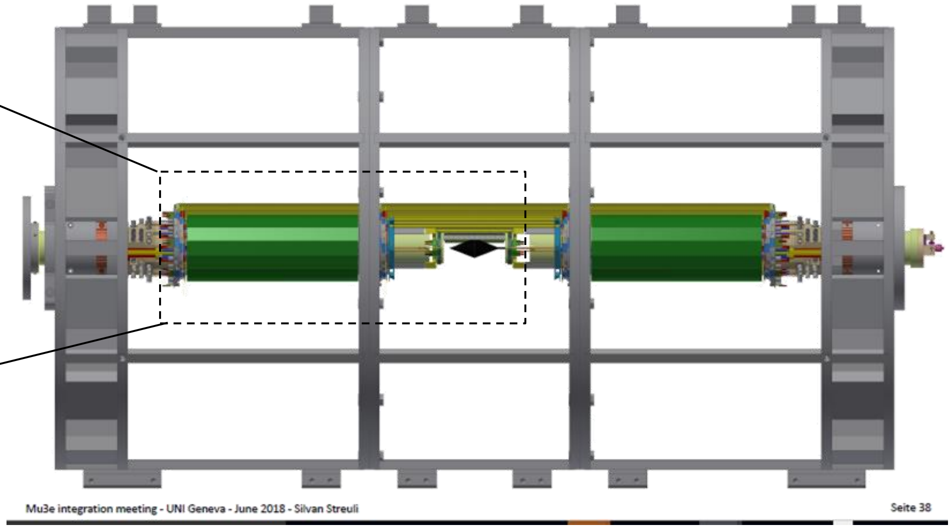
		half-shells	ladders/half-shell	chips/ladder	total chips	area (m²)
Phase 1	Central layer 1	2	4	6	48	0.02
	Central layer 2	2	5	6	60	0.02
		modules	**ladders/module**			
	Central layer 3	6	4	17	408	0.16
	Central layer 4	7	4	18	504	0.20
	Re-curl I layer 3	12	4	17	816	0.33
	Re-curl I layer 4	14	4	18	1008	0.40
Phase 2	Re-curl II layer 3	12	4	17	816	0.33
	Re-curl II layer 4	14	4	18	1008	0.40
	Total				**4668**	**1.87**

Material budget

Services run along upstream and downstream beam pipes and at the support rings. Material thus minimised in central region and for re-curling tracks outside layers 3 and 4.


support rings

beam pipe and services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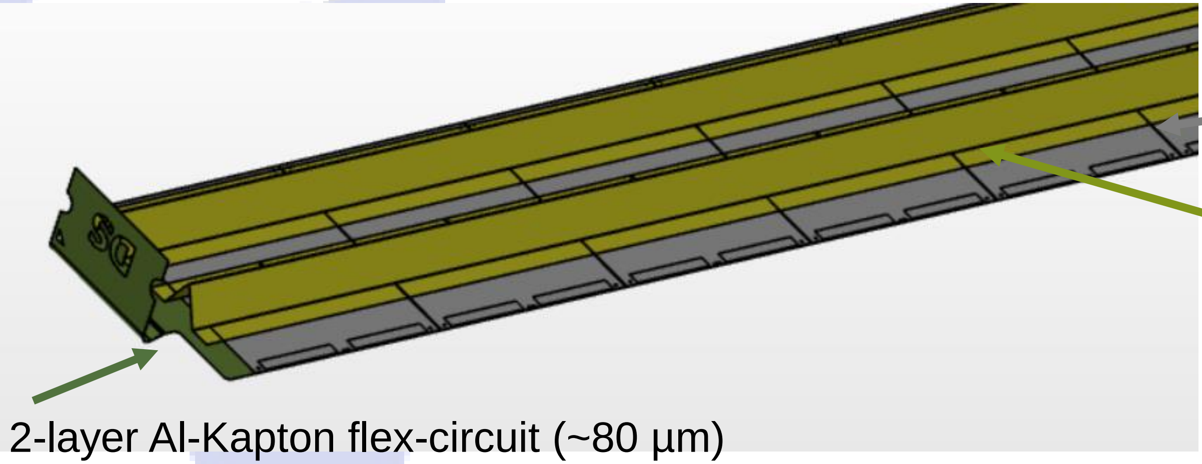
Beampipe is water cooled.
Only cooling in active volume uses cold gaseous Helium.

Material budget: MuPix ladders

example layer 4



18 MuPix MAPS chips (50 µm)

25 µm kapton v-folds

2-layer Al-Kapton flex-circuit (~80 µm)

Al 14 µm
PI 10 µm
Glue 5 µm
PI 25 µm
Glue 5 µm
Al 14 µm
PI 10 µm

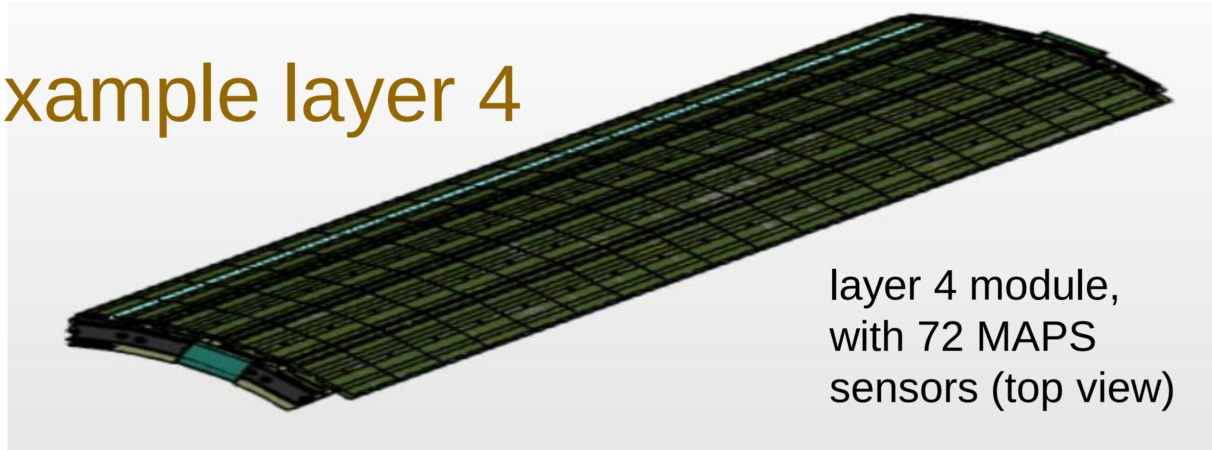
Foreseen lay-up of aluminium kapton flex circuit (LTU)

		Layer 1-2		Layer 3-4
	thickness [µm]	X/X_0	thickness [µm]	X/X_0
MuPix Si	45	$0.48 \cdot 10^{-3}$	45	$0.48 \cdot 10^{-3}$
MuPix Al	5	$0.06 \cdot 10^{-3}$	5	$0.06 \cdot 10^{-3}$
HDI polyimide & glue	45	$0.18 \cdot 10^{-3}$	45	$0.18 \cdot 10^{-3}$
HDI Al	28	$0.31 \cdot 10^{-3}$	28	$0.31 \cdot 10^{-3}$
polyimide support	25	$0.09 \cdot 10^{-3}$	≈ 30	$0.10 \cdot 10^{-3}$
adhesives	10	$0.03 \cdot 10^{-3}$	10	$0.03 \cdot 10^{-3}$
total	158	$1.15 \cdot 10^{-3}$	163	$1.16 \cdot 10^{-3}$

Provisional material budget for MuPix: ~0.11% X_0 per tracking layer

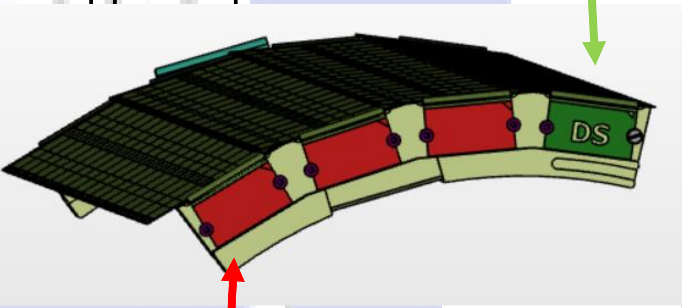
MuPix modules: example layer 4

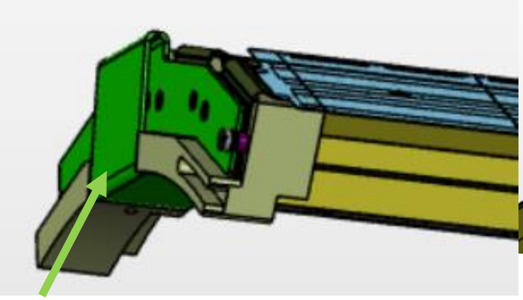
Ladders are electrically split in the middle with 9 chips read out from either end.



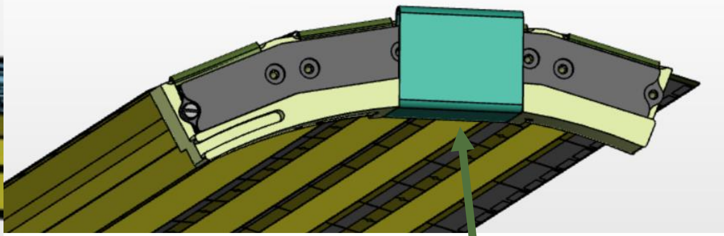
layer 4 module, with 72 MAPS sensors (top view)

At ladder end transfer from 2 layer aluminium-kapton to 4-5 layer copper-kapton circuit.

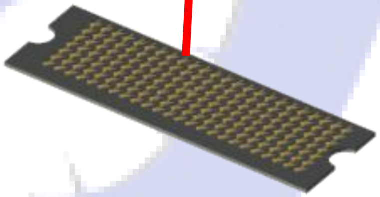




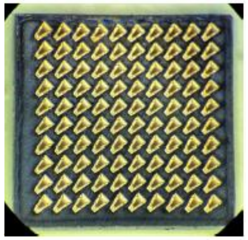
Carbon-fibre-resin clamp plate ensures the necessary mating force on the interposer stack



A further copper-aluminium flex combined the lines for 4 ladders



Ladder to module contact uses 7x12 array of compression contacts (SAMTEC)



Module to outside service tapes contact: 10x10 array, compression springs and solder balls. (SAMTEC)

Thermo-mechanical mock-up (1)

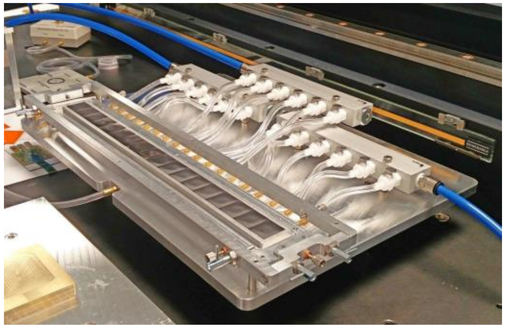
Currently starting production of a full **thermo-mechanical mock-up** of the central MuPix tracker. Four half shells (L1 &L2) and 13 outer modules (L3 & L4)

- Develop and qualify the assembly tooling and methods
- Verify the MuPix cooling model.

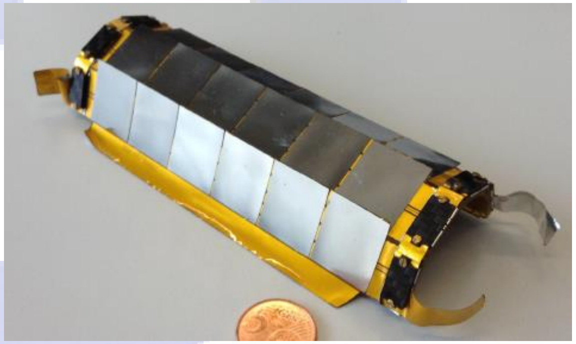
Two types of modules will be built

I. "tape-heater" modules with a resistive Al-kapton flex circuit. A subset of which will be equipped with 50µm steel dummy-chips.

Batch of layer 4 Tape-heater ladders.



Steel chips positioned on tooling jig with robotic gantry. *University of Oxford*



Layer 1 half-shell for thermo-mechanical mock-up. Steel chips on resistive kapton aluminium circuits. *University of Heidelberg*

Ladder mounting to module. *University of Liverpool*

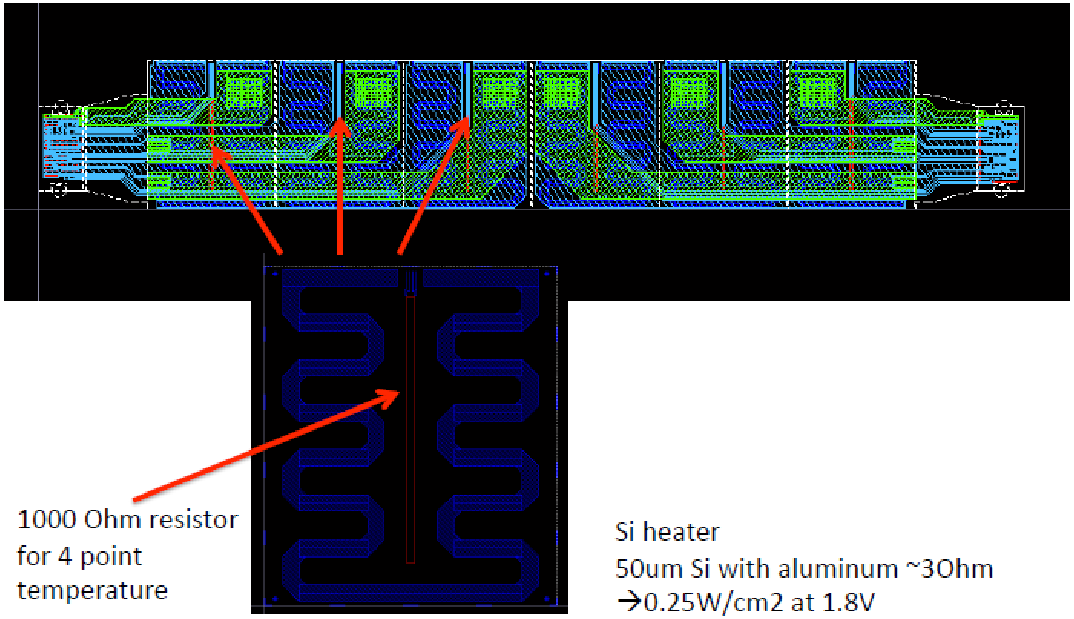
Thermo-mechanical mock-up (2)

Two types of modules will be built

II. “silicon heater” modules: 2-layer LTU Al-kapton flex, 50µm steel dummy-chips Silicon chips with resistive traces. Connected using SPTAB bonding.
  - Model for electrical services: number of lines slightly larger than for final detector module. Number of traces

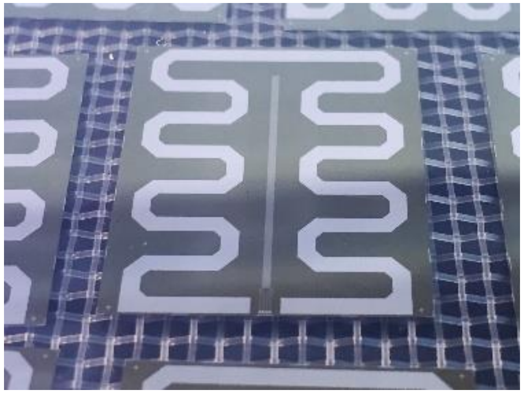
Layer 1&2 Ladder

H-C Kaestli (PSI)



1000 Ohm resistor for 4 point temperature measurement

Si heater
50um Si with aluminum ~3Ohm
→0.25W/cm2 at 1.8V

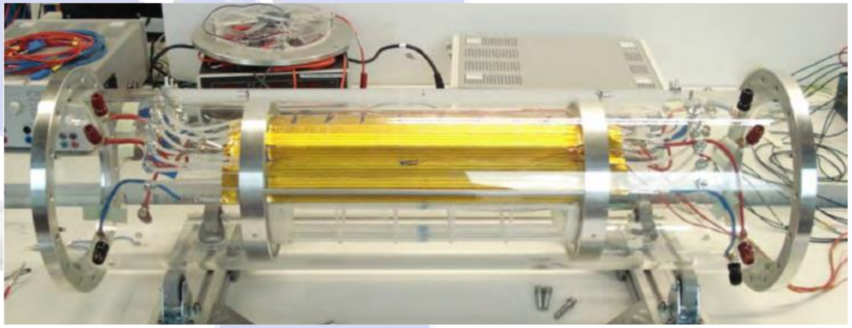


Silicon heater chips thinned to 50 micron.

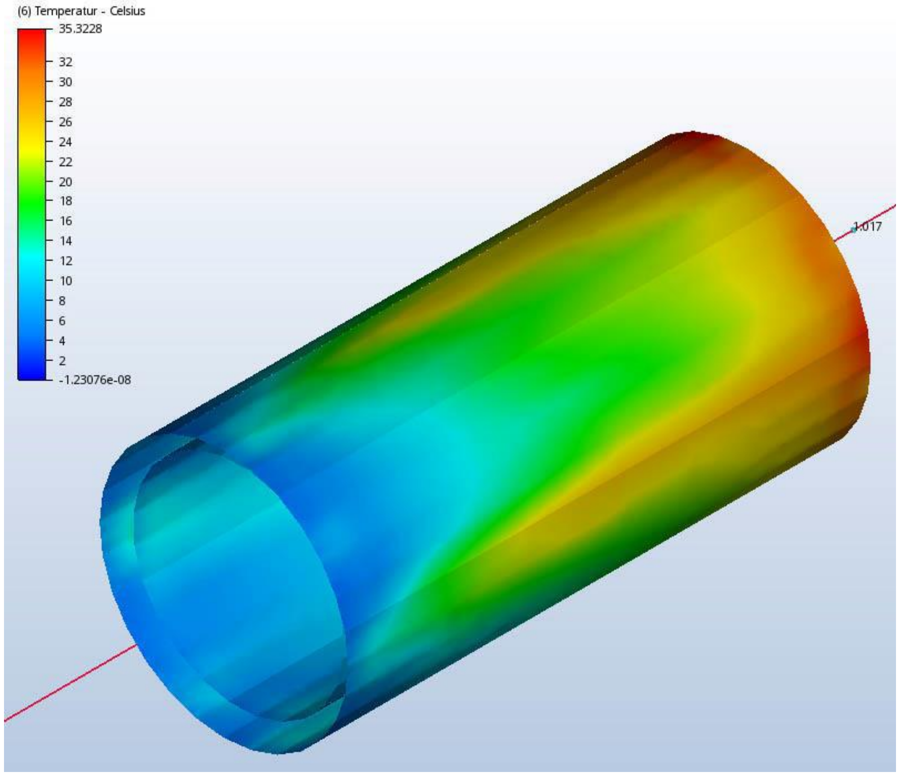
Thermo-mechanical mock-up (3)

Ultimate goal is to fully equip a mock-up of the central section of Mu3e dissipating ~1 kW (~250 mW/cm^2) and cool with cold gaseous helium.

1. Verify the cooling model and the simulated temperature gradients
2. Use as a test-bed for the cooling system controls (and to verify its simulation).



Set-up for cooling tests. *Heidelberg*



Thermal simulation Mupix.

Mu3e can live with a substantial temperature gradient, (most recent simulation ~35°C).

- CMOS sensor can generally operate warmer than hybrid sensors.
- Momentum resolution is scattering dominated
- Modules are spring mounted to absorb thermal expansion of few hundred microns.

Towards MuPix construction

Mu3e construction schedule:

- First Mu3e MuPix detector modules/half-shells with will be produced starting Q3 2019 with expected arrival first detector compatible chip, MuPix10.
- Central detector in place in 2020 and phase-I re-curl sectors added in 2021

MuPix construction:

- Assembly of thermo-mechanical test stand is used finalise and qualify the production tooling and processes for the inner and outer MuPix layers
- Work to prepare for QA and flex circuits has started. A programme of probing a large number of MuPix8 chips is now starting. This will also probing teach us about likely yield for MuPix chips.

In parallel:

- Development of QA procedures and set-ups is progressing in parallel. Critically Mu3e already uses a slice of the full DAQ system for multi-chip operation in the test beam programme.
- Development and prototyping of overall detector assembly tooling (using a rotation cage) has started
- Prototyping of services has started

HV CMOS (AMS → TSI)

MuPix Nik already discussed the MuPix sensor in detail.

- Successful programme with AMS up to MuPix9
- Forced move from AMS h18 to TSI 180 nm.
- Small prototype MuPix7 was already submitted to TSI. Received back very recently, and appears to preform identically to earlier AMS version.
- Mu3e now progressing well towards detector size chip MuPix10

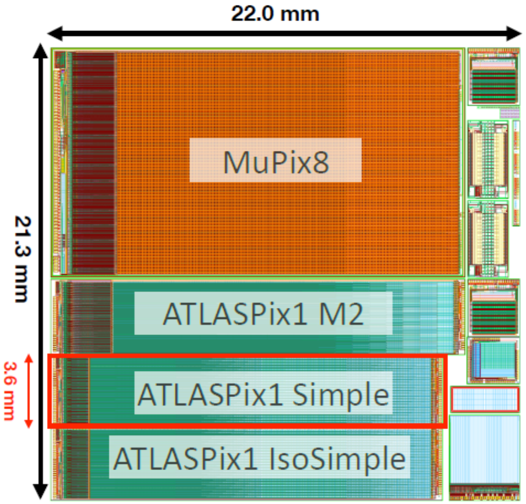
Another development

ATLASPIX (KIT, Geneva, Liverpool, Barcelona, Heidelberg, Bern and more joining)

Chip proposed for 5th barrel pixel layer for ATLAS

(would replace current default hybrid pixel option)

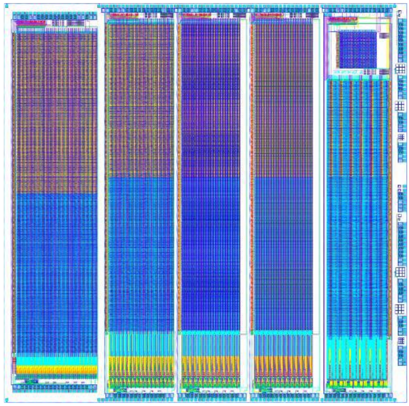
- Compared to Mupix, 130x40 μm^2 pixels with in-pixel comparator.
- Efficiency in test beam ~99.6%. Still good after 2x10^{15} 1 MeV neq
- ATLASPIX2 MPW submitted to both AMS and TSI
- Next step: 2 full size chip submission to TSI in Nov. 2018 and further iteration in Aug. 2019



HV CMOS (LFoundry)

Programme towards HV-CMOS chip for ATLAS ITK upgrade also include prototyping in Lfoundry 150 nm HV process.

LF-ATLASPIX – one submission so far mostly to demonstrate backup technology for ATLASPix (AMS/TSI)

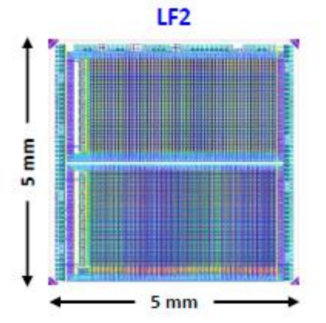


LF-ATLASpix

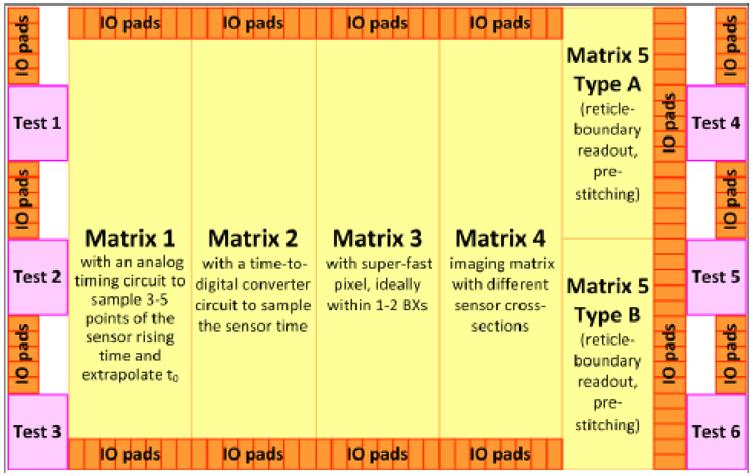
LF-MonoPix another collaboration is developing an independent chip with LFoundry

RD50 collaboration

More R&D oriented programme of HV-CMOS prototype submissions.Focus on radiation tolerance and optimising power consumption, timing performance, S/N, etc. So far 2 MPW submitions. Full size chip foreseen for 2019



RD50-LF2
50x50 μm^2
Analogue and digital electronics integtared



Test structure 1	Simple CMOS capacitors to study oxide thickness
Test structure 2	10 x 10 matrix of very small pixels with passive readout
Test structure 3	10 x 10 matrix of very small pixels with 3T-like readout
Test structure 4	Small matrix of pixels for TCT, e-TCT and TPA-TCT measurements
Test structure 5	Single pixels for sensor capacitance measurements
Test structure 6	...

Proposed layout full size submission RD50