MuPix7

A fast monolithic HV-CMOS pixel chip for Mu3e

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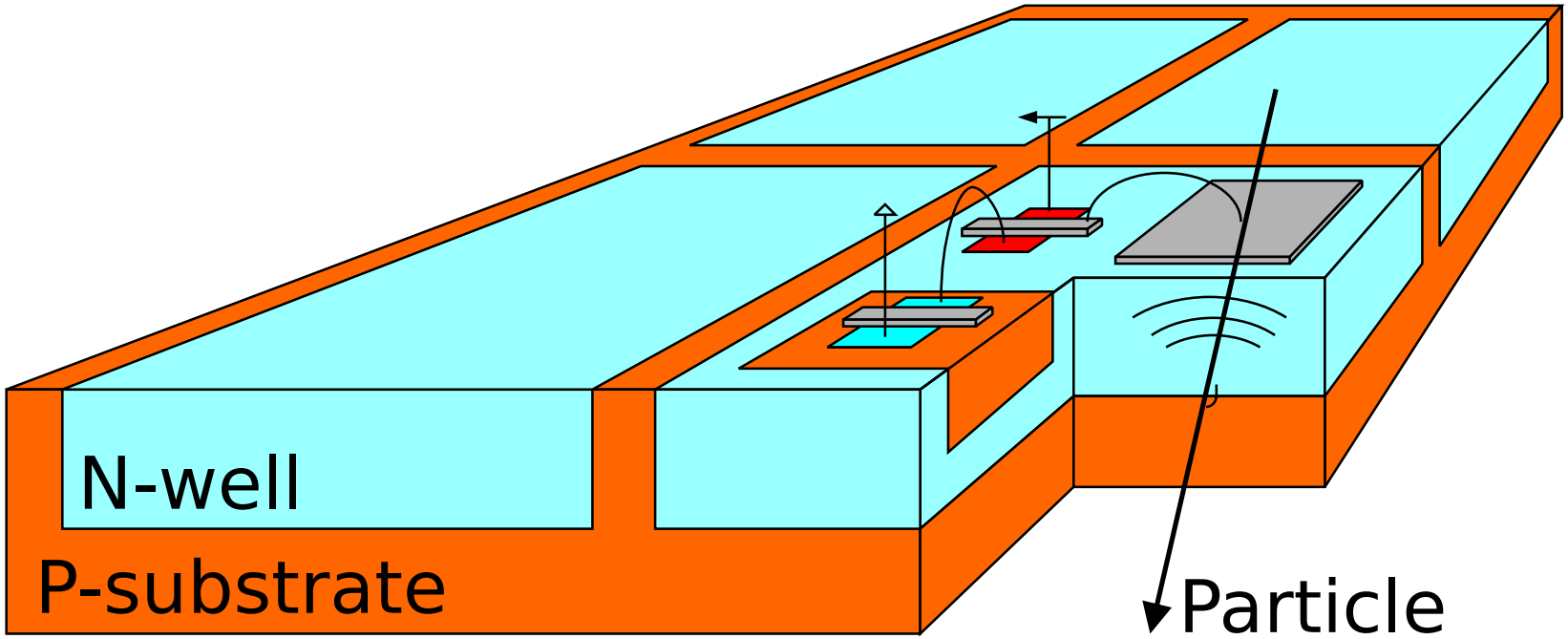
on behalf of the
Mu3e collaboration

Sep 8, 2016

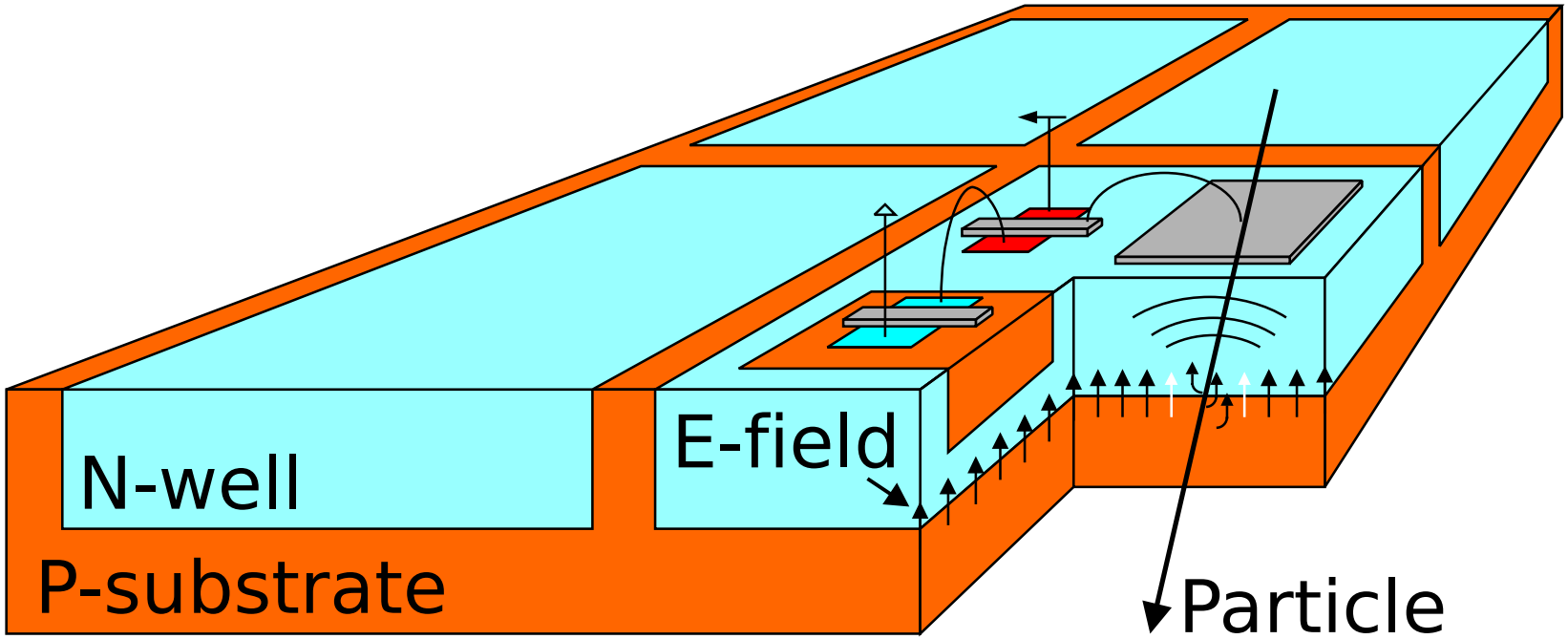
Introduction



Ivan Perić, Nucl.Instrum.Meth. A582 (2007) 876-885

- Analog pixel electronics floats on sensor diode: **monolithic design**

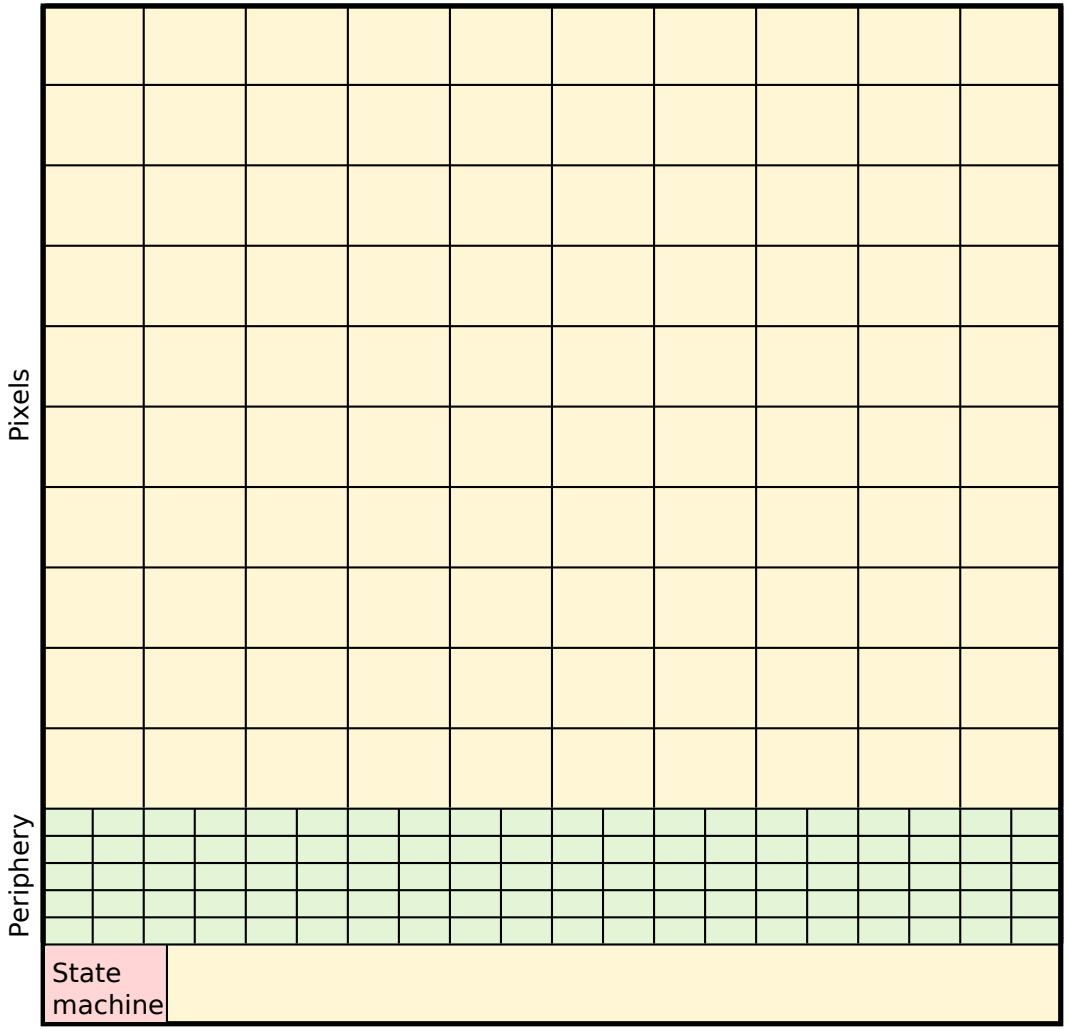
Introduction



Ivan Perić, Nucl.Instrum.Meth. A582 (2007) 876-885

- Analog pixel electronics floats on sensor diode: **monolithic design**
- Industry standard HV CMOS process allows for E-field across diode $\Rightarrow$ depletion zone of about 15 µm $\rightarrow$ drift dominates. Realised in MuPix chips.

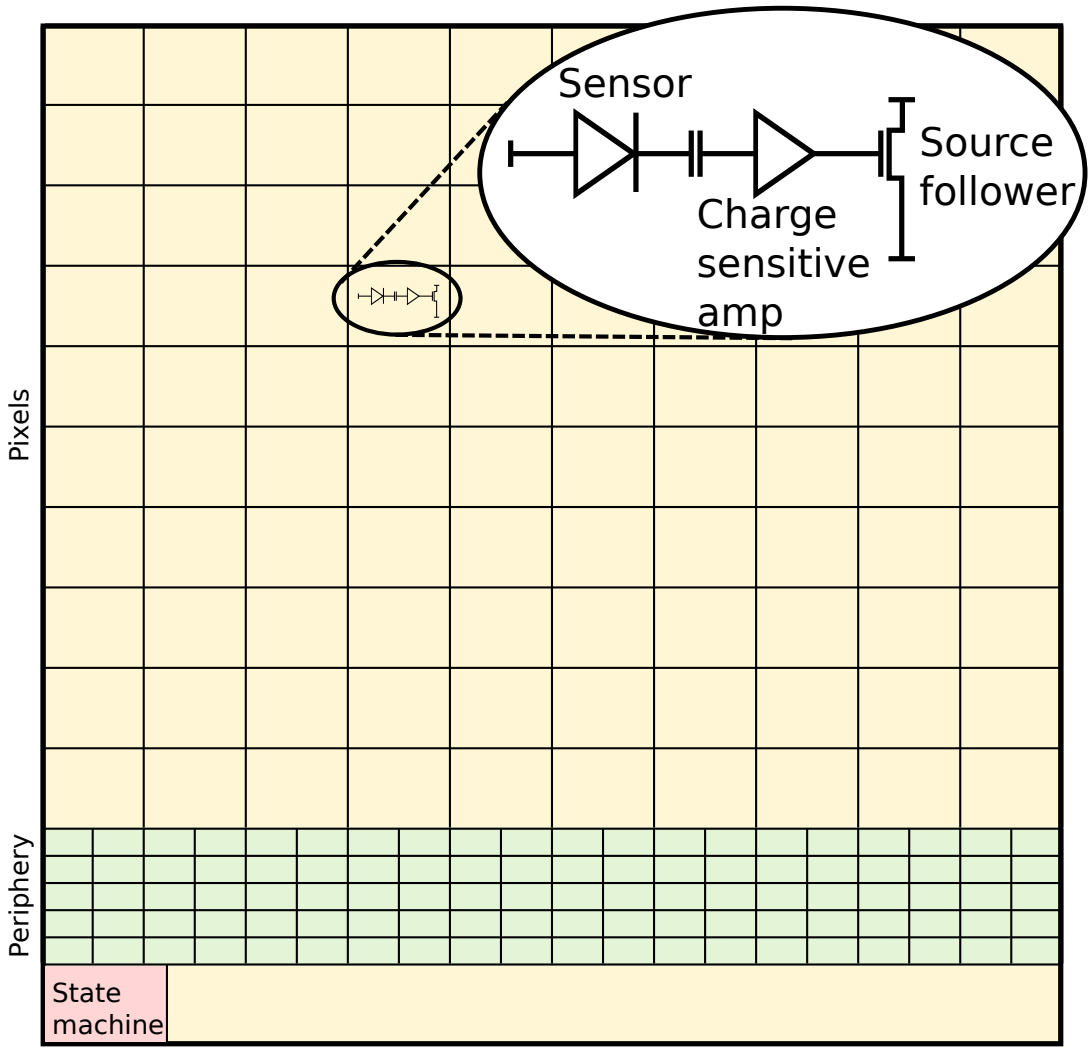
MuPix principle



The MuPix7 chip is a *high voltage monolithic active pixel sensor* (HV-MAPS) and consists of

- Active pixel matrix
- Mirror pixel in periphery
- State machine
- Plus support circuitry (VCO, PLL, etc., not shown)

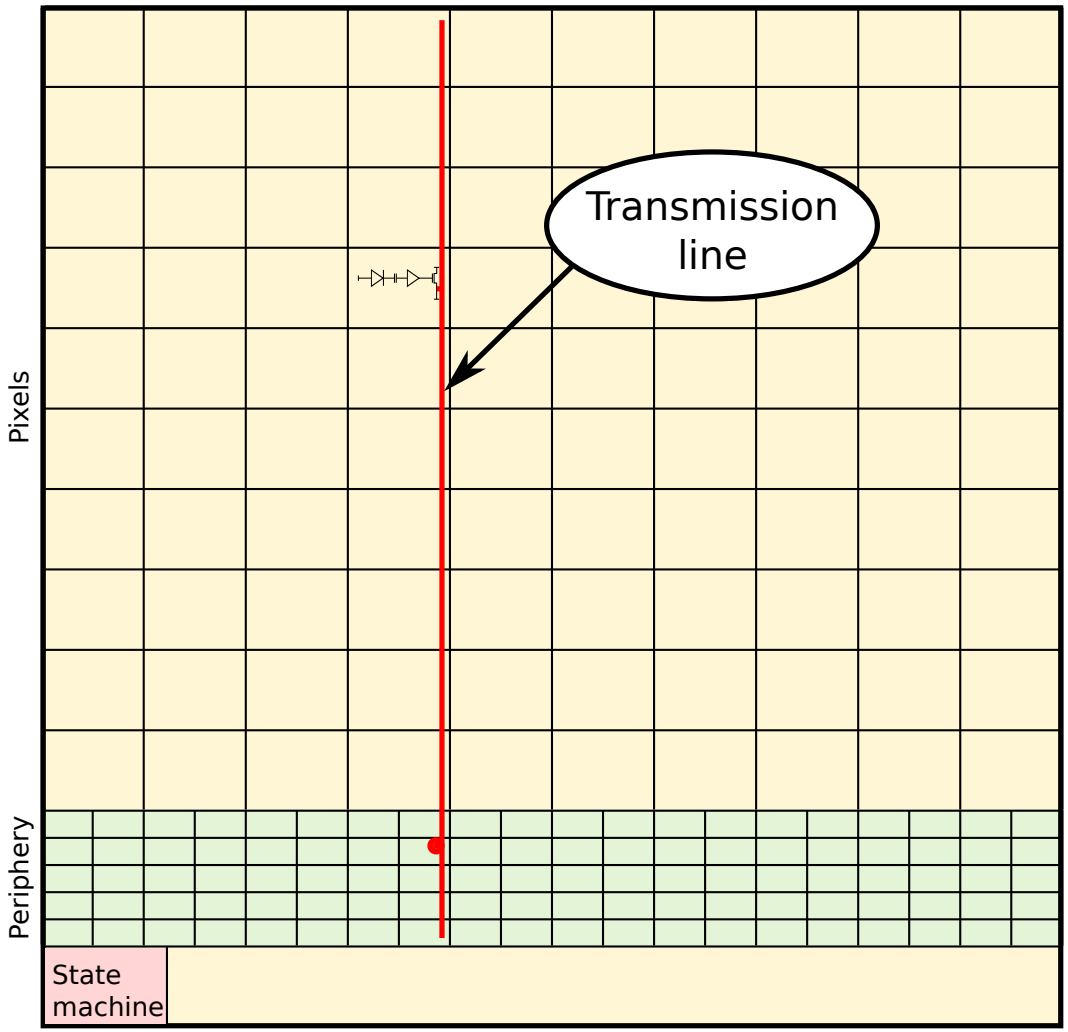
MuPix principle



The **analog cell** has

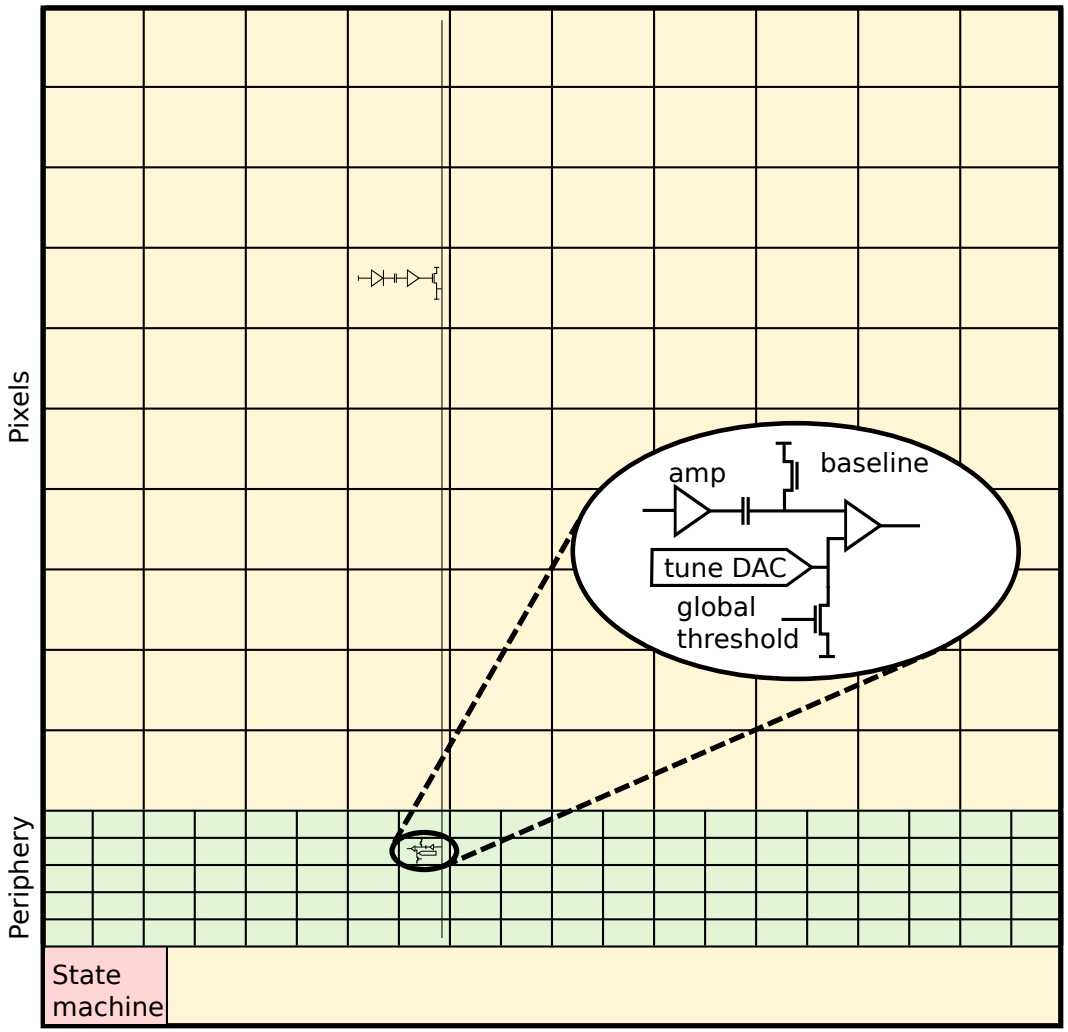
- a reverse biased sensor ($\approx -85\,\mathrm{V}$)
- a charge sensitive amplifier
- a source follower to drive...

MuPix principle



the **transmission line** to the corresponding mirror cell in the periphery.

MuPix principle

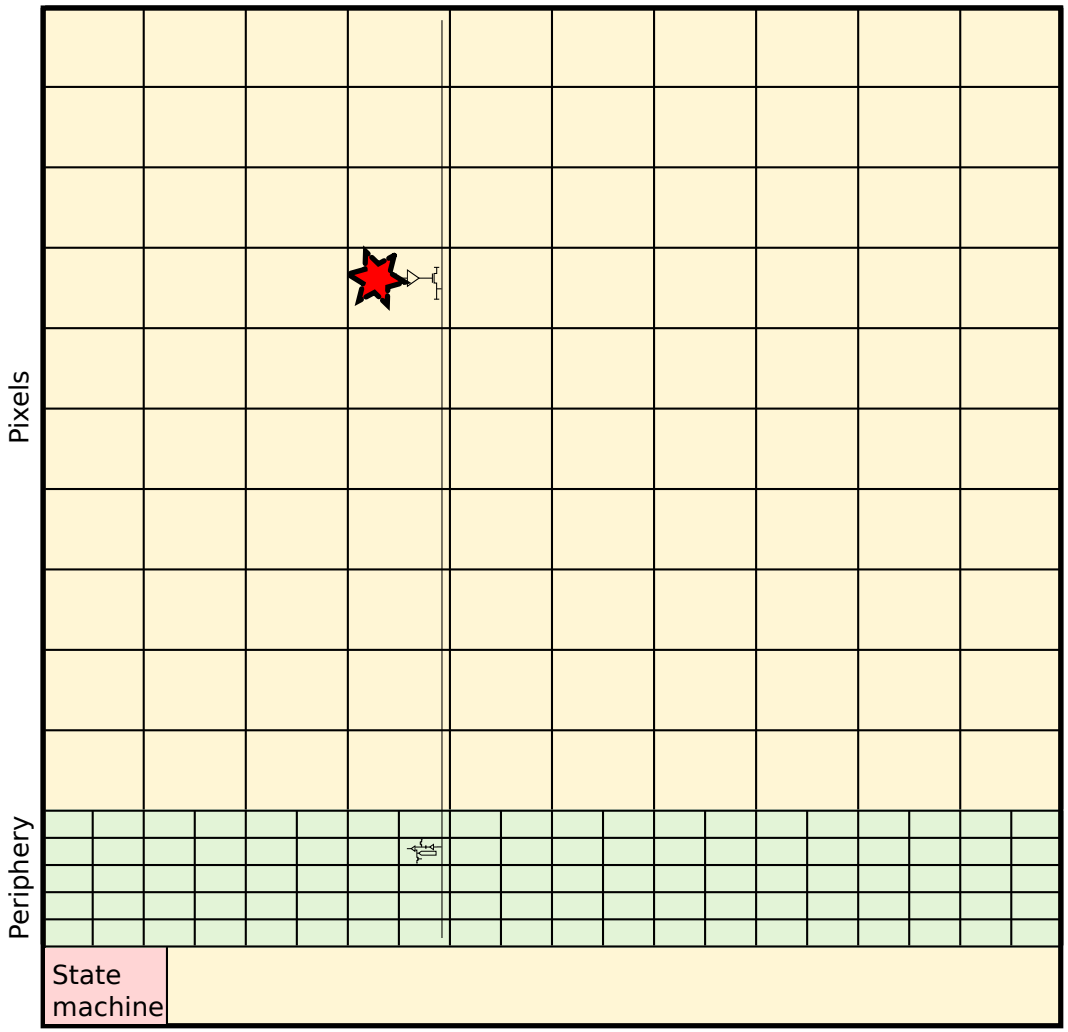


In the **mirror cell**, the transition from analog to digital happens:

- an amplifier
- a comparator
- tuning capabilities

This separation protects the analog cell from digital crosstalk.

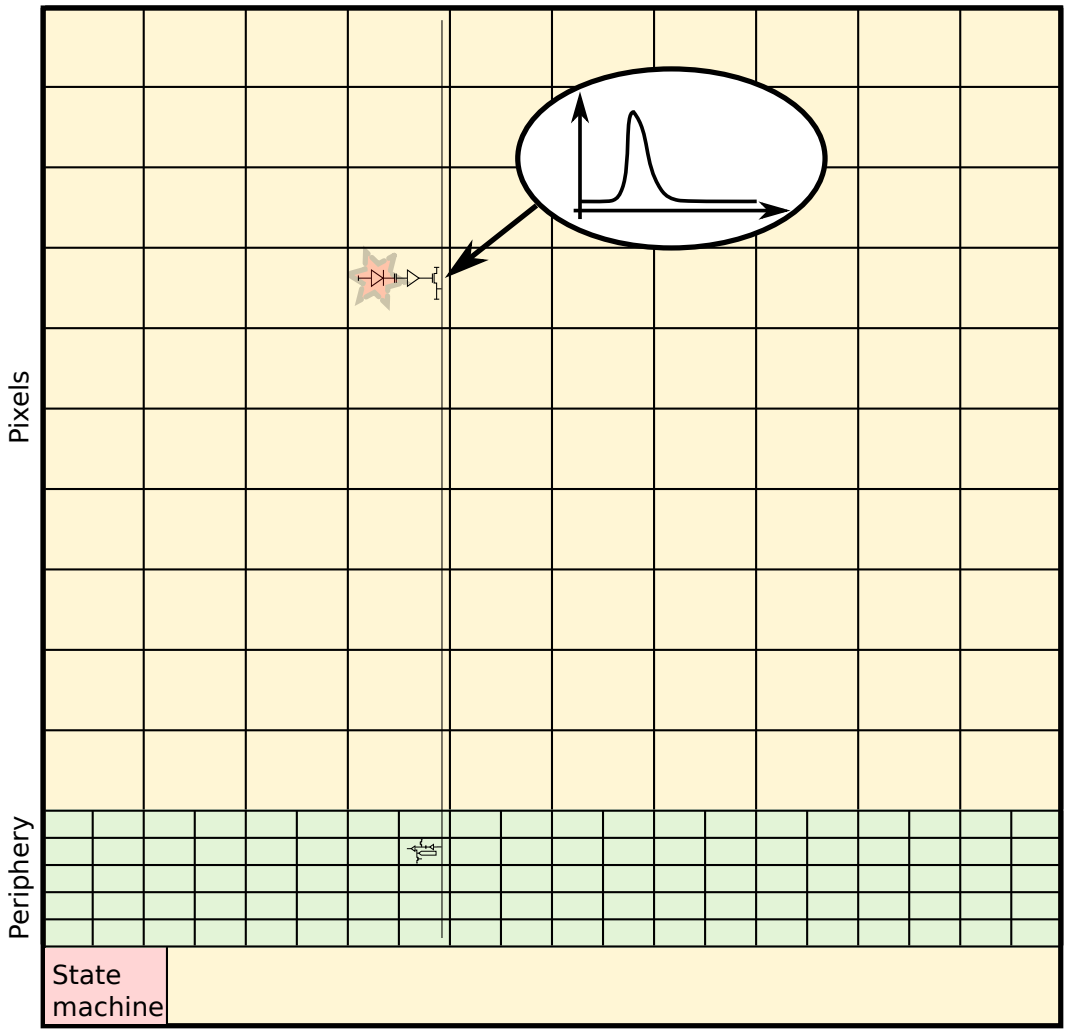
MuPix principle



All this results in a **non-shuttered**, **self-triggered** monolithic pixel chip.

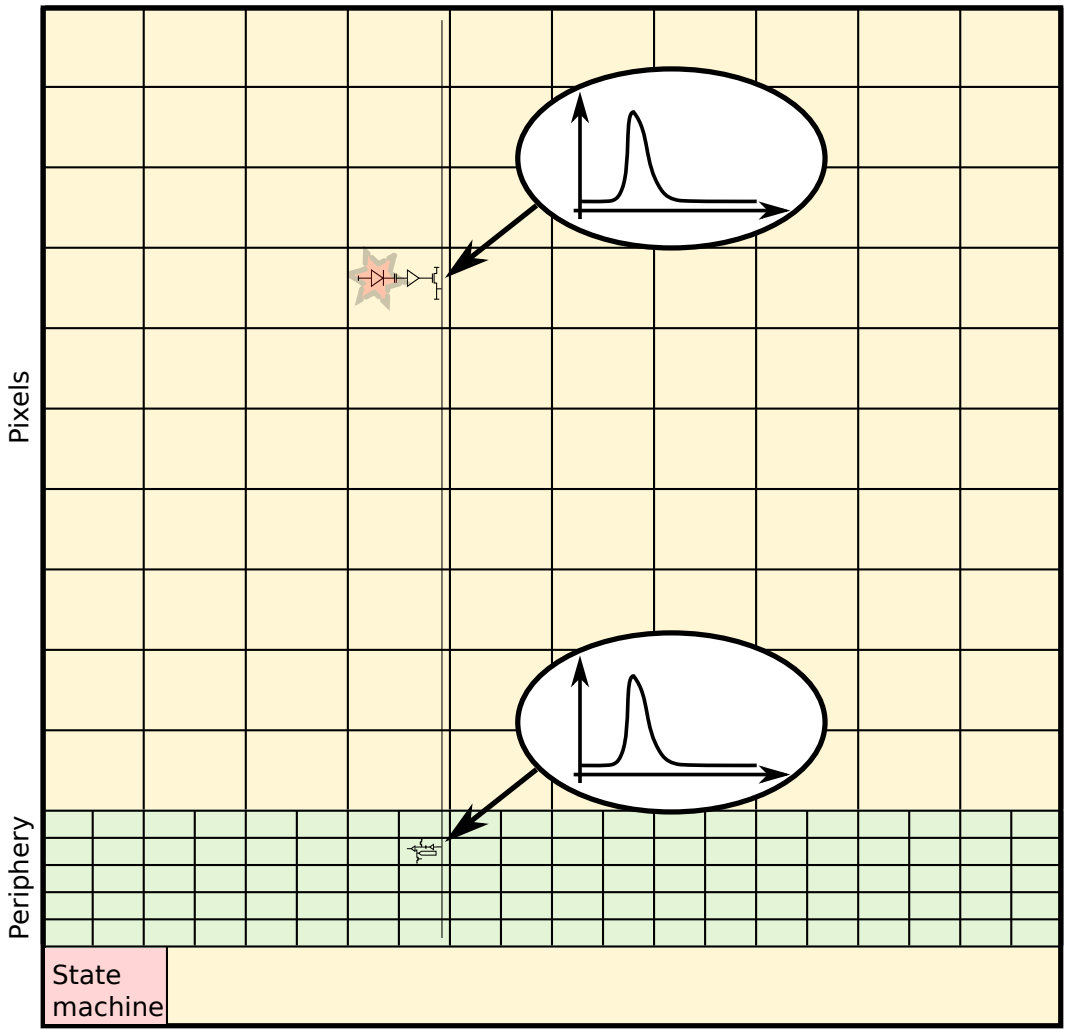
Upon a hit. . .

MuPix principle



. . . the charge sensitive amplifier sends a pulse proportional to the charge. . .

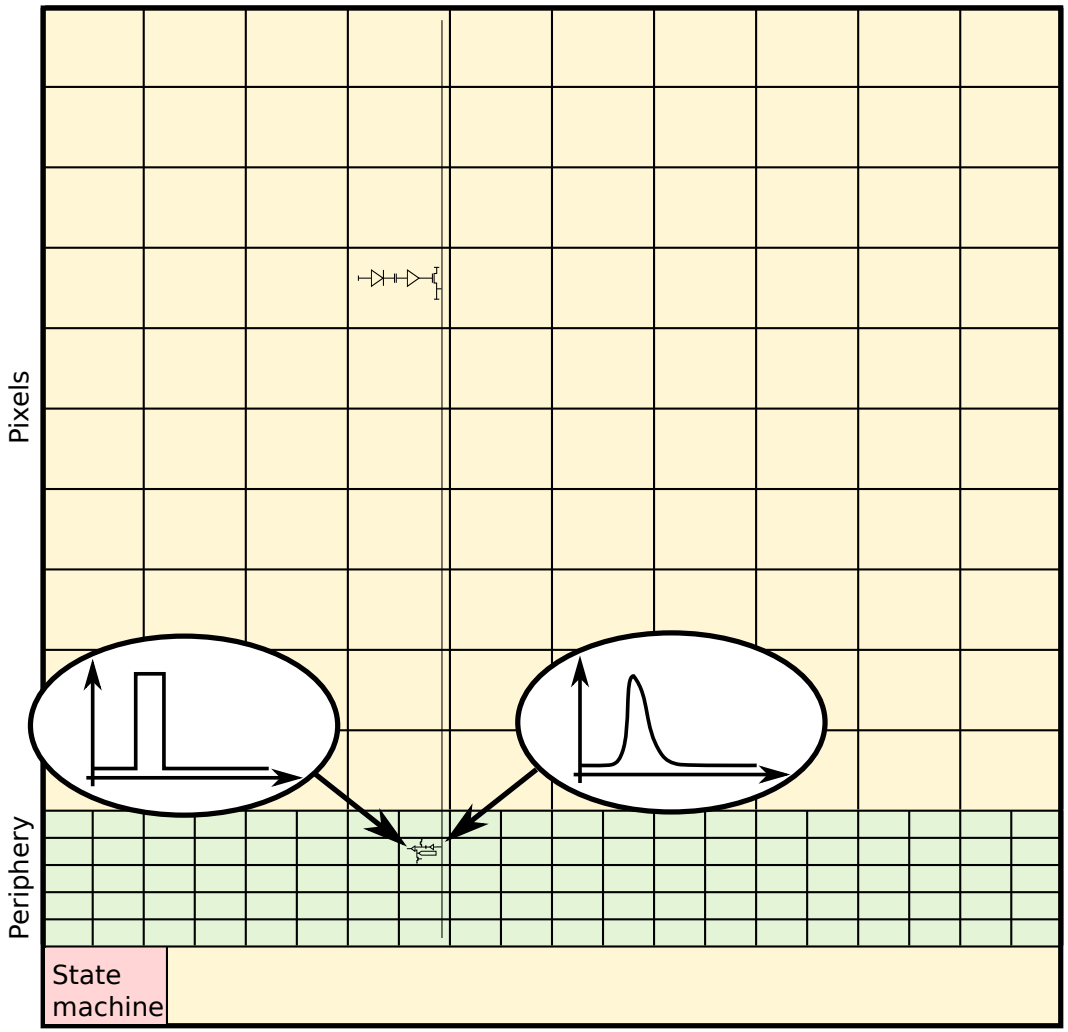
MuPix principle



. . . across the transmission line . . .

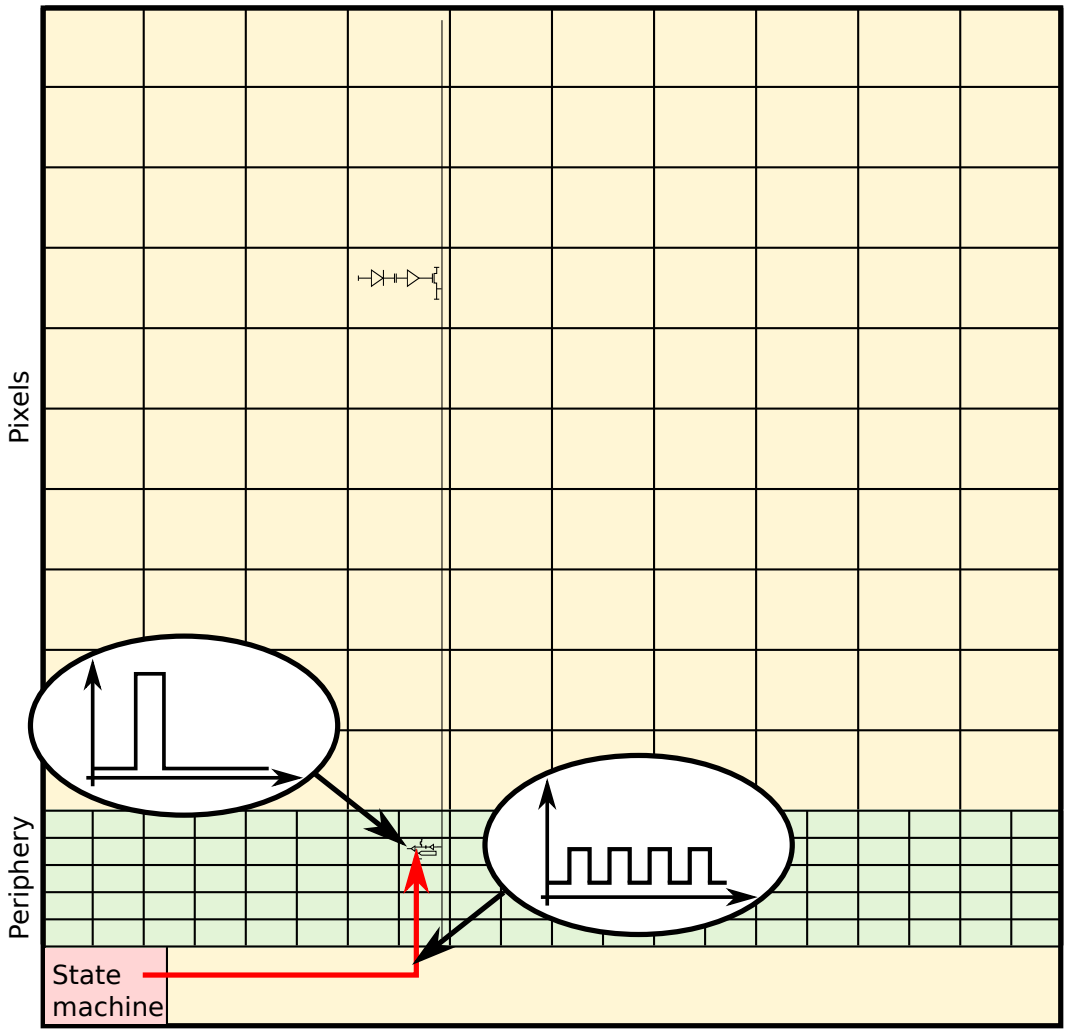
BTW: every pixel has its own transmission line

MuPix principle



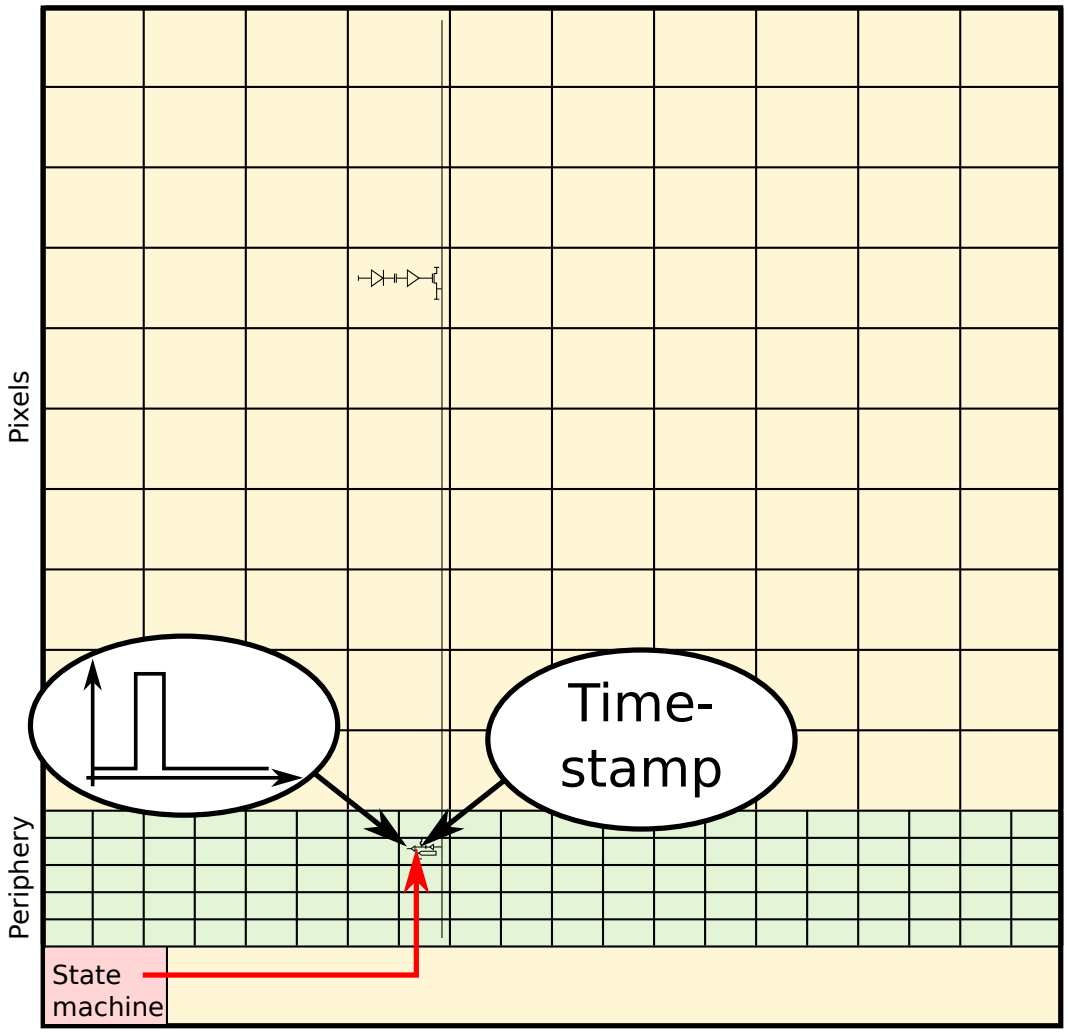
. . . and the comparator in the periphery creates a digital signal, if above threshold.

MuPix principle



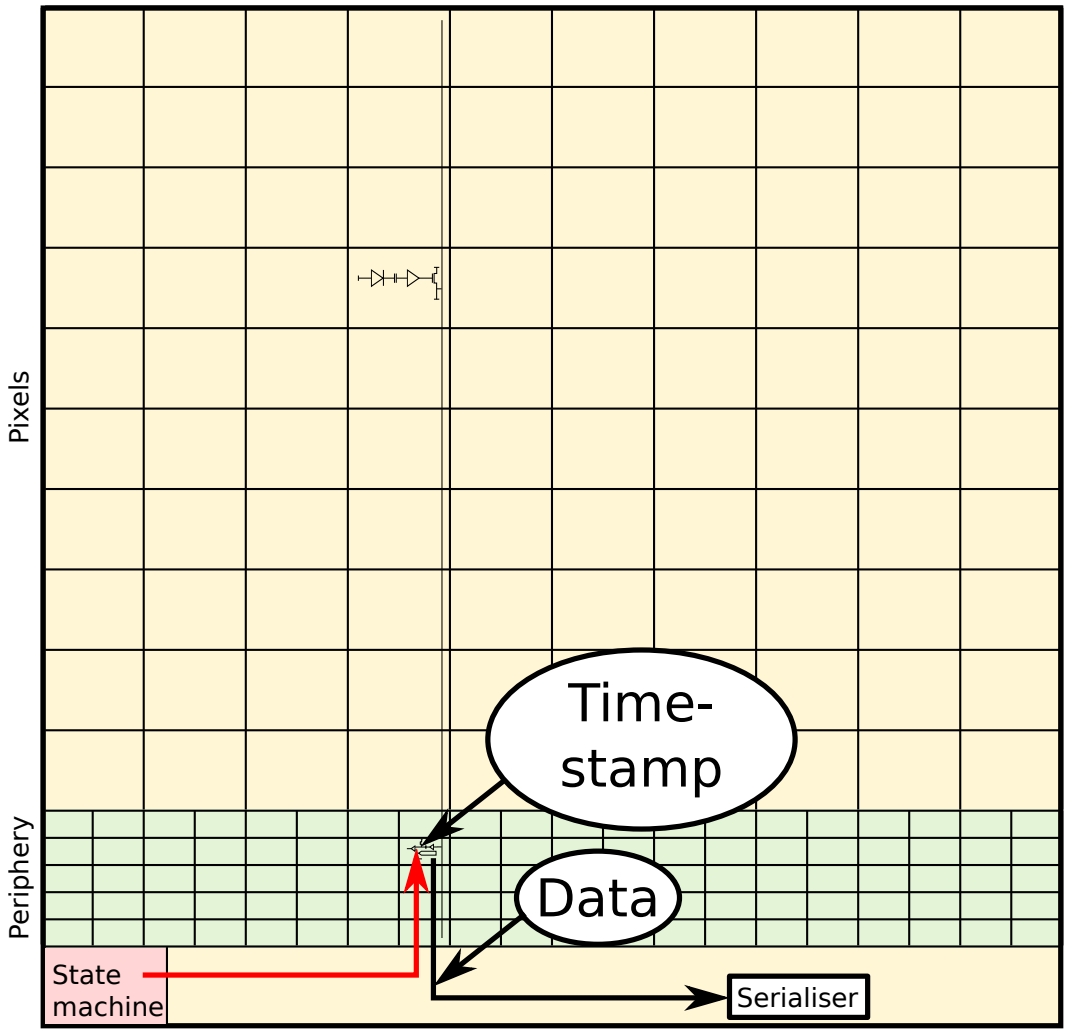
The state machine provides clock for a counter. . .

MuPix principle



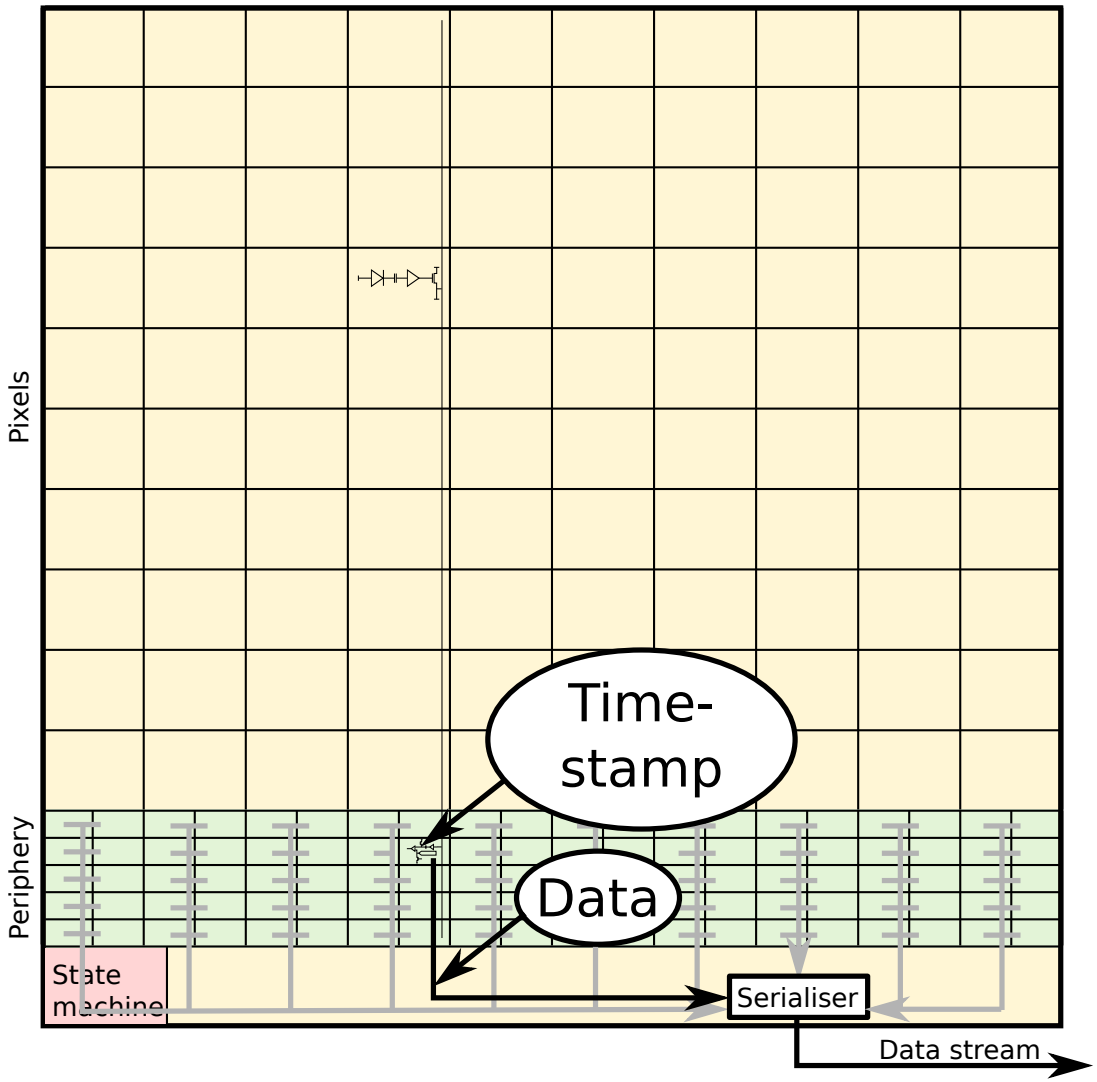
. . . in order to create a timestamp.

MuPix principle

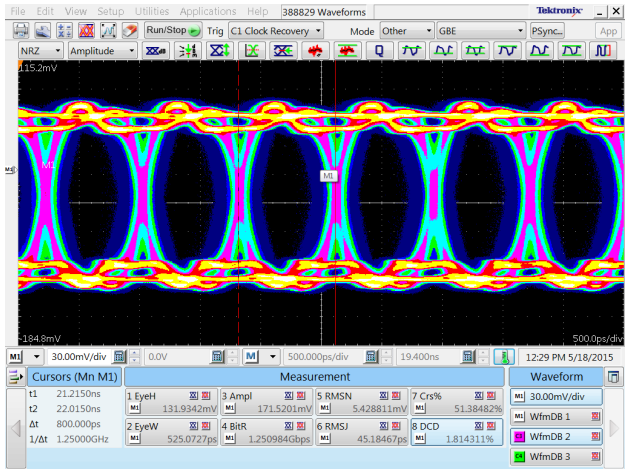


The data (pixel location, timestamp) goes through the serialiser...

MuPix principle

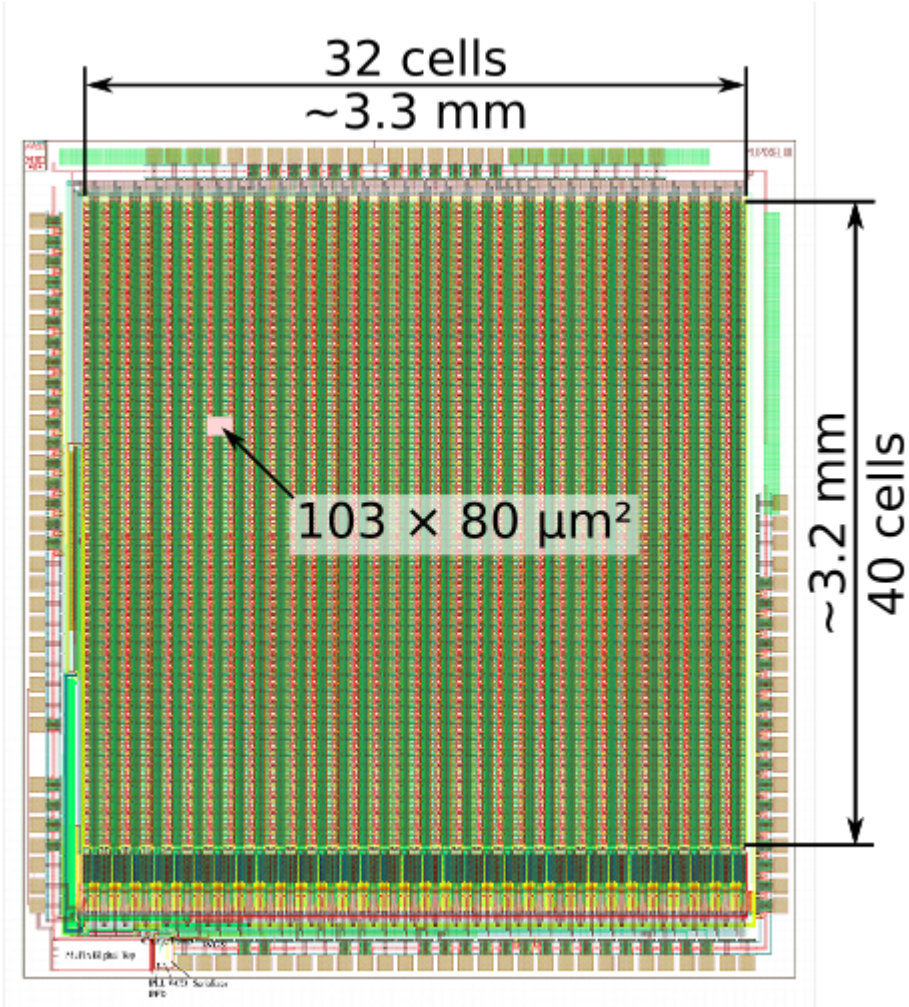


. . . and all the data is transmitted to the data stream at 1.25 Gbit/s.



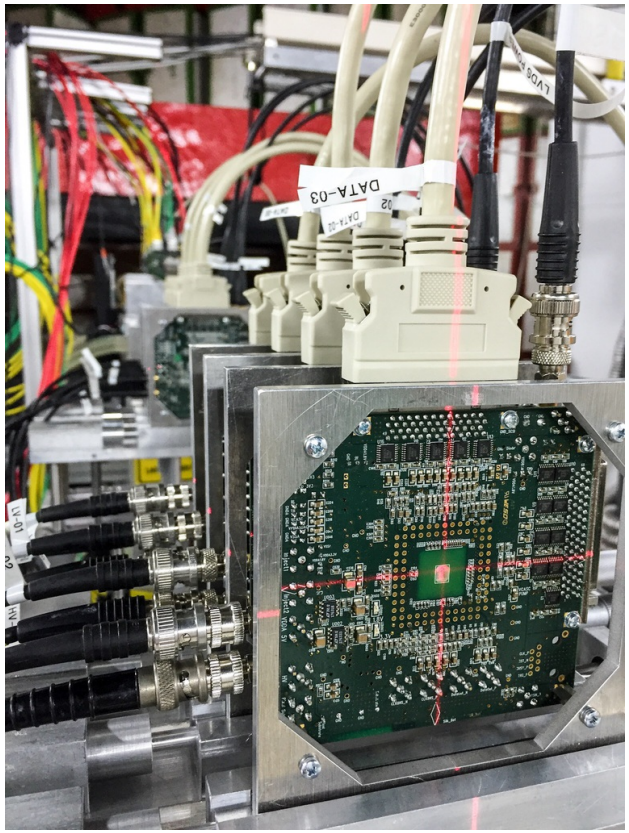
MuPix7

The MuPix7-chip is an implementation of this concept:



- Chip thinned down to 50 µm (nice feature of MAPS)
- Process: AMS 180 nm HV-CMOS

MuPix7: Test beams



Several MuPix7 testbeam campaigns:

- Mainz MAMI, 0.4...1.5 GeV e^-
- CERN SPS, 180 GeV π
- PSI πM1, 250 MeV π^+, μ^+, e^+ mix
- DESY, 4 GeV e^+

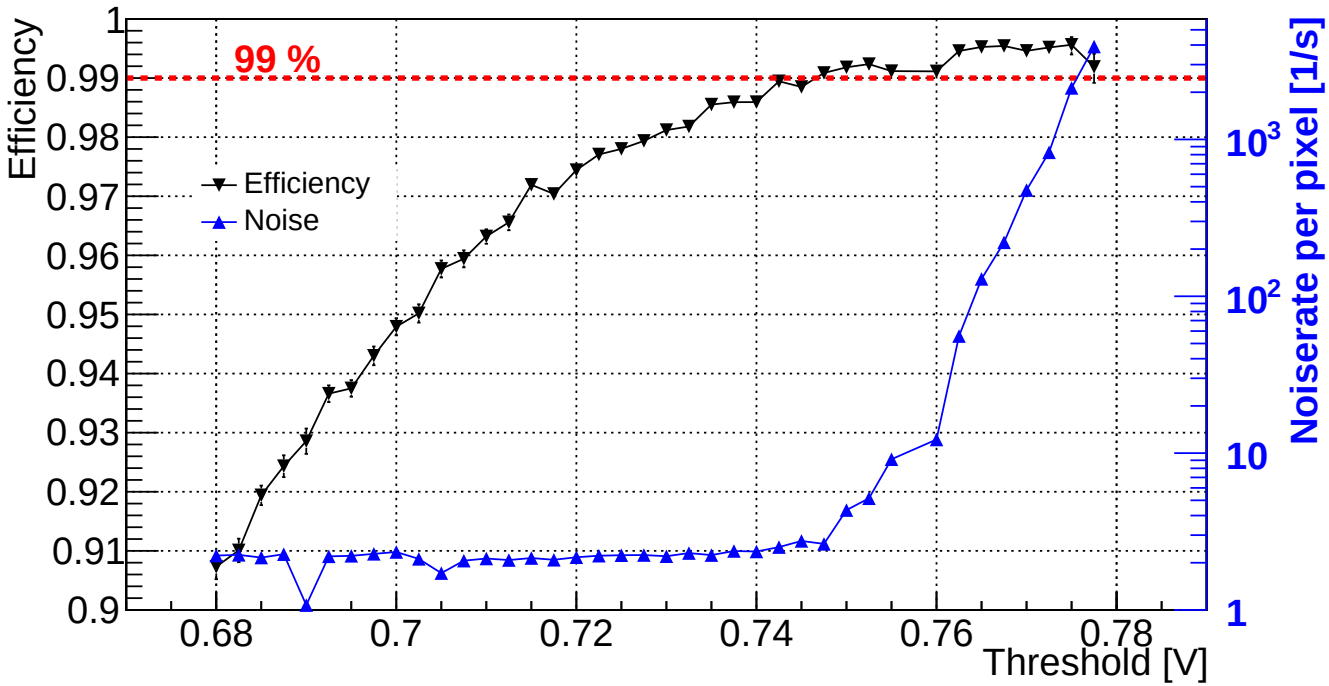
Own telescopes using MuPix7 (in 4 and 8 plane configurations).

At DESY, the EUDET telescope was used as well (MIMOSA chips).

What follows is a selection of results from those campaigns.

MuPix7: Efficiency

Efficiencies of DUT in a telescope:

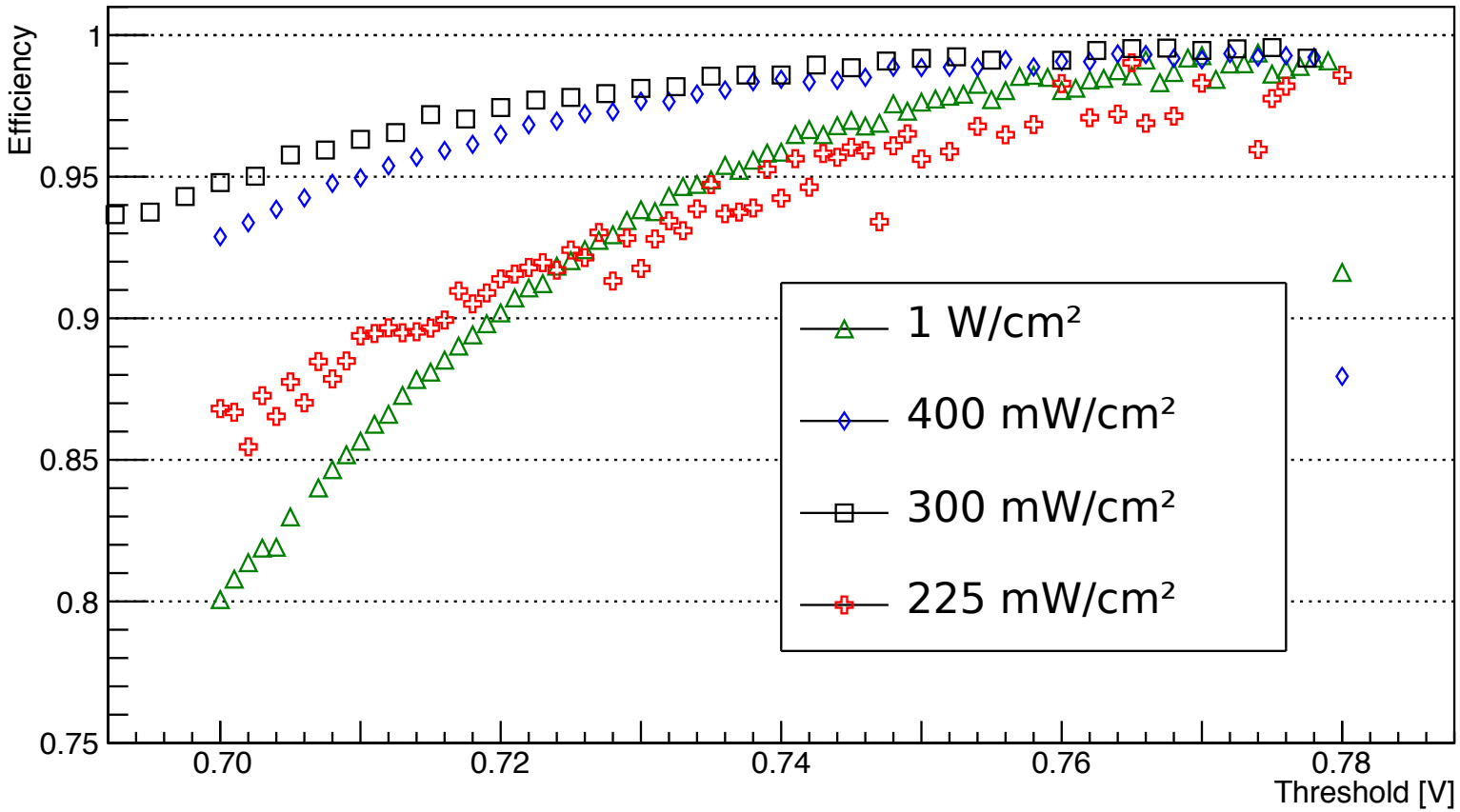


Technique: Extrapolate tracks to DUT. Power consumption: 300 $\mathrm{mW/cm^2}$.

Data taken at PSI

MuPix7: Efficiency

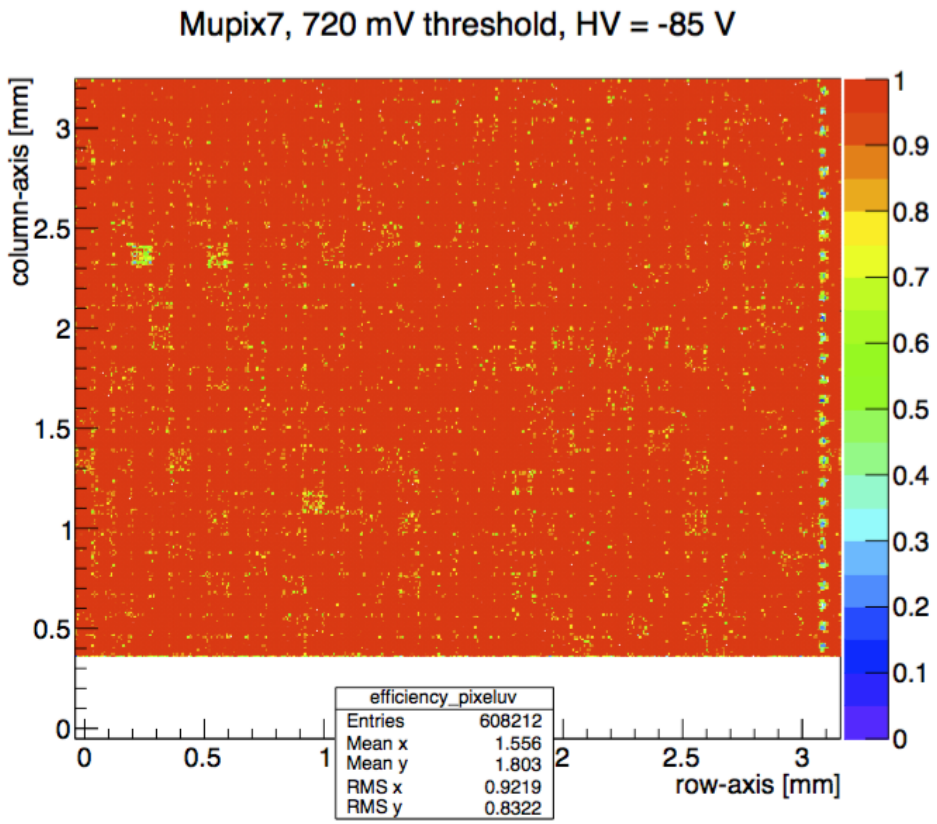
Settings live in a phase space of 13 DACs, hence we tested different tunes:



Data taken at PSI

MuPix7: Efficiency

Here is a pixel efficiency map made with sub-pixel resolution (EUDET telescope @ DESY):

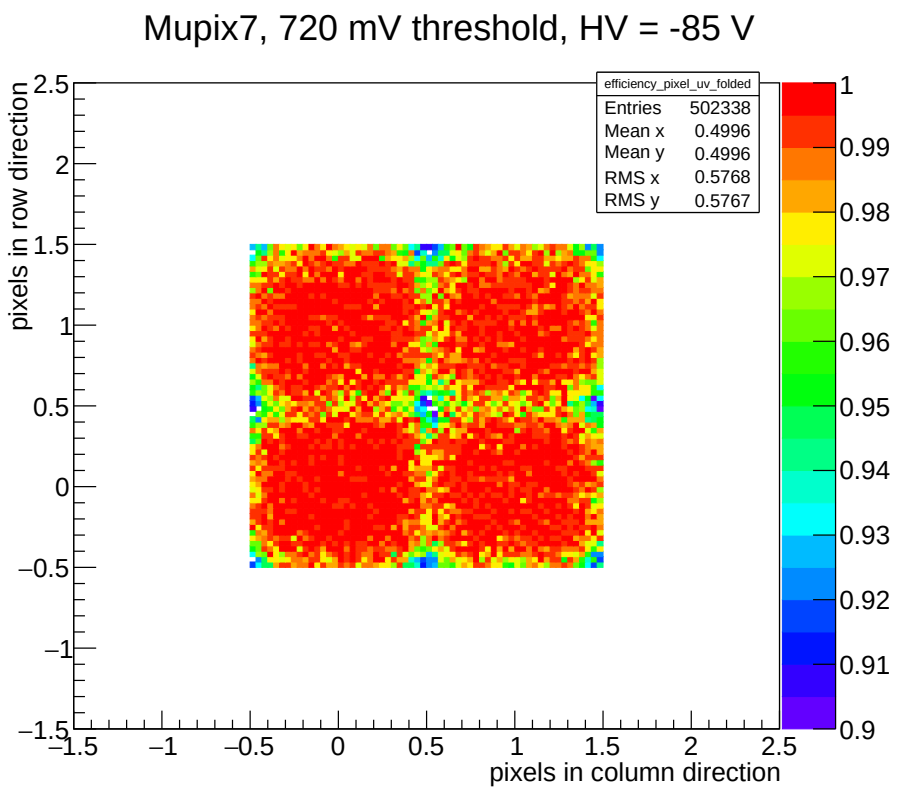


Less optimal threshold used to enhance pixelated structure.

Pixels in rightmost column have different structure, excluded in overall efficiencies.

MuPix7: Efficiency

Same measurement folded into a 2×2 pixel sub-matrix:

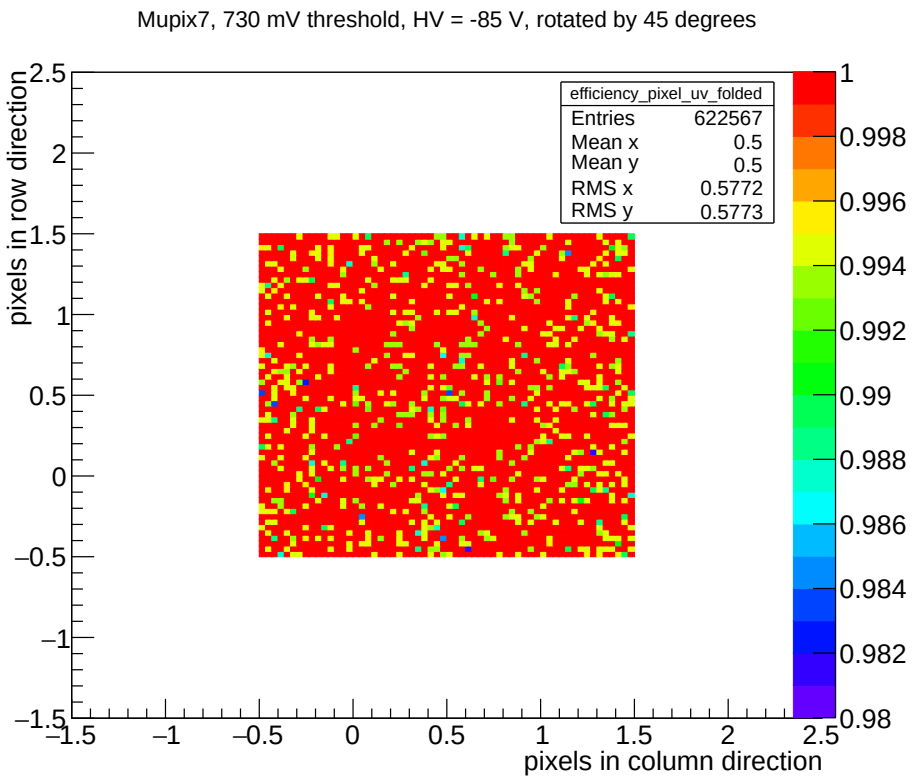


We are inefficient at the edges and corners.

No surprise: Single bit readout with one threshold. In a perfect 4-corner hit, each pixel sees only 1/4 of the charge.

MuPix7: Efficiency

Rotating the DUT by 45° easily increases the depth of the depletion zone by $\approx \sqrt{2}$:



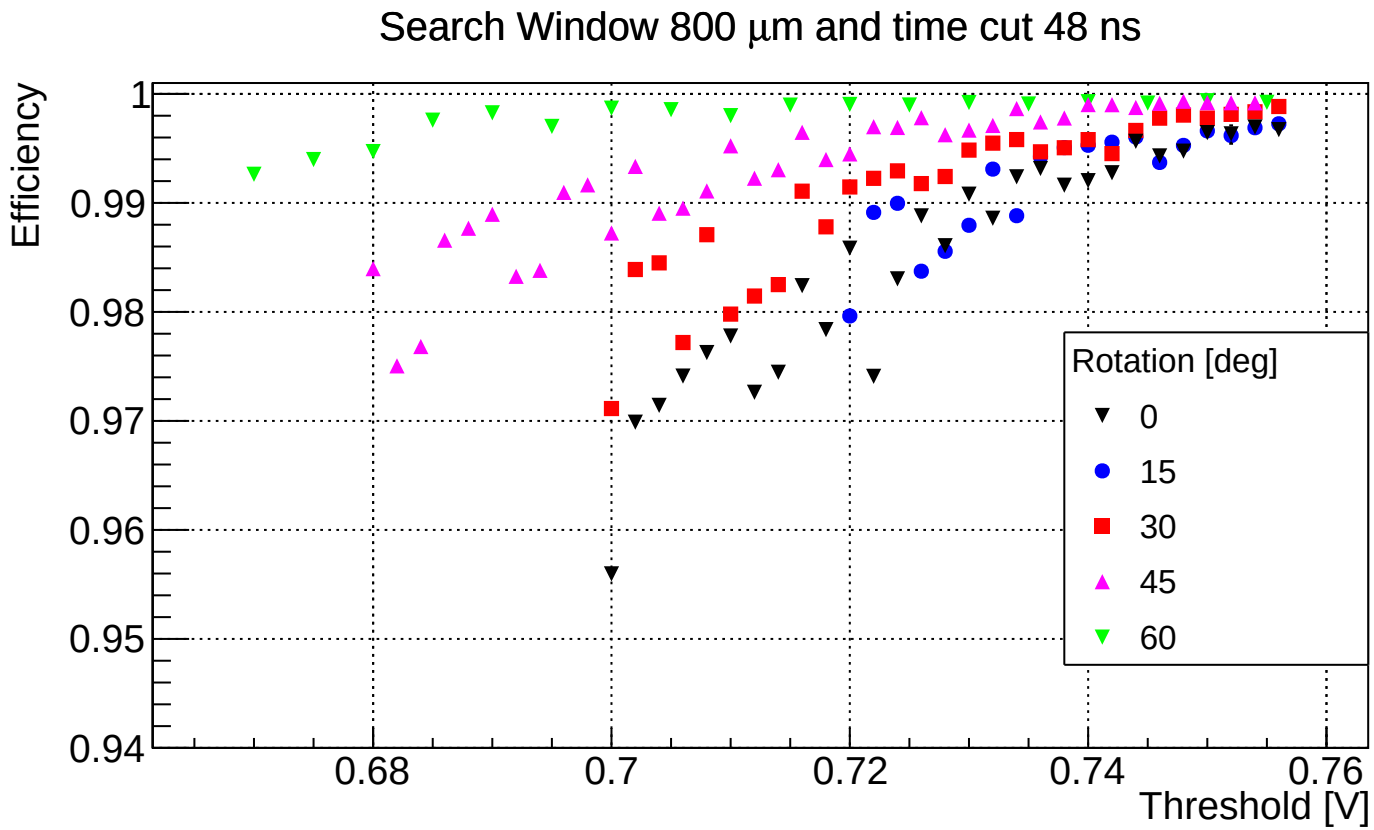
Pixel became fully efficient. Observe the change in scale.

Higher resistivity substrate could be used for mitigation.

Setup:

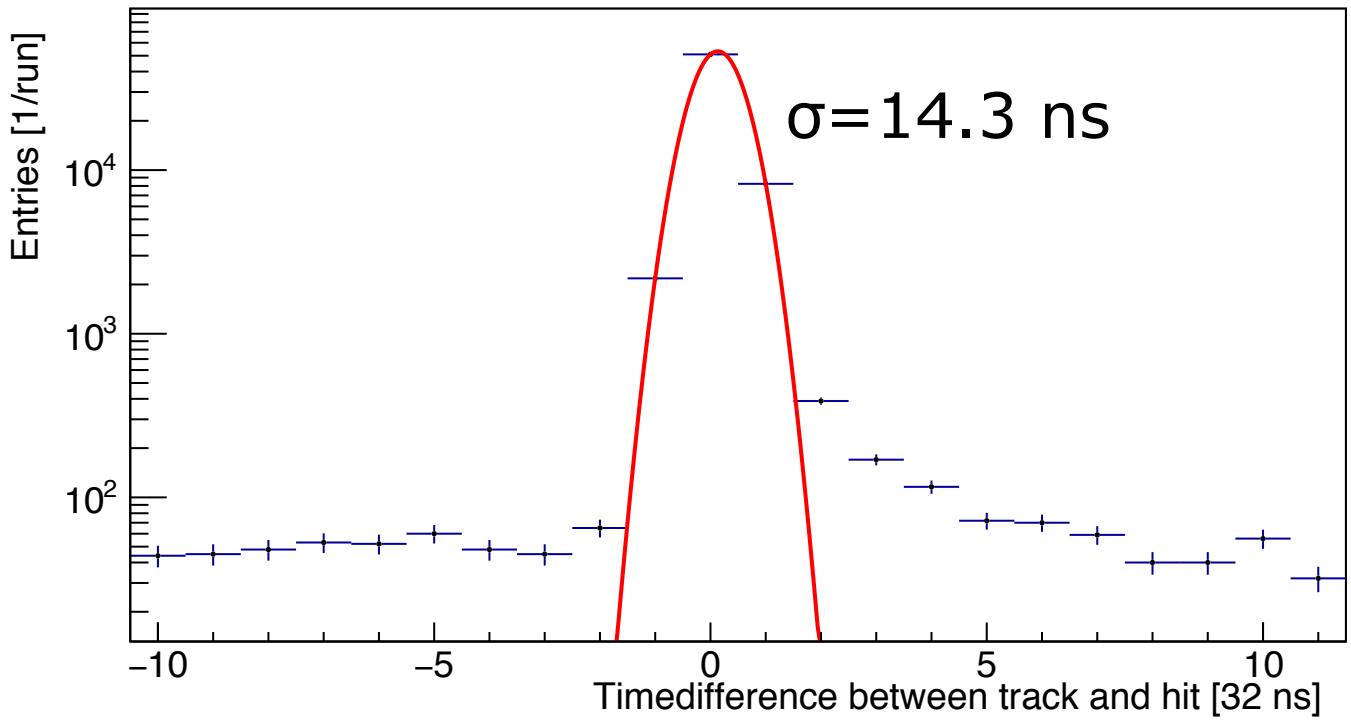
MuPix7: efficiency of tilted sensor

Or for different rotation angles:



Data taken at DESY

MuPix7: Time resolution

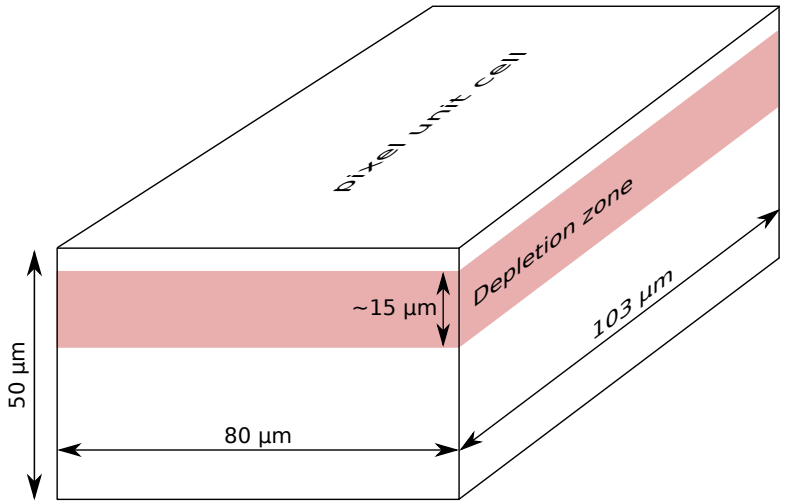


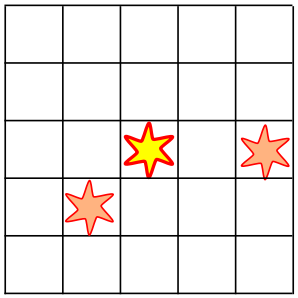
Technique: Scintillator coincidence signal as reference. Plotted timestamp scintillator − timestamp MuPix7 (300 mW/cm^2)
Improvement planned by implementing time-walk compensation.

MuPix7: Crosstalk

We did not see any direct crosstalk between neighbouring pixels, except for charge-sharing.

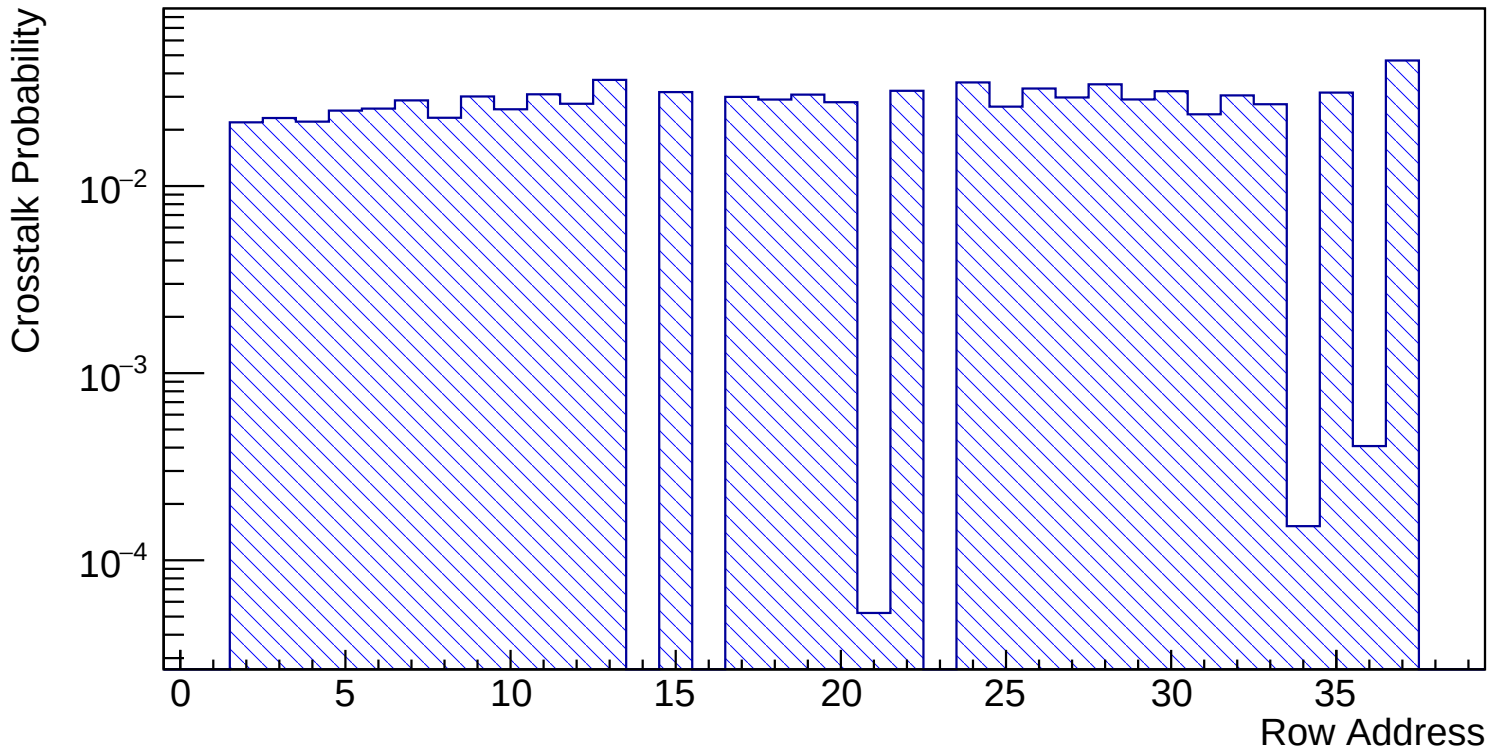
Here, charge sharing is minimal.





But we observed something. If we ask for telescope events with 3 pixel hits in the DUT, one hit on a track, we got crosstalk...

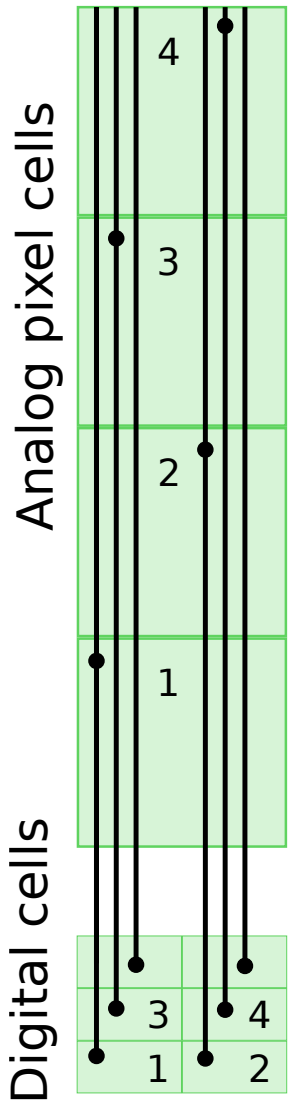
MuPix7: Crosstalk



Histogram shows fraction of events having 3 hits vs. row.

Do we understand the pattern?

MuPix7: Crosstalk



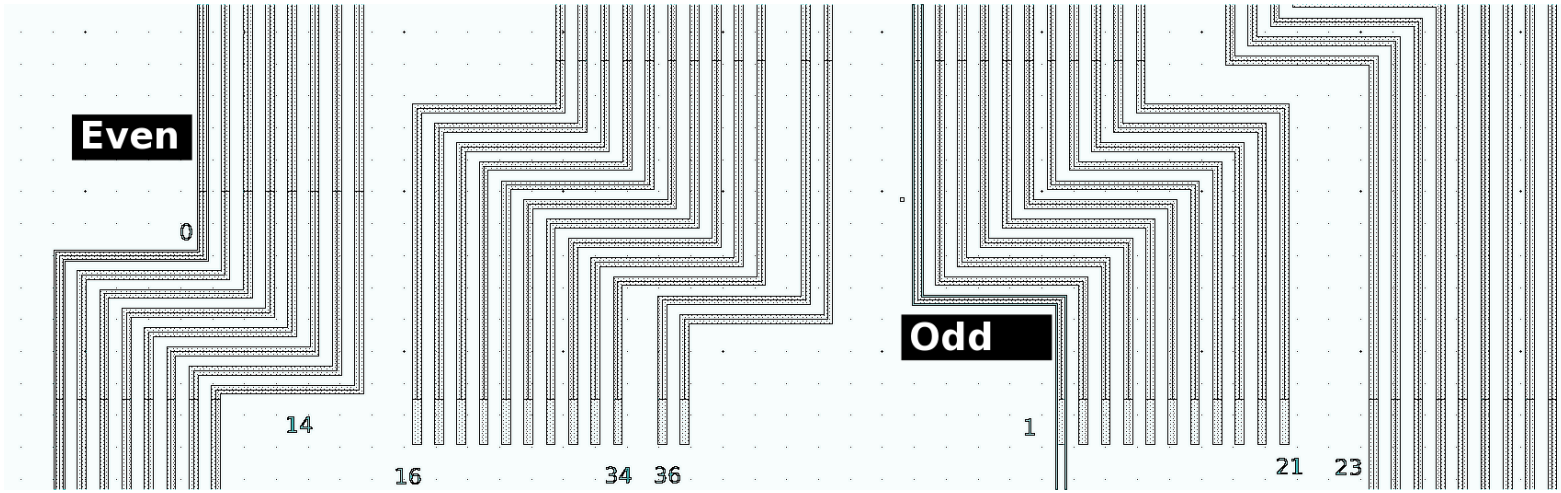
Recall: MuPix has spatially separated analog and digital parts.

Pixel cells (sensor and preamp) are connected **point-to-point** to a corresponding digital cell (comparator, logic).

Long, single-ended transmission lines can couple signals.

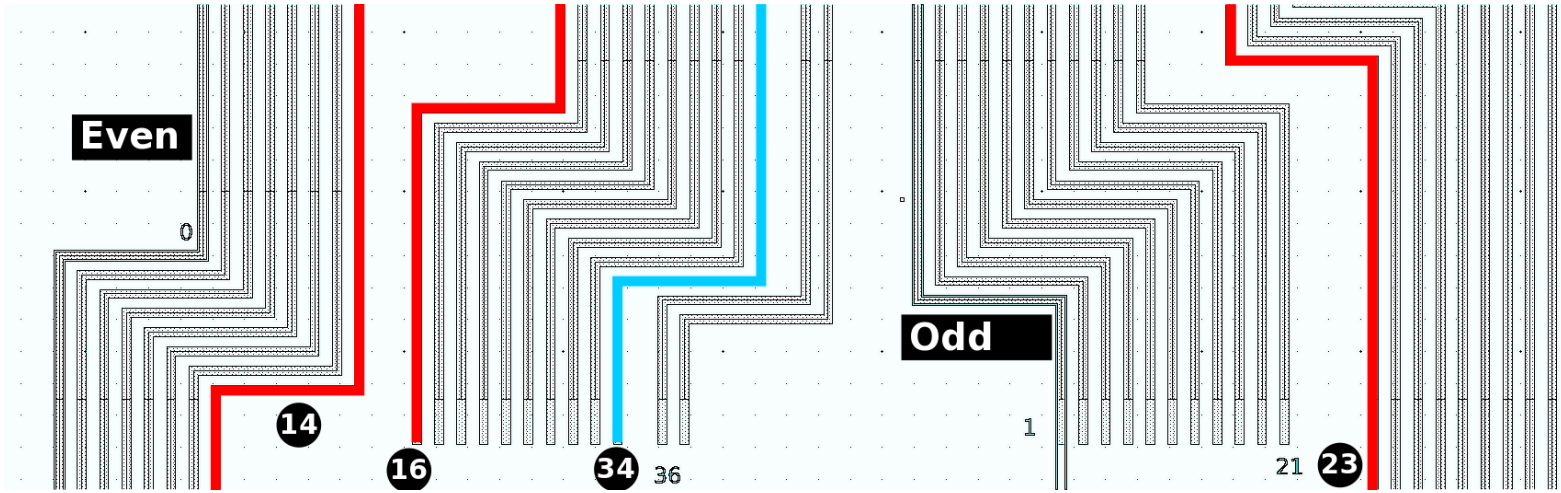
But still: Why the holes in the distribution?

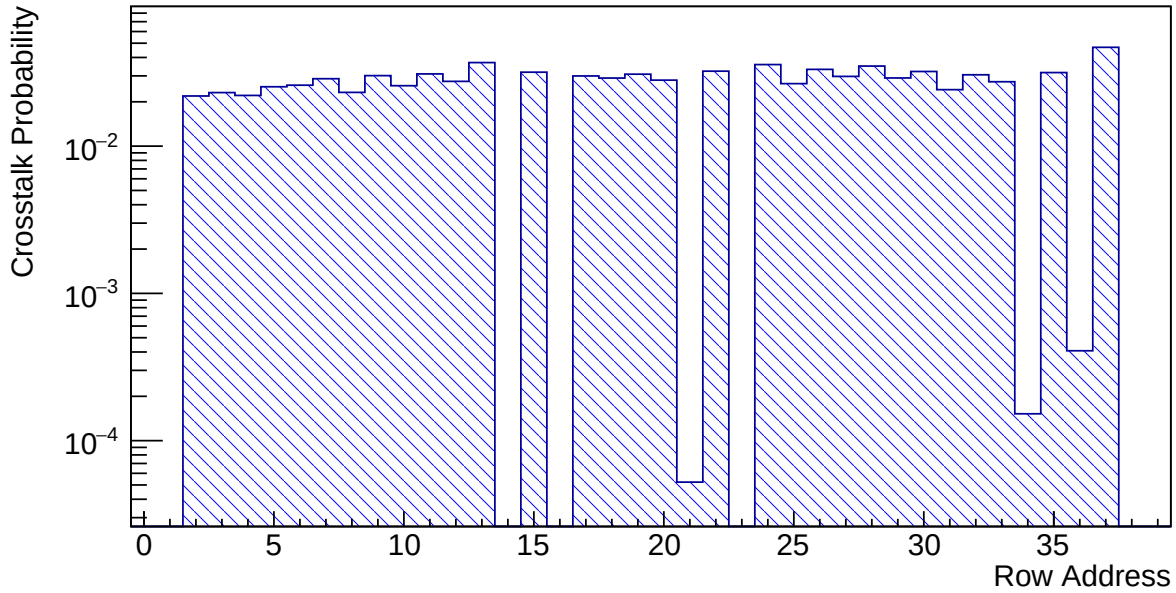
MuPix7: Crosstalk



The space distribution between lines is not uniform. Does the pattern match?

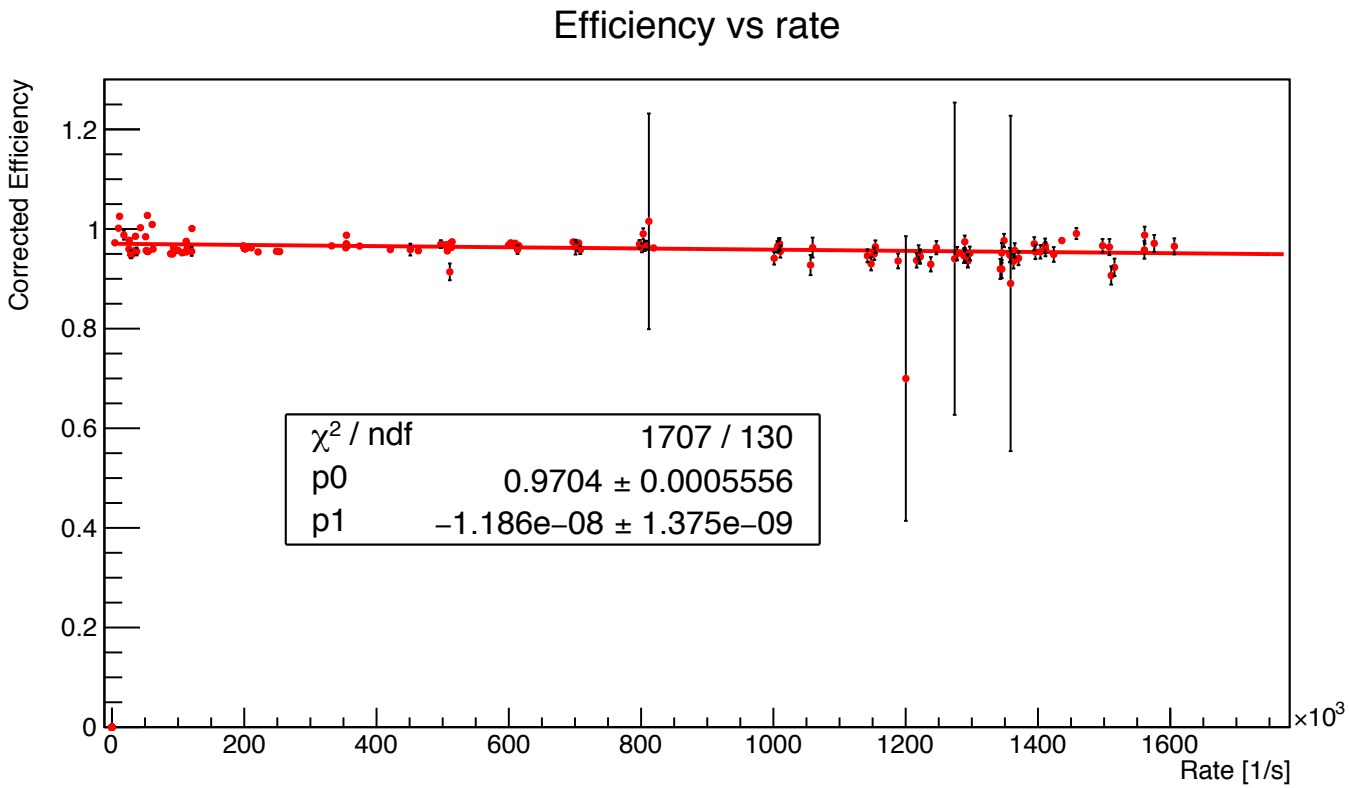
MuPix7: Crosstalk





MuPix7: DAQ performance

Studied rate dependence at **MAMI** using 855 MeV e^- focused on 5×5 pixels.



Rate of $1.6 \times 10^6\,\mathrm{s}^{-1}$ on 5×5 corresponds to $7.8 \times 10^8\,\mathrm{Hz/cm^2}$.
No rate dependence seen.

Note: This tests pixel cell rate. Full chip illuminated at that rate would saturate readout stream, but not pixels itself.

MuPix7

In summary, with MuPix7 we could show:

- We have a **fully functional HV-MAPS chip**, $3 \times 3\,\mathrm{mm}^2$
- **High rate** capabilities of pixel cells demonstrated.
- **Crosstalk** on chip seen (of a special type only).
- We routinely operate systems of up to 8 chips in testbeams reliably.
- More on low-material module design tomorrow by S. Dittmeier (Teaser: 1‰ of X_0 per layer).
- Ready for next step...

Sorry, had no time to talk about the interesting physics and detector design of Mu3e, but check out `https://www.psi.ch/mu3e/`

Towards MuPix8

Goals:

- **Scaling-up** from $3 \times 3\,\mathrm{mm}^2$ to $20 \times 20\,\mathrm{mm}^2$ (active area)
- All **pads on one edge** (required for integration studies)
- **Submission**: September 2016
- Issues addressed:
  - Crosstalk
  - Streamlined slow control
  - Part of chip will feature rad hard design
- Foundry (AMS) now provides **higher-resistivity substrate** ($20\,\Omega\mathrm{cm} \rightarrow 80\,\Omega\mathrm{cm}$). Expect higher signal, hence higher efficiency at edges/corners.

Acknowledgements

- The **Mu3e** pixel team for all the great work.
- The efficiency measurements for several power settings have been performed at the Test beam Facility at **DESY** Hamburg (Germany), a member of the Helmholtz Association (HGF).
- We would like to thank the **PSI** for providing high rate test beams under excellent conditions.
- We owe our **SPS** test beam time to the SPS team and our LHCb colleagues, especially Heinrich, Kazu and Martin.
- We thank the Institut für Kernphysik at the JGU Mainz for giving us the opportunity to take data at **MAMI**.

ENCORE

Mu3e

You may have wondered why we are doing this.

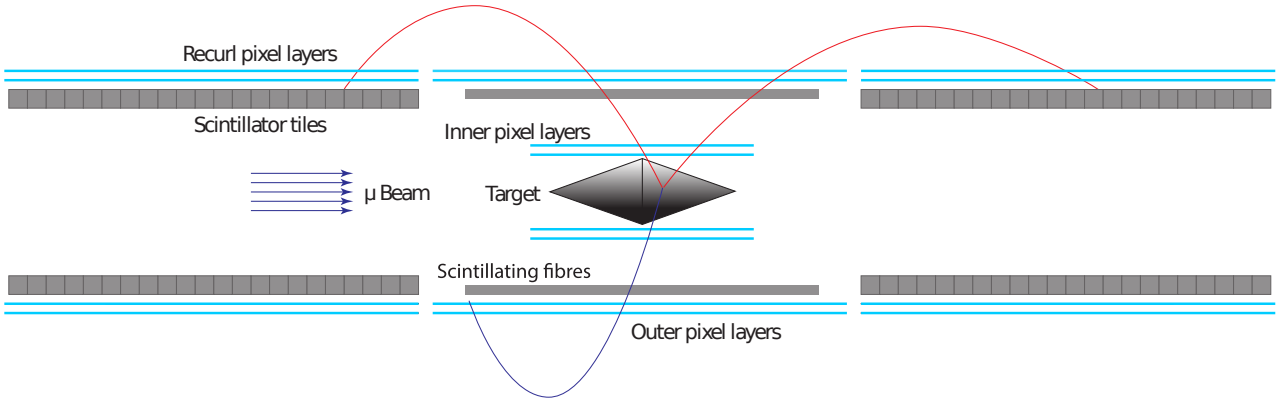
Mu3e

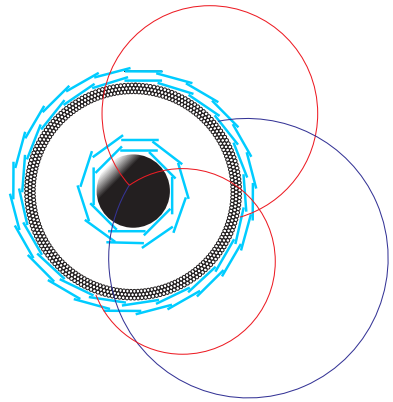
You may have wondered why we are doing this.

Its unique features allow for low-energy high-rate precision physics: **Mu3e**.

Mu3e

The Mu3e experiment, Phase-Ib configuration:





Key requirements:

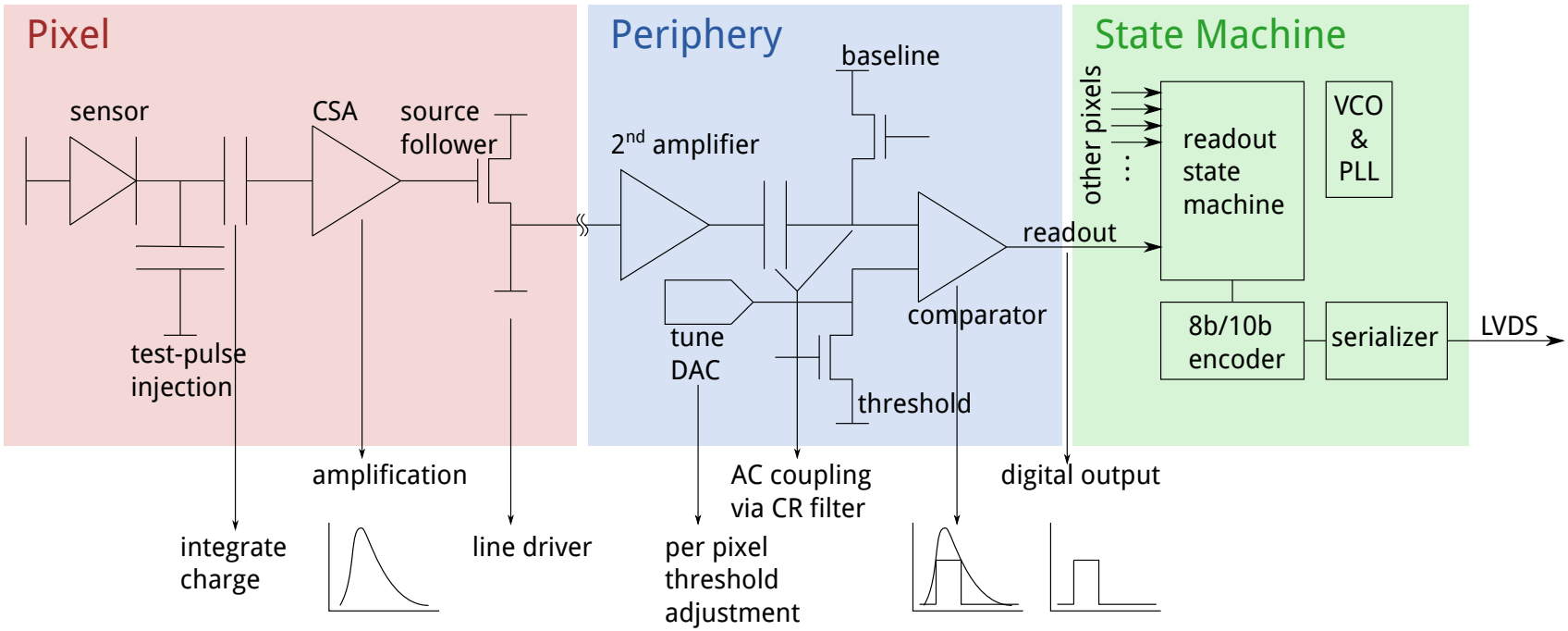
- High rate: 10^8 muon stops on target per second
- Time resolution (pixels): 20 ns
- Vertex resolution: about 200 µm
- Momentum resolution: about 0.5 MeV
- Low material budget: 1‰ X_0 per pixel layer

This translates to the following chip requirements:

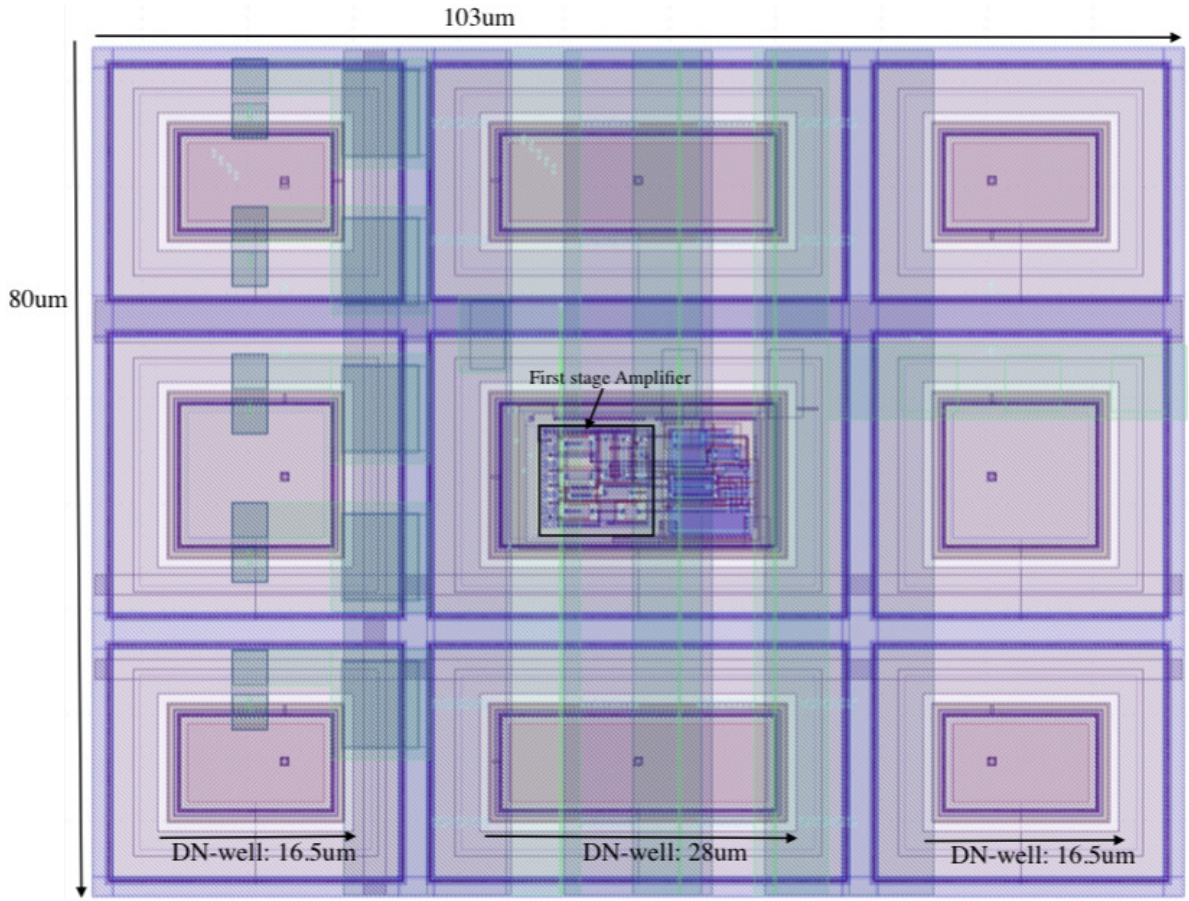
	Requirement	MuPix7	Conclusion
Pixel size (μm^2)	80×80	103×80	$\rightarrow$ MuPix8
Sensor size (mm^2)	20×20	3×3	$\rightarrow$ MuPix8
Thickness (μm)	50	50	ok
Bandwidth per chip (Gbit/s)	3×1.25	1×1.25	$\rightarrow$ MuPix8
Hit rate (MHz/cm^2)	2.5	5.5	ok
Spatial resolution (μm)	< 100	$103/\sqrt{12}$	ok
Time resolution (ns)	< 20	11	ok
Efficiency (%)	> 99	99.5	ok
Power (mW/cm^2)	≤ 300	≤ 300	ok

More on material budget and cooling requirements in the talk by S. Dittmeier tomorrow.

MuPix7 block diagram



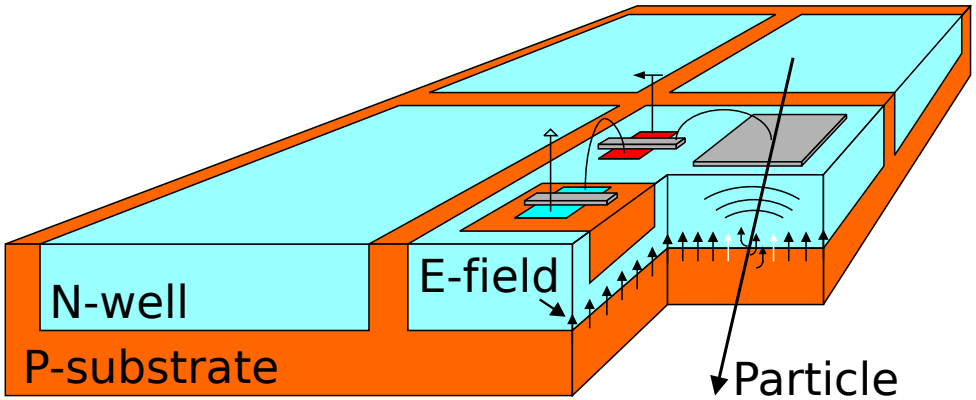
Pixel unit cell



Observe the 3×3 diode design. The analog electronics is on top of the center diode.

Mu3e

We use a High-Voltage **Monolithic** Pixel Sensor (HV-MAPS):



- HV CMOS technology used automotive and audio industry
- Reverse biasing up to $-85\,\mathrm{V}$ routinely ($-93\,\mathrm{V}$ tested)
- Thinning to $50\,\mu\mathrm{m}$ possible and done
- Self-triggered, continuous readout (no shutter, darkframe etc.)

Mu3e

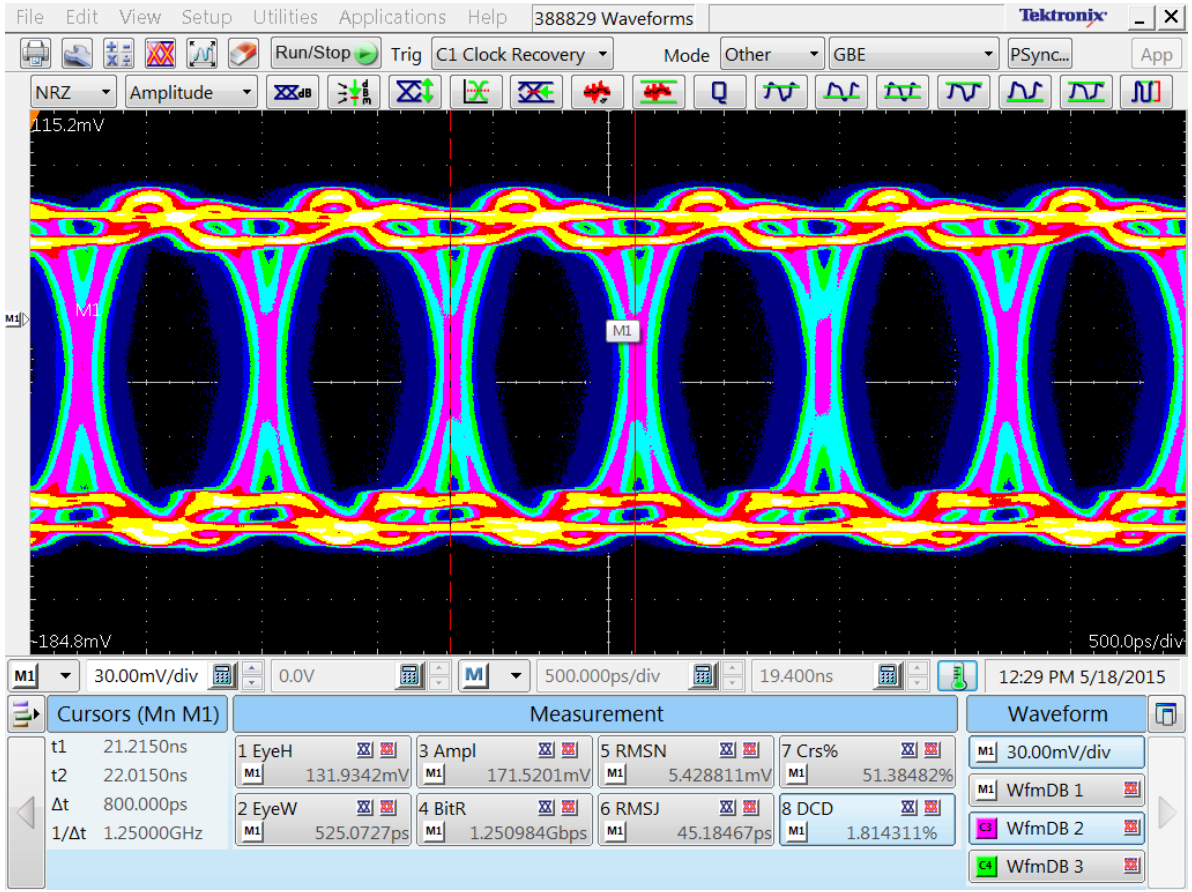
Several generations of MuPix chips realised:

Version	Year	Main features
MuPix1/2	2011/12	Analog prototype chips
MuPix3	2013	First digital readout
MuPix4	2013	Working digital readout and timestamping
MuPix6	2014	Readout bugs fixed, double-staged preamplifier
MuPix7	2014	Fast serial readout (1.25 Gbit/s), internal state machine, internal clock generation

MuPix3–7 have an active area of $3.2 \times 3.2\,\mathrm{mm}^2$, chip size is $\approx 3.5 \times 4\,\mathrm{mm}^2$.
MuPix7 pixel size: $103 \times 80\,\mu\mathrm{m}^2$, making up a 32×40 matrix.

MuPix7: Fast serial readout signal

Signal quality of fast readout signal at 1.25 Gbit/s is very good:

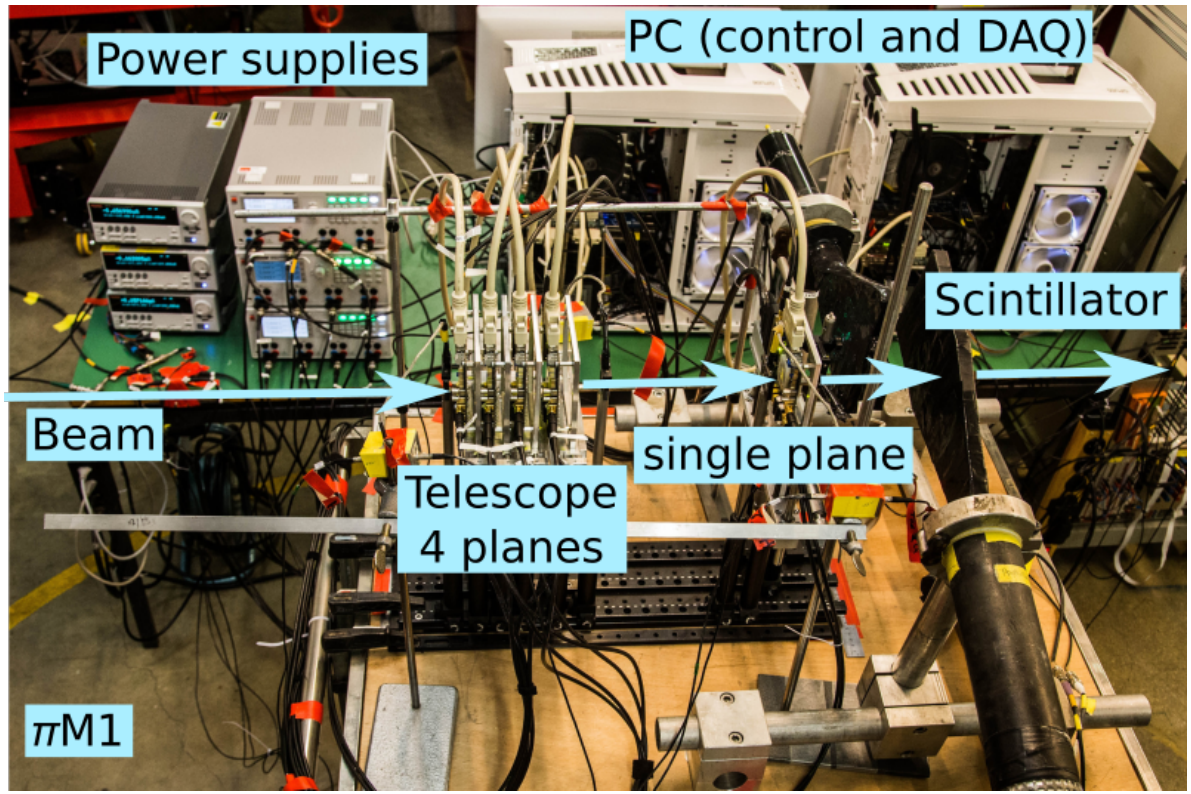


Clock is at 125 MHz, high speed clock internally generated.

Measured on test bench using chip on standard test board.

MuPix7: Telescope

Telescope setup, e.g. at PSI πM1:



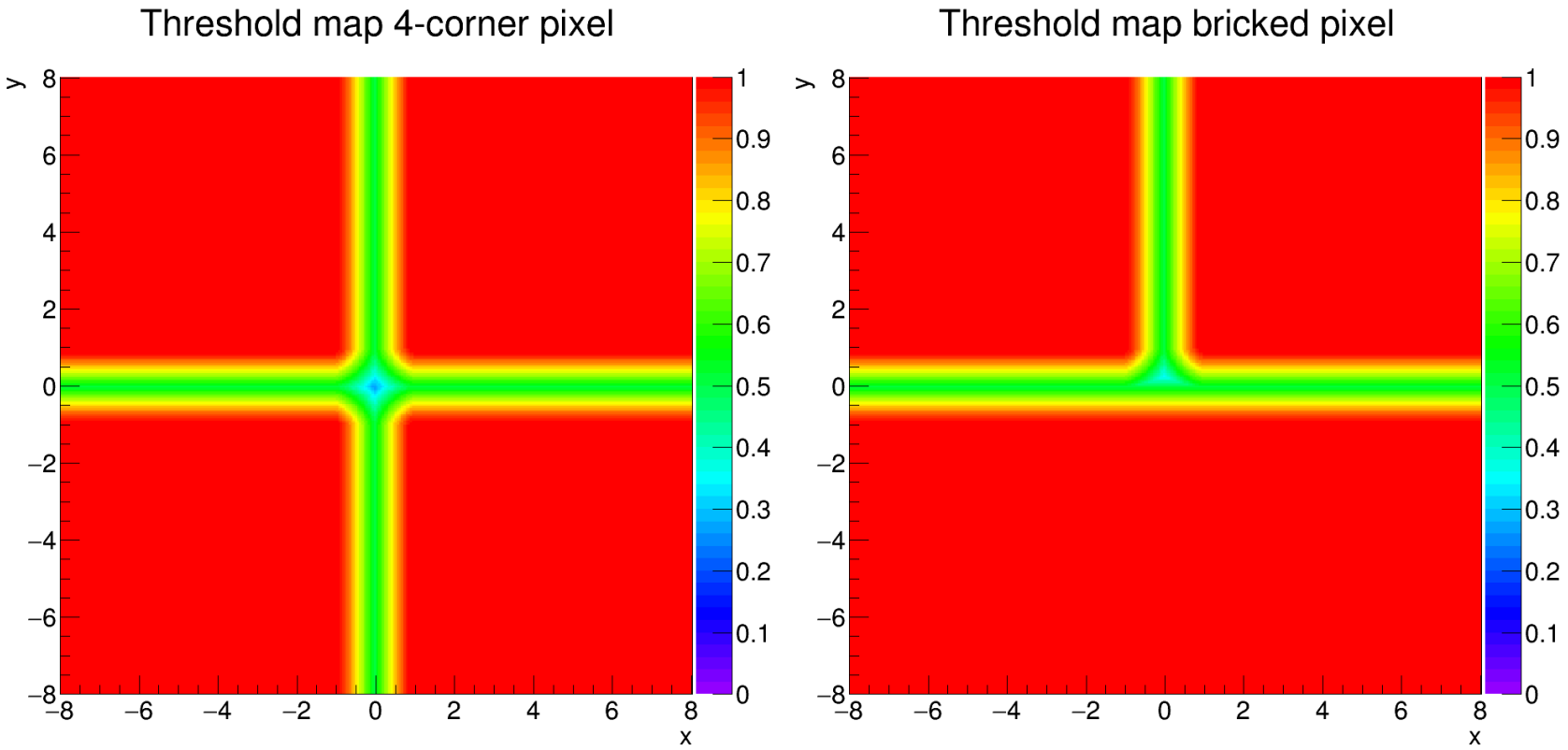
Telescope with 4 MuPix7 planes, 1 plane elected as DUT

MuPix7

Integration studies:

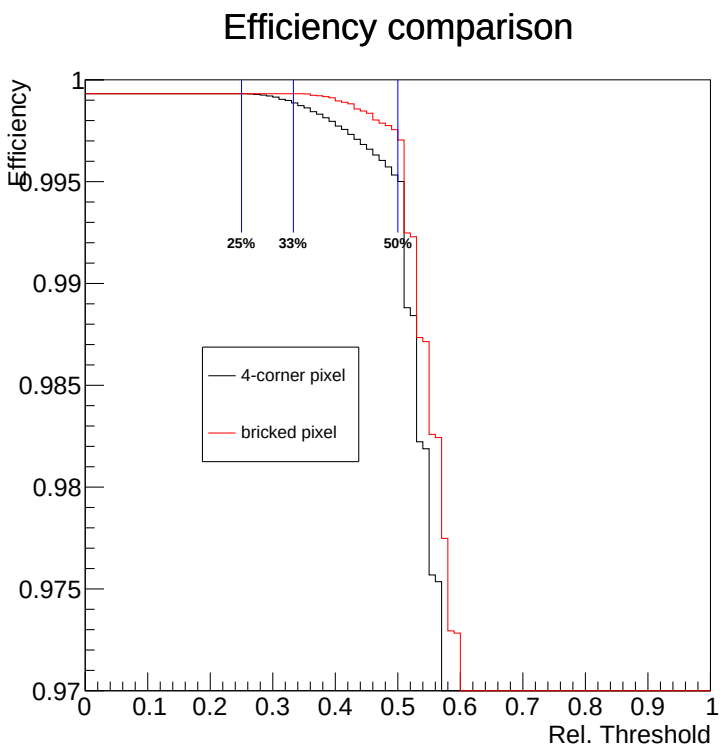
- Build a **prototype of an inner layer module**: 2×3 chips.
- Studies with different **flex print options** (1 signal layer, 2 power layers):
  - **Traditional:** 3 layer copper: conservative but reliable, too much material for final design ($2‰\ X_0$)
    $\Rightarrow$ Electrical integration studies
  - **Baseline:** 1 copper layer (signal), 2 aluminium layers (power/GND), sandwiched ($1.2‰\ X_0$ possible)
    $\Rightarrow$ Copper technology has nice spacing (10 µm feature sizes available)
  - **Optimal:** 2 layer Aluminium, if necessary with one additional layer. Uses pad-bonding ($1‰\ X_0$)
    $\Rightarrow$ Technology implemented by ALICE. Riskier approach, new territory but promising.

Efficiency of 4-corners vs. bricked layout



ToyMC for a sample charge cylinder with unit radius. Shows fraction of charge seen in the pixel under the impact center. Range $[-8, 8]$ corresponds to a pixel of 80 µm size and 5 µm charge radius.

Efficiency of 4-corners vs. bricked layout



Efficiency vs. threshold (arbitrary units).

A 4-corner pixel starts to loose hits if threshold is above 25% of full charge generated.

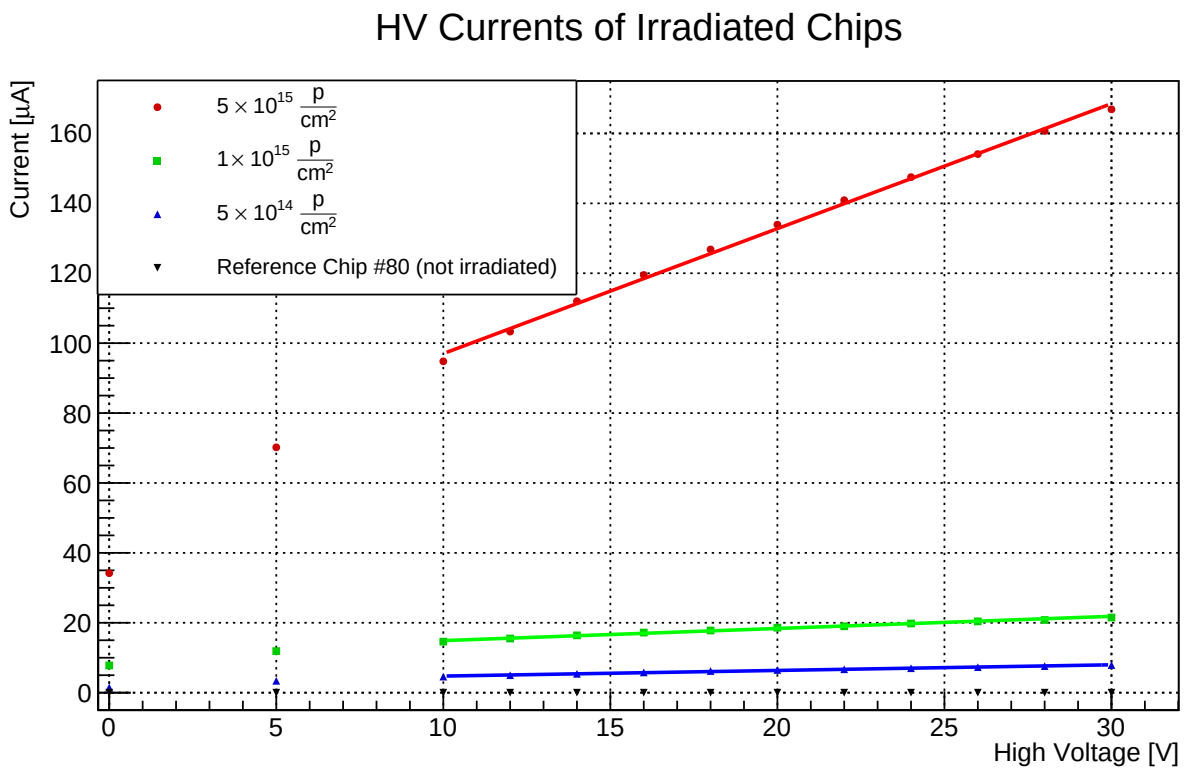
Bricked pixel gives some headroom.

MuPix7: Radiation hardness

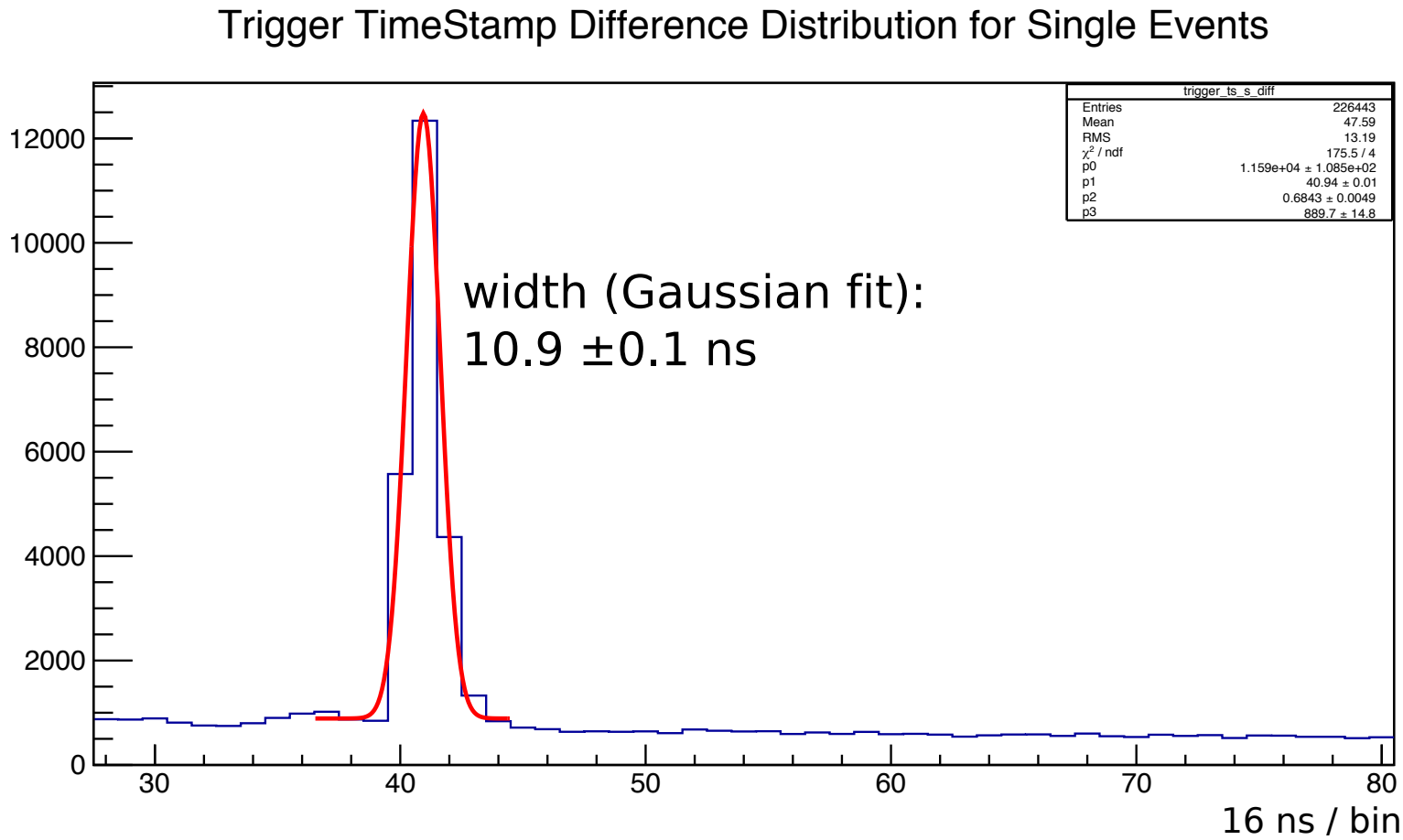
- MuPix7 is **not a rad-hard design**. Full stop.
- Rad-hardedness is not a requirement for the Mu3e experiment (low energetic electrons).
- Nevertheless we irradiated samples at SPS with approx. 1.5×10^{15} and 7.8×10^{15} protons/cm^2.
- Leakage current rises. Especially between HV and n-well. Thermal run-away above 55 V.
- **Digital part still functional**, e.g. state machine runs without any hiccups.
- Chips can be tuned to operate. Noisier than unirradiated. Efficiency lower. Data analysis ongoing.
- Rad-hard design studies started within our group.

MuPix7: Radiation hardness

MuPix7 is *not* a rad hard design. Nevertheless we tested it:



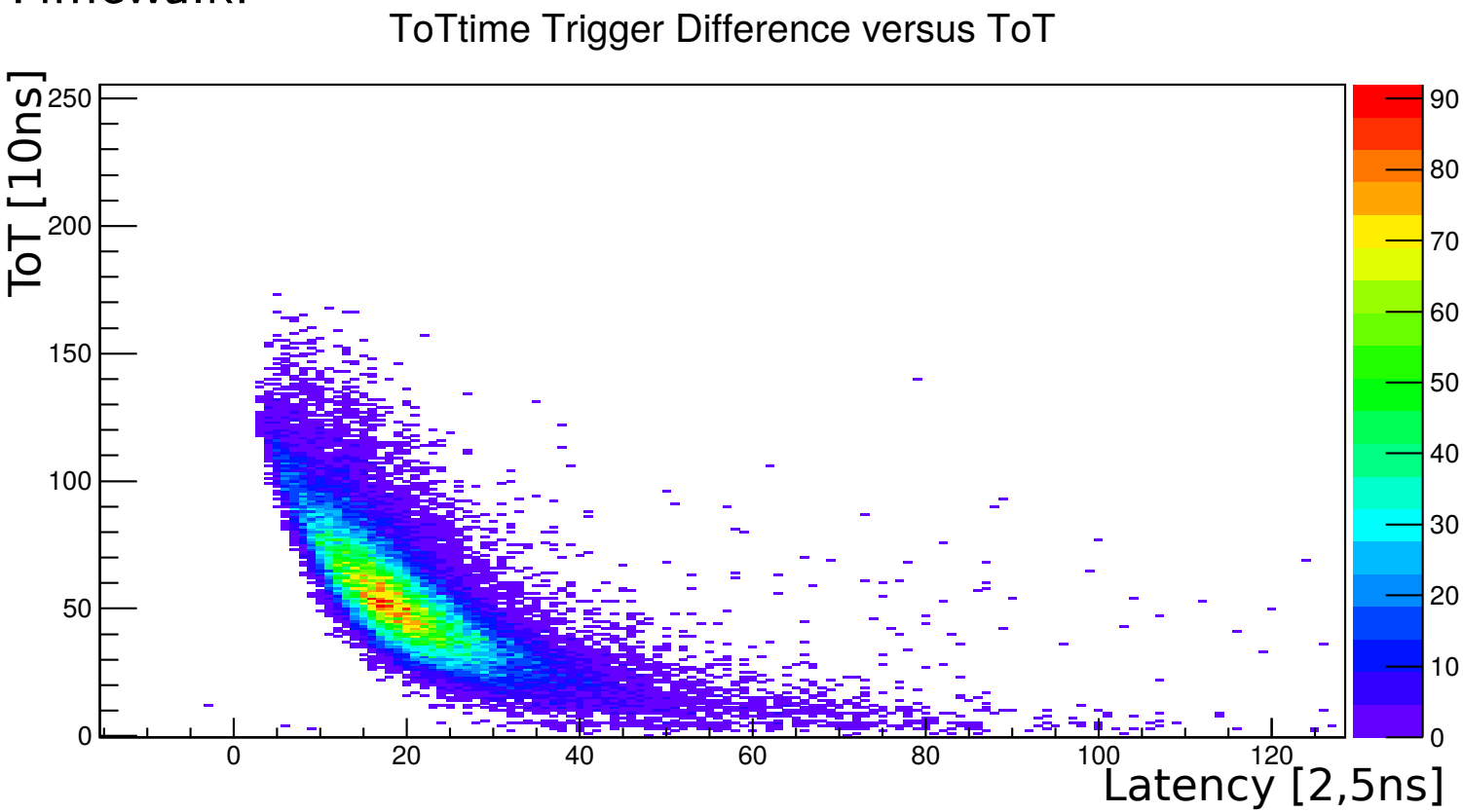
MuPix7: Time resolution



Technique: Scintillator coincidence signal as reference. Plotted timestamp scintillator − timestamp MuPix7 (Settings used: 1000 mW/cm^2)

MuPix7: Time resolution

Timewalk:



ToT can be measured for one selected pixel. Anticorrelation clearly visible (Settings used: 1000 mW/cm^2).

MuPix7: DAQ performance

- **CERN SPS**: MuPix7 run successfully at rates of about **500 kHz** (on chip)[1].
- Speed limit of MuPix7 telescope: about **1 million tracks per second**. Can be increased by optimising DMA transfer.
- Fast data transfer and reconstruction demonstrated (simulation and at DESY).
  - Hits sorted on FPGA
  - Transferred to memory using DMA
  - Processed in GPU for track reconstruction.

  300 MB/s with simulated data achieved[2].

[1] Exact rate determination difficult due to saturated DAQ.

[2] This is processing speed, not write to disk.