# Strip Technology and HVMPAS

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# Overview

- High-Voltage CMOS Sensors - introduction
- Summary of the old results
- High-Voltage CMOS Sensors for ATLAS

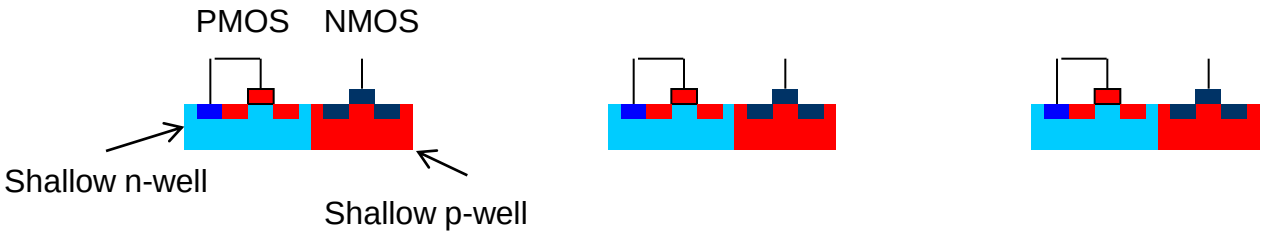
# High-voltage CMOS pixel detectors or “smart diode arrays”

# HV CMOS detectors

- The distinguishable property of HV CMOS sensors is that the CMOS pixel electronics is placed inside the sensor diode.
- This allows:
- 1) Construction of pixel arrays without insensitive regions.
- 2) High reverse biasing of the sensor diodes.
- 3) Fast charge collection based on drift.

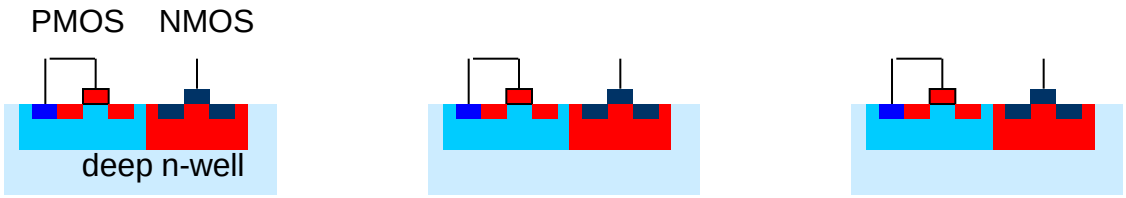
# HV CMOS detectors

- We start with a low voltage process:
- PMOS and NMOS transistors are placed inside their shallow wells.



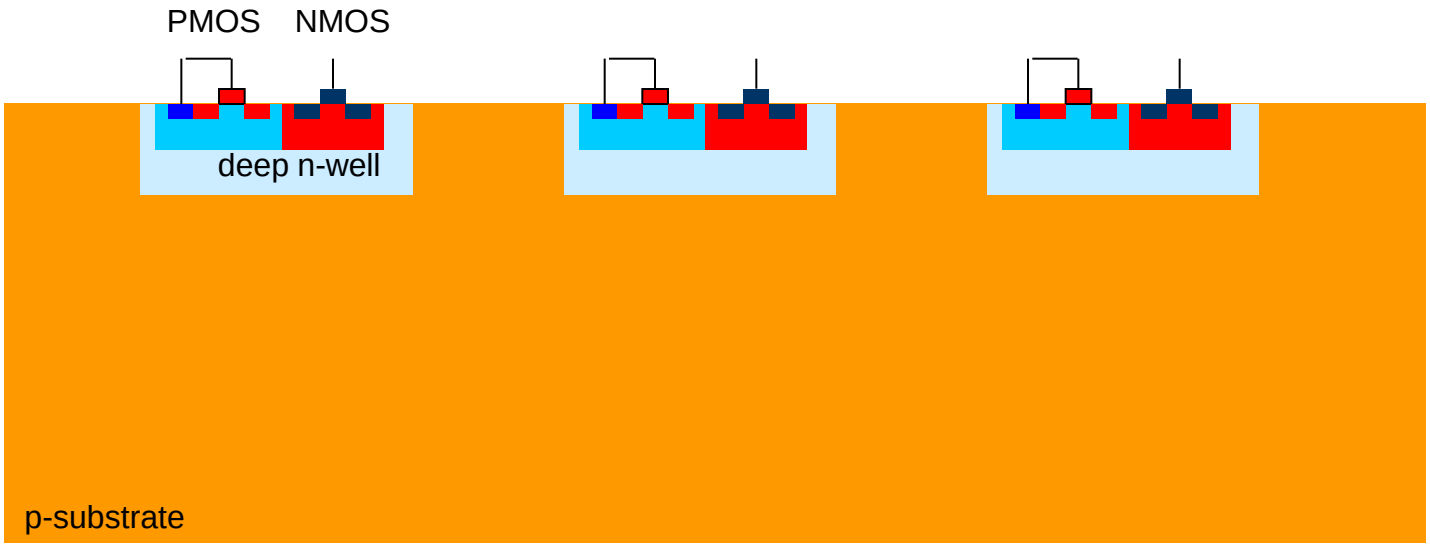
# HV CMOS detectors

- A deep n-well surrounds the electronics of every pixel.



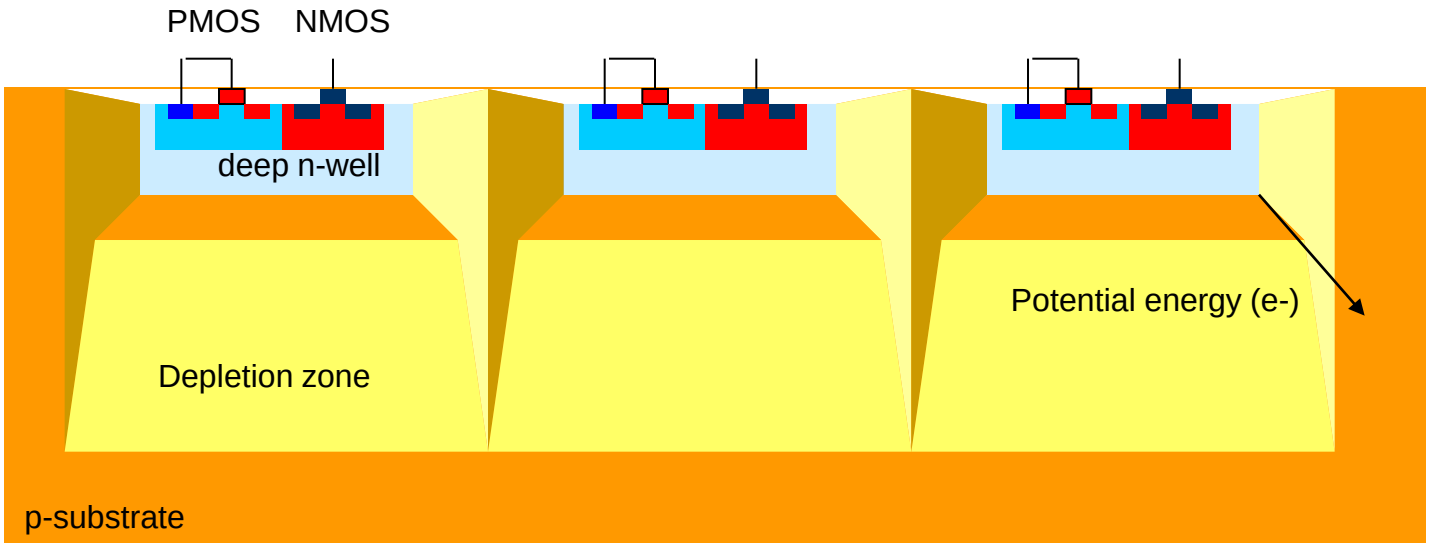
# HV CMOS detectors

- The deep n-wells isolate the pixel electronics from the p-type substrate.



# HV CMOS detectors

- Since the pixel-transistors do not “see” the substrate potential, the substrate can be biased low without damaging the transistors.
- In this way the depletion zones in the volume around the n-wells are formed.
- => Potential minima for electrons



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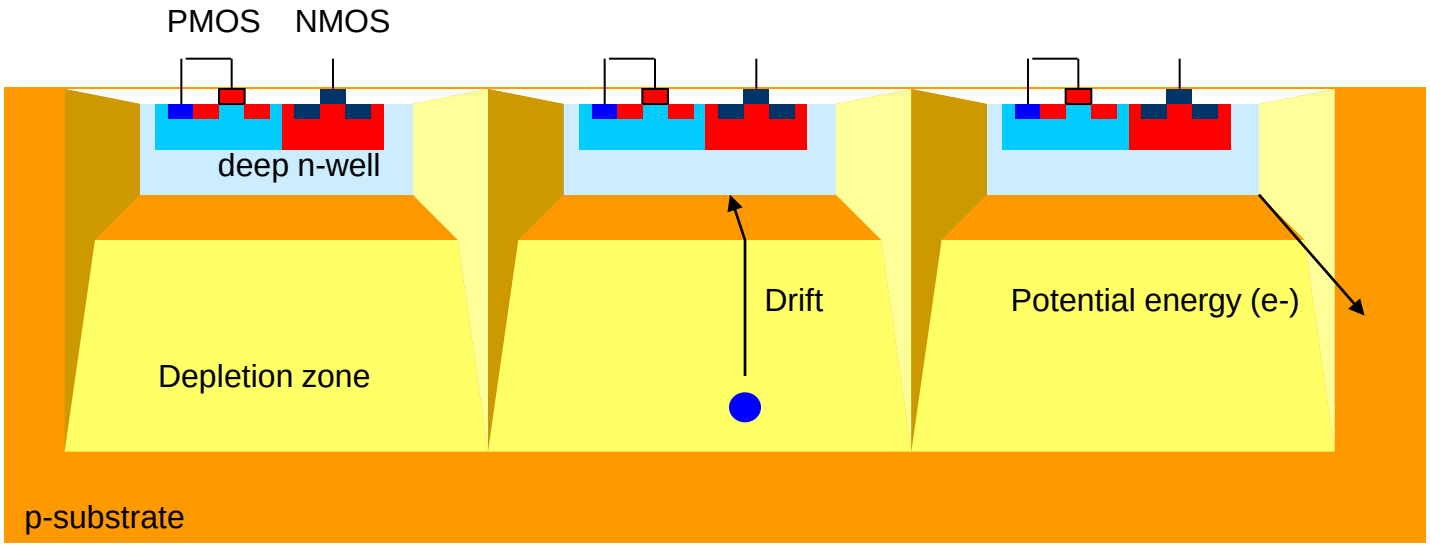
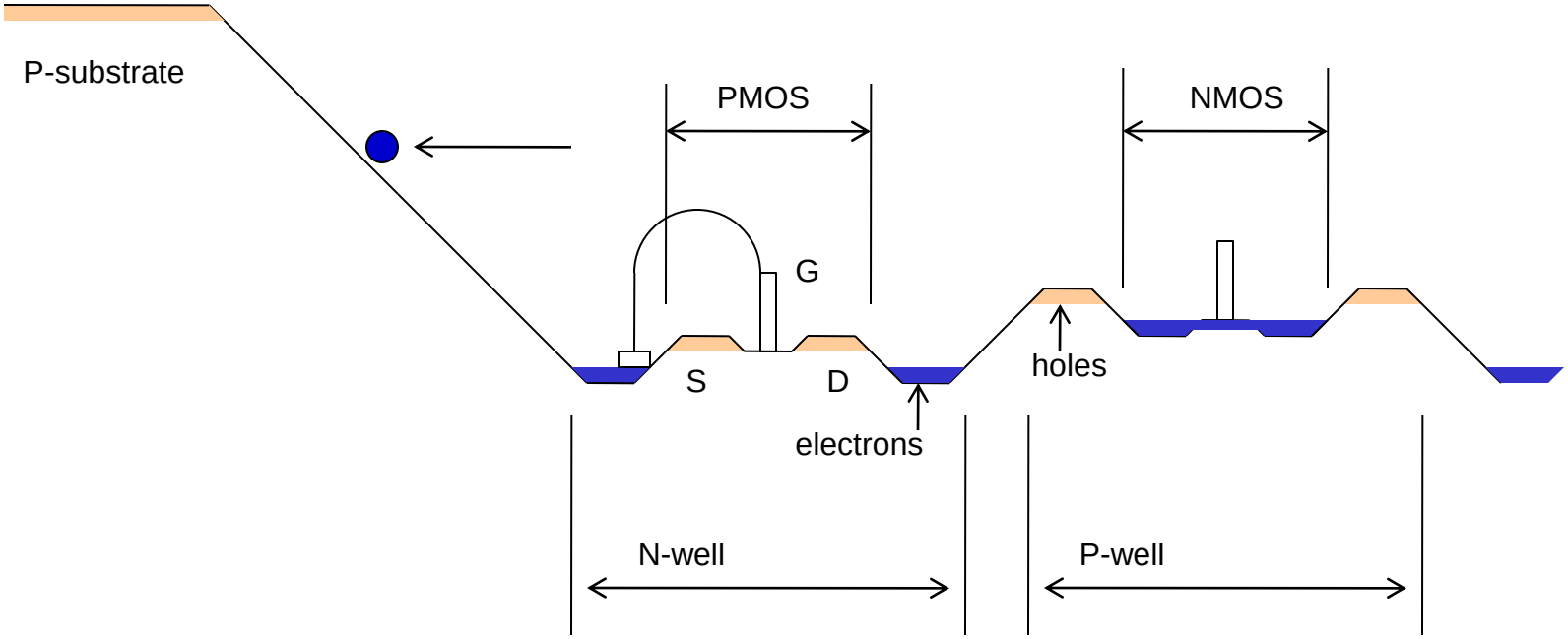
- Charge collection occurs by drift



- Collected charge causes a voltage change in the n-well.
- This signal is sensed by the amplifier – placed in the n-well.



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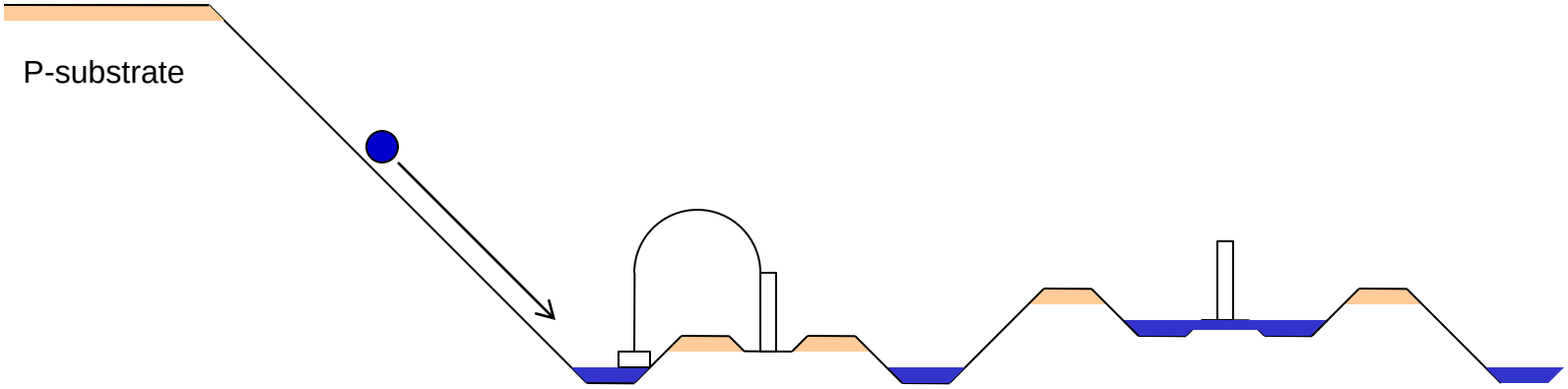

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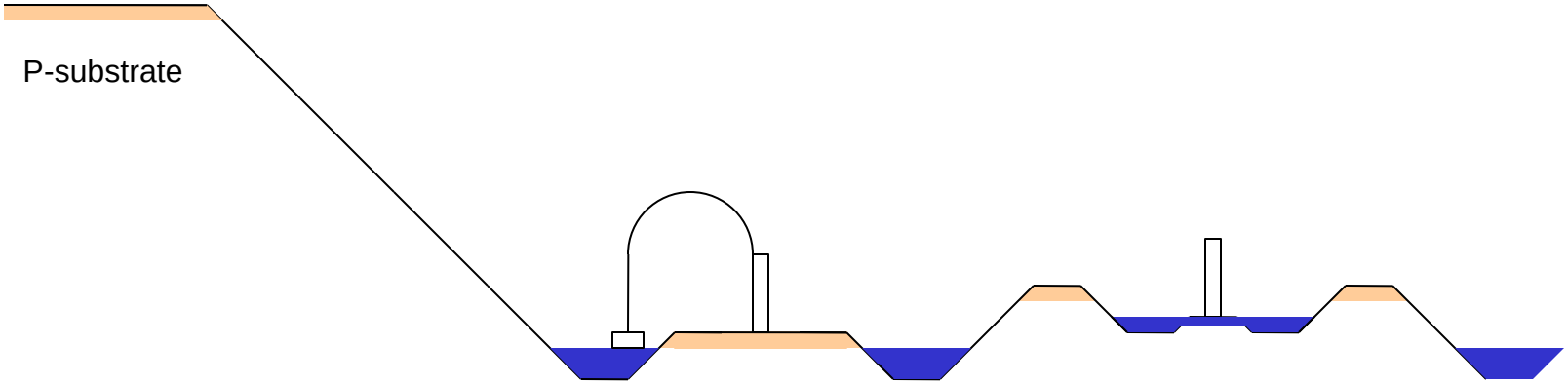
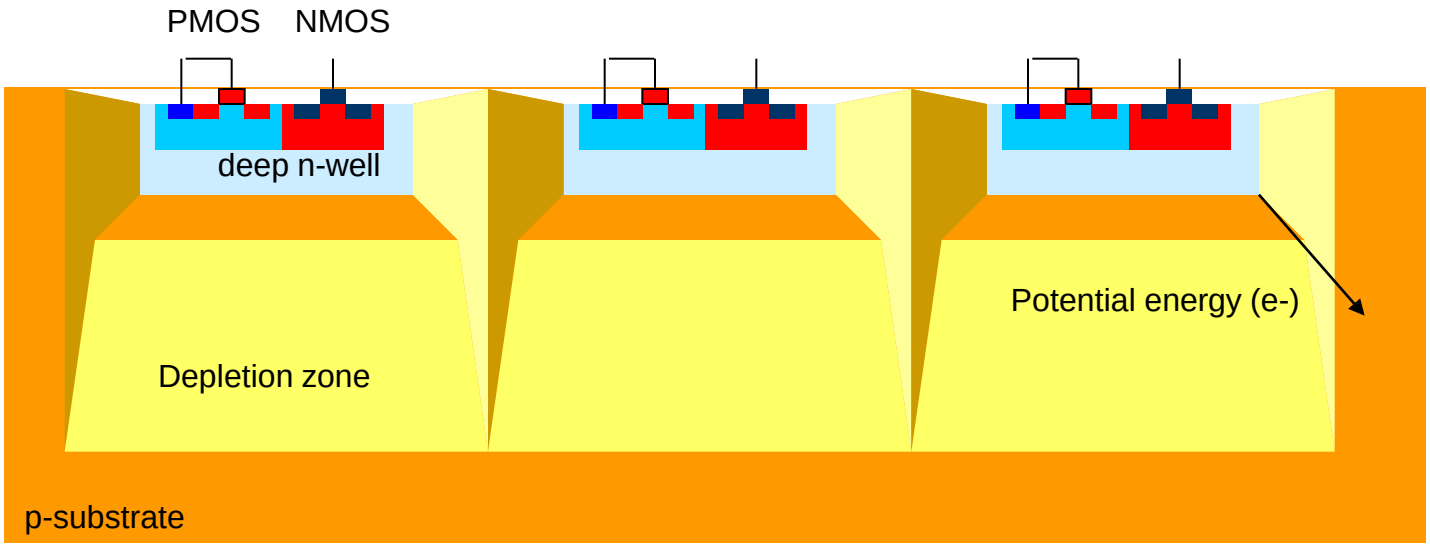


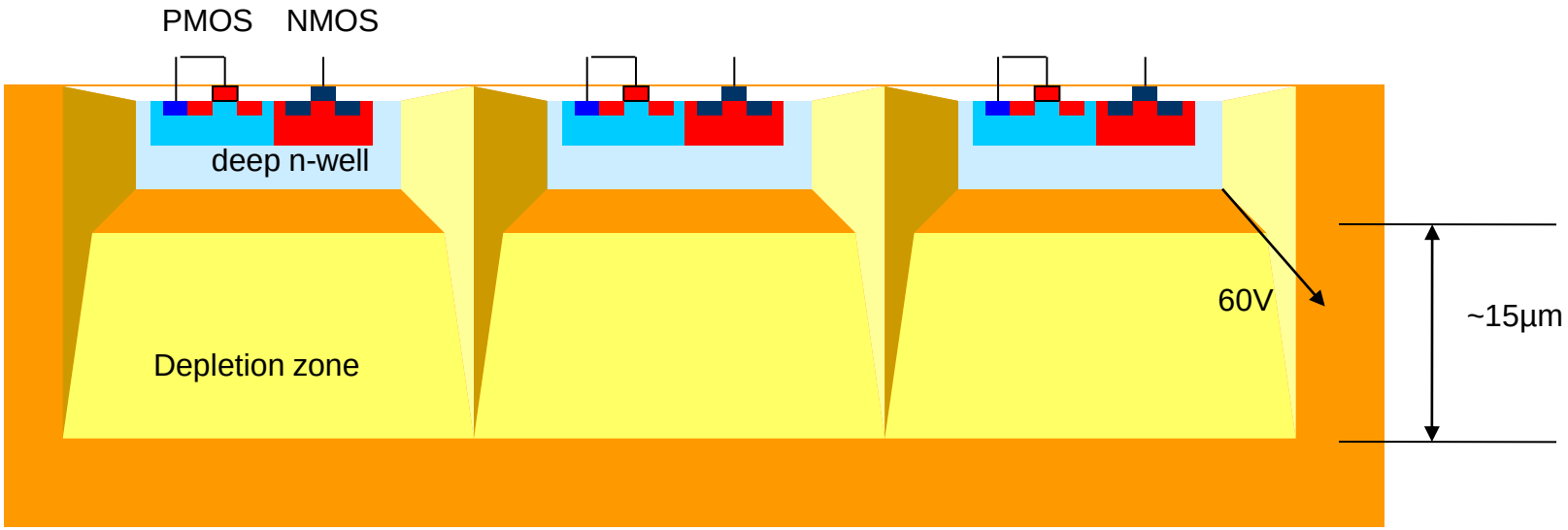
# HV CMOS detectors

- Maximizing of the depleted regions improves performances (less capacitance and noise, more signal) – the best results can be achieved in high-voltage technologies.



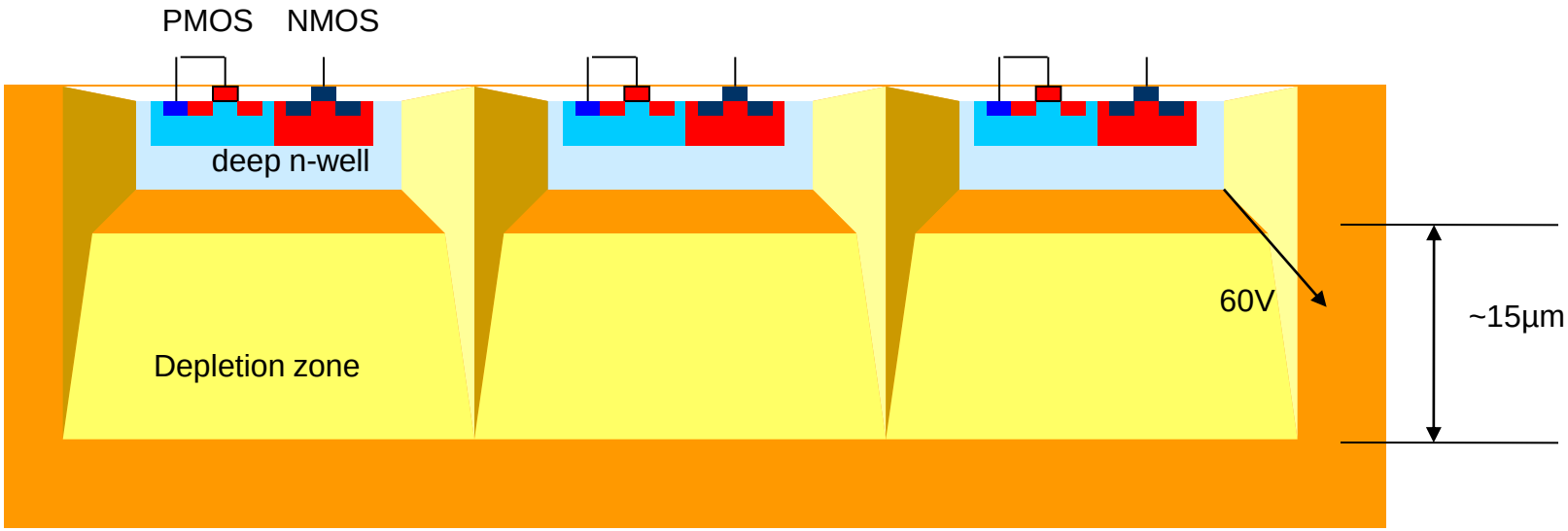
# HV CMOS detectors

- Example AMS 350nm HVCMOS: Typical reverse bias voltage is 60 V and the depleted region depth ~15 μm.



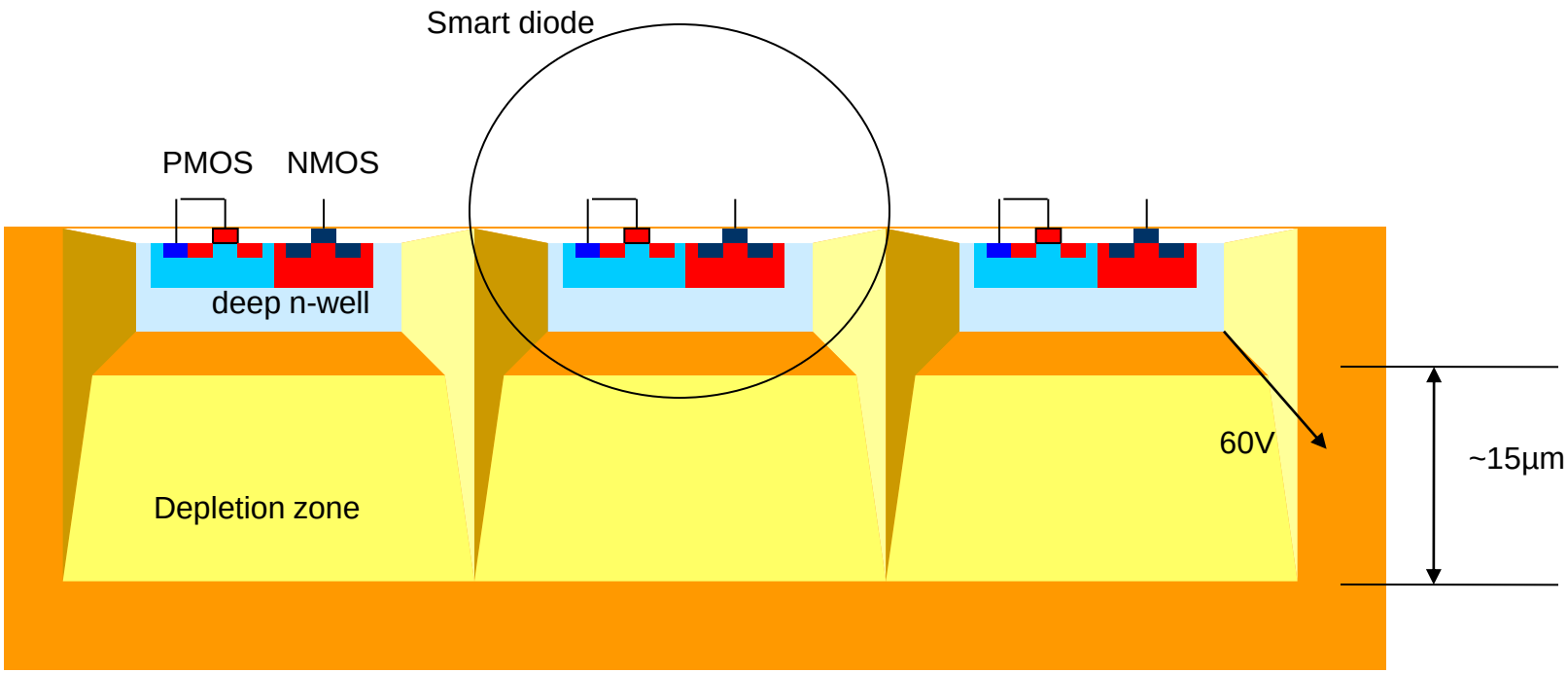
# HV CMOS detectors

- Example AMS 350nm HVCMOS: Typical reverse bias voltage is 60 V and the depleted region depth ~15 μm.
- 20Ωcm substrate resistance -> acceptor density ~ $10^{15}$ $cm^{-3}$



# HV CMOS detectors

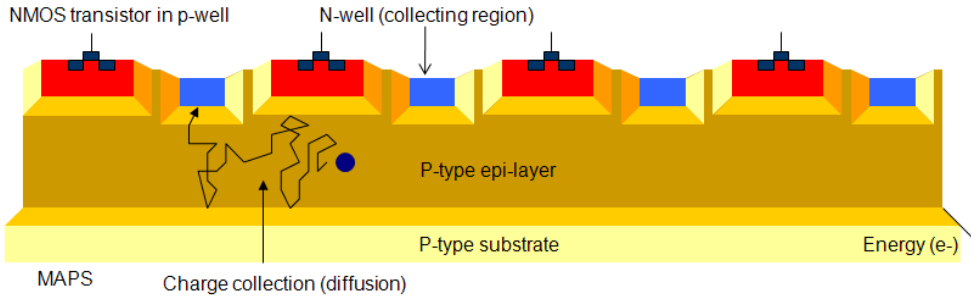
- Since the sensor diodes are equipped with electronics we call them “smart” and the structure “smart diode array”.
- The structure can be designed also in LV processes that have a deep n-well that surrounds *both* types of shallow wells entirely.
- An example of such a LV technology is UMC 180nm.



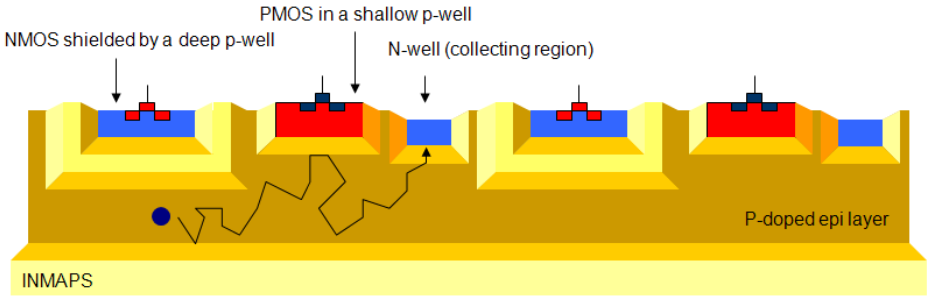
# CMOS pixel flavors

- CMOS pixel flavors:

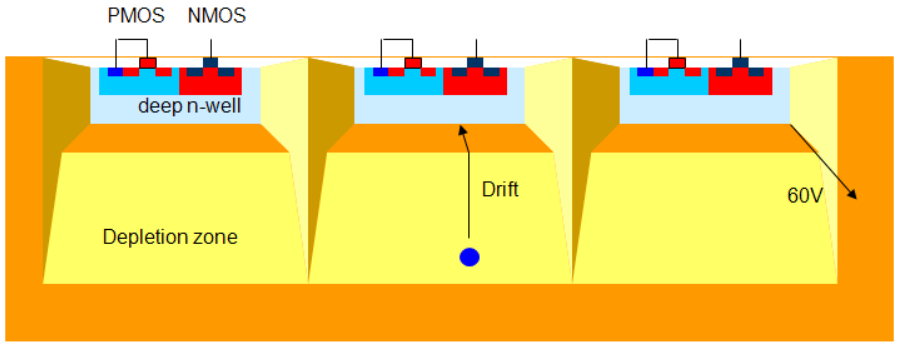
Standard MAPS



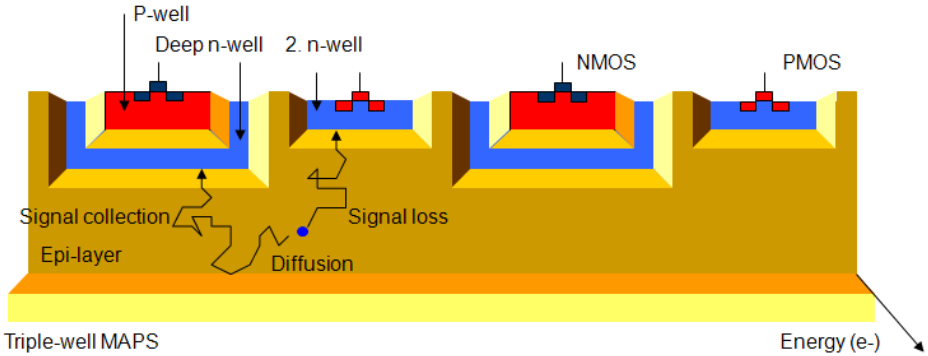

INMAPS



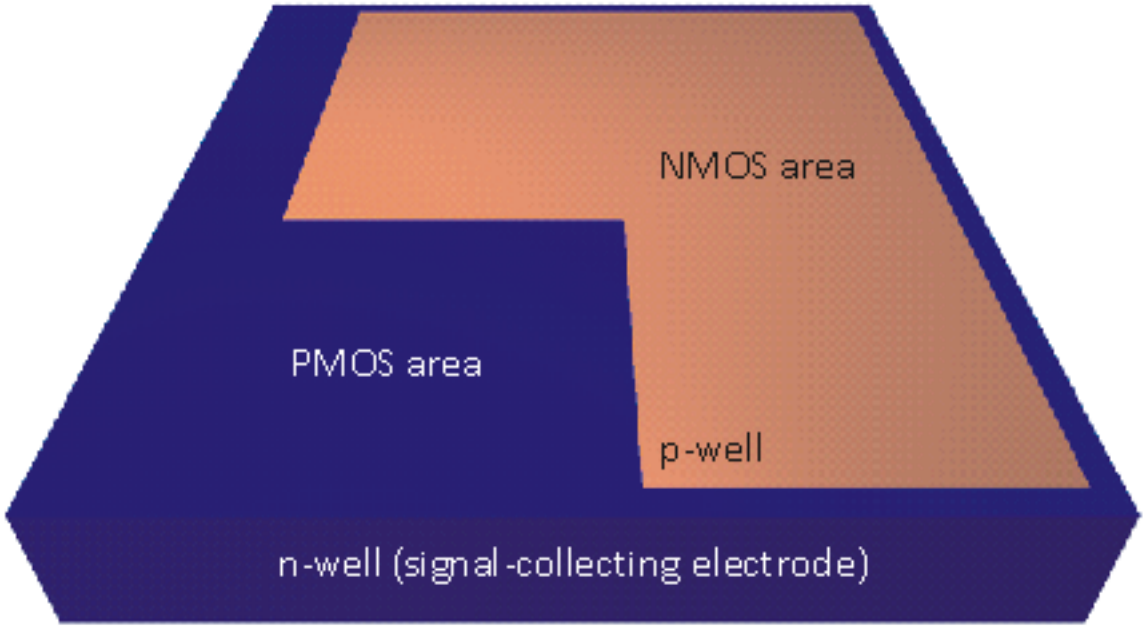

„HVMAPS“ – HVCMOS or SDA



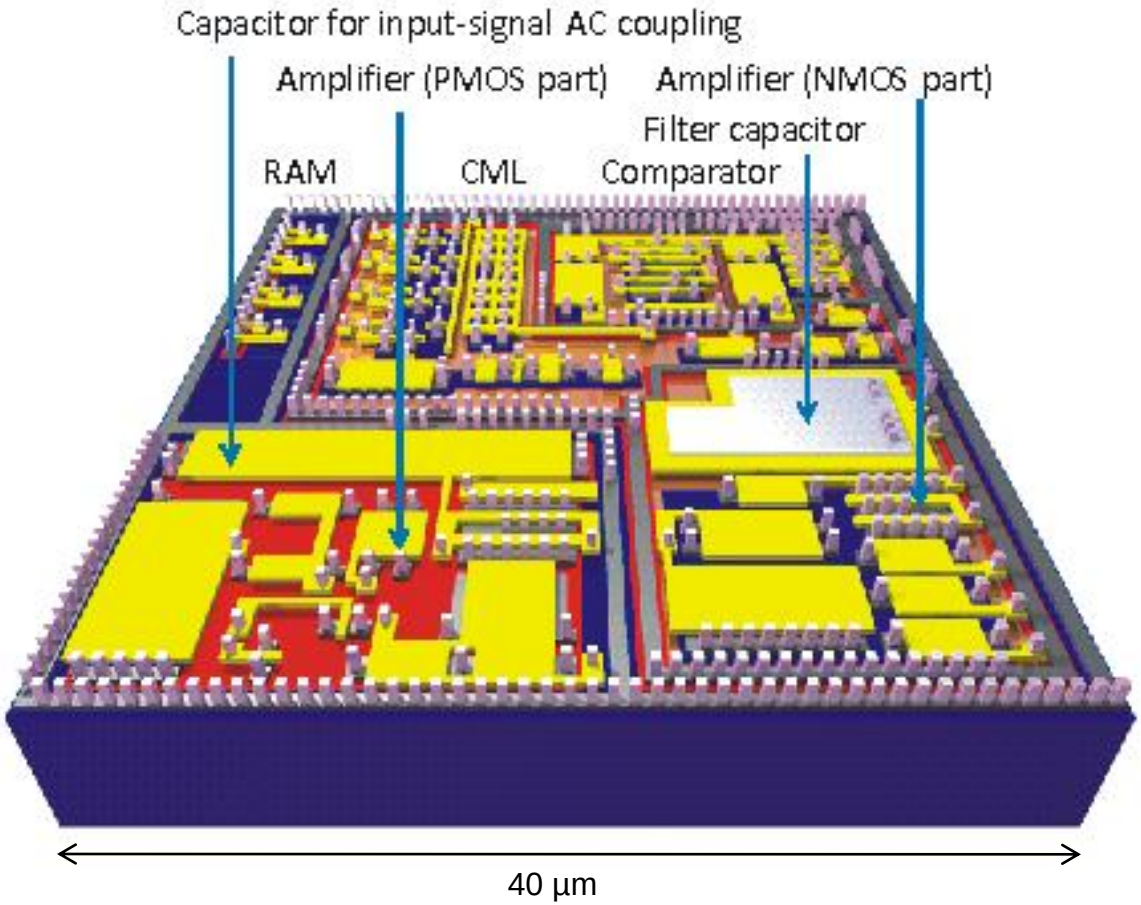

TWELL MAPS



# A “smart diode” layout



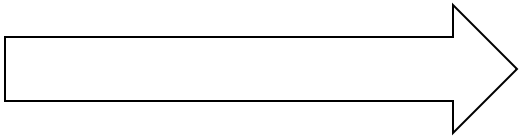
# Layout example: intelligent diode



# Project results

# Project history

2006



„Proof of principle“ phase

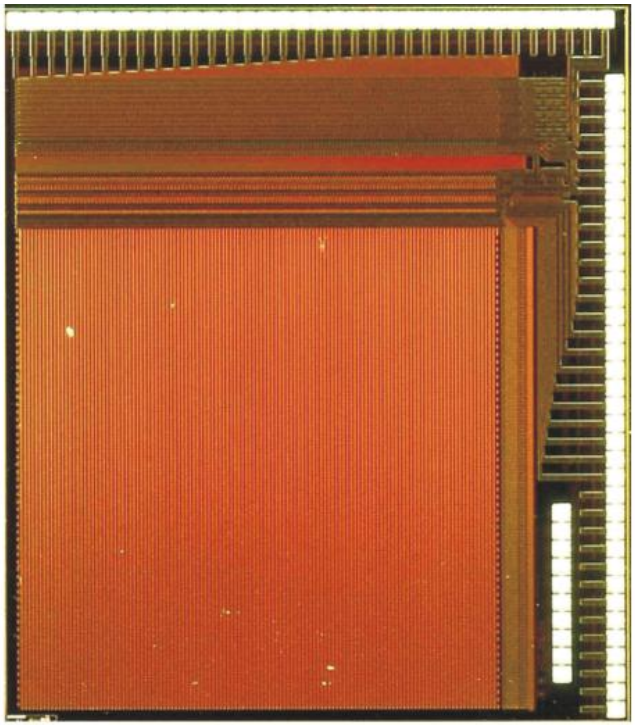
350nm AMS HV technology

1) Simple (4T) integrating pixels with pulsed reset and rolling shutter RO
(Possible applications: ILC, transmission electron microscopy, etc.)

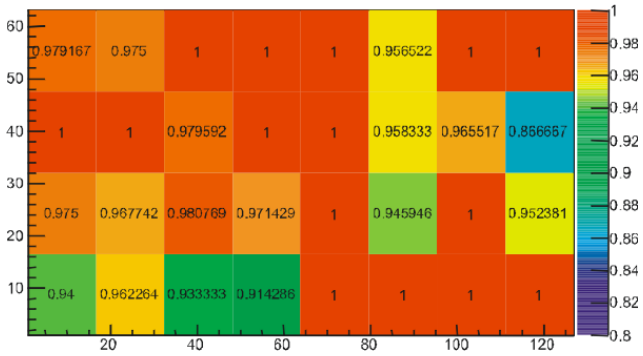
2) Pixels with complex CMOS-based pixel electronics
(Possible applications: CLIC, LHC, CBM, etc.)

3) CCPDs based on a pixel sensor implemented as a smart diode array

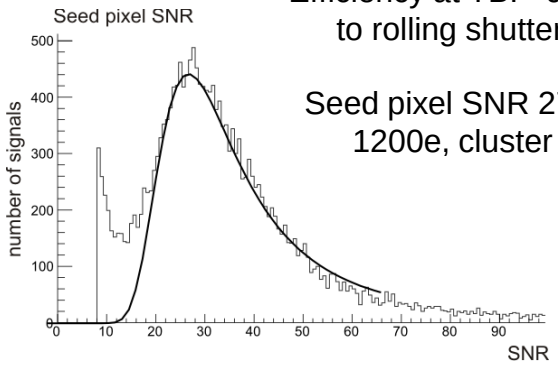
# Project history



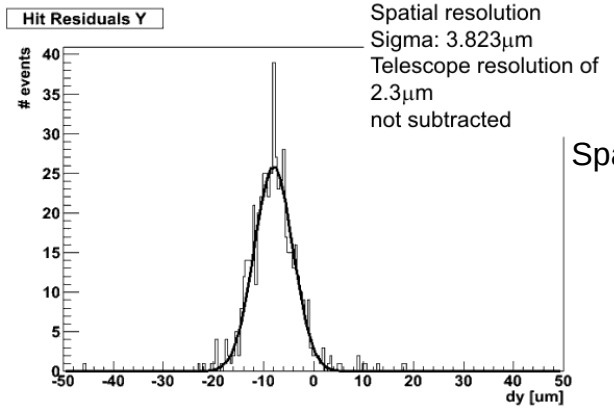
The type 1 chip HVPixelM:
Simple (4T) integrating pixels with pulsed reset and rolling shutter RO
21x21 µm pixel size




Efficiency at TB: ~98% (probably due to rolling shutter effects

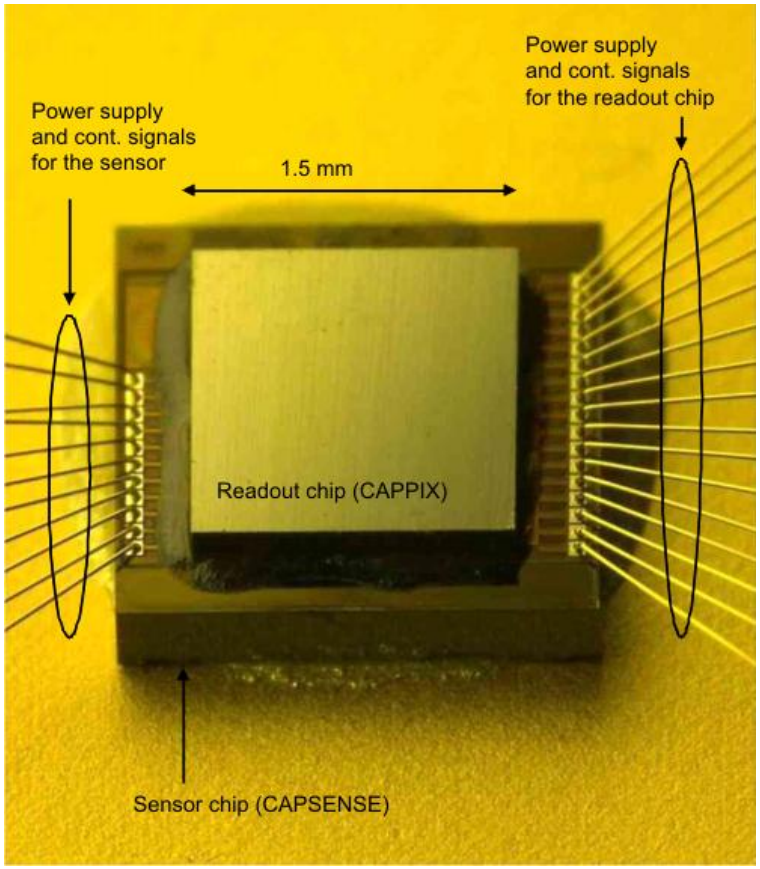



Seed pixel SNR 27, seed signal 1200e, cluster 2000e

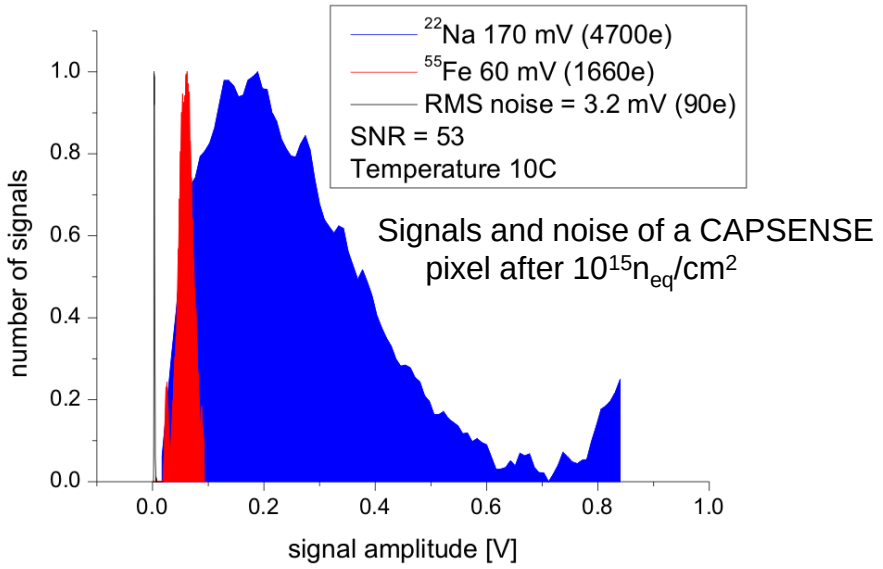



Spatial resolution 3-3.8µm

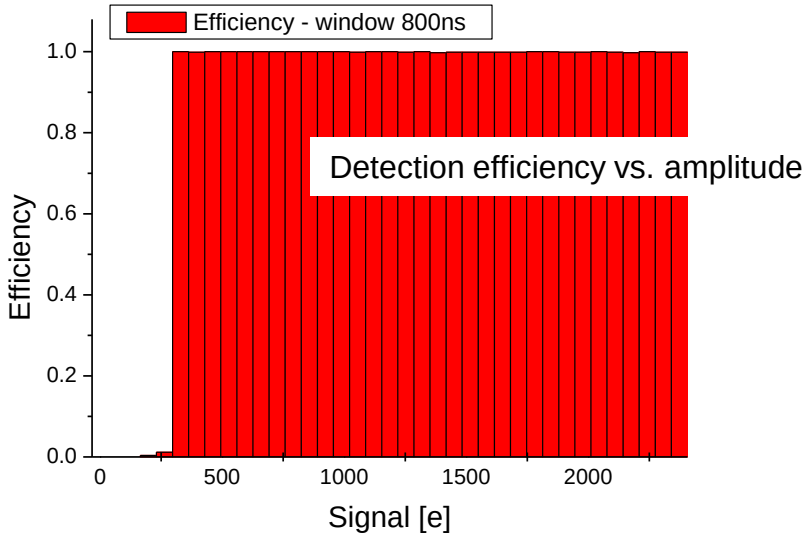
# Project history




CAPPIX/CAPSENSE edgeless CCPD
50x50 µm pixel size



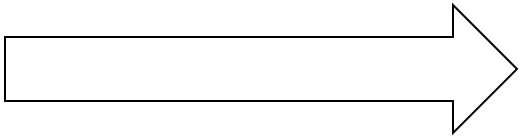

Signals and noise of a CAPSENSE pixel after $10^{15} n_{eq}/cm^2$




Detection efficiency vs. amplitude

# New projects

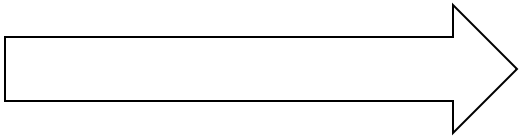
2006

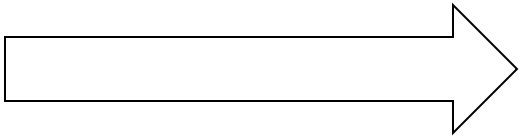


„Proof of principle“ phase

350nm AMS HV technology

65nm UMCLV technology





180nm AMS HV technology

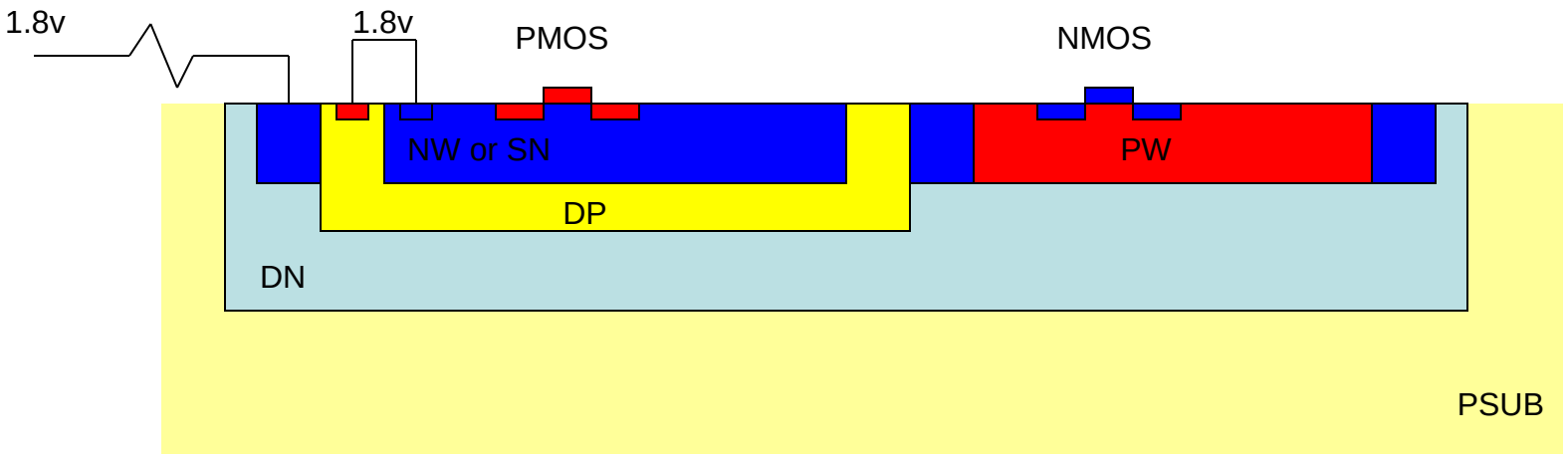
Applications:
1) Transmission electron microscopy integrating pixels with pulsed reset and rolling shutter RO – in-pixel CDS

2) Mu3e experiment at PSI
Monolithic CMOS pixels with CSA

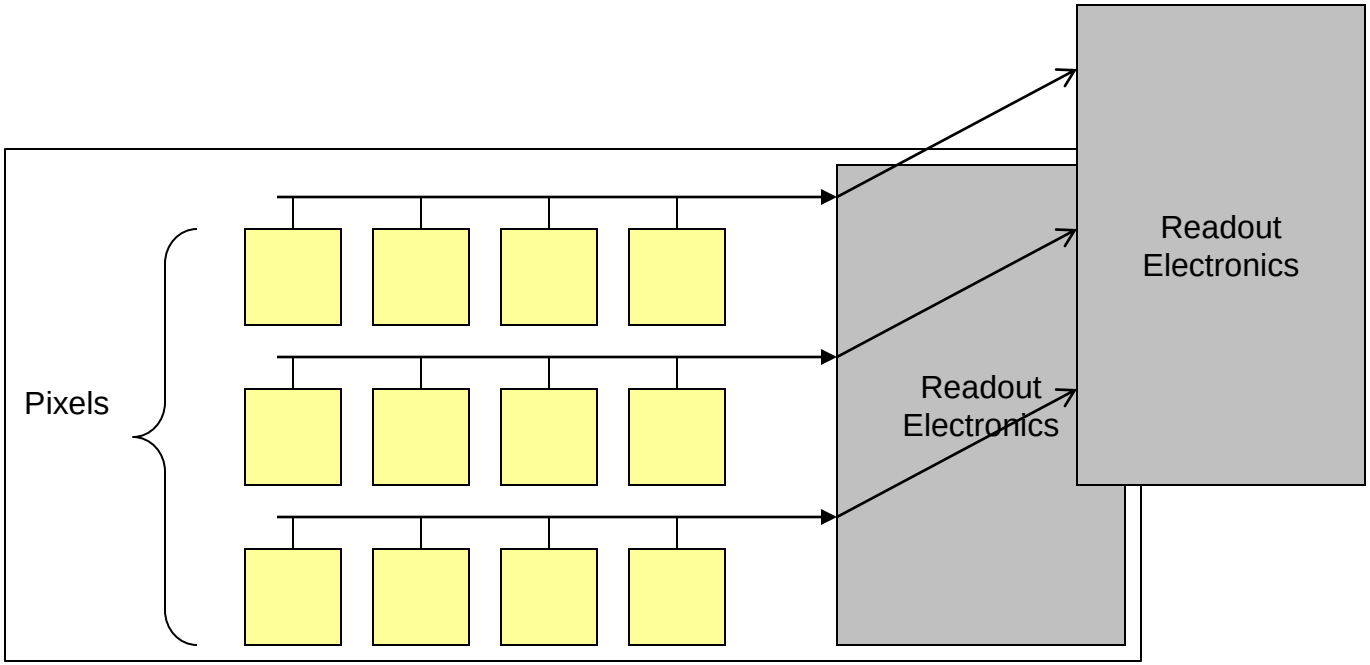
**3) ATLAS (and CLIC)**
**CCPDs based on smart sensors**

# Technology issues – crosstalk

- Capacitive feedback into the sensor (n-well)
- Many important circuits do not cause problems: charge sensitive amplifier, simple shaper, tune DAC, SRAM but…
- "Active" (clocked) CMOS logic gates and sometimes comparators cause large crosstalk
- Possibility 1: Implement the circuits only using NMOST: effects on radiation tolerance, layout area, power consumption, etc.
- Possibility 2: Place the active digital circuits on the chip periphery or on separate chip.
- Possibility 3: Isolate PMOST from n-well using an additional standard technology feature – the deep P-well – we still haven't tested it…

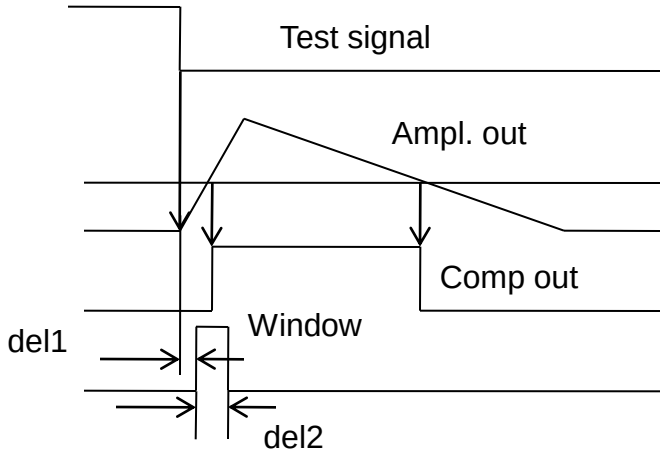


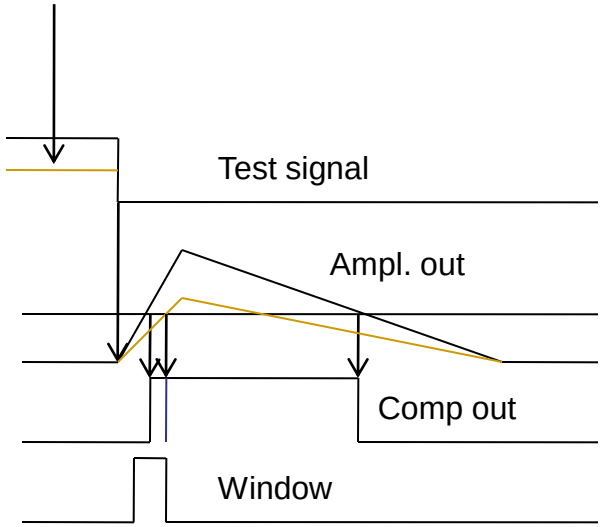
- Pixel electronics is based on a charge-sensitive amplifier and optionally a comparator.
- The pixel signal/address is sent as an analog information.
- The signal processed by the digital circuits are on the chip periphery or on a separate chip.
- 1) Mu3e: The pixel signal is processed on the sensor chip itself -> monolithic pixel detector.
- 2) ATLAS: intelligent sensor concept. The pixel address is transmitted to an existing readout chip, like FEI4 or an strip-readout chip.



# Time walk measurement

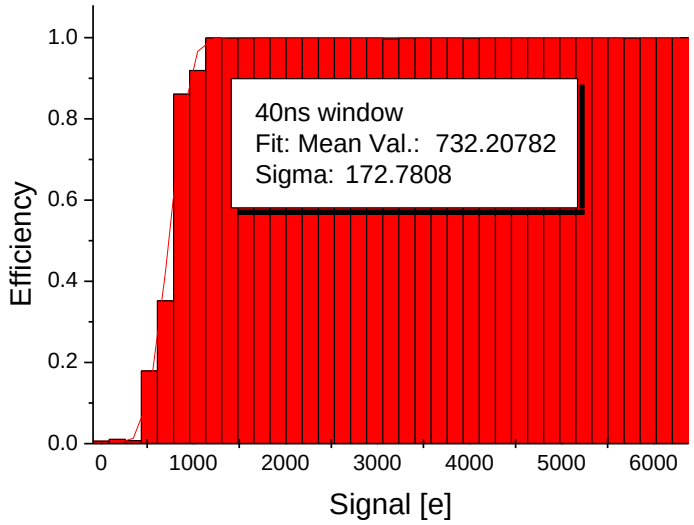
- The digital part accepts only the comparator signals that are within the trigger window.
- Time resolution tests possible.
- Time resolution is the sum of time walk and signal collection time.



# Time walk measurement

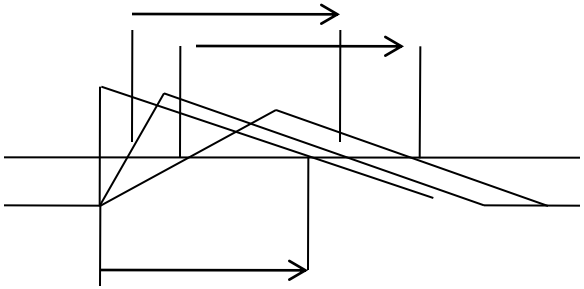
- In-time efficiency vs. signal amplitude (40ns time window).
- Detection of signals > 1230 e with 40ns time resolution possible.
- Power consumption of the pixel 7.5µm.
- We expect at least 1500 e from MIPs.

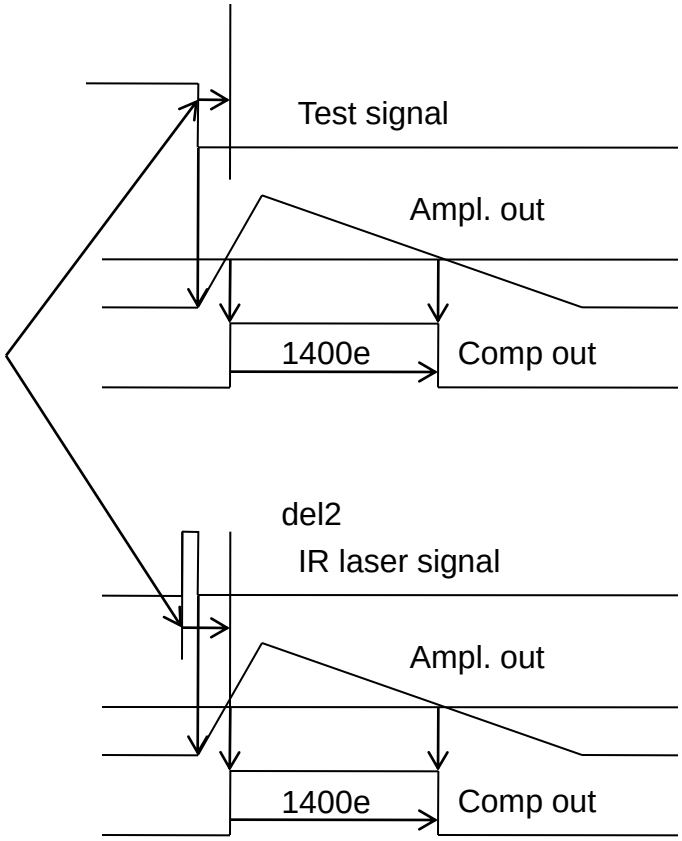


# Collection time measurement

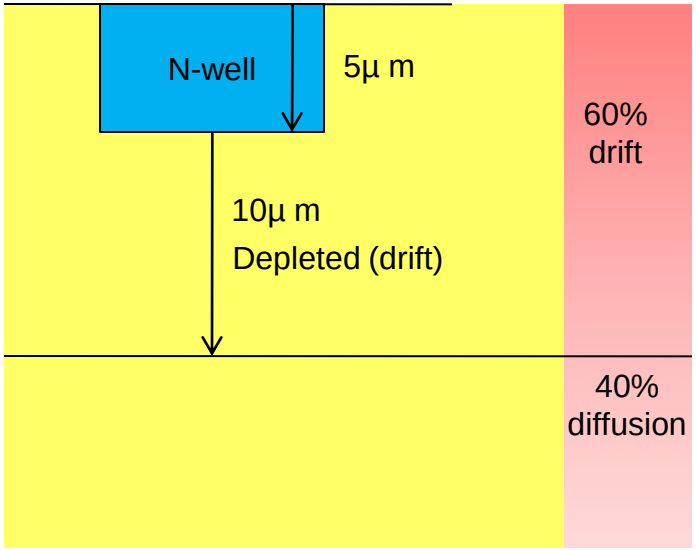
- Comparison of the response delay to capacitive test pulse (delay only caused by the amplifier) and the delay to IR pulse (delay caused by the amplifier and collection time).
- To assure that amplifier delay is equal, we equalize the signal amplitudes for both injections.
- The amplitudes are measured as ToT.

ToT is proportional to the input charge.
It does not depend on the amplifier rise times.



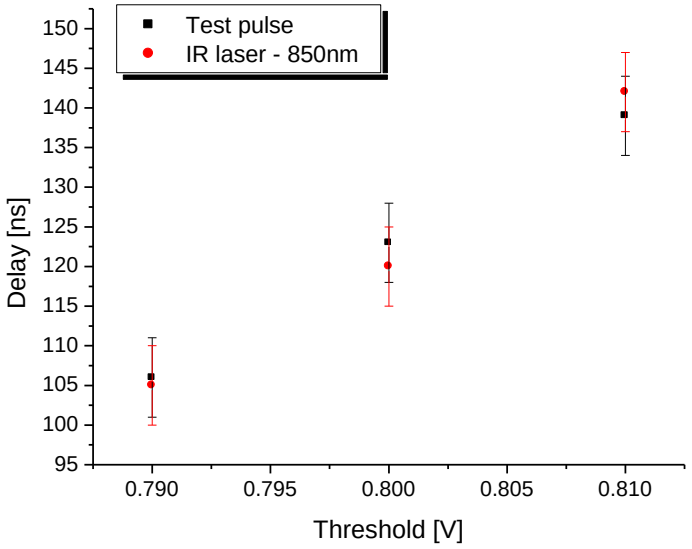


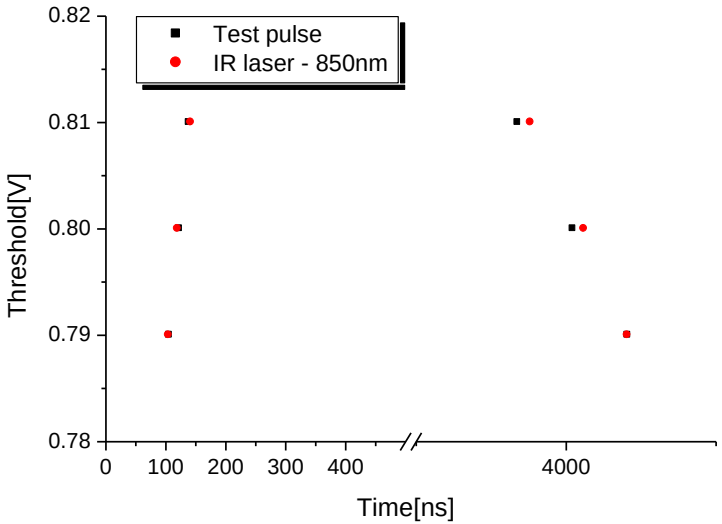

Absorption of 850nm light ~14µm
Similar spatial distribution of the charge generation as for MIPs



# Collection time measurement

- Charge collection time – IR laser, comparison with the fast capacitive injection.
- No measurable delay versus the capacitive test pulse.



# High-Voltage CMOS Detectors for ATLAS

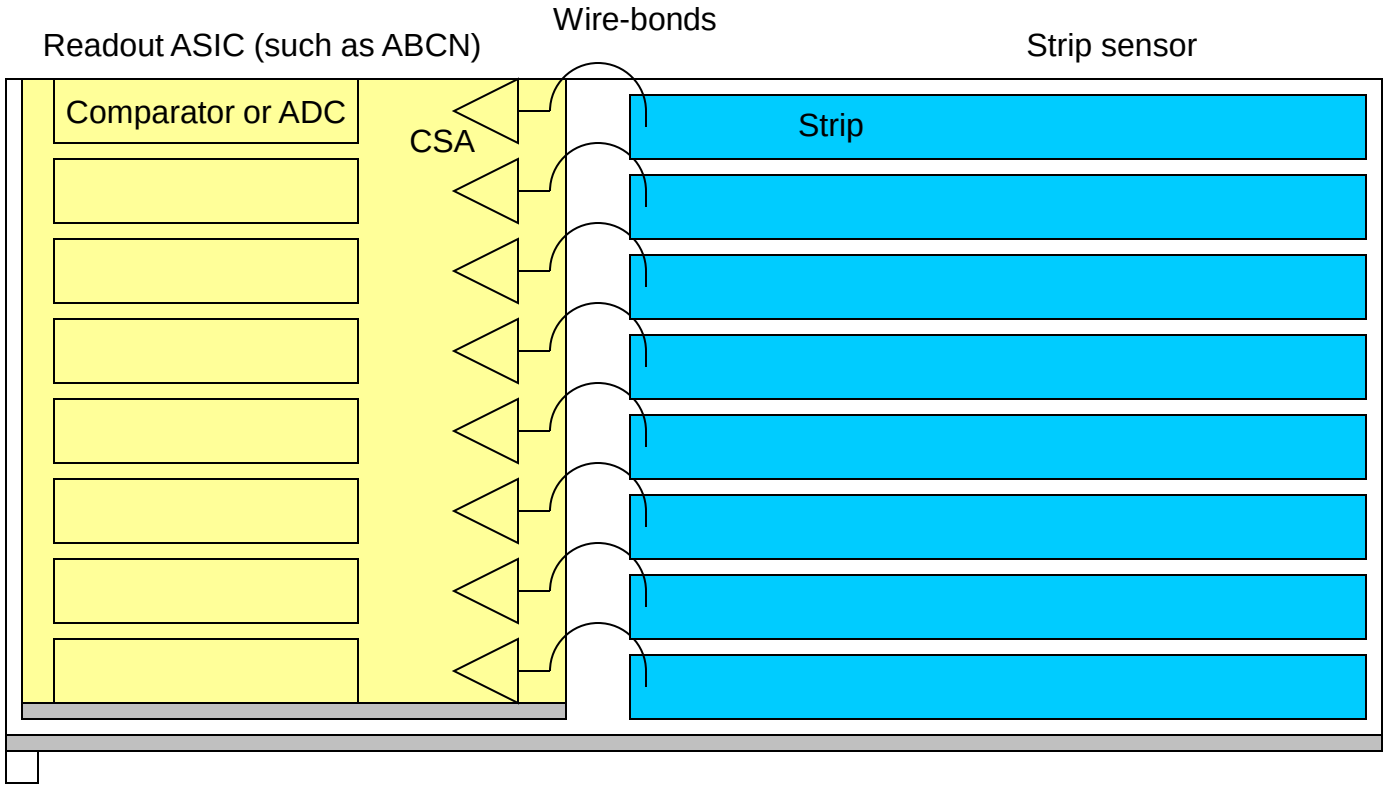
# High-Voltage CMOS Detectors for ATLAS/CLIC

- Smart sensor concept
- We use one of the existing RO chips for the readout of a HVCMOS sensor.
- This approach simplifies the design of sensor and allows us to use the existing readout- and data-acquisition-systems.

# Strip-like Concept

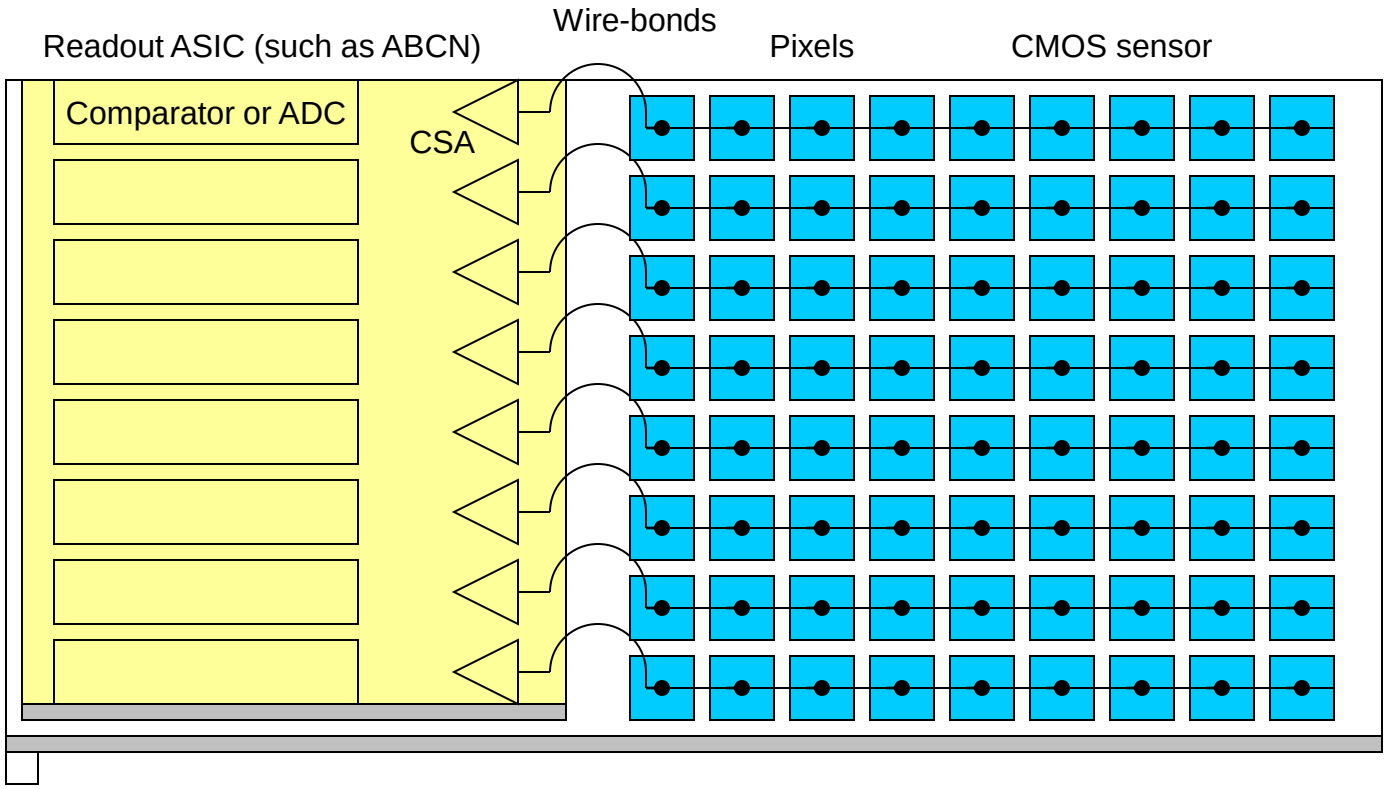
# Pixel detector compatible to strip-readout electronics

- The present LHC strip detectors consist of large-area strip sensors that are connected by wire bonds to multi-channel ASICs
- We use the strip readout ASIC for the readout of our SDA sensor



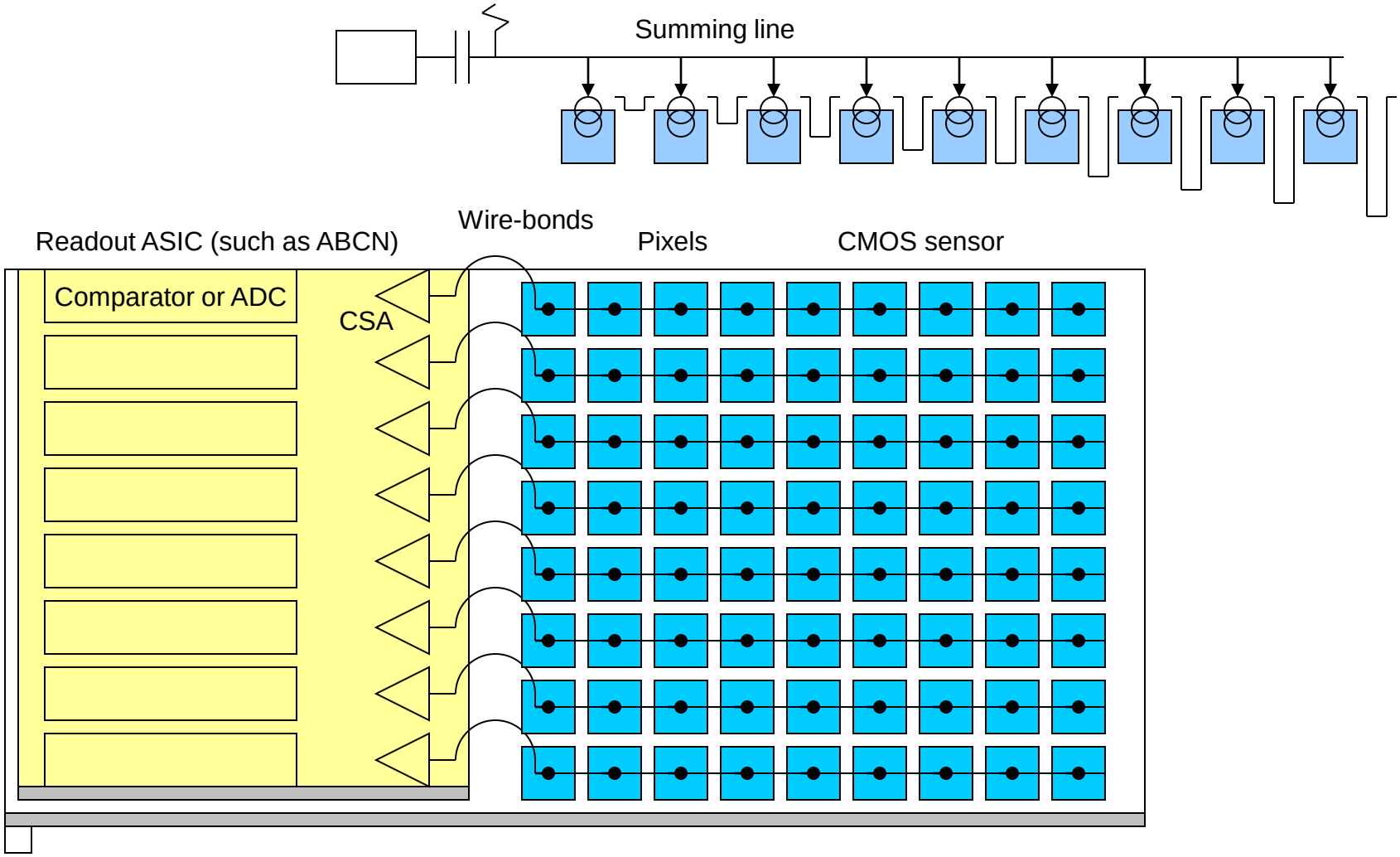
# Pixel detector compatible to strip-readout electronics

- We replace a strip with a line („gang“) of pixels

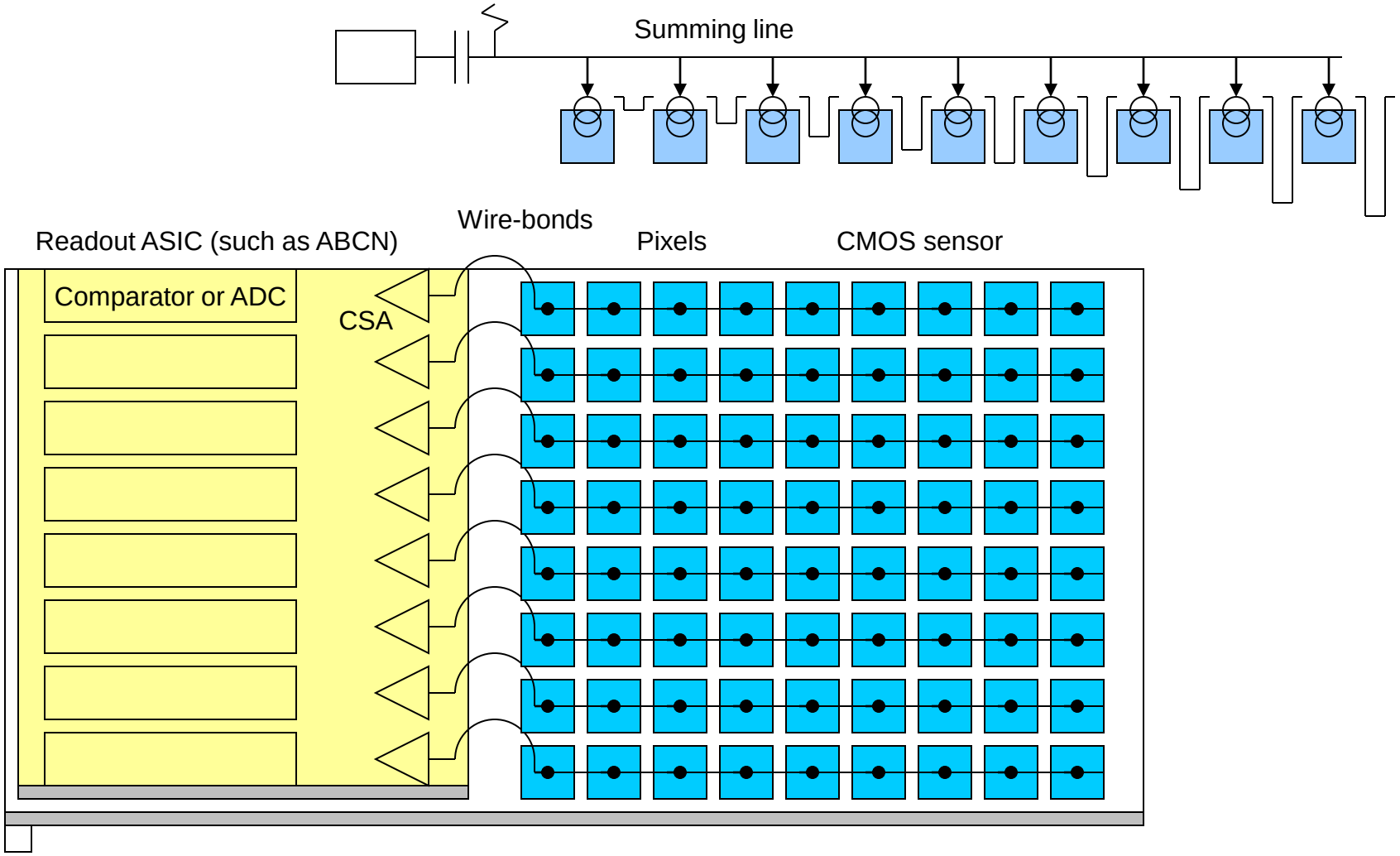


# Pixel detector compatible to strip-readout electronics

- Every pixel generates a digital current pulse with unique amplitude
- The pixel outputs are summed, converted to voltage signal and transmitted to readout ASIC by capacitive coupling

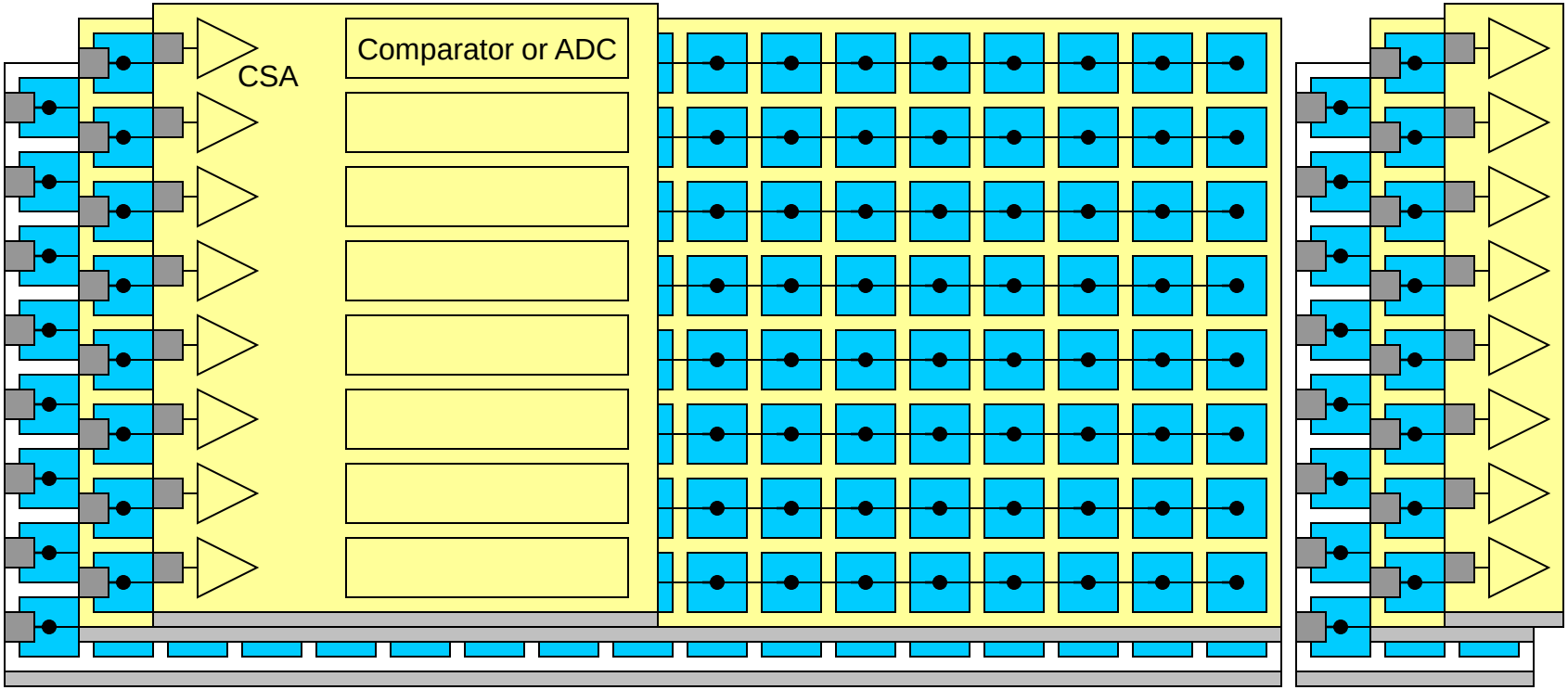


- The pixel address is transmitted as analog information



# Simultaneous readout from two 2D sensitive layers

- Simultaneous readout from two 2D sensitive layers. Signals from two sensor layers can be easily combined in a single readout ASIC



# Pixel detector compatible to strip-readout electronics

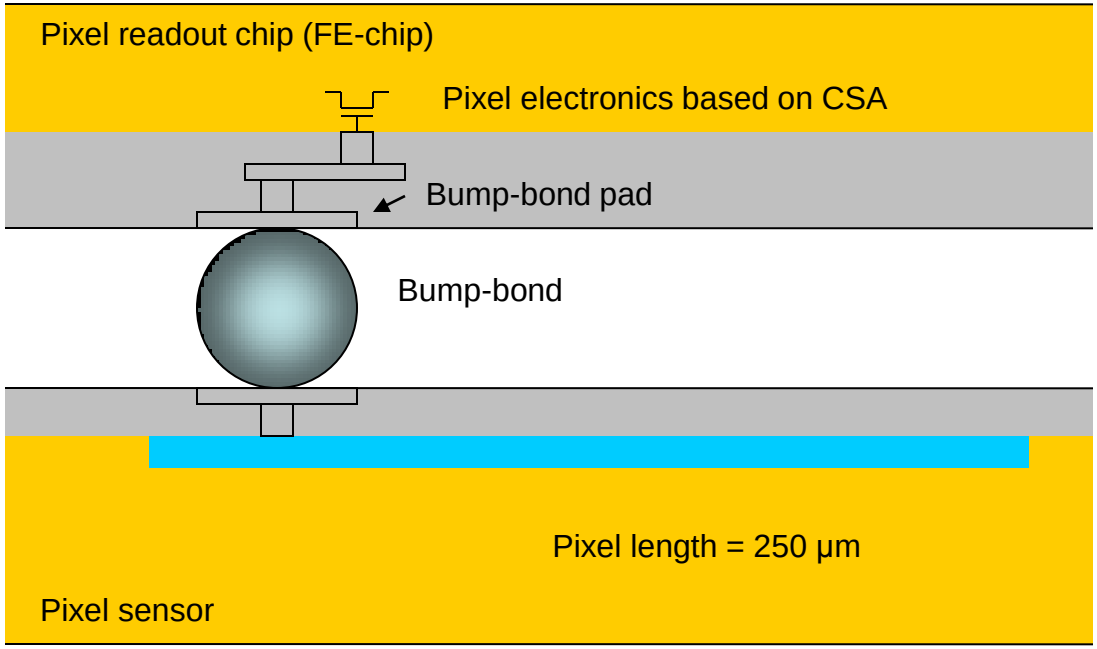
- A large area CMOS sensor can be produced by stitching several 2cm x 2cm wafer reticles.
- Any arbitrary pixel group pattern is possible.
- Advantages:
- Commercial sensor technology – lower price per unit area.
- Intrinsic 2D spatial resolution (e.g. 25 μm x 125 μm binary resolution)
- No need for bias voltages higher than 60V.
- Operation at temperatures above 0C is according to tests possible (irradiations to $10^{15}$ $n_{eq}/cm^2$).
- Thinning possible.

# CCPD Concept

# CCPD for ATLAS pixel detector

- We use one of the existing RO chips for the readout of an intelligent HVCMOS sensor.
- This approach simplifies the design of sensor and allows us to use the existing readout- and data-acquisition-systems.
- Intelligence: the pixels are able to distinguish a signal from the background and to respond to a particle hit by generating an address information.

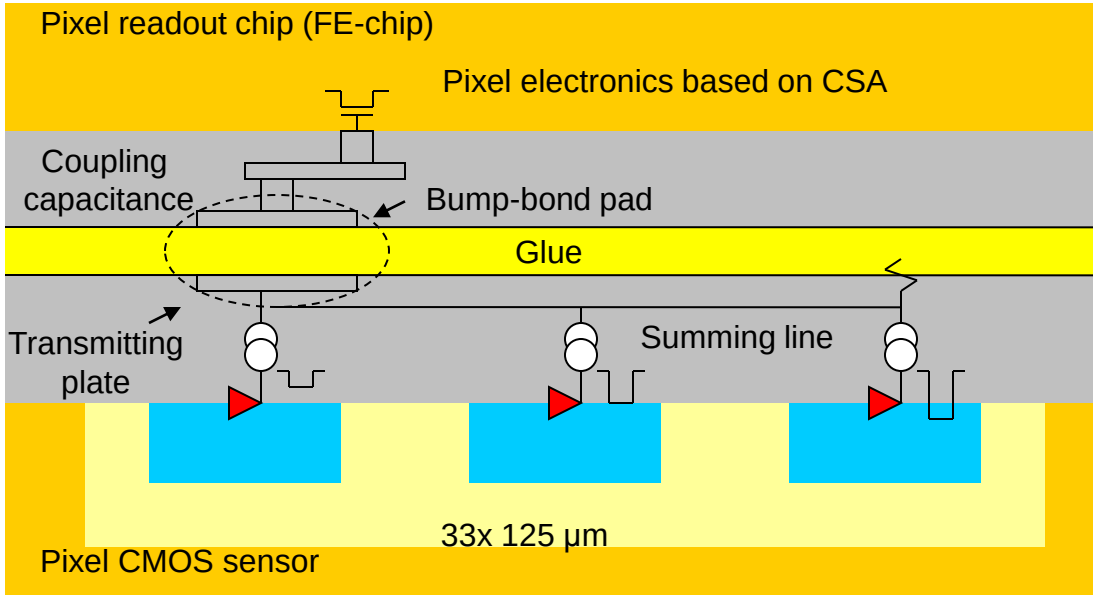
We replace the standard bump-bonded sensor with…



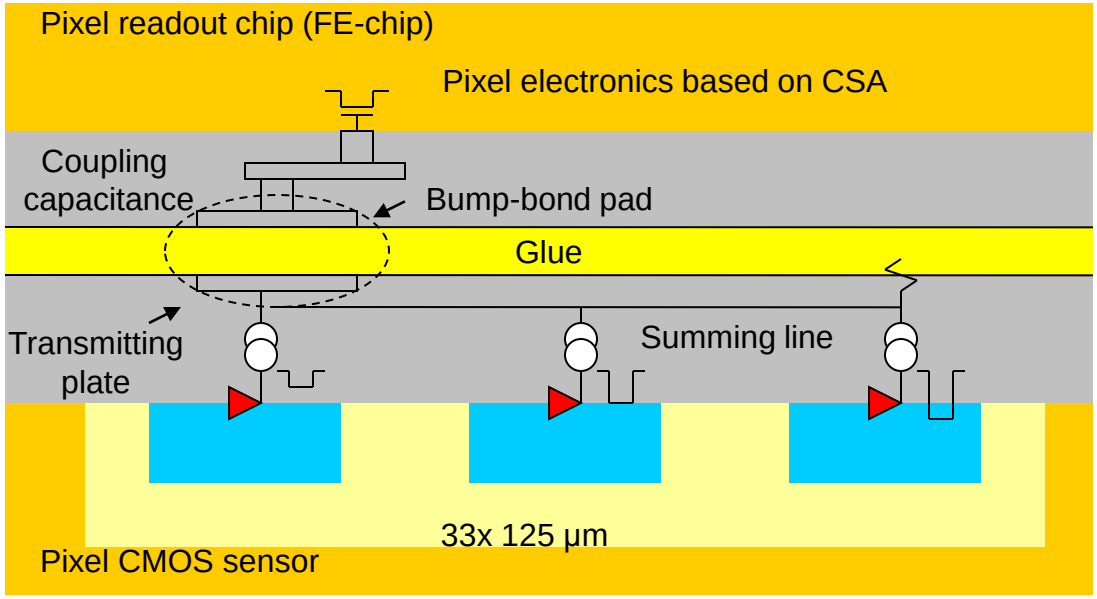
# CCPD for ATLAS pixel detector

- The HV CMOS sensor pixels are smaller than the standard ATLAS pixels, in our case 33μm x 125μm - so that three such pixels cover the area of the original pixel.
- The HV pixels contain low-power (~ 7μW) CMOS electronics based on a charge sensitive amplifier and a comparator.

…the capacitive coupled HV CMOS sensor



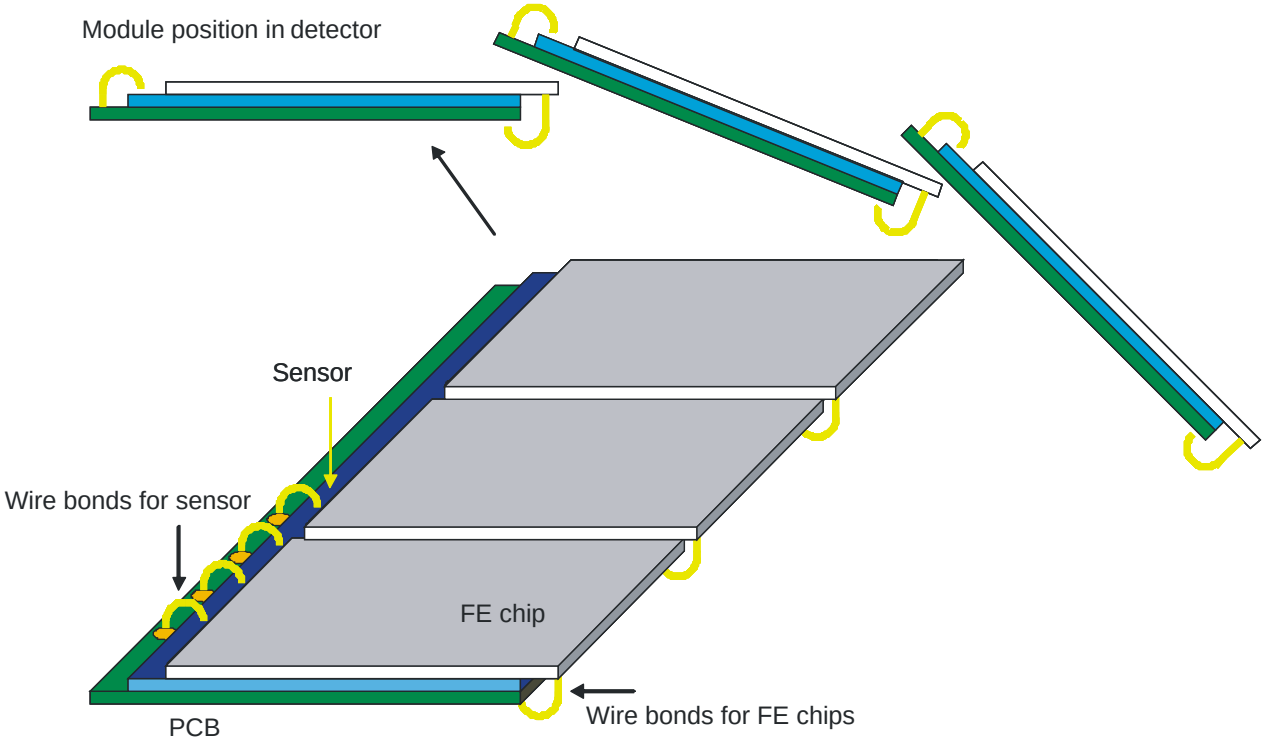
- The electronics responds to a particle hit by generating a pulse.
- The signals of a few pixels are summed, converted to voltage and transmitted to the charge sensitive amplifier in the corresponding channel of the FE chip using AC coupling.
- Each of the pixels that couple to one FE receiver has its unique signal amplitude, so that the pixel can be identified by examining the amplitude information generated in FE chip.
- In this way, spatial resolution in φ- and z-direction can be improved.



# Advantages compared to existing detectors

- No need for bump-bond connection between the sensor and readout chip – lower price, better mechanical stability, less material.
- Commercial technology – lower price.
- No need for bias voltages higher than 60V.
- Operation at temperatures above 0C is according to tests possible (irradiations to $10^{15}$ $n_{eq}/cm^2$).
- Increased spatial resolution (e.g. 25μm x 125μm binary resolution) with the existing FE chip
- Smaller clusters at high incidence angles.
- Possibility of sensor-thinning without signal loss. Since we do not use bumps and FE chips can be thinned as well, the amount of material would be very low.
- Interesting choice for other experiments where low-mass detectors are needed such as CLIC, ILC, CBM, etc...

# Module concept



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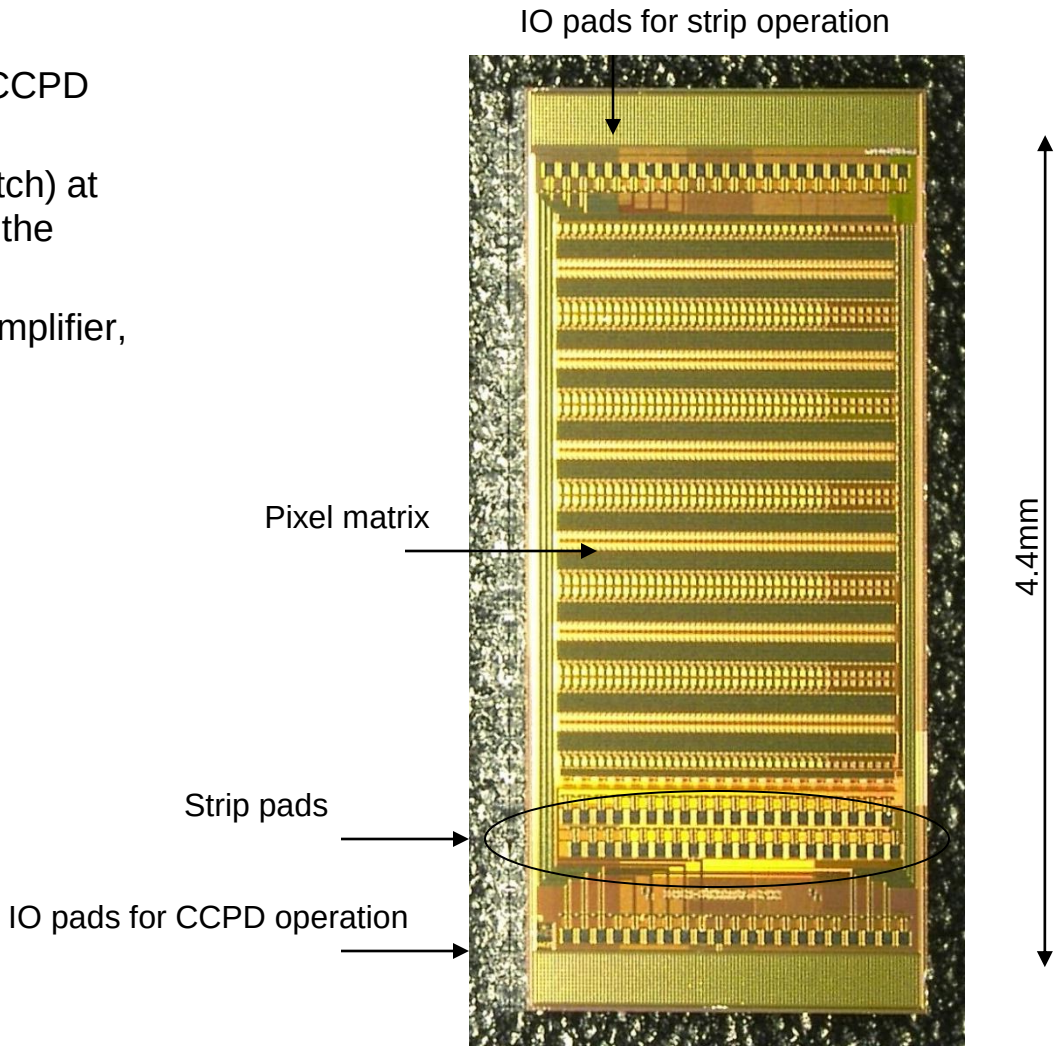
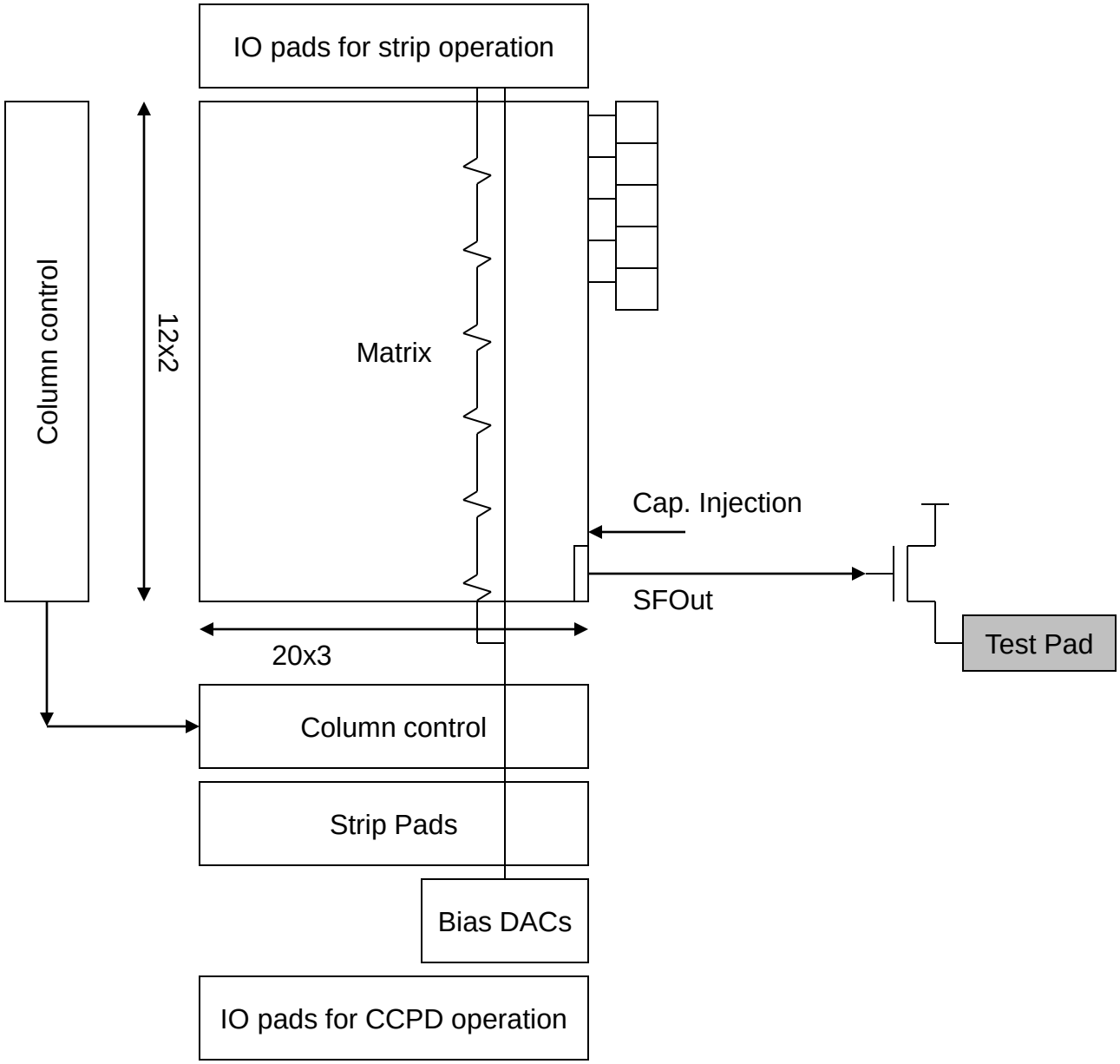
# Test Chip HV2FEI4

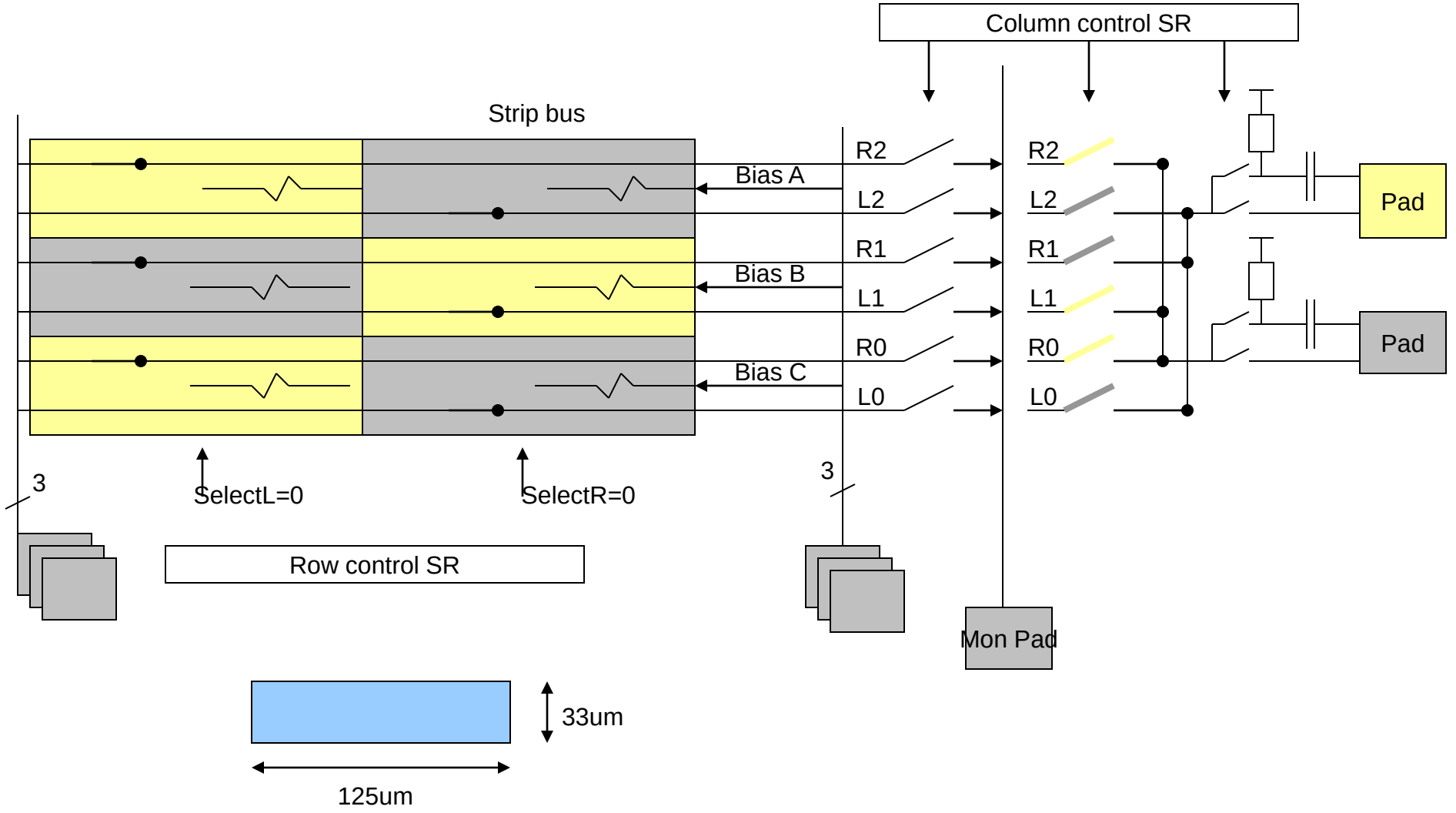
- Pixel matrix: 60x24 pixels
- Pixel size 33 μm x 125 μm
- 21 IO pads at the lower side for CCPD operation
- 40 strip-readout pads (100 μm pitch) at the lower side and 22 IO pads at the upper side for strip-operation
- Pixel contains charge sensitive amplifier, comparator and tune DAC.



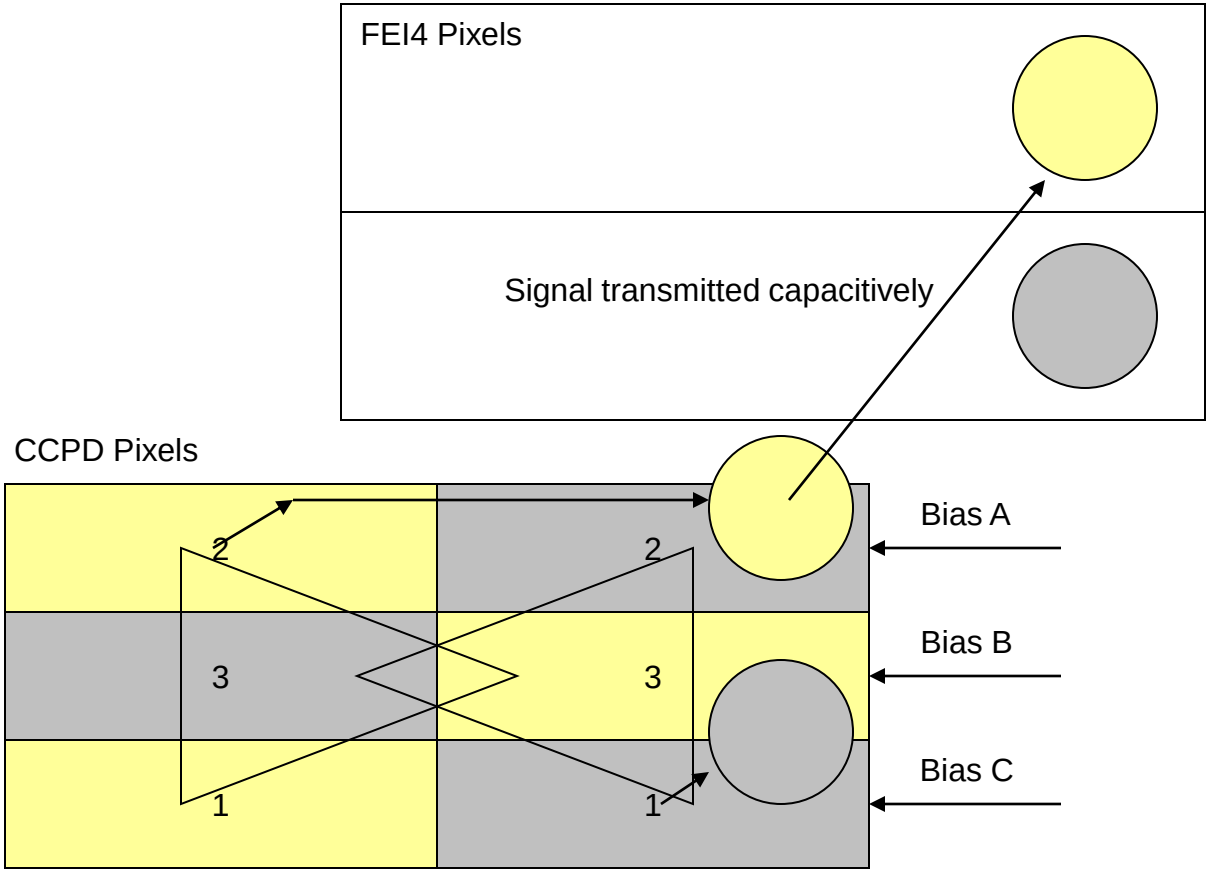
# HV2FEI4 - Architecture

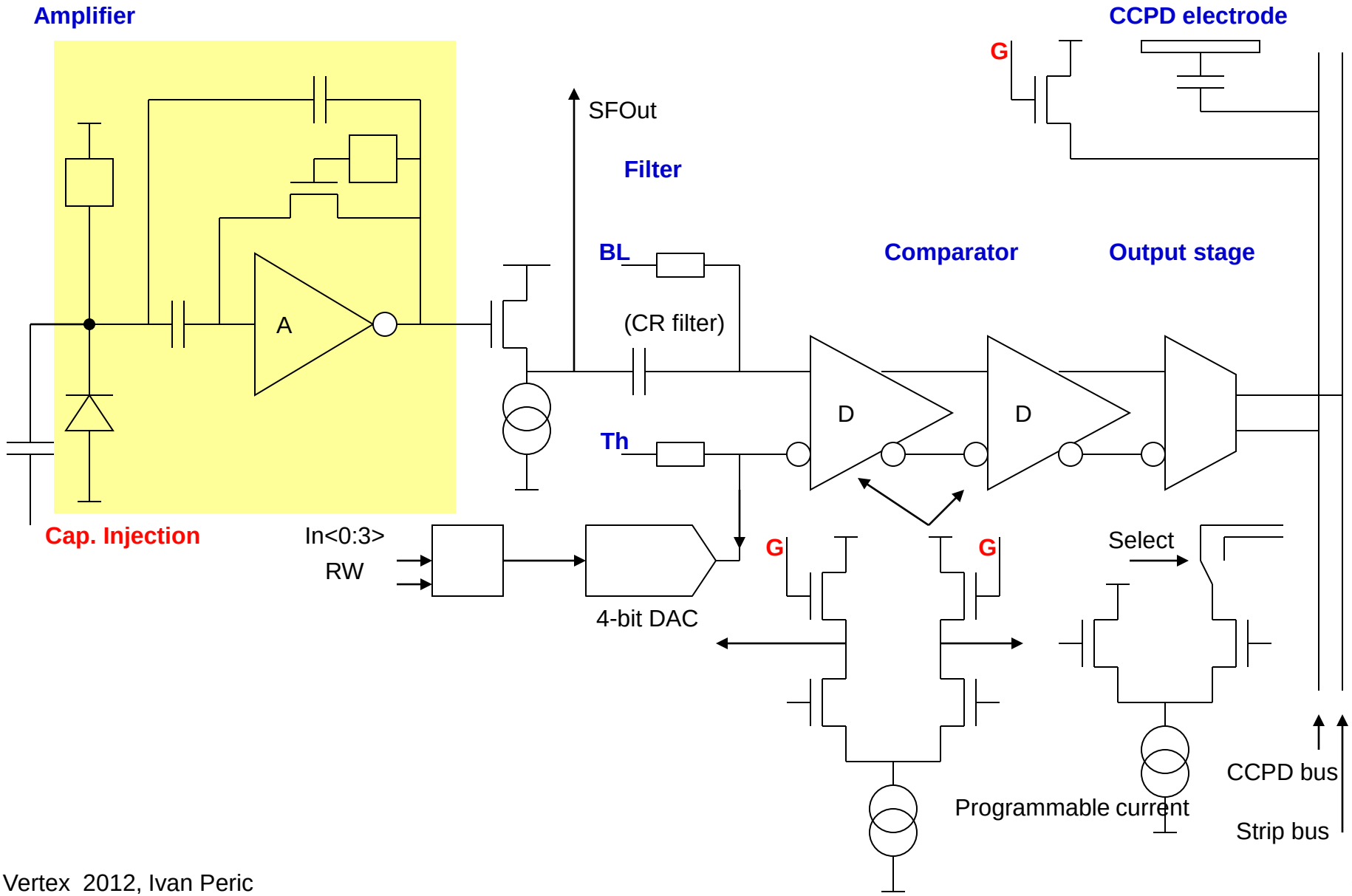


# Strip and Test-Operation

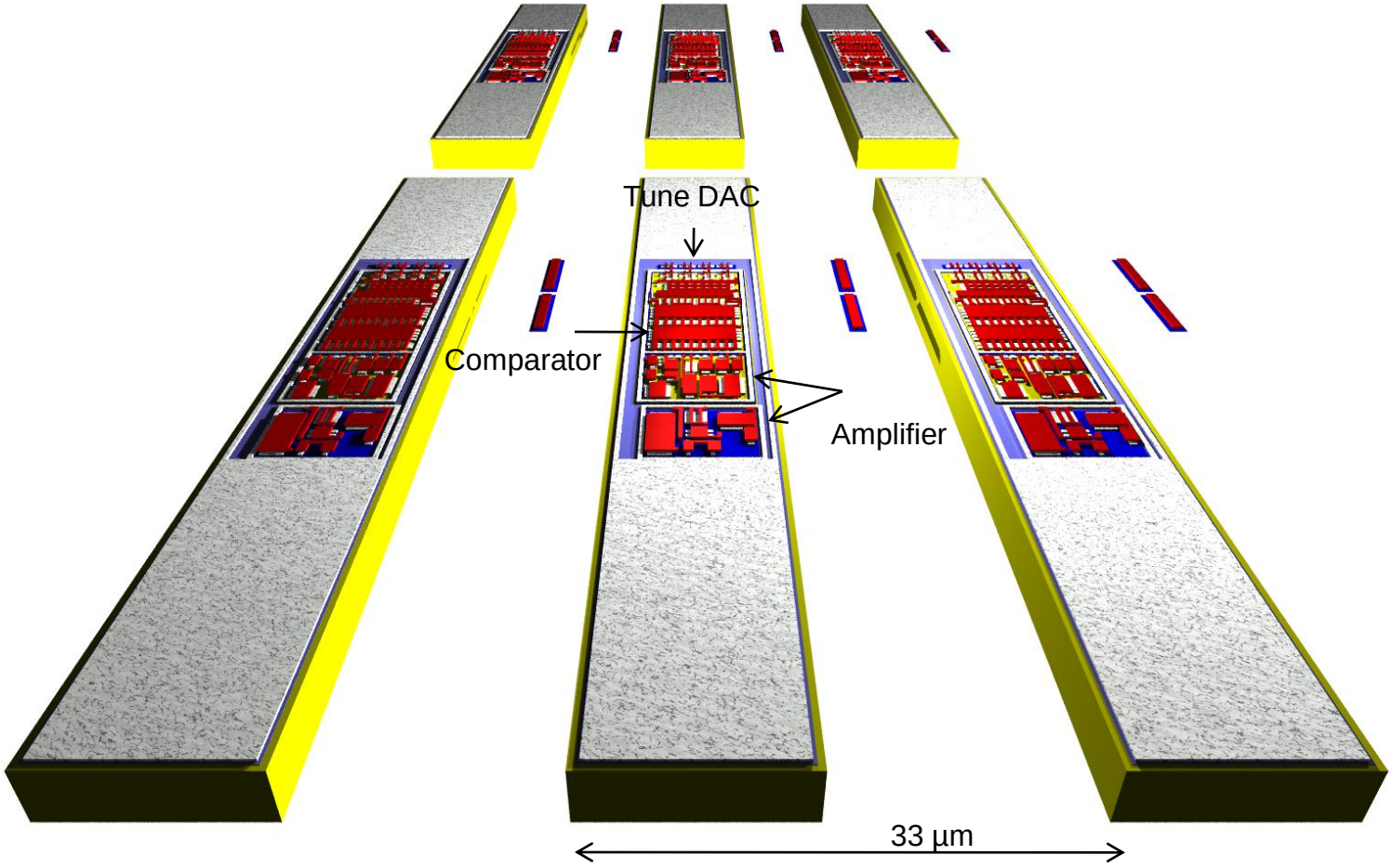


# CCPD Operation




Amplifier
CCPD electrode
G
SFOut
Filter
BL
Comparator
Output stage
(CR filter)
A
D
D
Th
Cap. Injection
In<0:3>
RW
4-bit DAC
G
G
Select
CCPD bus
Programmable current
Strip bus

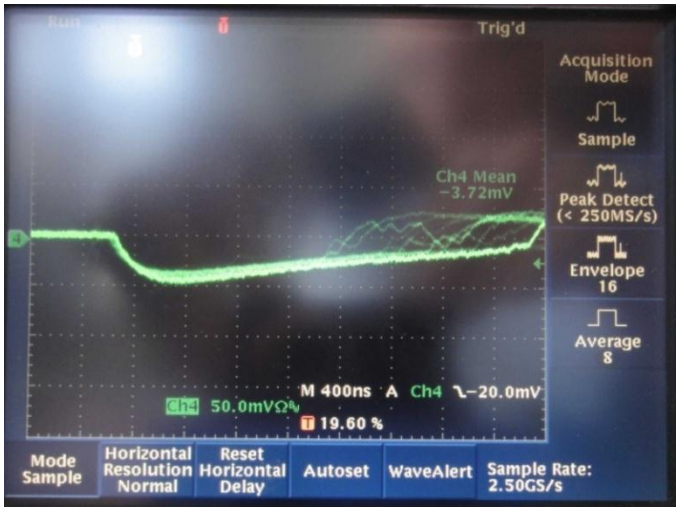
# 6 Pixels – Layout

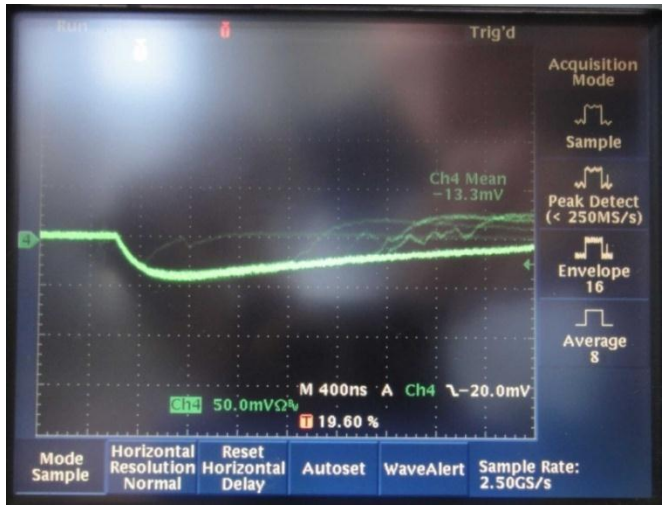


# Experimental results
# (strip operation)

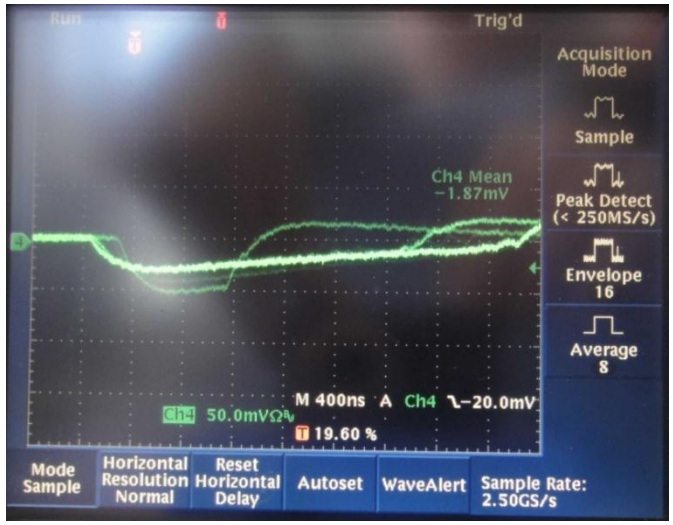
# Strip-like operation

"Hit-bus" operation – $^{55}$Fe signals – three pixel columns (each 24 pixels) readout in parallel
The amplitude is set to be equal for every pixel



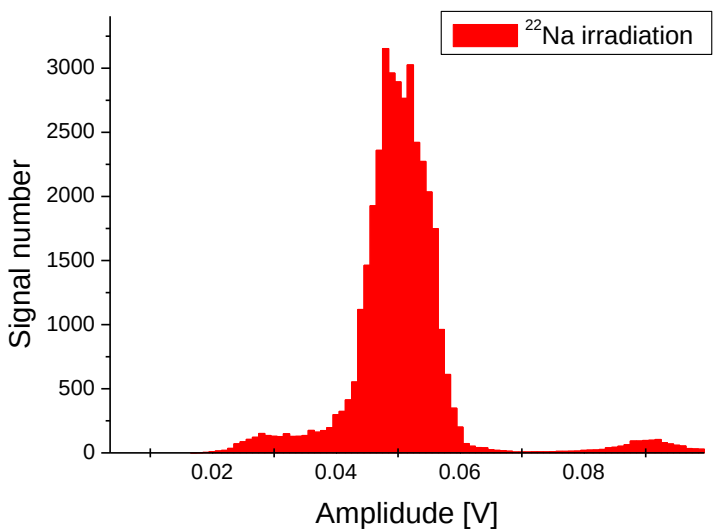



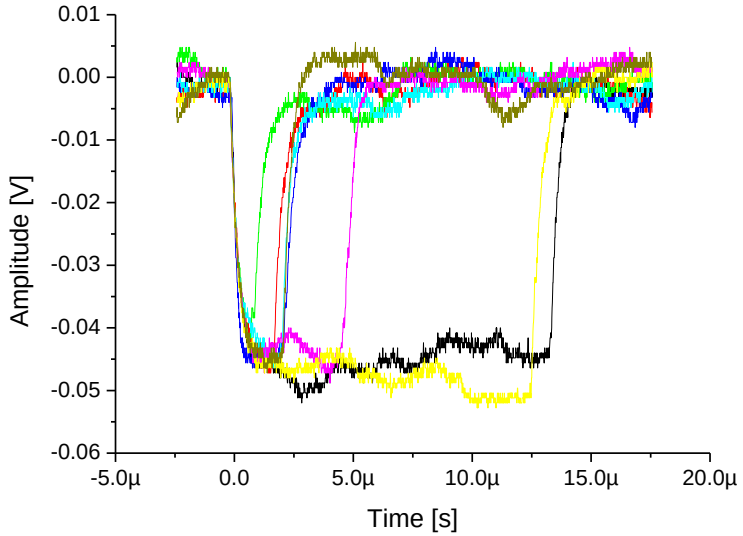

Strip like operation – $^{55}$Fe signals – three pixel columns (each 24 pixels) readout in parallel
The amplitude depends on pixel position

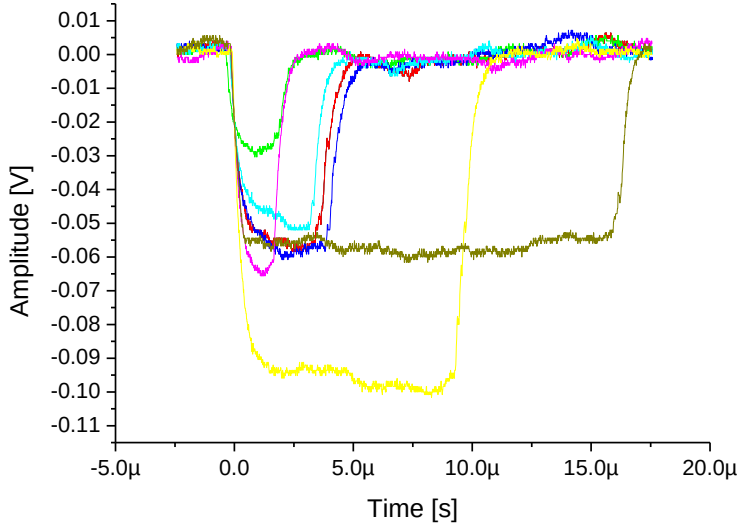
# Strip-like operation

"Hit-bus" operation – $^{22}$Na signals – one pixel columns (24 pixels) readout in parallel
The amplitude is set to be equal for every pixel - values around 50mV



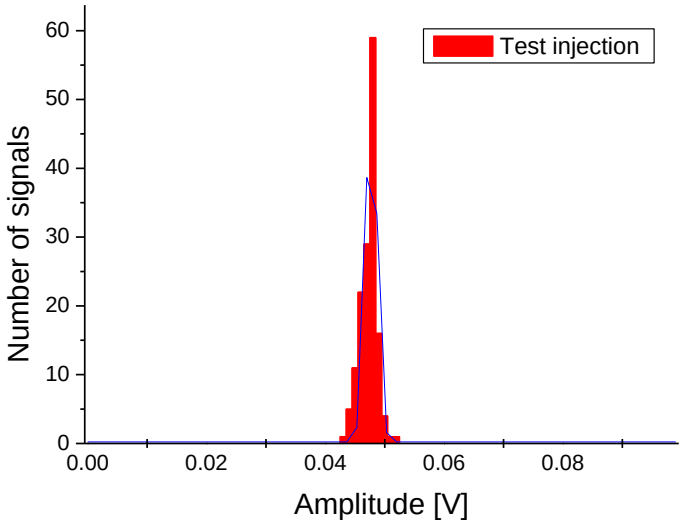



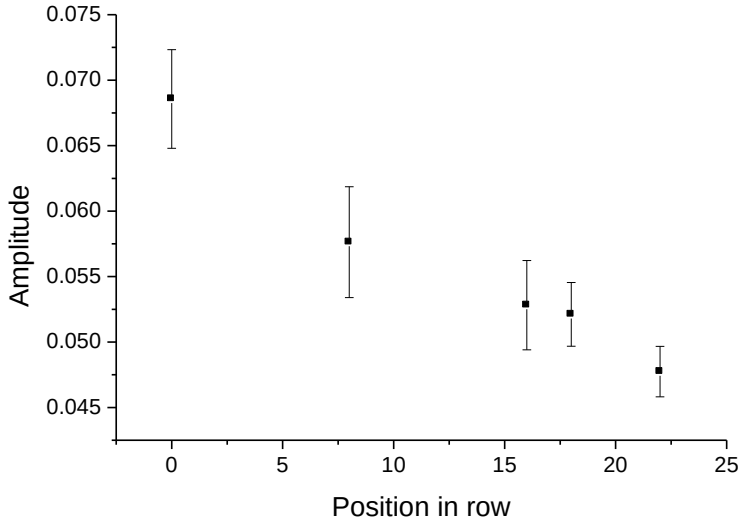

"Hit-bus" operation – $^{22}$Na signals – one pixel columns (24 pixels) readout in parallel
The amplitude depends on pixel position



# Strip-like operation

"Hit-bus" operation – test injection pulses (~ 1700e)
The amplitude depends on pixel position



# Irradiation at PS (CERN)

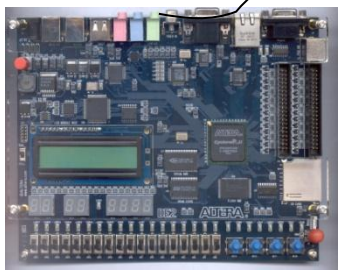
The system allows to read by using the MONITOR signal, and to write the HV2FEI4 chip

Irradiation area

The on-board LVDS chip runs to load the HV2FEI4 chip.

The Analog current-shaped "Monitor" signal is read-back and amplified through an analog amplifier

RS232



DE2 board

LVDS 20m long cable

4 signals

5V max

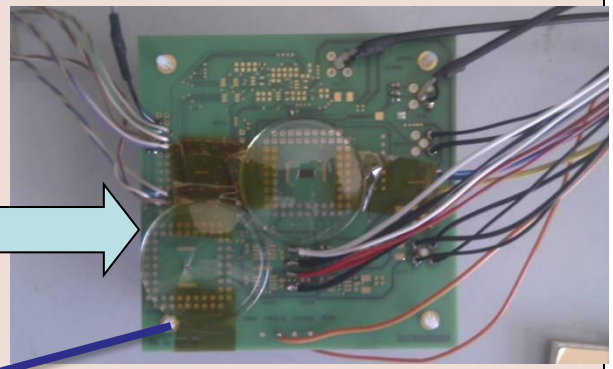
3,3V

io

Lvds

5m

4 signals



Monitor signal 20m long cable

Monitor signal

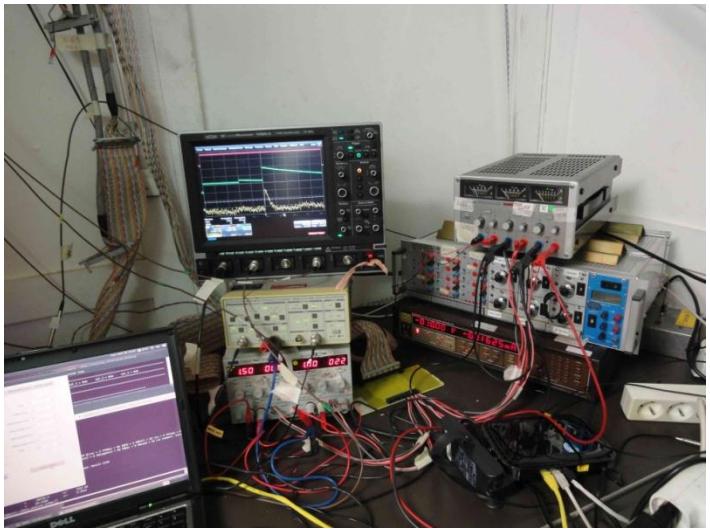
0,4V max

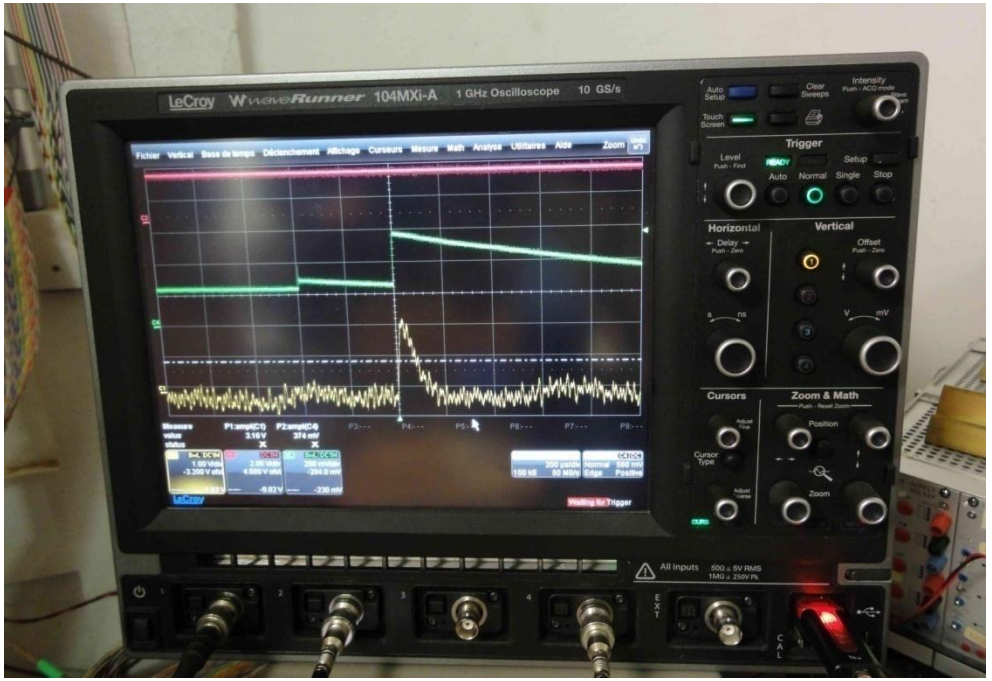
HV2FEI4

Board n°2

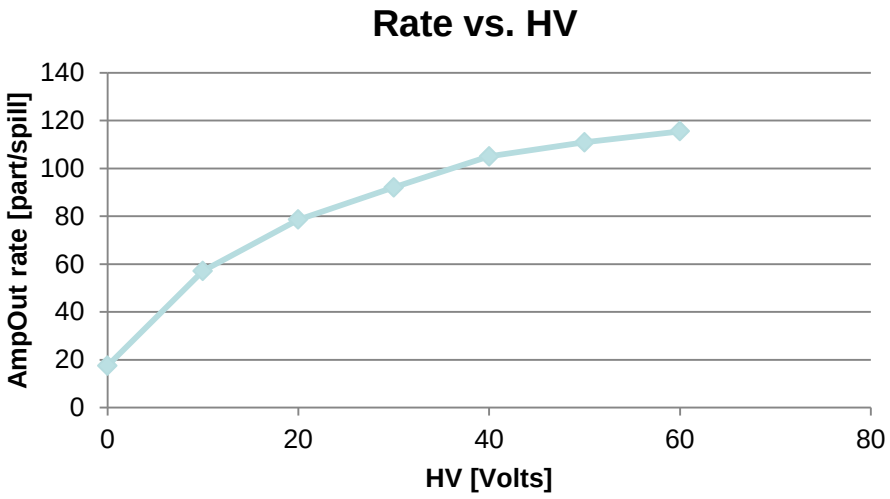
VDDA – VSSA – Threshold – Gate – HV

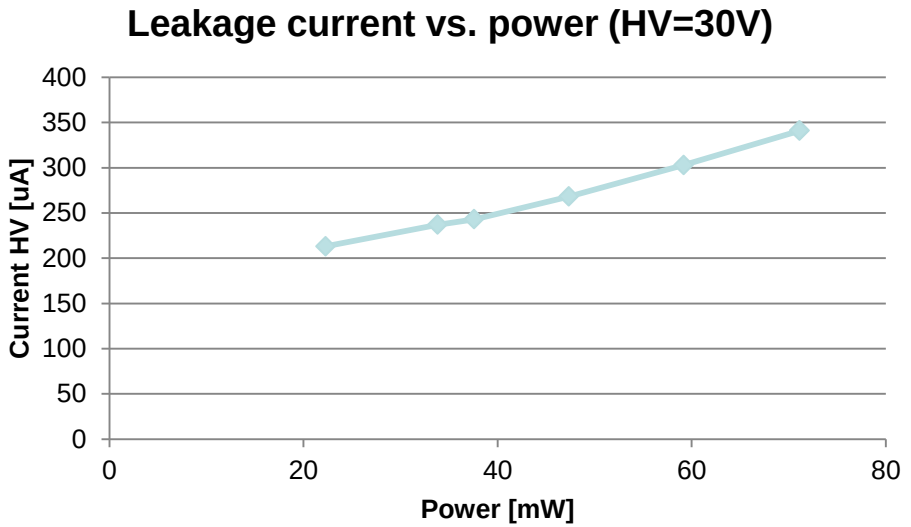
# Results after 144 MRad

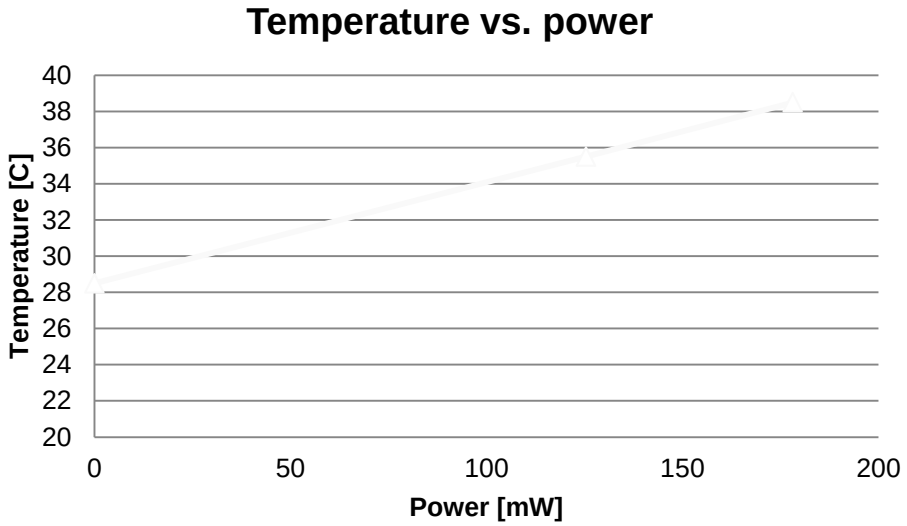


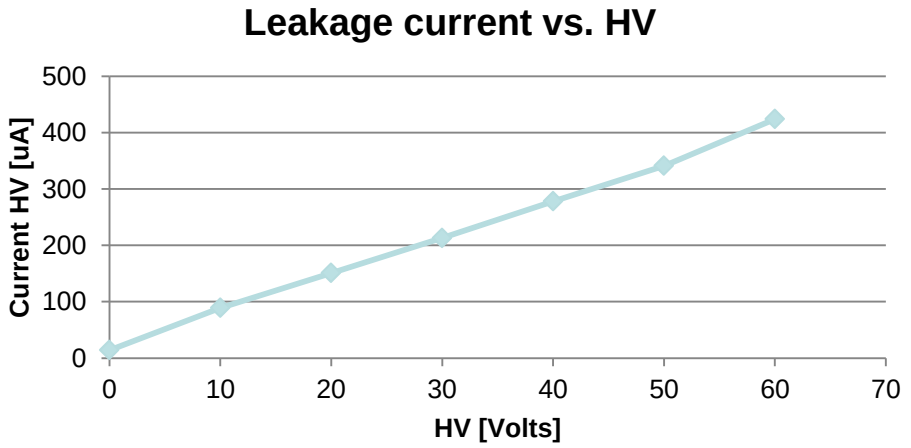


# Results after 144 MRad



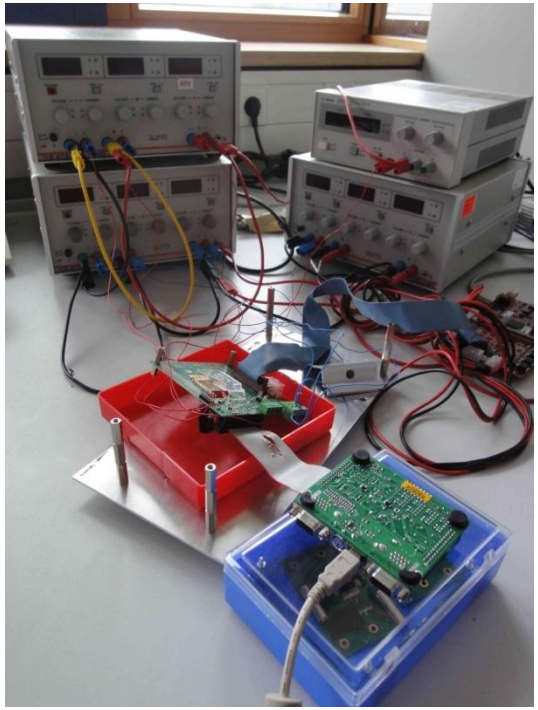



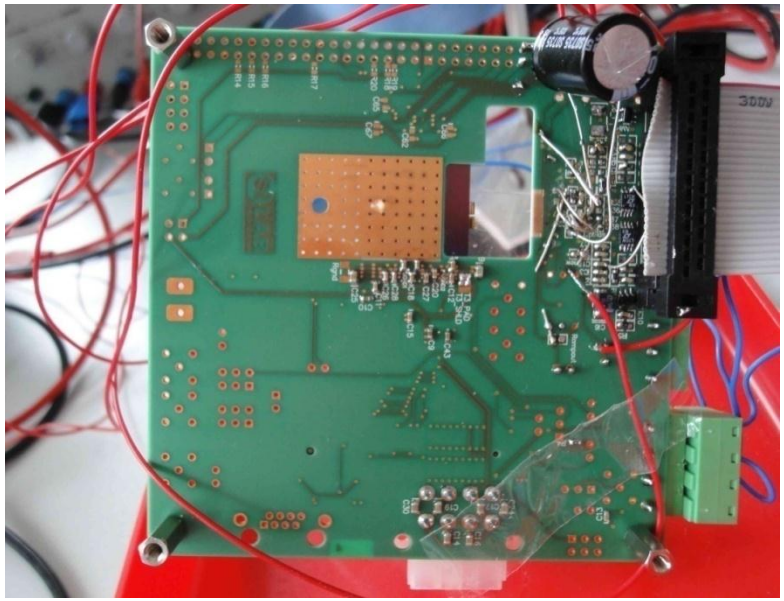



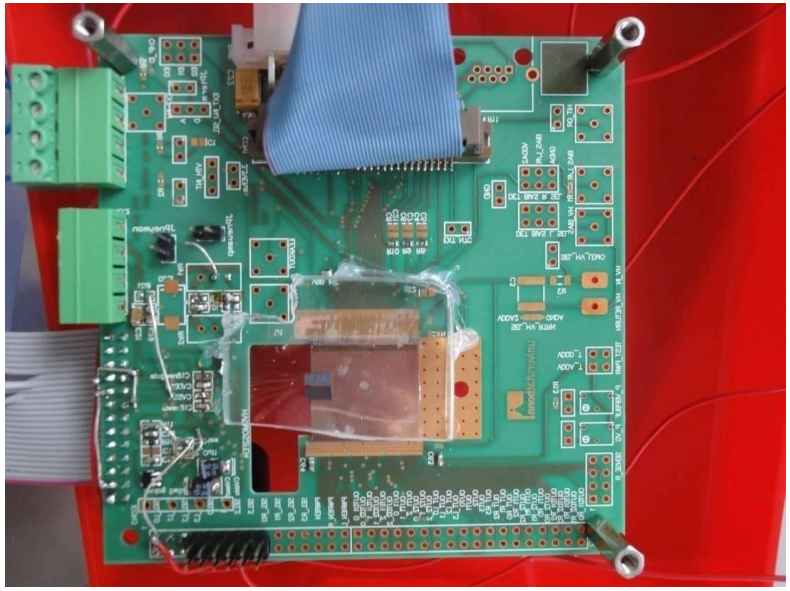



# Experimental results
# (CCPD operation)

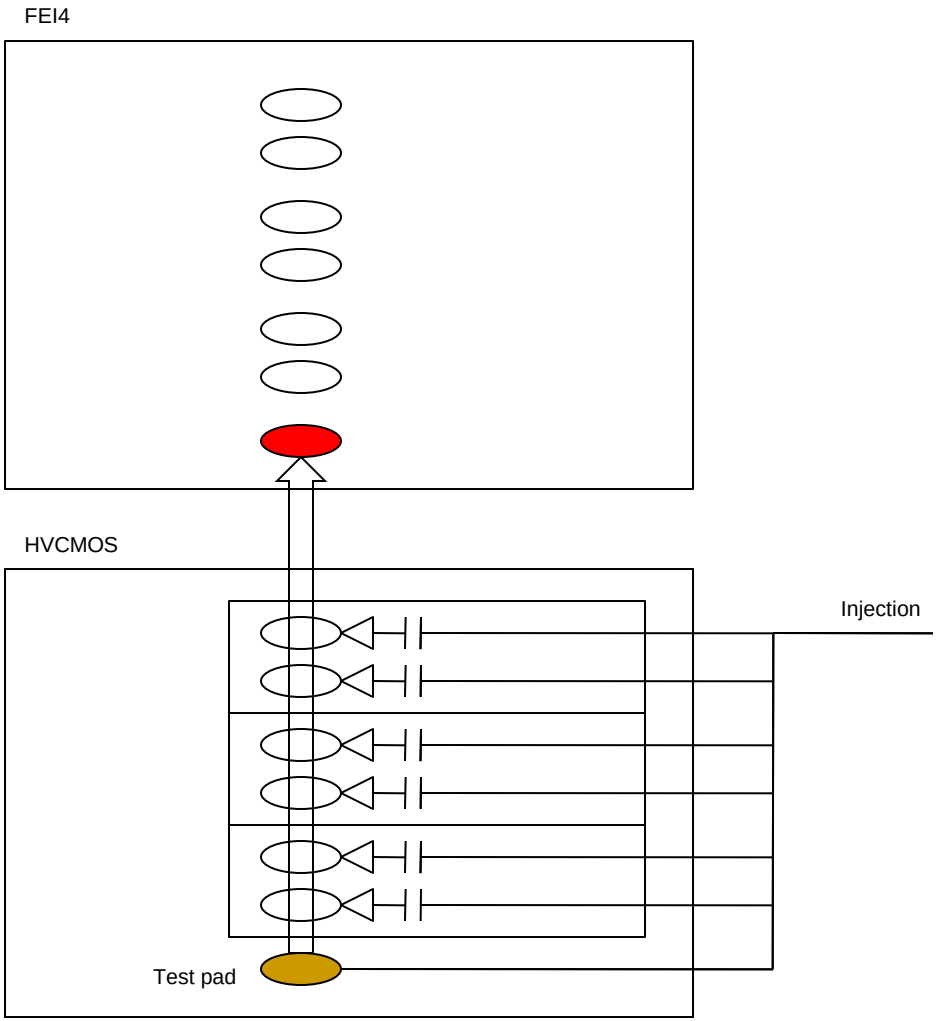
# Measurement setup



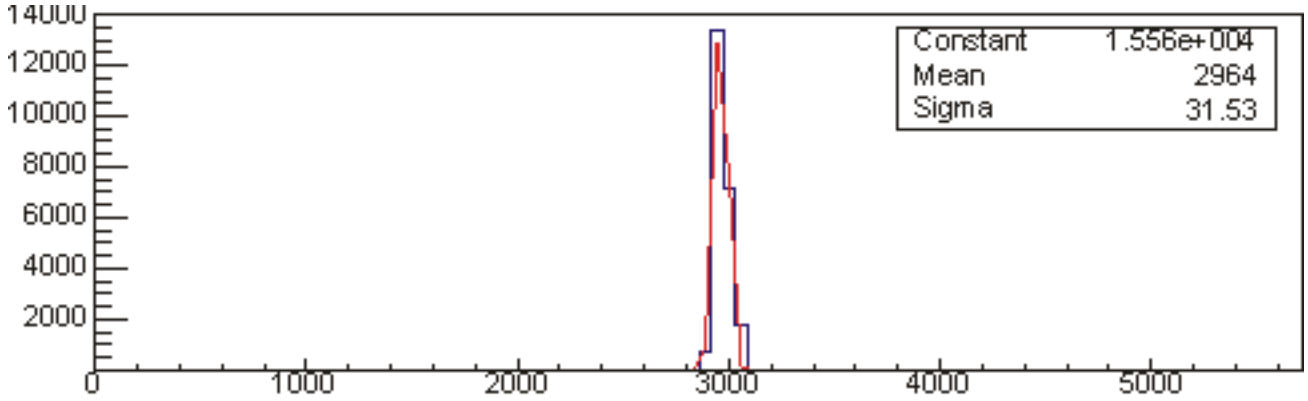


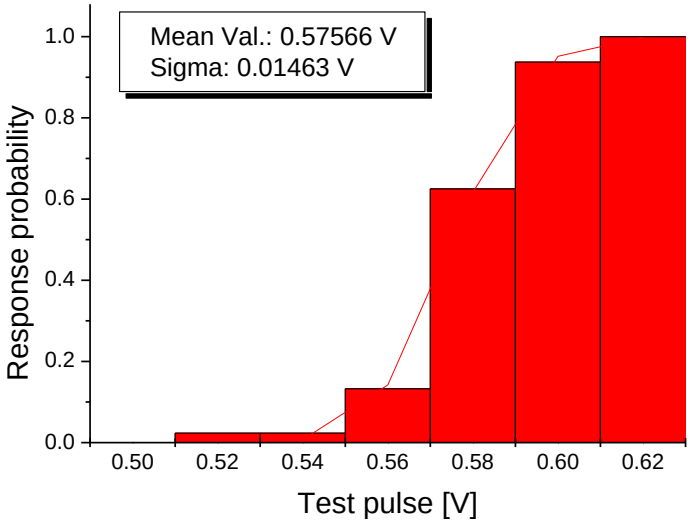



# Measurements with test pad

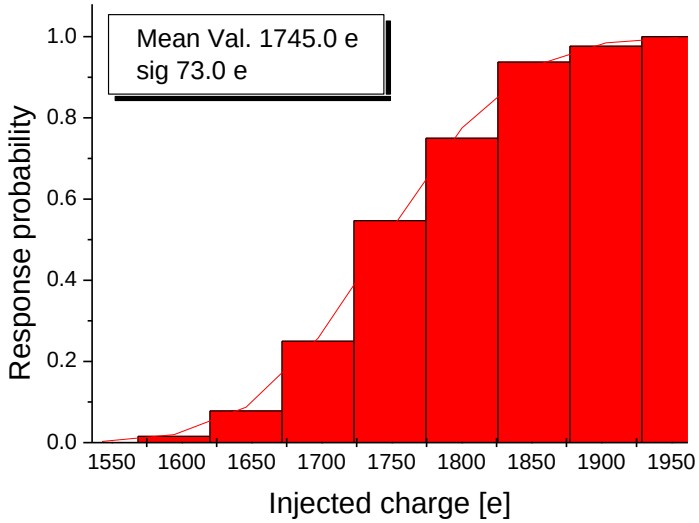


# Measurements with test pad



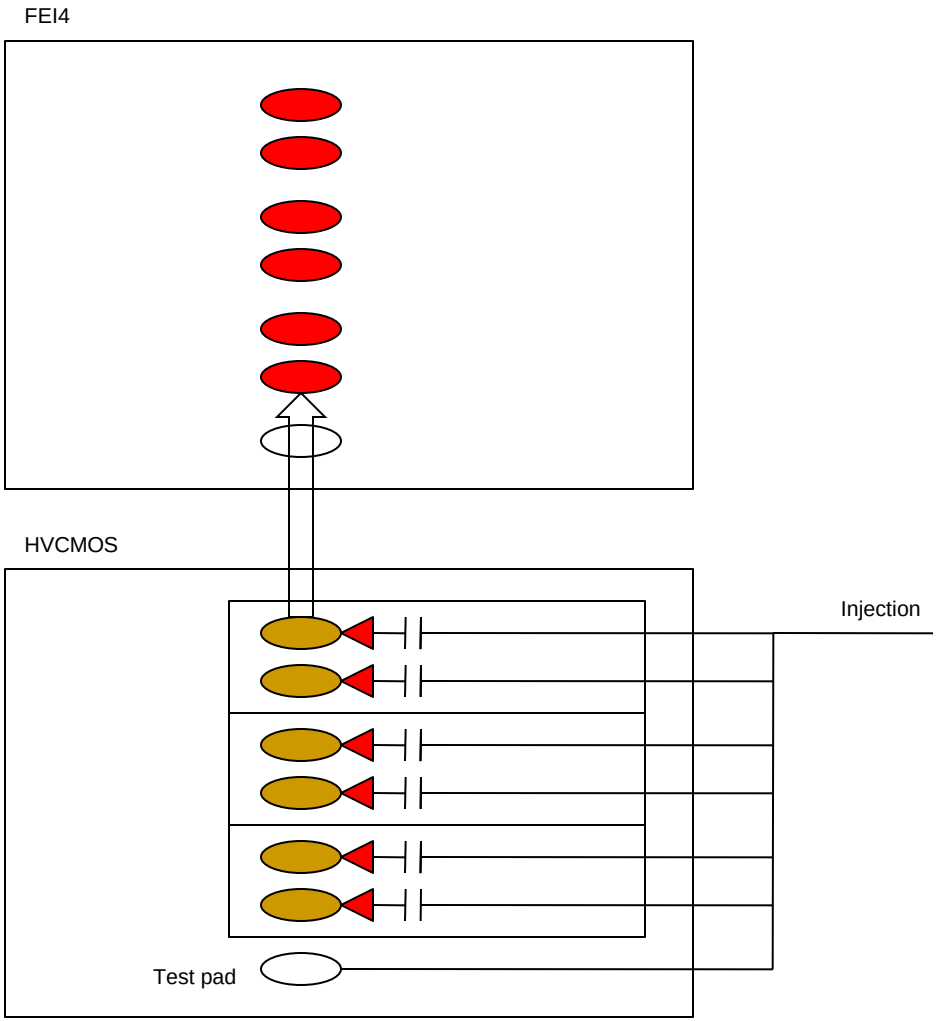



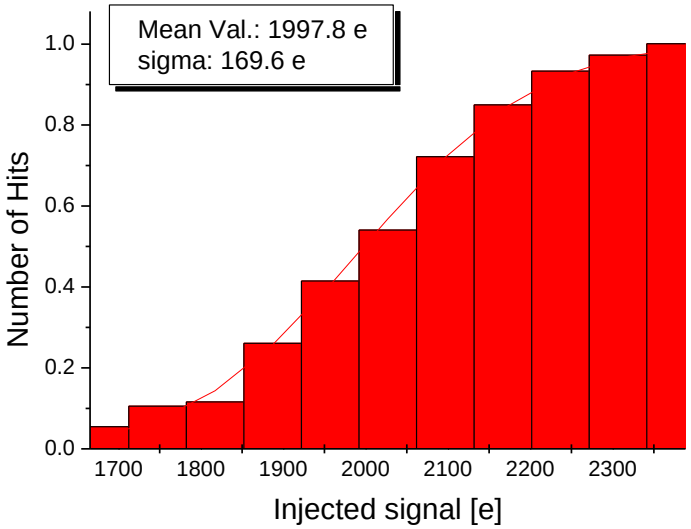

0.577V -> 2964e =>
Capacitance = 0.824fF



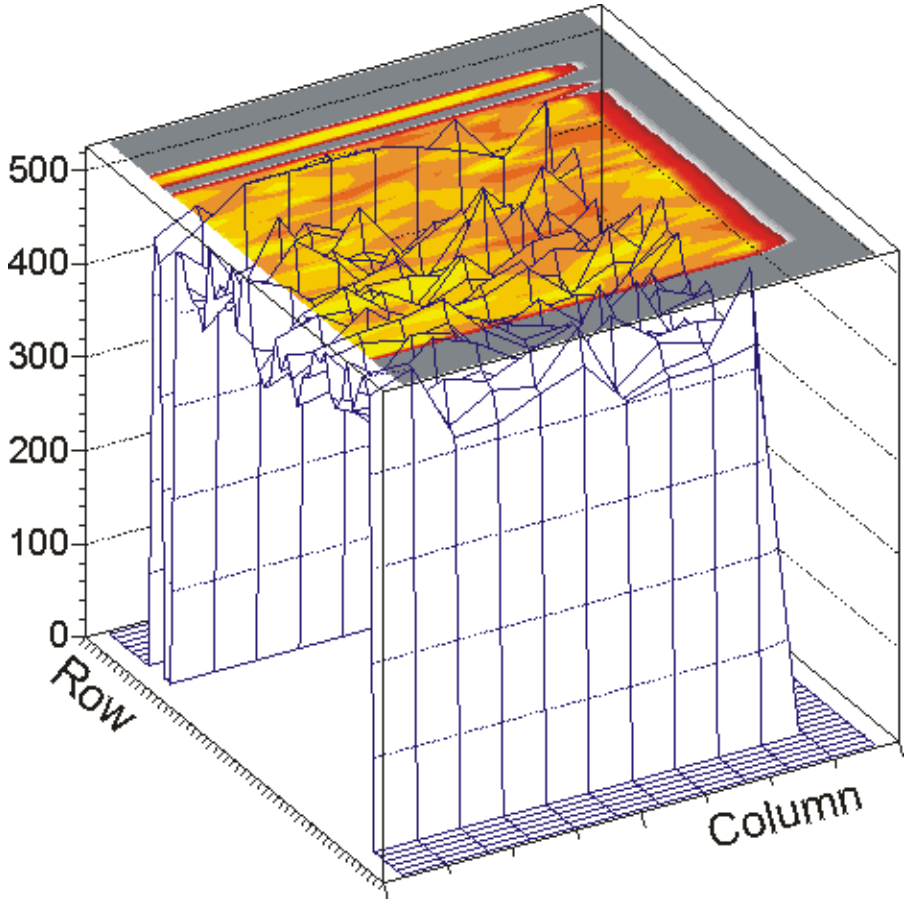

Calibrated input: FEI4 noise 73e
(FEI4 threshold was set to 1300e)

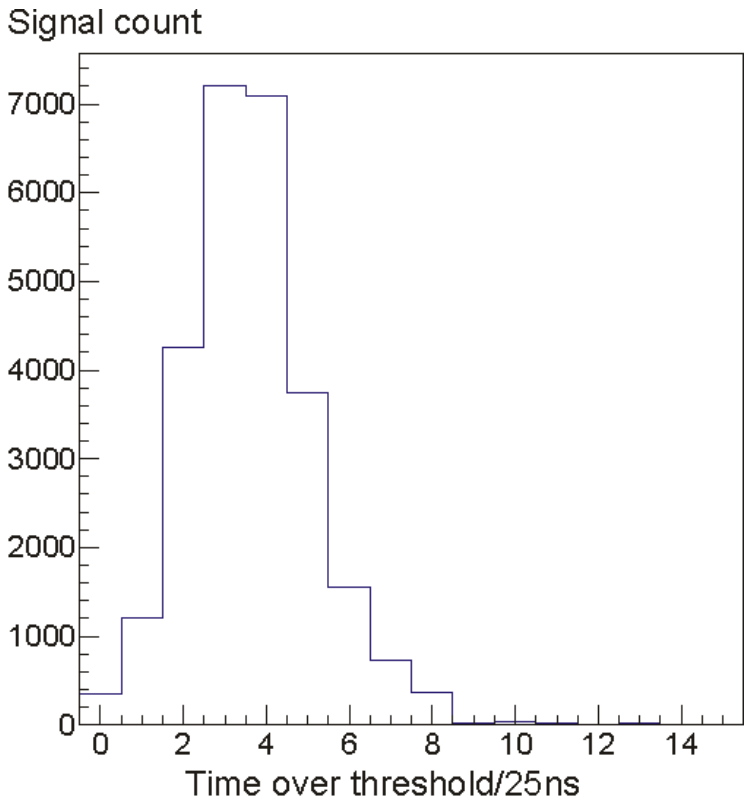
# Measurements with active pixels and test injection



# Measurements with Na22 beta source



# Conclusions

- We are investigating the use of HVCMOS technology for ATLAS detectors
- The concept: Intelligent sensors in HVCMOS technology readout by the existing readout ASCIs
- Advantages:
- Commercial sensor technology – lower price per unit area.
- No need for bias voltages higher than 60V.
- Operation at temperatures above 0C is according to tests possible (irradiations to $10^{15}$ $n_{eq}/cm^2$).
- Thinning possible.
- Test chip HV2FEI4 has been tested in the stand alone mode and as a CCPD readout with FEI4
- First measurements with a strip readout chips will be done soon.
- In stand alone mode, we measure good performances of the HVCMOS chip
- In CCPD mode, noise somewhat increased due to non optimal setup
- Irradiation ongoing, we have reached 180MRad so far, the detector still works – leakage current increased (temperature: 38C).

Thank you

# Backup Slides

# Experimental results - overview

HVPixel1 – **CMOS in-pixel electronics with hit detection**
Binary RO
Pixel size 55x55µm
**Noise 60e**
**MIP seed pixel signal 1800 e**
Time resolution 200ns

**Capacitive coupled hybrid detector**

CCPD2 -**capacitive coupled pixel detector**
Pixel size 50x50µm
Noise 30-40e
Time resolution 300ns
**MIP SNR 45-60**

**Irradiations of test pixels**
**60MRad – MIP SNR 22 at 10C (CCPD1)**
**$10^{15} n_{eq}$ MIP SNR 50 at 10C (CCPD2)**

HV2FEI4 chip (first test next week!!!)
**CCPD for ATLAS pixel detector**
Readout with FEI4 chip
**Reduced pixel size: 33x125µm**
RO type: capacitive and strip like
3 pixels connected to one FEI channel

**Monolithic detector – continuous readout with time measurement**

MuPixel –
**Monolithic pixel sensor for Mu3e experiment at PSI**
Charge sensitive amplifier in pixels
Hit detection, zero suppression and time measurement at chip periphery
Pixel size: 39x30 µm (test chip)
(80 x 80 µm required later)
MIP seed signal 1500e (expected)
Noise: ~40 e (measured)
**Time resolution < 40ns**
**Power consumption 7.5µW/pixel**

**Monolithic detector - frame readout**

PM2 chip - frame mode readout
Pixel size 21x21µm
4 PMOS pixel electronics
128 on-chip ADCs
Noise: 21e (lab) - 44e (test beam)
MIP signal - cluster: 2000e/seed: 1200e
Test beam: **Detection efficiency >98%**
**Seed Pixel SNR ~ 27**
Cluster signal/seed pixel noise ~ 47
**Spatial resolution ~ 3.8 µm**

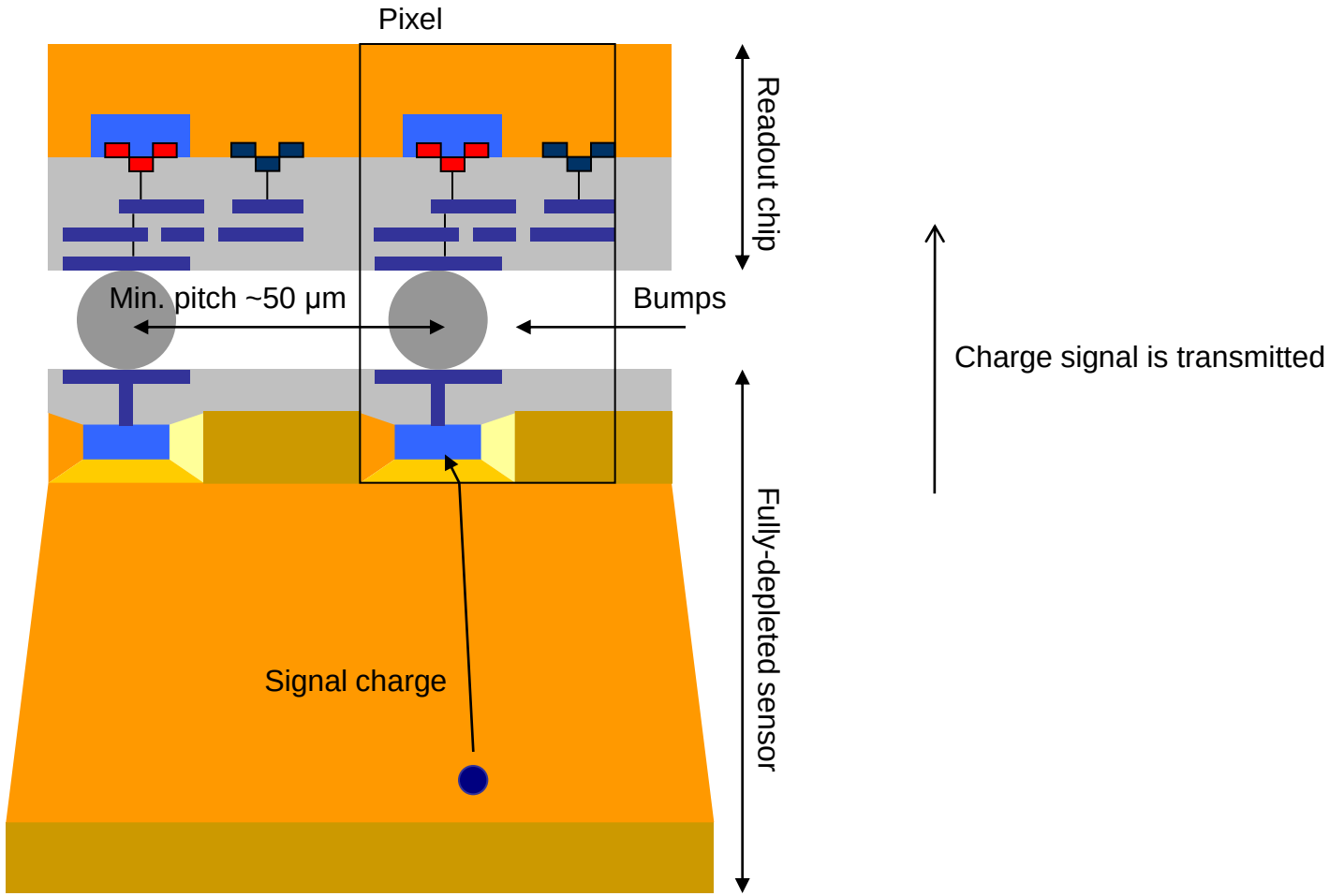
HPixel - frame mode readout
**In-pixel CMOS electronics with CDS**
128 on-chip ADCs
Pixel size 25x25 µm
Noise:60-100e (preliminary)
MIP signal - cluster: 2100e/seed: 1000e (expected)

SDS - frame mode readout
**Pixel size 2.5x2.5 µm**
4 PMOS electronics
Noise: 20e (preliminary)
MIP signal (~1000e - estimation)

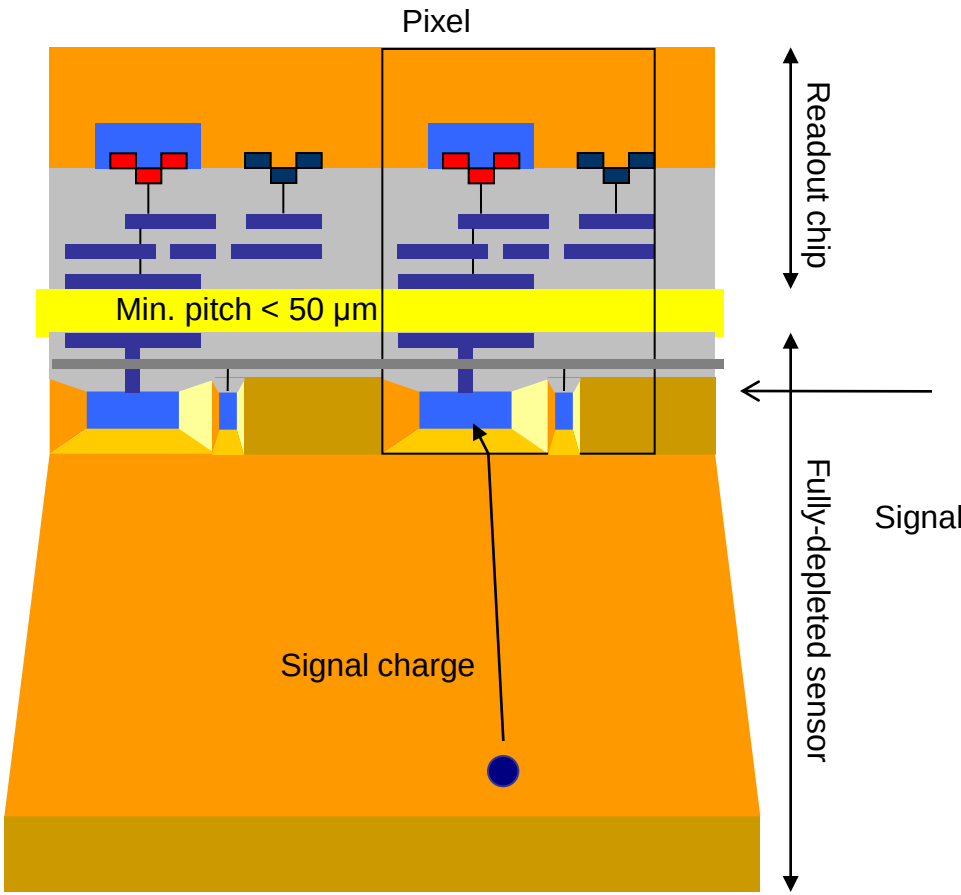
1. Technology 350nm HV – substrate 20 Ωcm uniform
2. Technology 180nm HV – substrate 10 Ωcm uniform
3. Technology 65nm LV – substrate 10 Ωcm/10 µm epi

# Capacitively Coupled Pixel Detectors
# CCPDs

# Standard hybrid detector



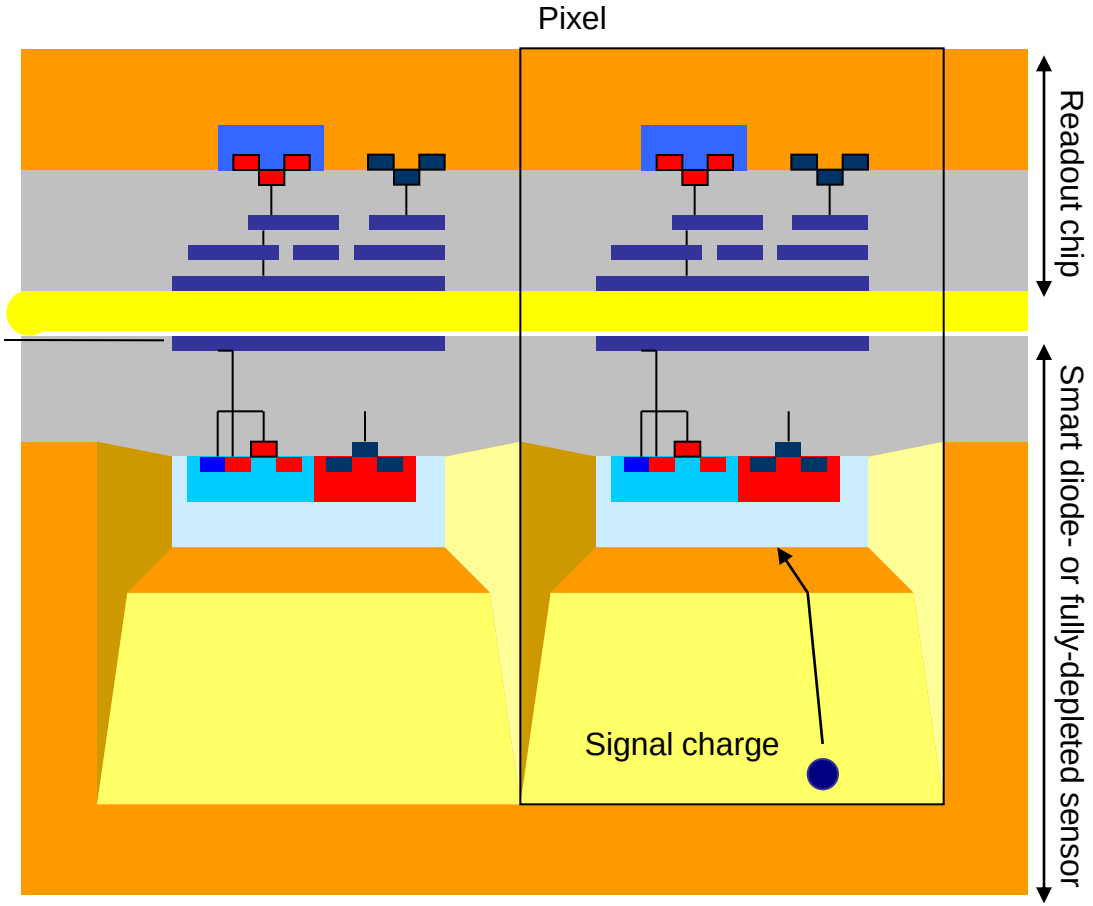
# CCPD with a “passive” sensor




Voltage signal is transmitted
Requires bias resistors on the sensor
Can be implemented as punch-through structure

Signal ~30mV for 250µm thick sensor (Cdet = 100fF)

# Active CCPD




Signal >30mV for very thin sensors

Sensor implemented as SDA
Advantage:
Charge to voltage amplification on the sensor chip
Typical voltage signal ~100mV
Easier capacitive transmission
Can be thinned without signal loss