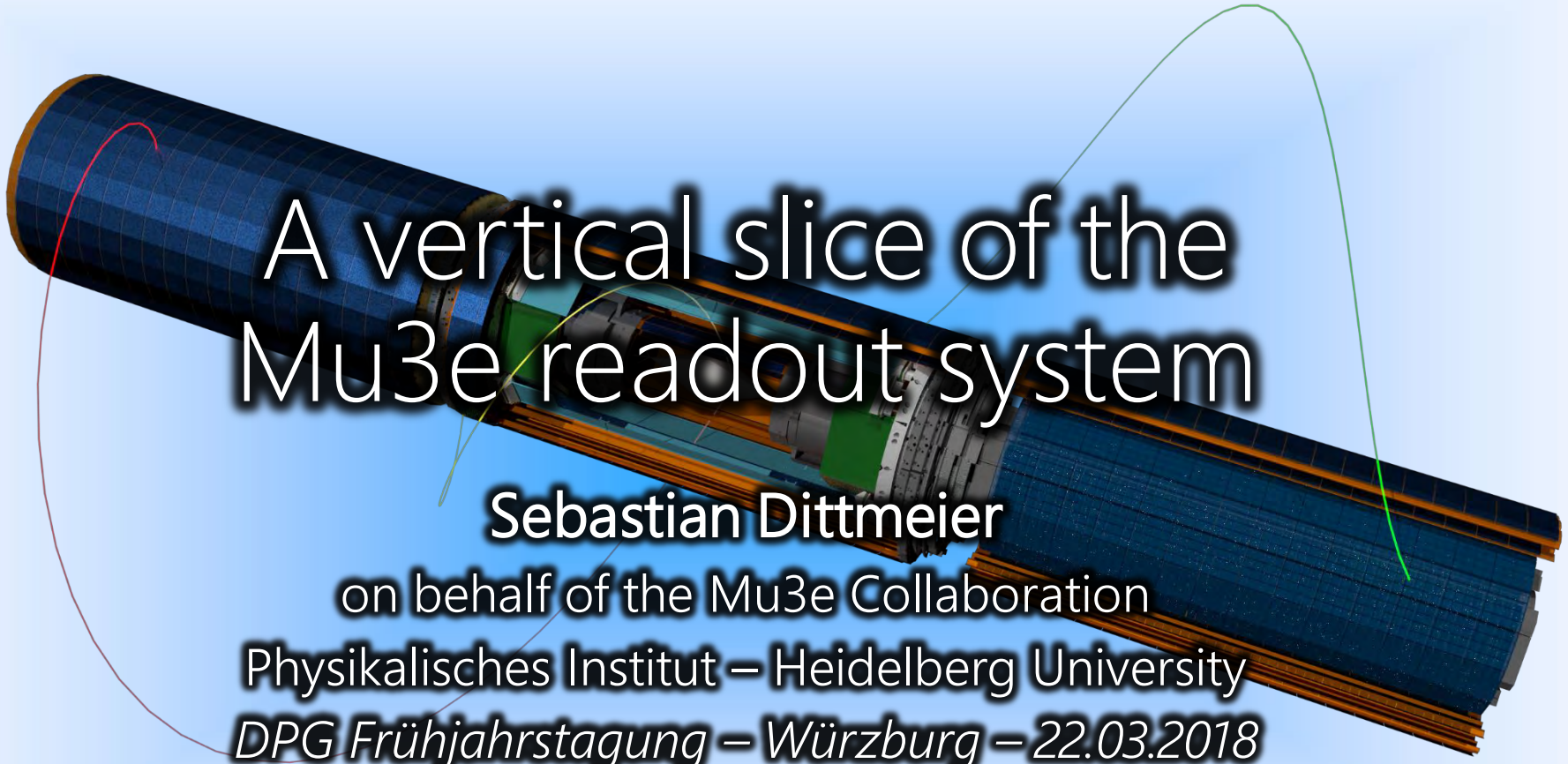


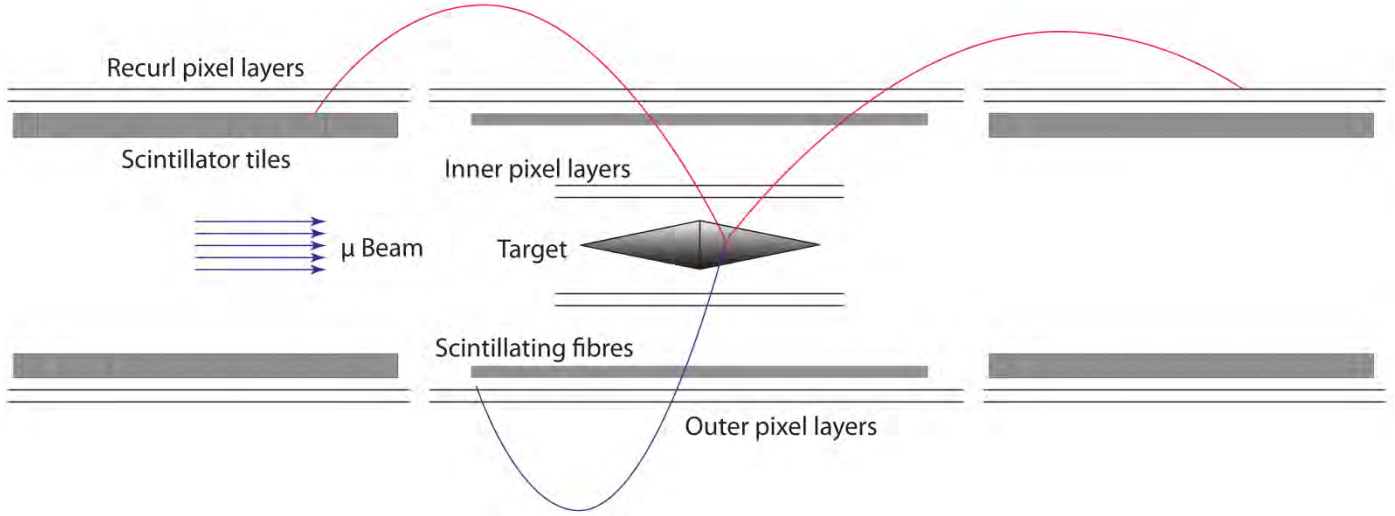
A vertical slice of the Mu3e readout system

Sebastian Dittmeier
on behalf of the Mu3e Collaboration
Physikalisches Institut – Heidelberg University
DPG Frühjahrstagung – Würzburg – 22.03.2018

INTERNATIONAL MAX PLANCK RESEARCH SCHOOL
PT FS
FOR PRECISION TESTS OF FUNDAMENTAL SYMMETRIES

The Mu3e experiment

Searching for the charged lepton flavor violating decay $\mu^+ \rightarrow e^+e^-e^+$

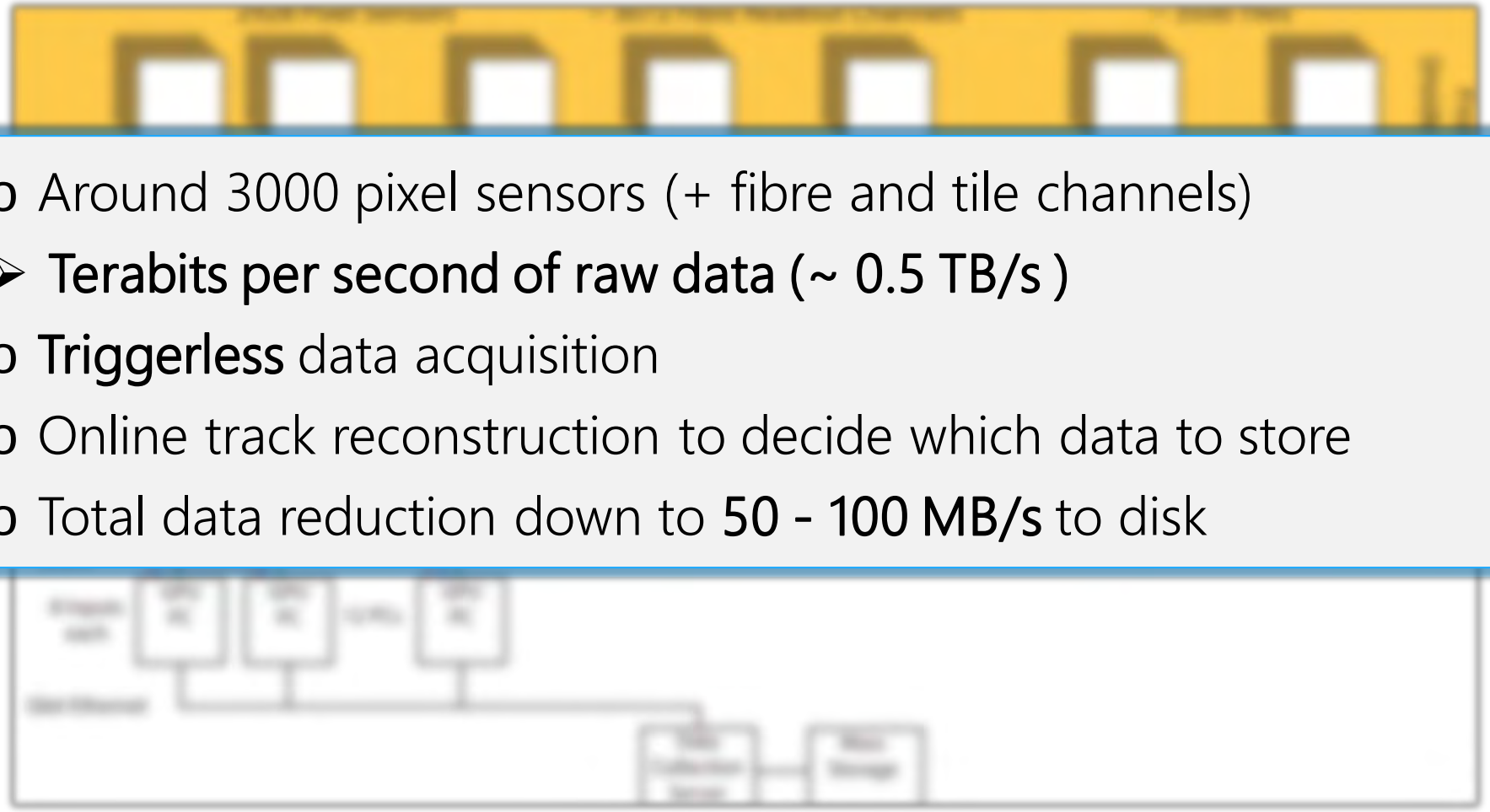


- High rates of muons $\mathcal{O}(10^9\ \mathrm{s}^{-1})$ to reach sensitivity goal $\mathcal{O}(10^{-16})$
- **Stopped muons** decay in a solenoidal magnetic field of $\mathrm{B} = 1\mathrm{T}$
- Low momentum electrons: $p_e \leq 53\ \mathrm{MeV/c}$
- ➢ **Thin and fast silicon pixel tracking detector**

The Mu3e pixel sensors – *MuPix*

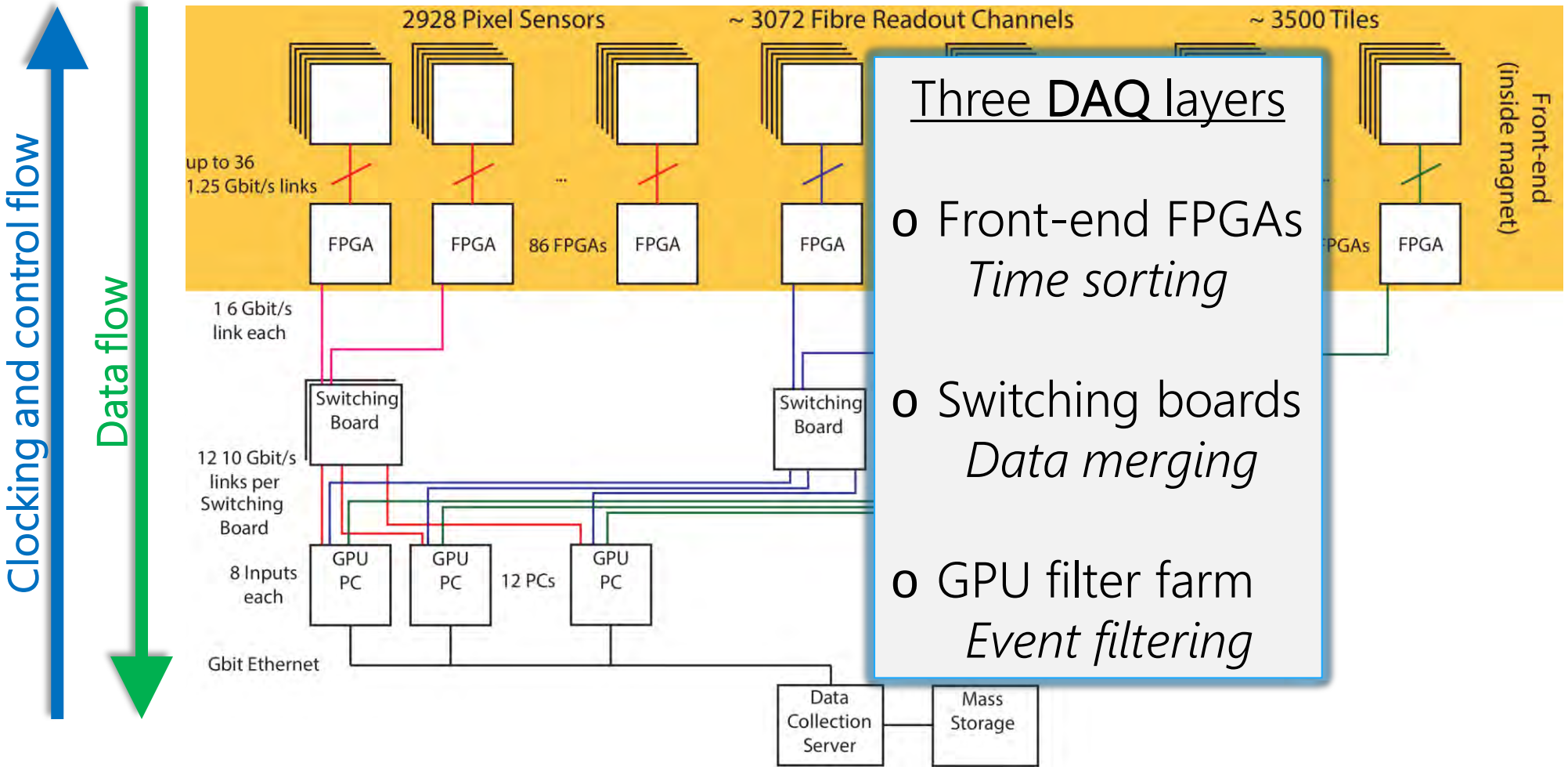
- High Voltage Monolithic Active Pixel Sensors
- Current Prototype: ***MuPix8***
  as seen in talks on Monday, session T5 Pixel-Detektoren I
- **Integrated** readout state machine
- **Serial** data outputs @ 1.25 Gb/s
- **Untriggered, zero-suppressed** readout
- **Position priority based** readout:
  Hit chronology not strictly conserved

The Mu3e readout concept



- Around 3000 pixel sensors (+ fibre and tile channels)
- ➢ **Terabits per second of raw data (~ 0.5 TB/s)**
- **Triggerless** data acquisition
- Online track reconstruction to decide which data to store
- Total data reduction down to **50 - 100 MB/s** to disk

The Mu3e readout concept



Three **DAQ** layers

- Front-end FPGAs
  Time sorting
- Switching boards
  Data merging
- GPU filter farm
  Event filtering

Hardware components – Mu3e pixel readout –

Pixel sensors
Large prototype: MuPix8
operational

Front-end FPGA
Prototype boards: Stratix IV
operational

Switching board
PCIe40 (LHCb development)
delivery 2018

PC
FPGA on PCIe card: Arria 10
GPU: GTX1080Ti

Hardware components
– A vertical slice of the pixel readout –

Pixel sensors
Large prototype: MuPix8
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Front-end FPGA
Prototype boards: Stratix IV
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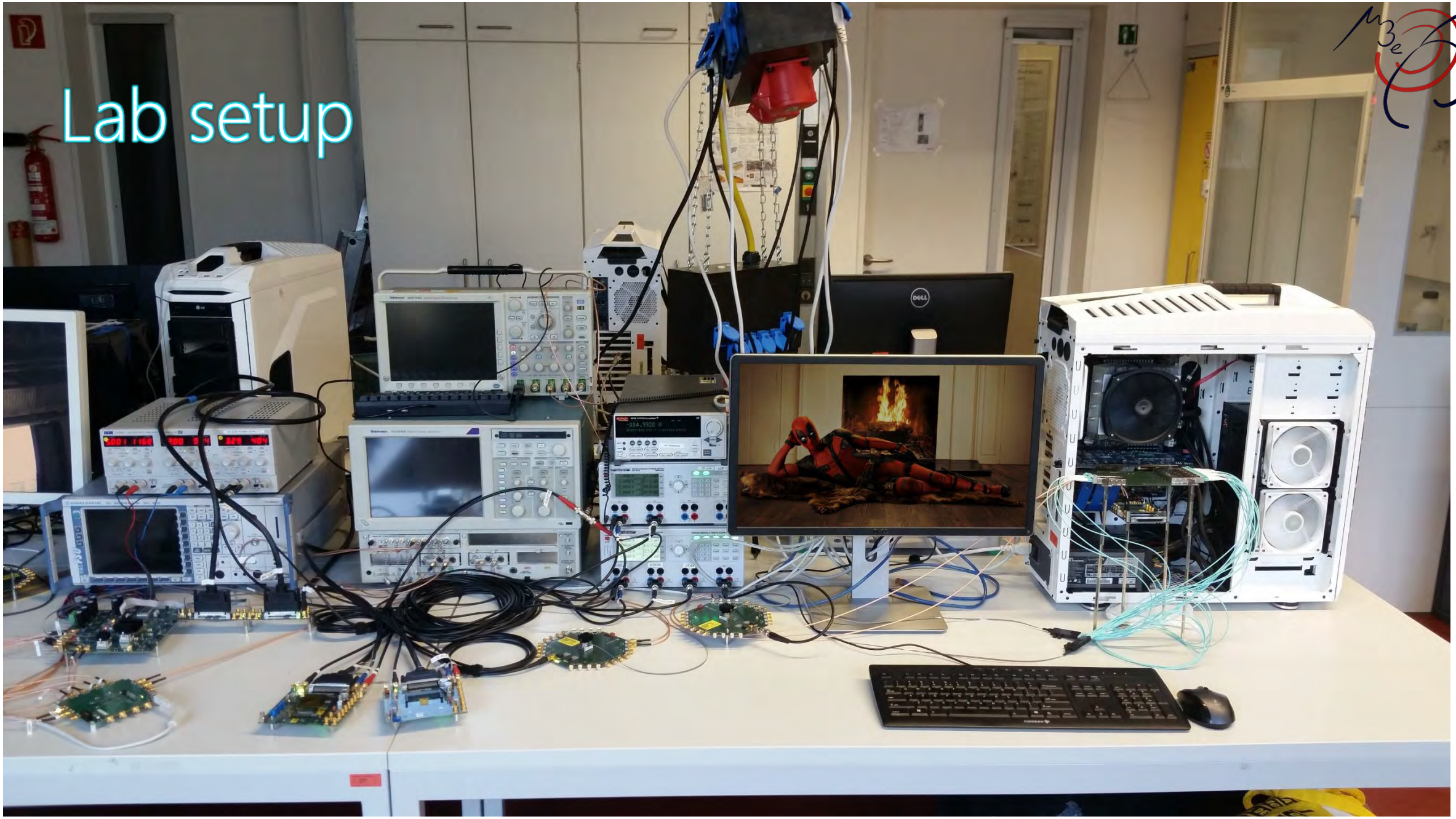
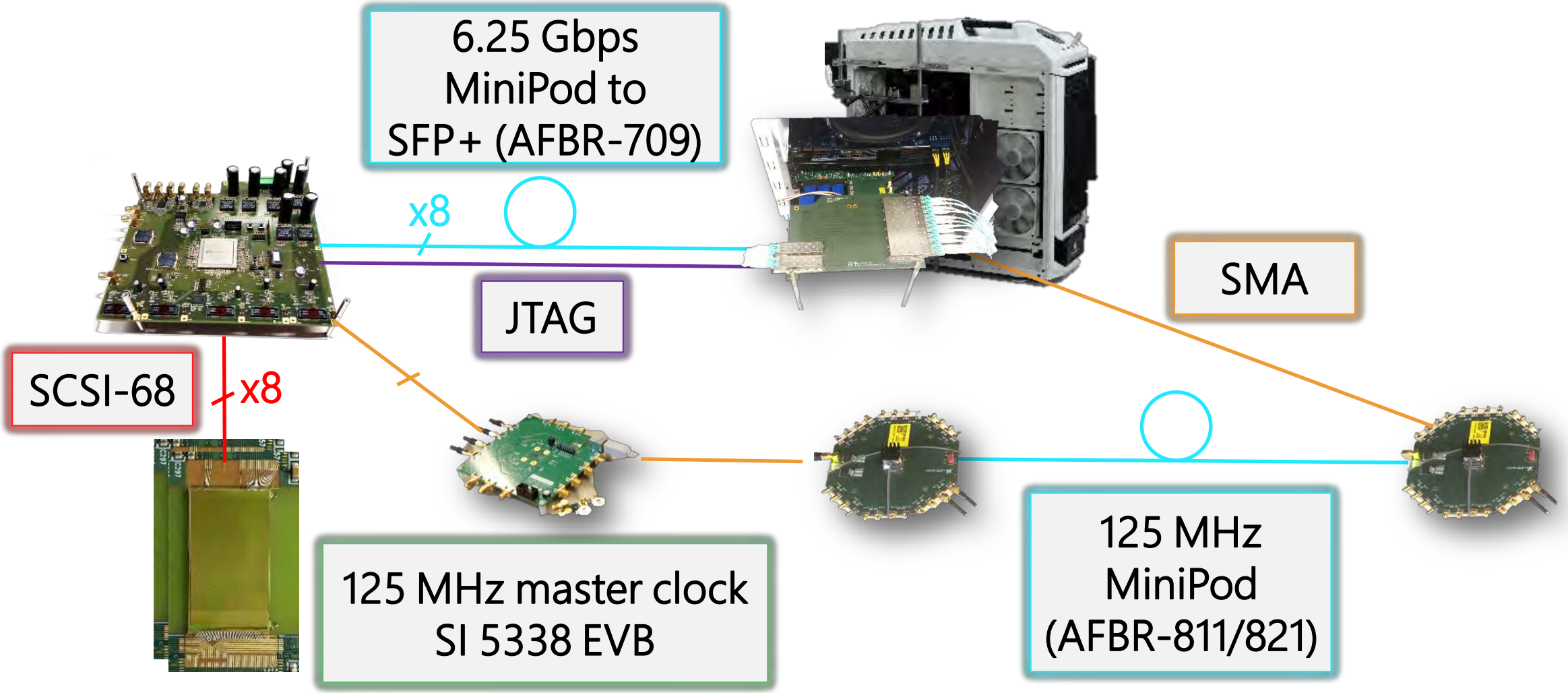
Switching board
PCIe40 (LHCb development)
delivery 2018

PC
FPGA on PCIe card: Stratix IV

Lab setup



Optical and electrical connections



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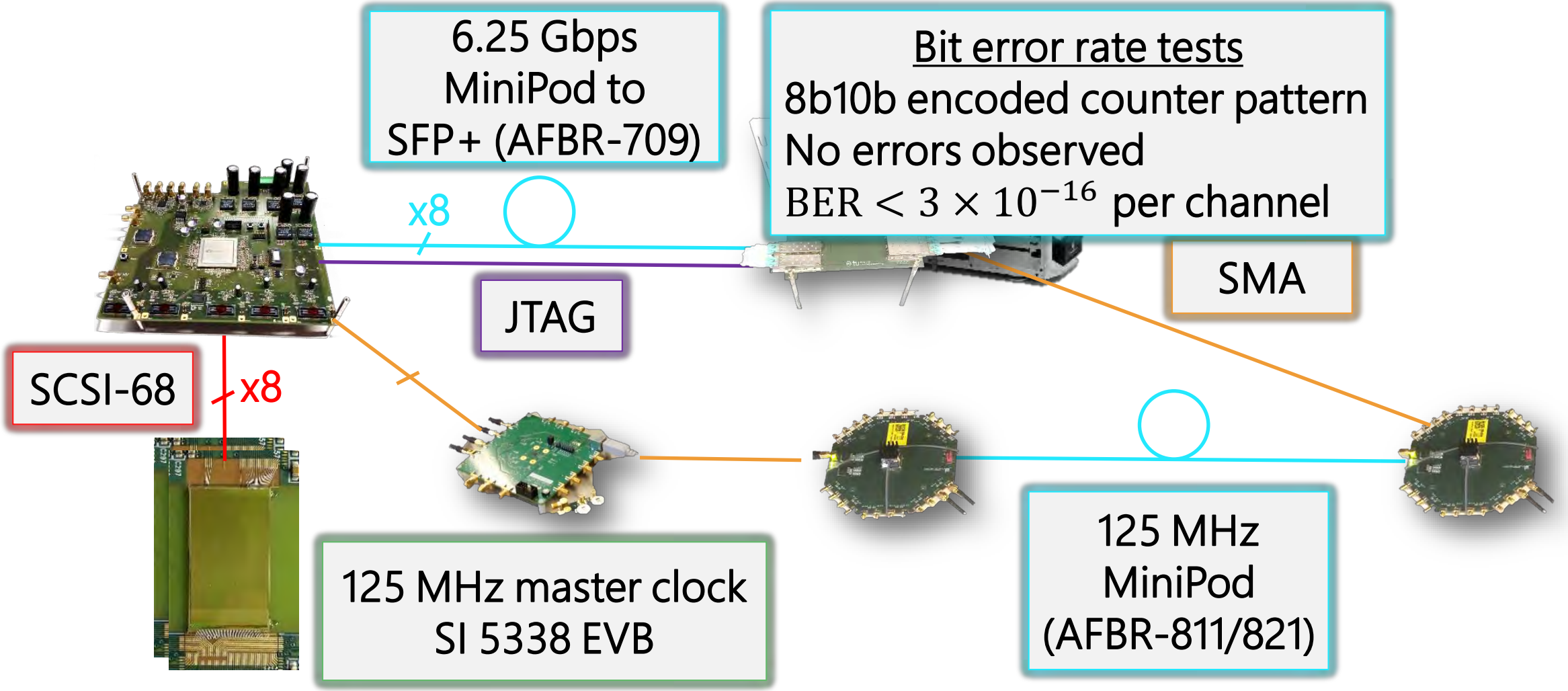
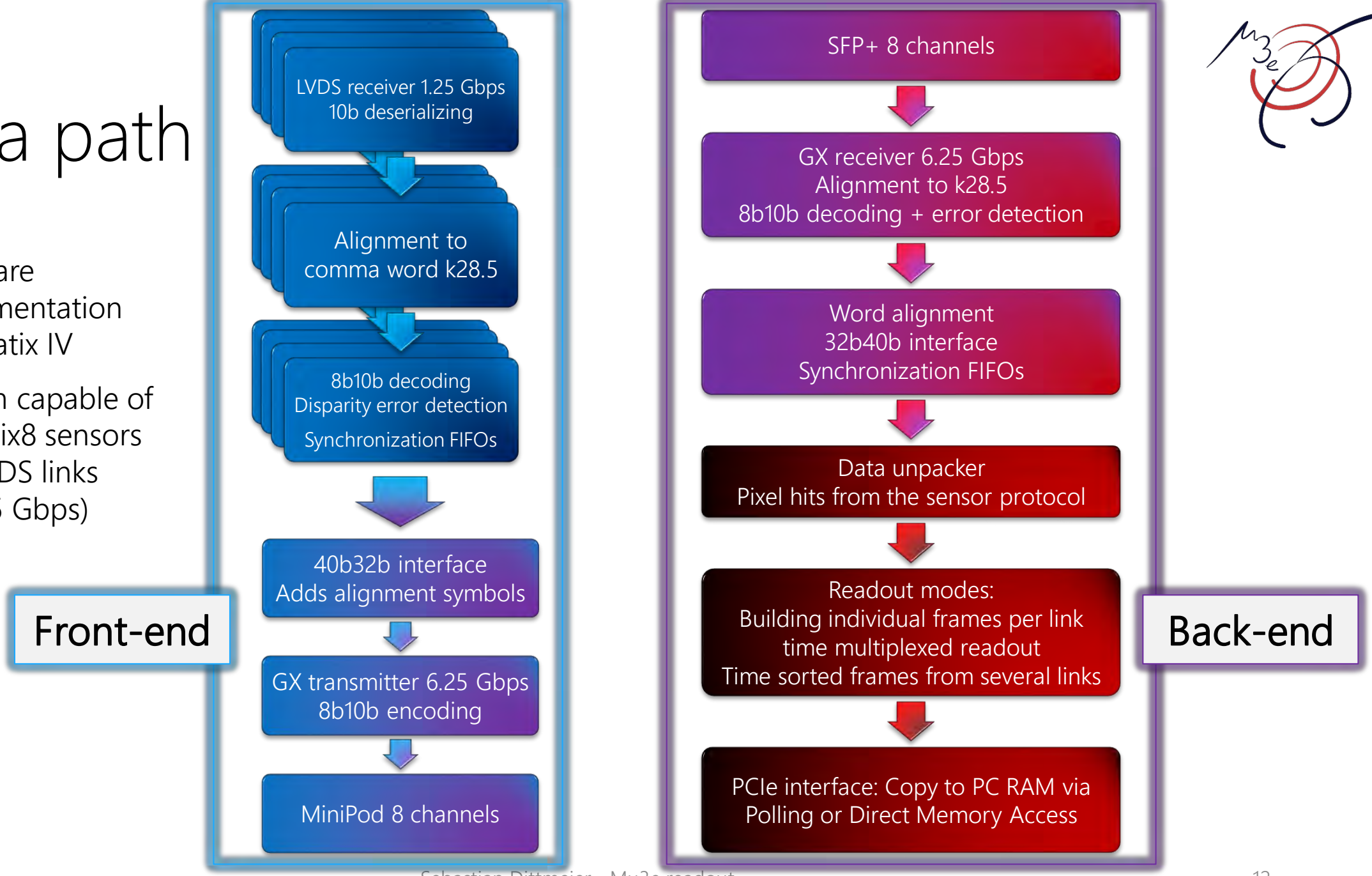


Slow control of front-end FPGA

- Currently implemented in a TCL script
- Direct access to NIOS soft-core via JTAG
- Used for reset and enable signals
- Independent software running on NIOS controls
  - Transceiver analog settings
  - Access to bit error rate measurements
  - Peripheral slow control

Data path

- Firmware implementation on Stratix IV
- System capable of 8 MuPix8 sensors (32 LVDS links @ 1.25 Gbps)



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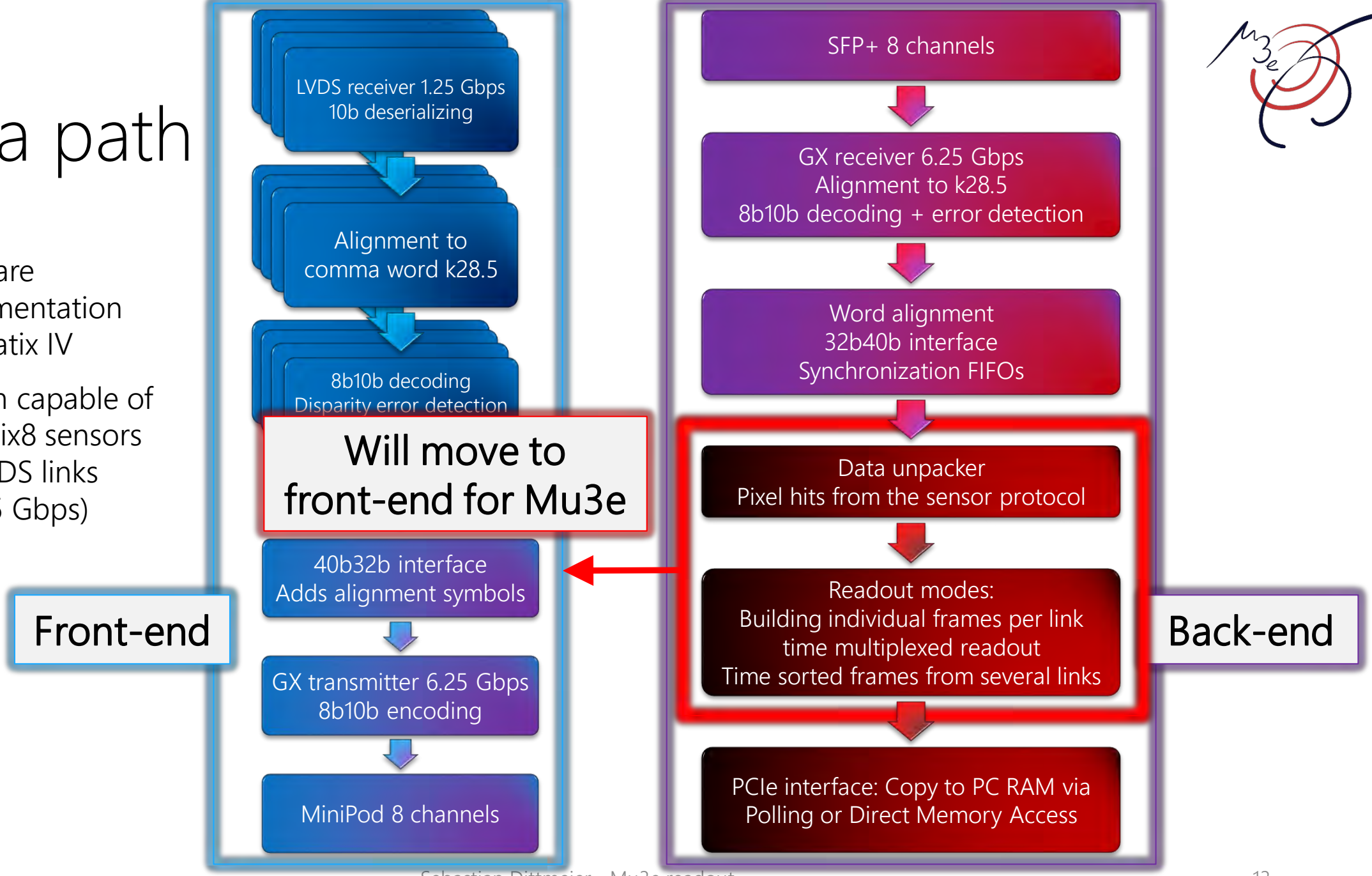
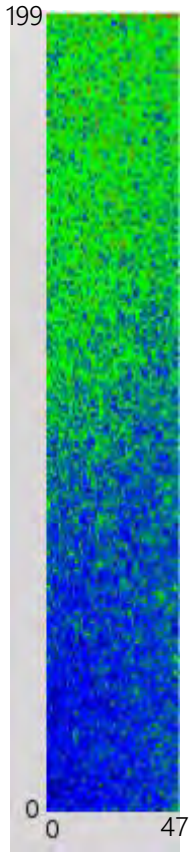


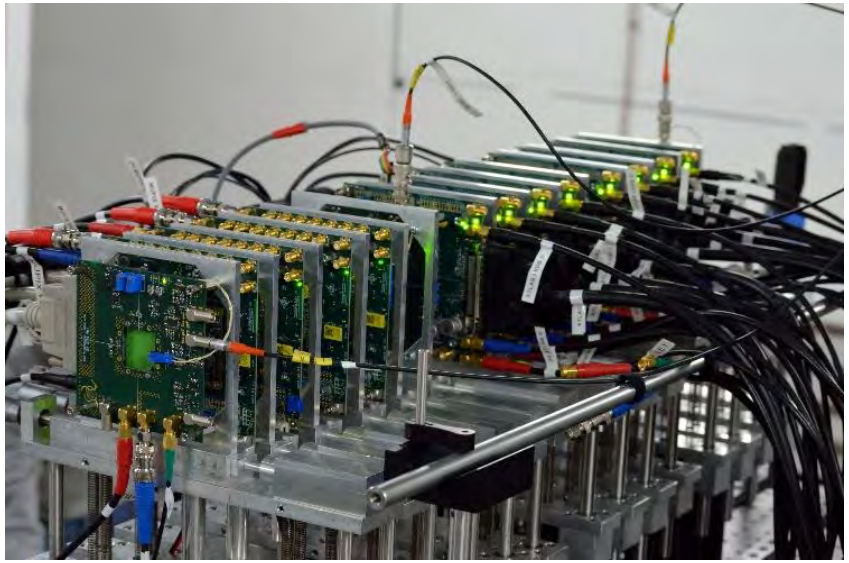
Operational tests: source and test beam

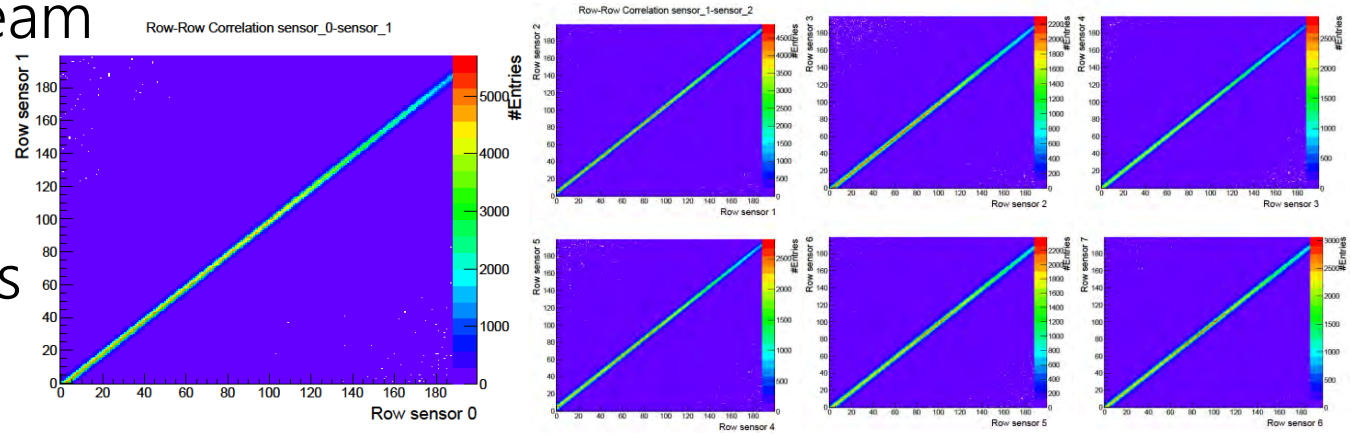
- Successful operation of two MuPix8 in parallel using vertical slice setup in the lab
  - Configuration of sensors ✓
  - Data transmission from sensors to front-end ✓
  - Data transmission from front-end to back-end ✓
  - Sensor responds to Sr90 source ✓



Operational tests: source and test beam

- Successful operation of two MuPix8 in parallel using vertical slice setup in the lab
  - Configuration of sensors ✓
  - Data transmission from sensors to front-end ✓
  - Data transmission from front-end to back-end ✓
  - Sensor responds to Sr90 source ✓
- Successful operation at a test beam at DESY with 8 sensors
- Used as tracking telescope
- Correlation of pixel row positions





Summary and outlook

- Implementation of a vertical slice of the Mu3e pixel readout
- Setup includes
  - Large pixel sensor (MuPix8)
  - Protoype front-end board
  - Optical data and clock transmission

- Successfully tested in the lab with Sr90 source and at a test beam at DESY

- Move more firmware to the front-end, reduce bandwidth
- Operation of several boards in parallel
- Include switching board into the readout chain