The MuPix8 Chip
A monolithic large scale pixel sensor

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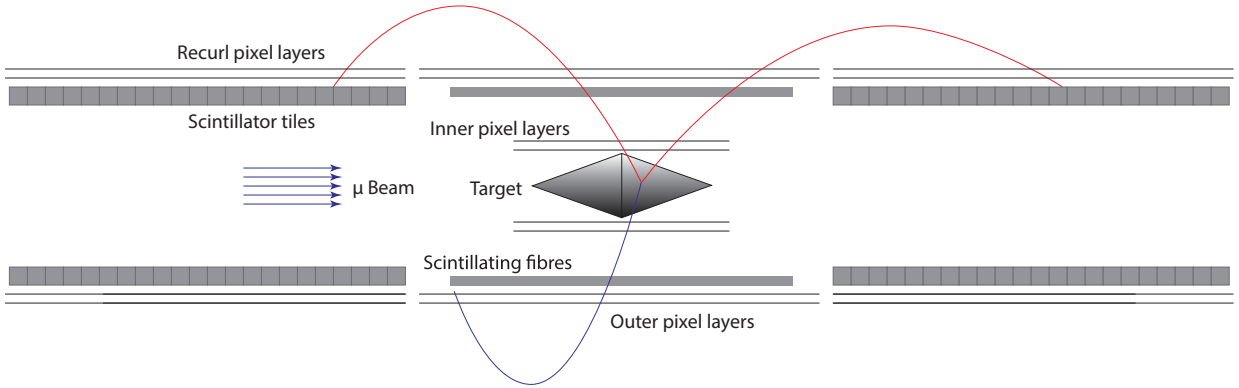
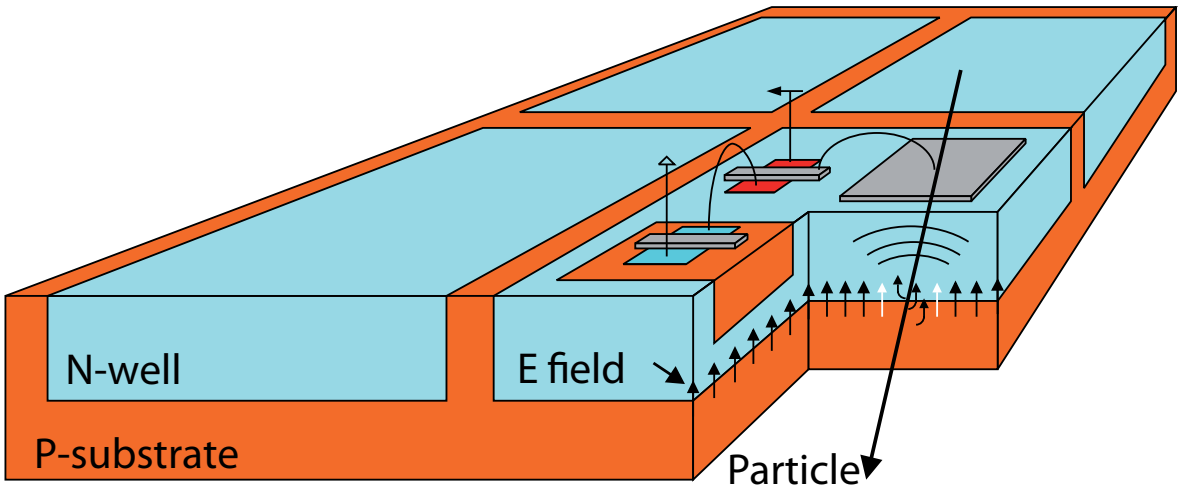
The Mu3e Experiment

Searching for the charged Lepton Flavor Violating decay $\mu^+ \to e^+e^-e^+$



- sensitivity goal of one in 10^{16} decays, requires high muon rates of $10^9\,\mathrm{s}^{-1}$
- reconstruction of electron trajectories in a 1 T solenoidal magnetic field
- multiple coulomb scattering dominated ($p_e < 53\,\mathrm{MeV/c}$)

High Voltage - Monolithic Active Pixel Sensor (HV-MAPS)



I.Peric, P. Fischer et al., NIM A 582 (2007) 87

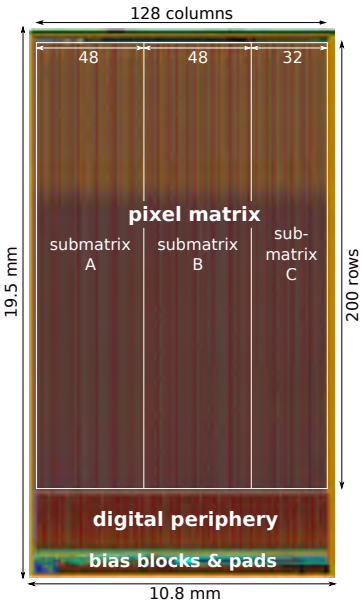
- low ohmic substrate ($20\,\Omega\,\mathrm{cm}$ - $200\,\Omega\,\mathrm{cm}$)
- high voltage ($-120\,\mathrm{V}$)
- AMS 180nm HV-CMOS
- depleted n-well diode
- charge collection via drift
- no additional readout chip
- thinned to $50\,\mu\mathrm{m}$

Road to the first full scale Mu3e Pixel Sensor

MuPix7

First
fully monolithic
prototype

MuPix8

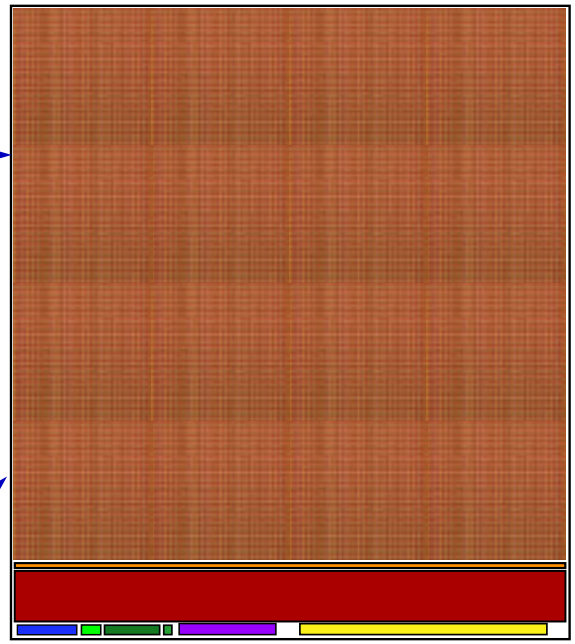


Scalability

MuPix9

Detector Integration

MuPix10



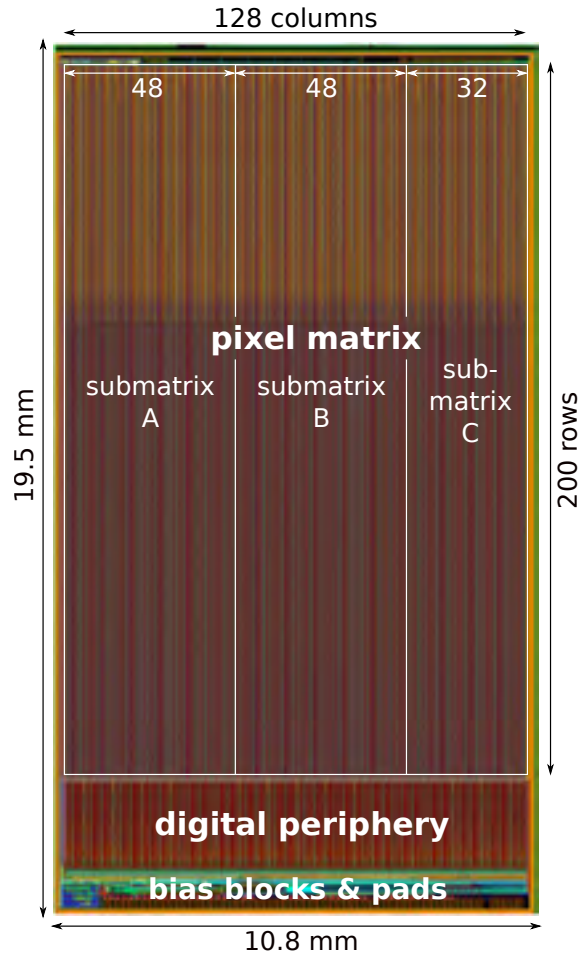
Full scale Mu3e sensor chip

MuPix8 Design Features

- $2 \times 1\,\mathrm{cm}^2$ chip size
- pads on one edge

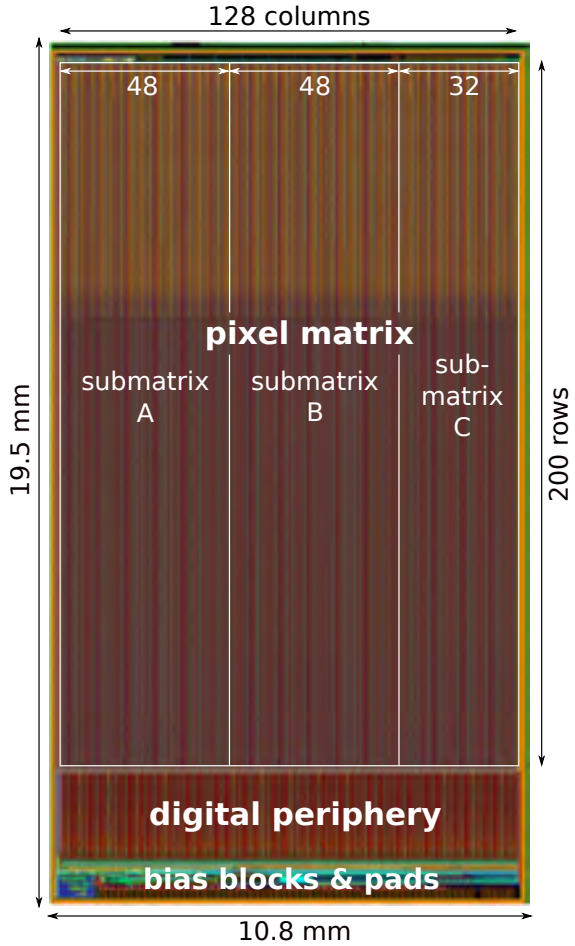
→ flexprint readiness

- improve time resolution
- radiation hard design
- increase active volume ($80\,\Omega\,\mathrm{cm}$ substrate)

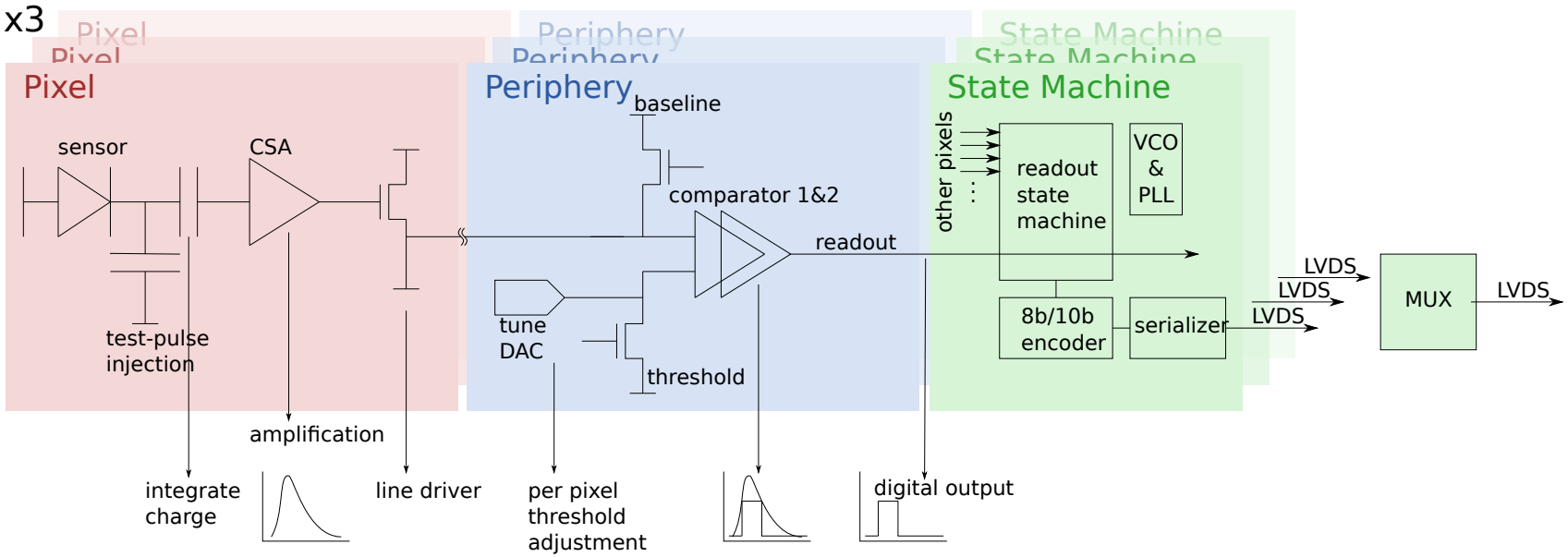


MuPix8 Chip

- $81 \times 80\,\mu m^2$ pixel size
- 128×200 pixels
- $16 \times 10\,mm^2$ active area
- 3 matrix partitions

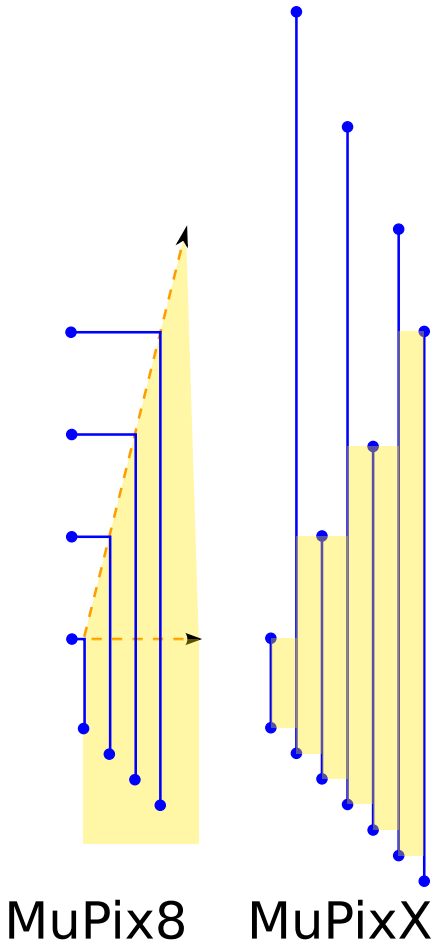


MuPix8 Architecture



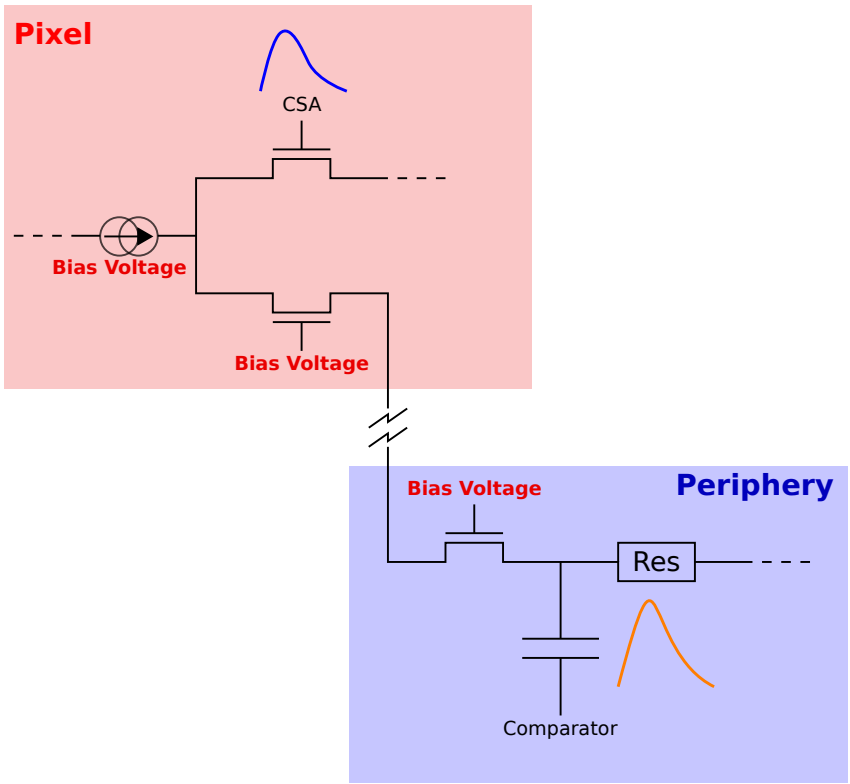
- timewalk reduction circuitry
- 3 sub-matrices with dedicated data output
- additional merged data output

Crosstalk and Signal Transmission



- very dense routing:
  2 metal layers, 200 signals
  300 nm spacing
- 1 sub-matrix source follower
- 2 sub-matrices current driven

Crosstalk and Signal Transmission



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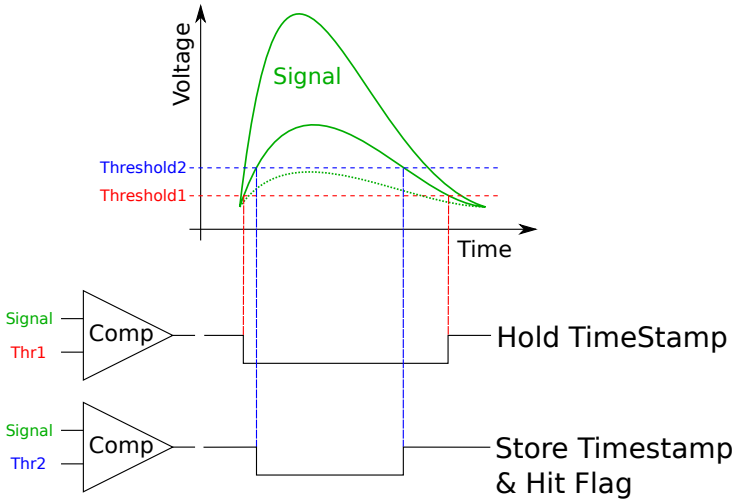
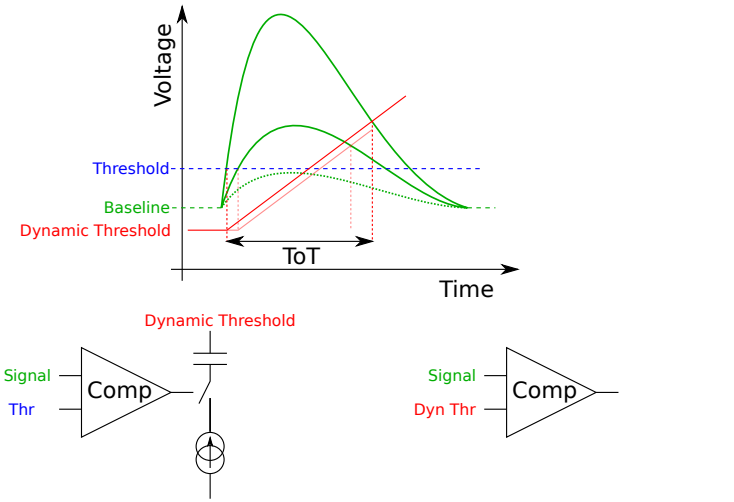
Pixel Digital Cell



2-threshold
On-Chip correction

- 3 time walk correction approaches
- 2 comparators
- 5 tune bits + pixel switch
- 10(+6) timestamp bits

Pixel Digital Cell



Start Ramp
& Store Timestamp

Store ToT Timestamp
& Hit Flag

voltage ramp
Off-Chip correction

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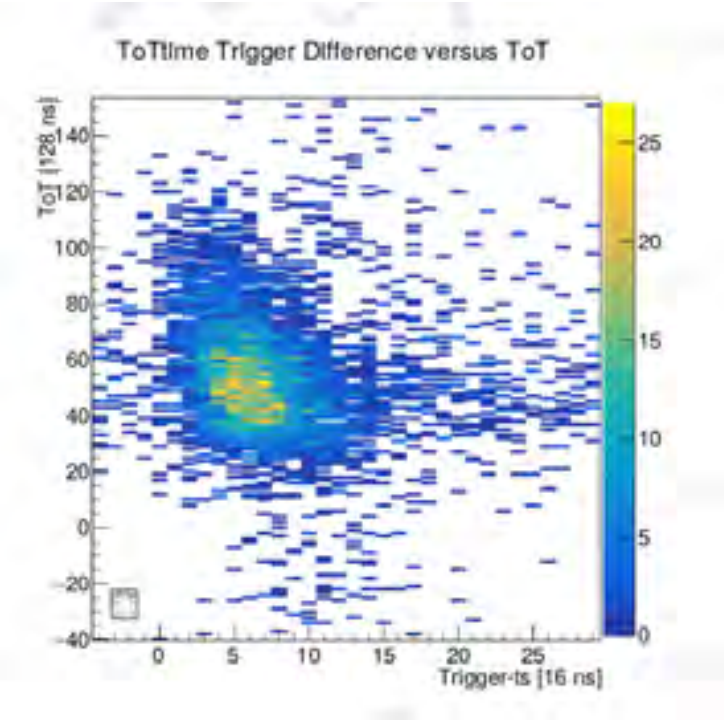
Pixel Digital Cell



- 3 time walk correction approaches
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Slow Control Interface - Status

- 6 single ended signals
- no chip address
- readback of DAC values

$\Rightarrow$ not feasible for module production with two layer flexprints

Slow Control Interface - Required Changes

- reduction of I/0 connections
- differential Inputs → solved
- using a SC Bus (Chip Address)
- readback of Chip Information via Data stream

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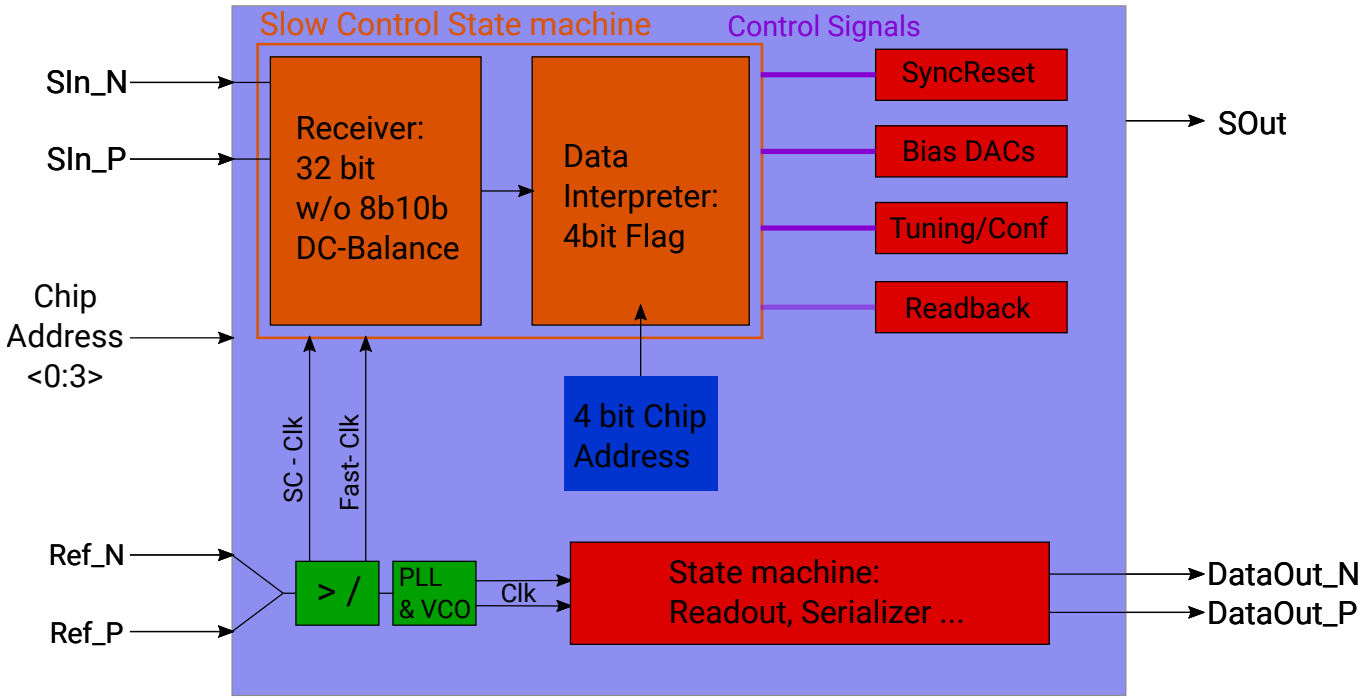

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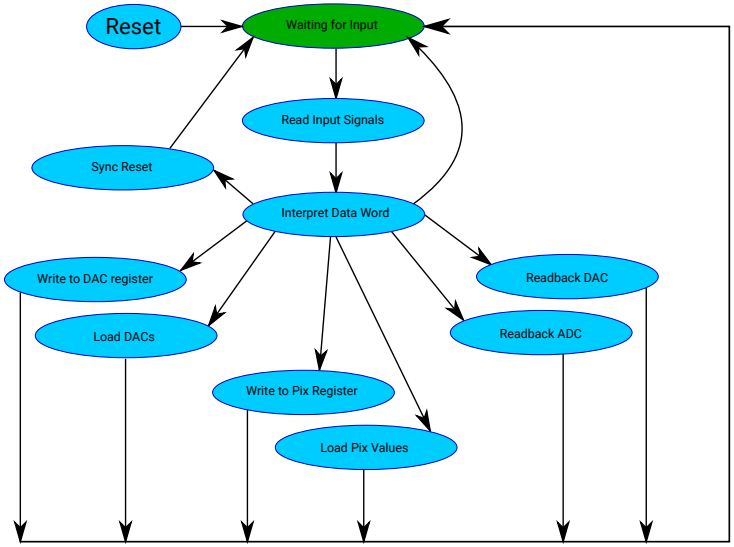
Slow Control Interface - The MuPix9



- custom 32bit protocol
- chip address
- broadcast synchronous reset
- standalone and integrated available
- expected this summer

More on MuPix9 by Alena Weber (T 5.10)

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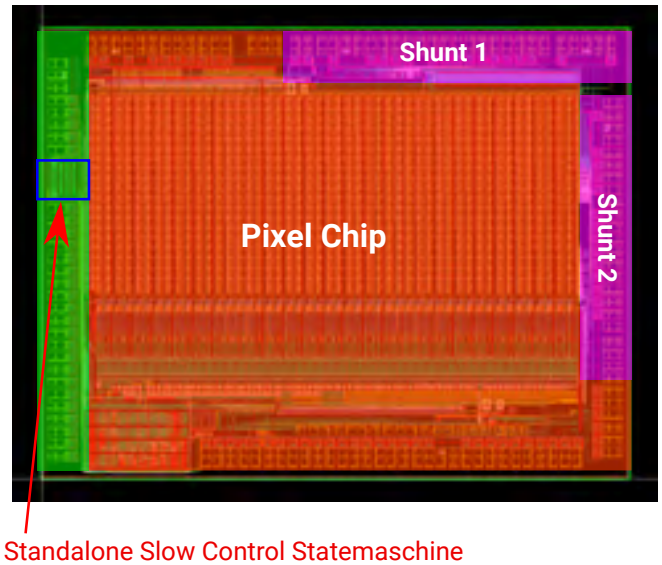

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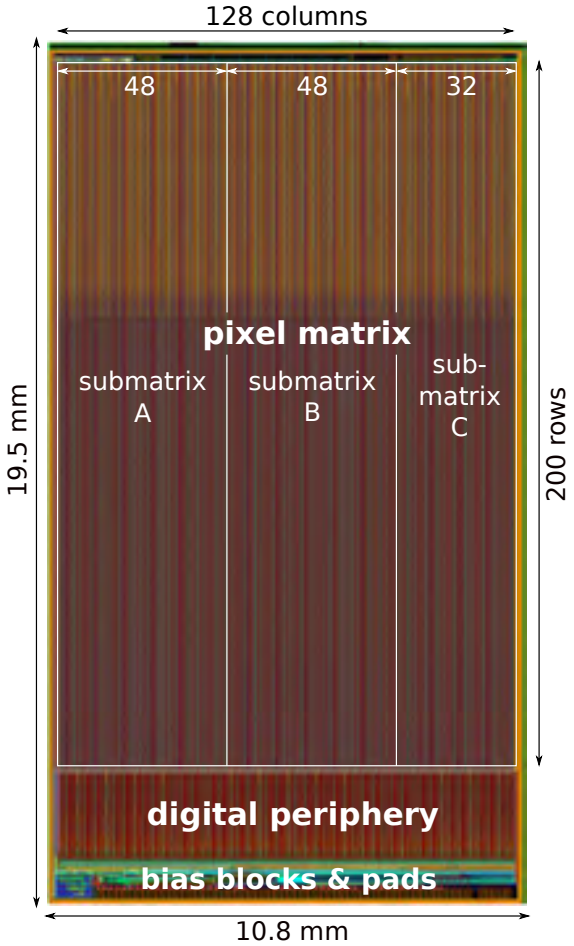
Conclusion & Outlook



- more to explore on MuPix8: Bandgap, merged link, ...
- many parts silicon proven
- design decisions have to be made
- start of MuPix10 design soon