Readout of the Mu3e pixel detector

Sebastian Dittmeier on behalf of the Mu3e Collaboration

Physikalisches Institut - Universität Heidelberg

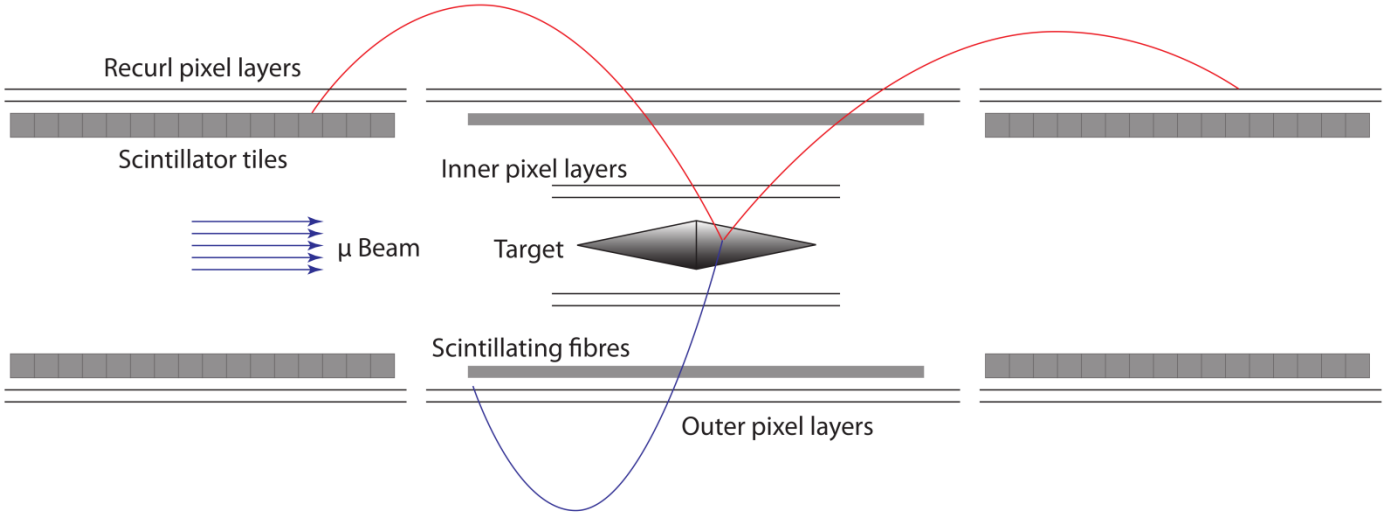
DPG-Frühjahrstagung - Münster – 29.03.2017

INTERNATIONAL MAX PLANCK RESEARCH SCHOOL

PT FS FOR PRECISION TESTS OF FUNDAMENTAL SYMMETRIES

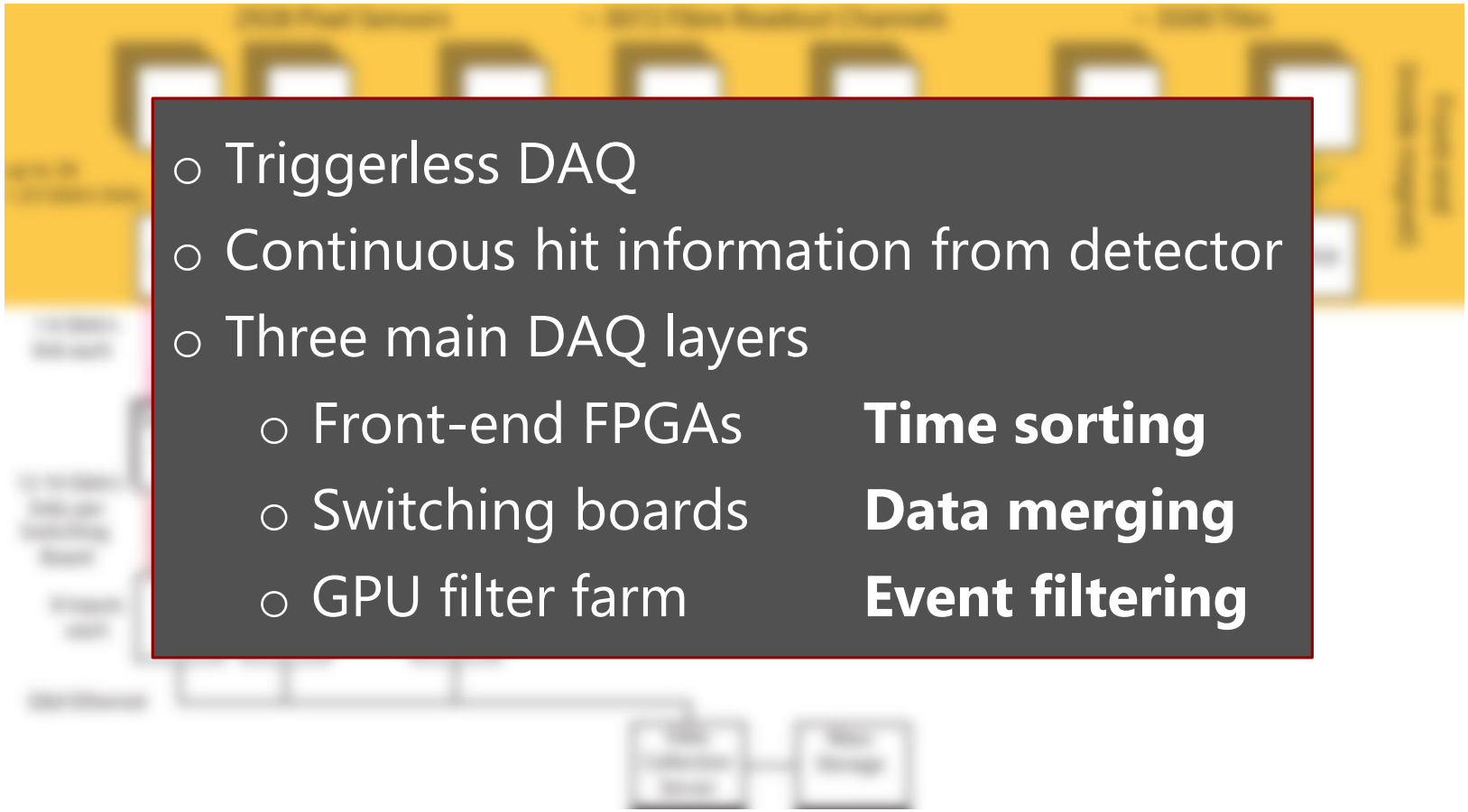
The Mu3e Experiment

Search for the charged lepton flavor violating decay $\mu^+ \rightarrow e^+e^-e^+$



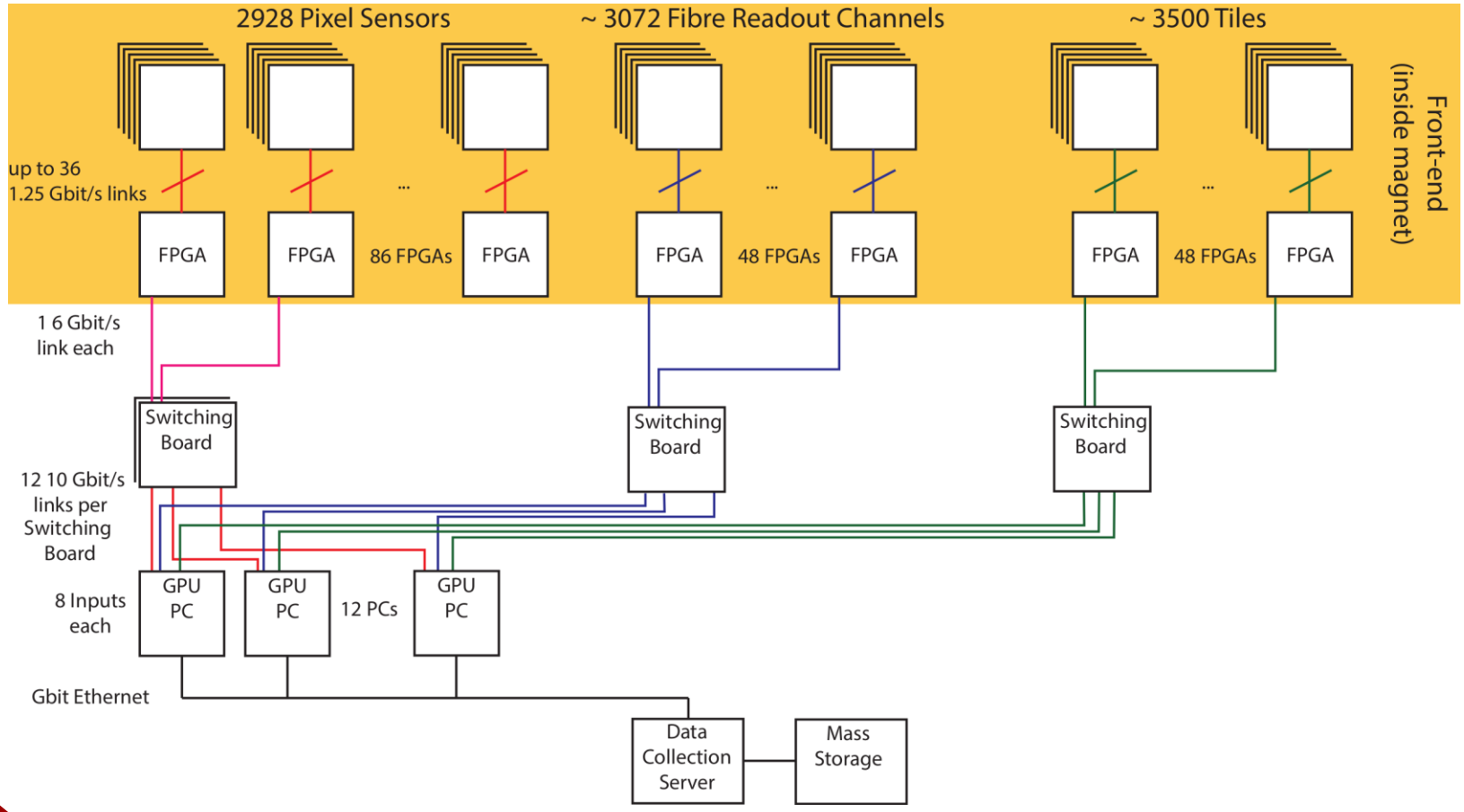
- **Stopped muons** decay in a solenoidal magnetic field of **B = 1T**
- Low momentum electrons $\boldsymbol{p_e \leq 53\ \mathrm{MeV/c}}$
- **Multiple scattering** dominates momentum resolution
- Thin silicon pixel tracking detector

Data Acquisition Concept



- Triggerless DAQ
- Continuous hit information from detector
- Three main DAQ layers
  - Front-end FPGAs **Time sorting**
  - Switching boards **Data merging**
  - GPU filter farm **Event filtering**

Data Acquisition Concept



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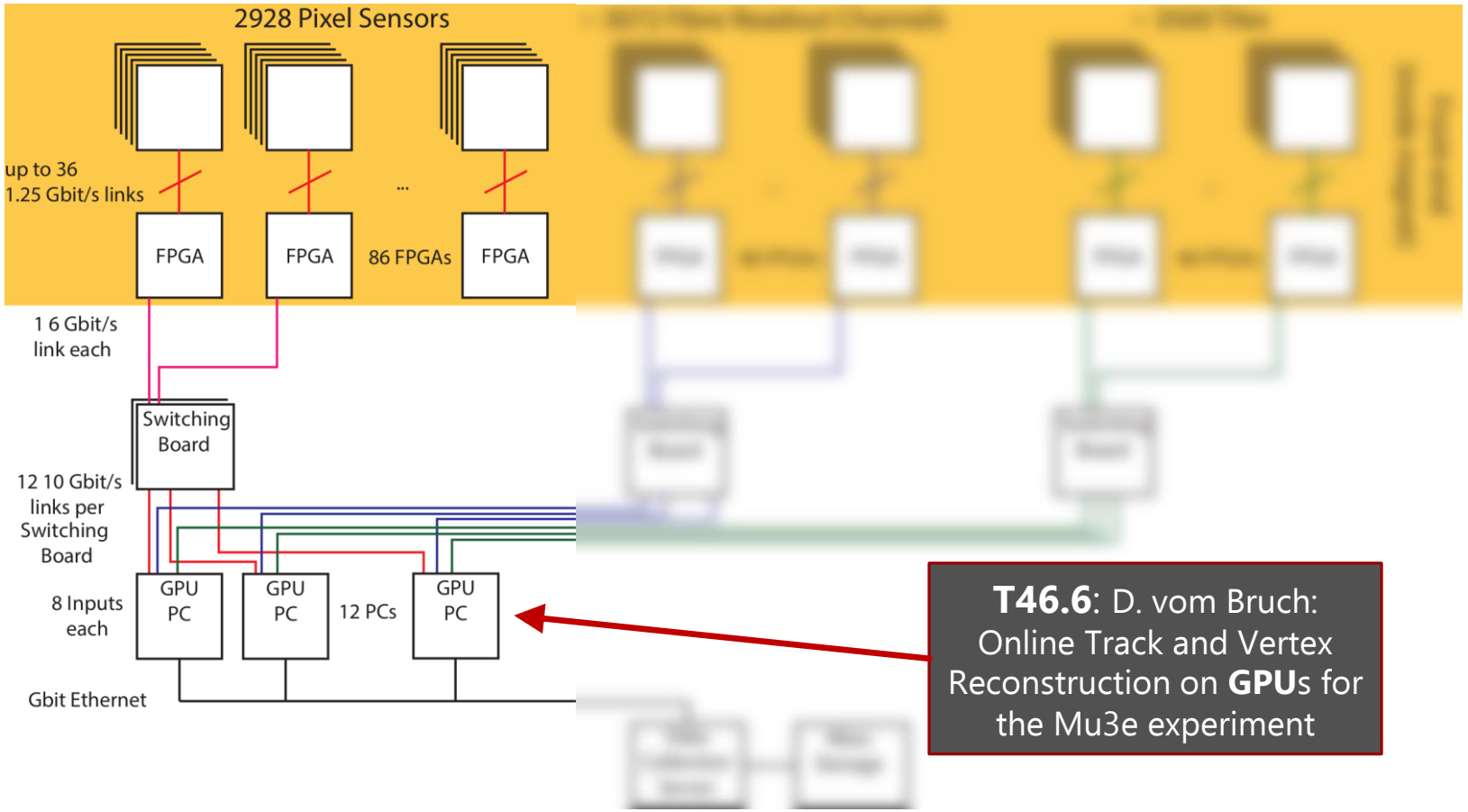
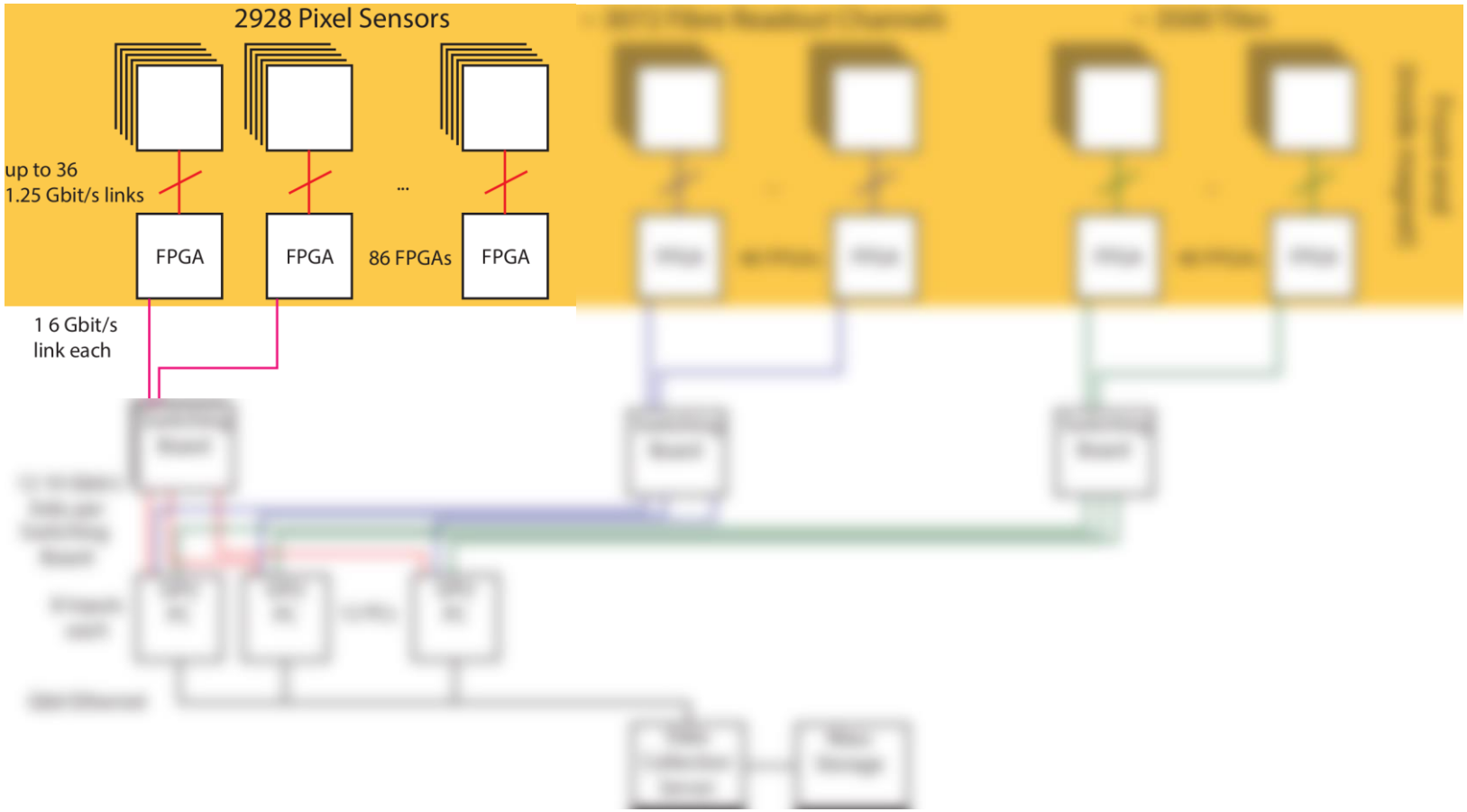


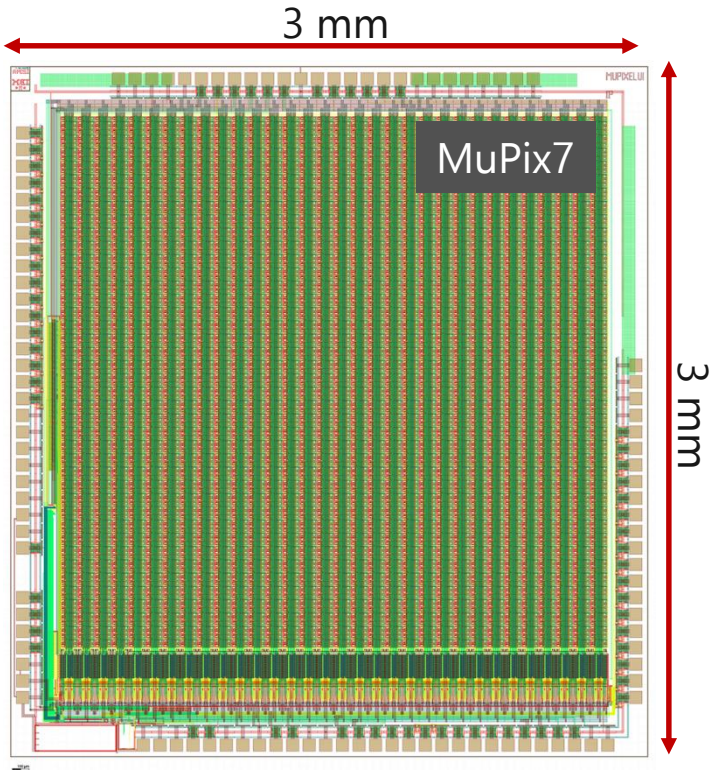
T46.6: D. vom Bruch: Online Track and Vertex Reconstruction on **GPU**s for the Mu3e experiment

Data Acquisition Concept



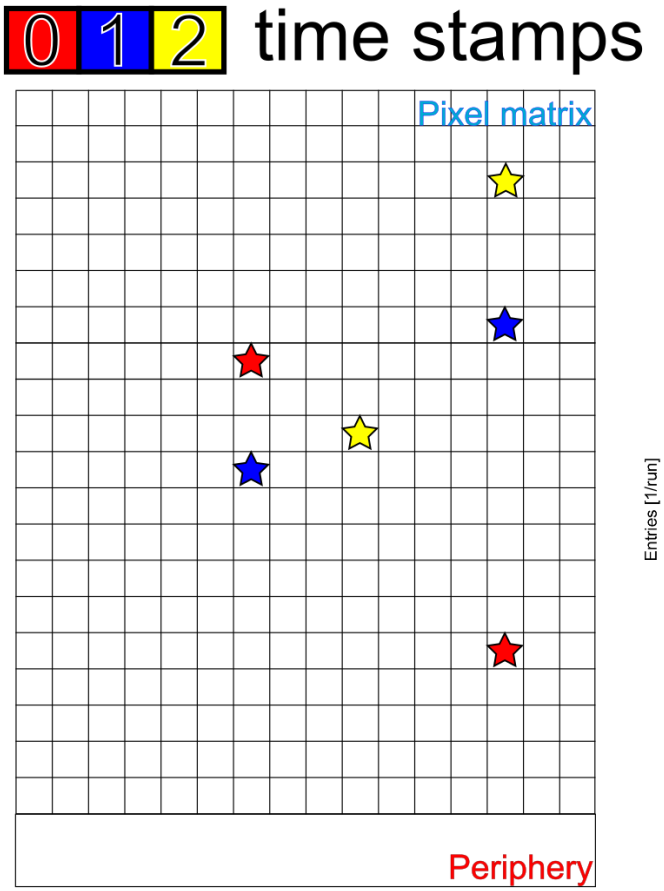
Pixel Sensors for Mu3e: MuPix

- **H**igh **V**oltage **M**onolithic **A**ctive **P**ixel **S**ensors (HV-MAPS)
- Charge collection via drift
- Signal amplification and processing
- Latest prototype: MuPix7
- Integrated readout state machine
- Hit information is transferred via serial data link @ 1.25 Gb/s
- Next prototype submitted: MuPix8

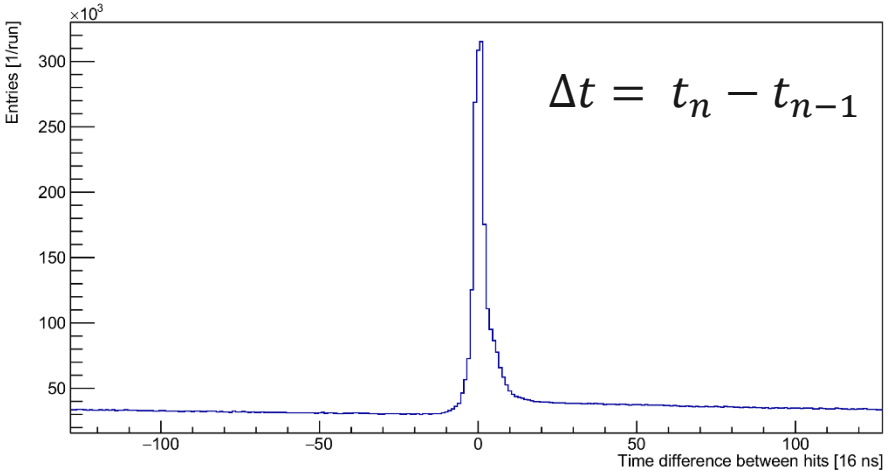


- T26.5: L. Huth - Irradiated MuPix7
- HK 18.1: H. Augustin - The MuPix8
- T94.8: A. Herkert – Mu3e Pixel Tracker

MuPix7 – Readout



- Internal state machine
- Hit timestamp + pixel address
- Column-wise readout
- Non-chronological readout



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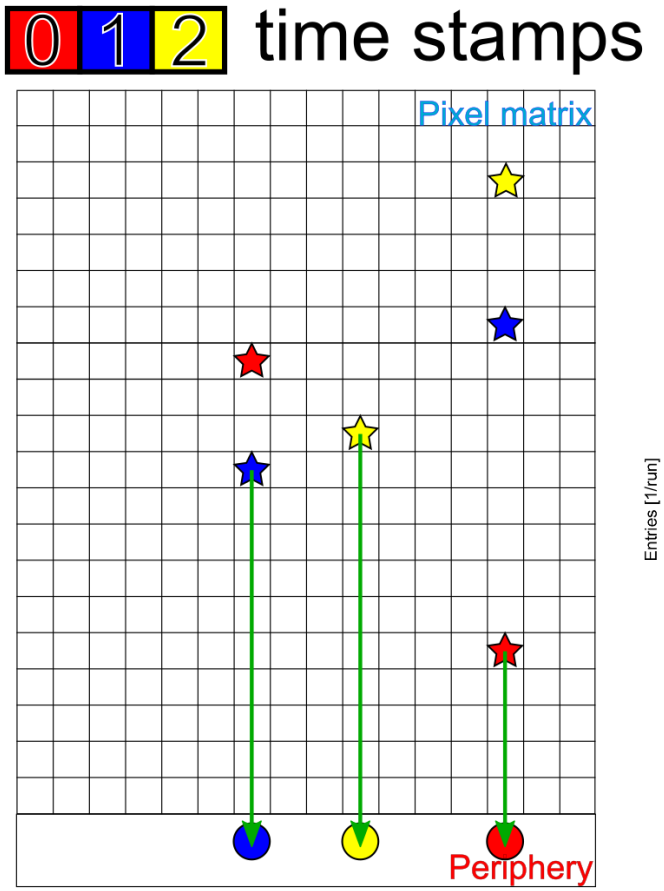

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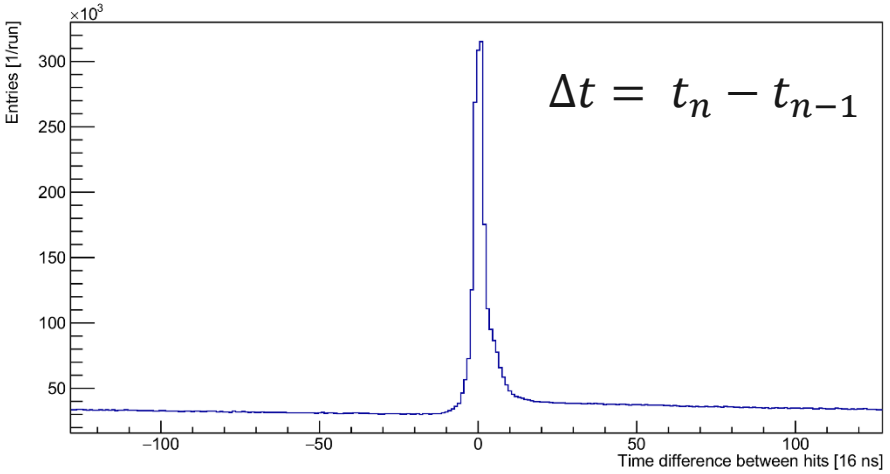

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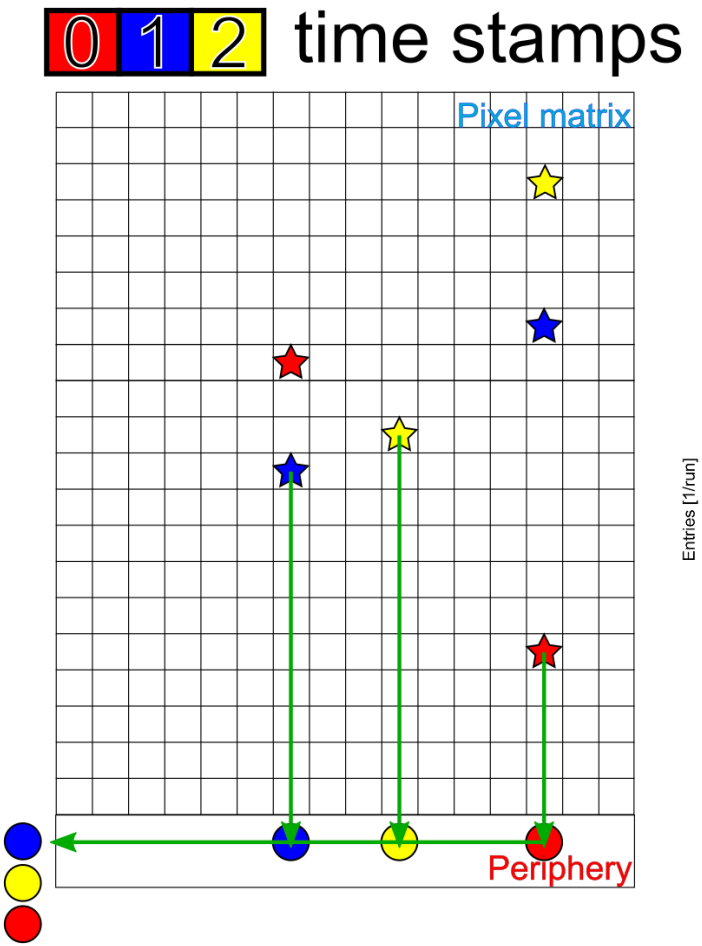

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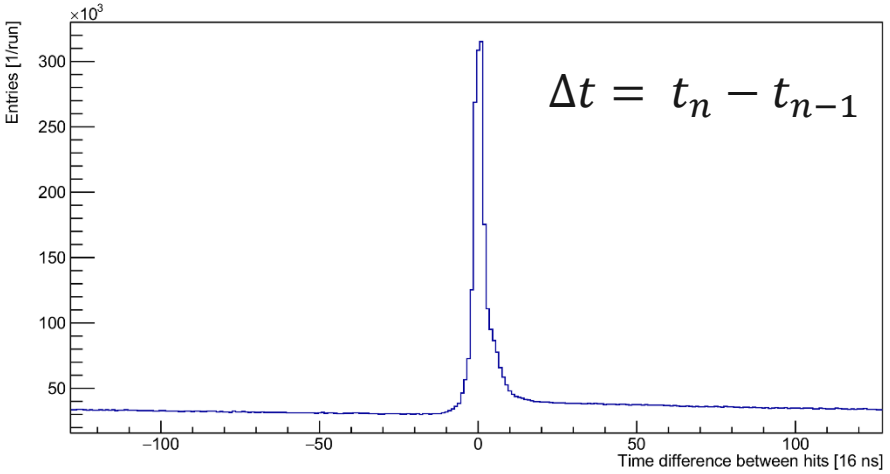

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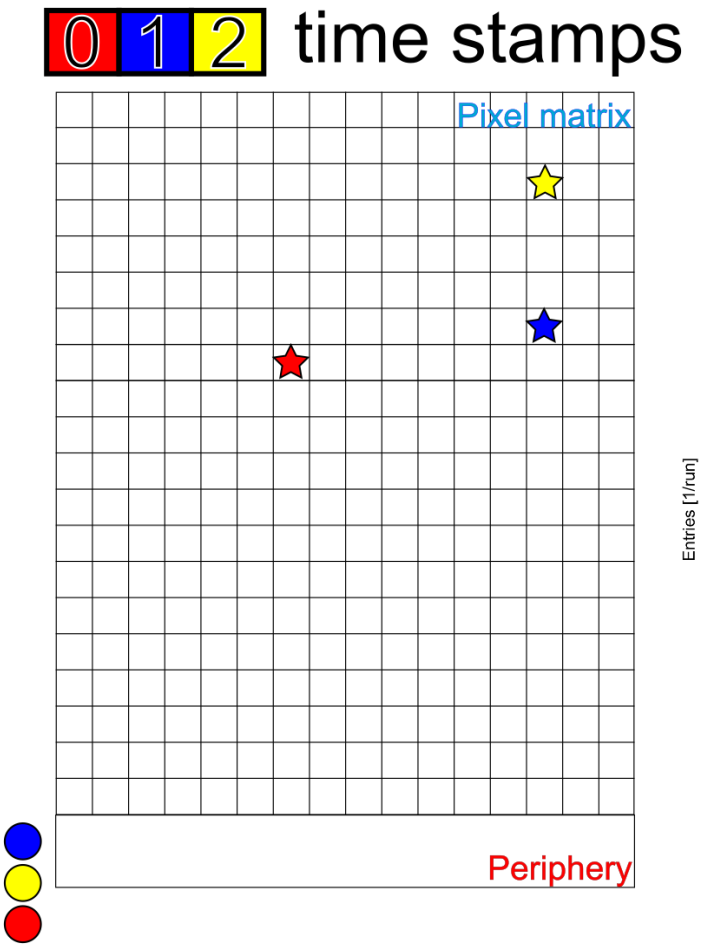

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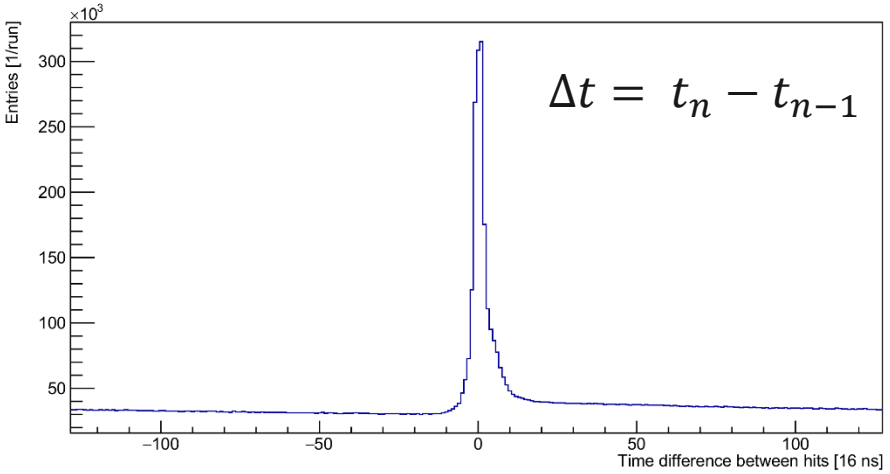

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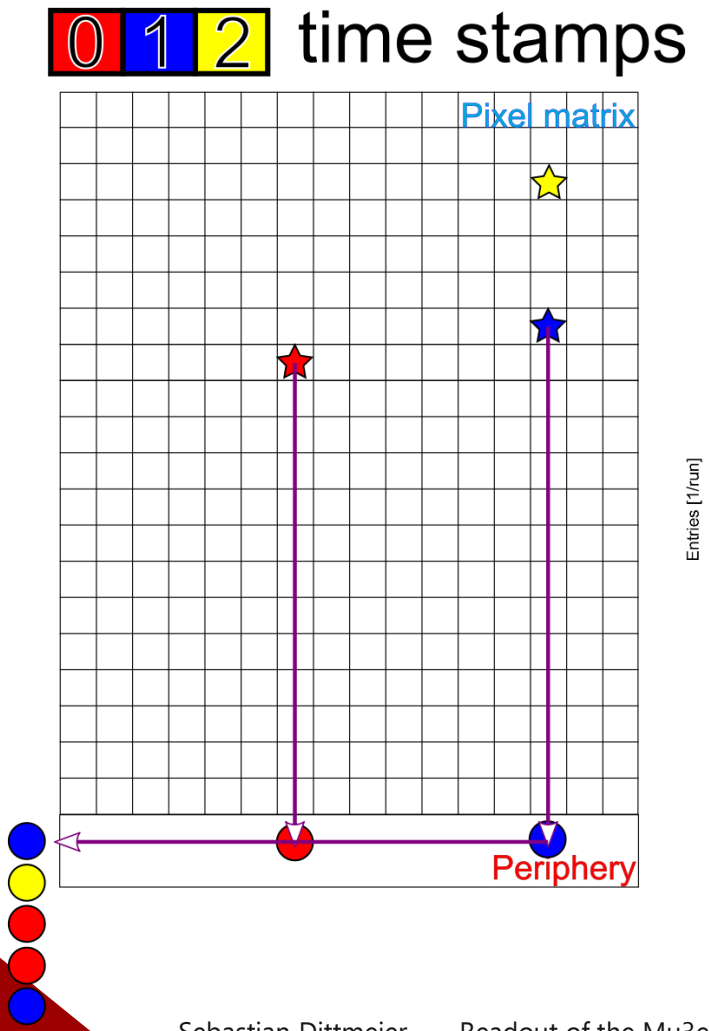

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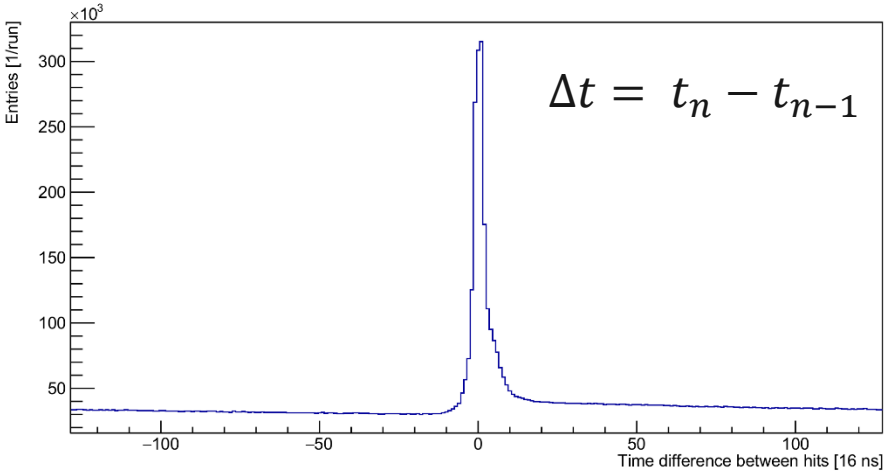

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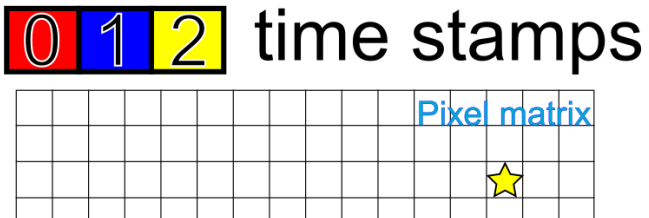

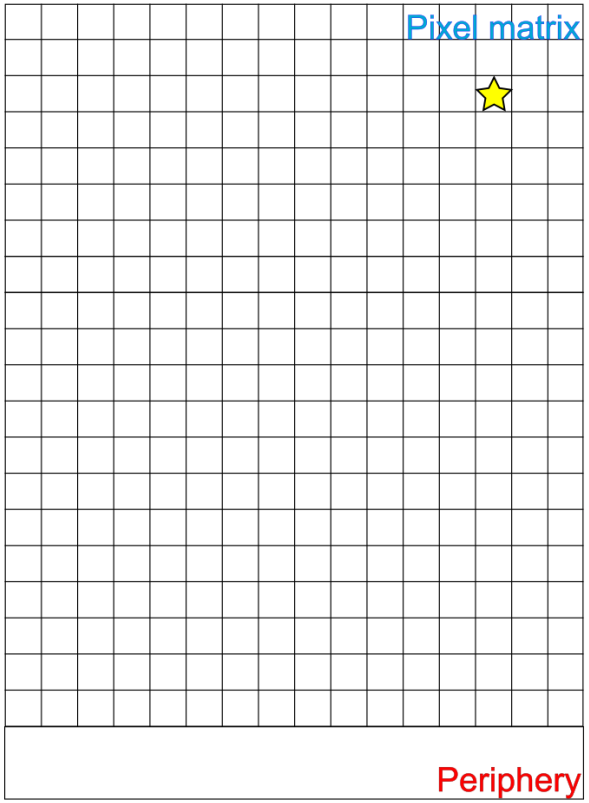

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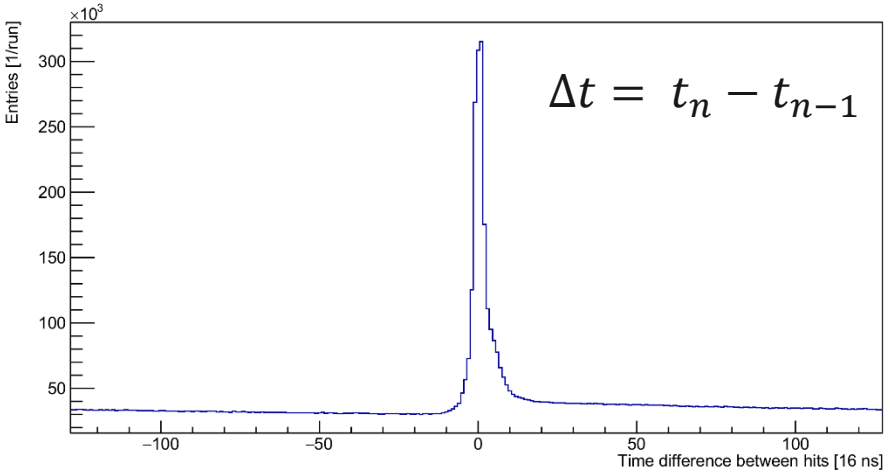

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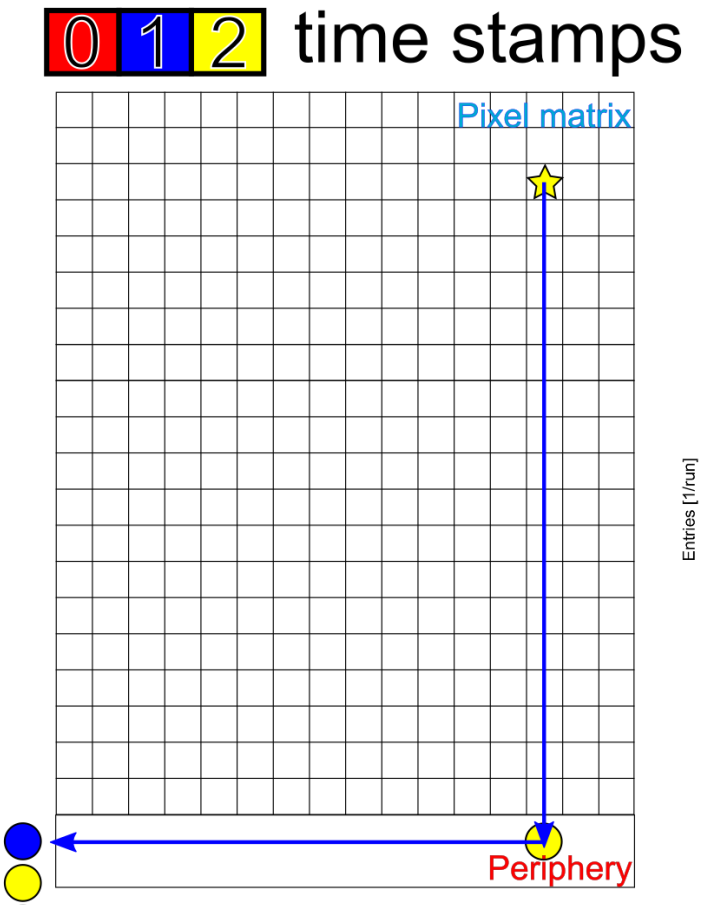

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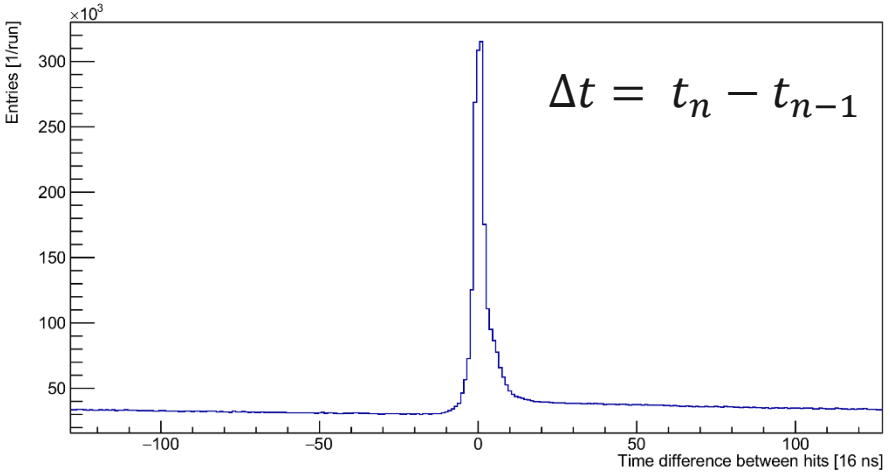
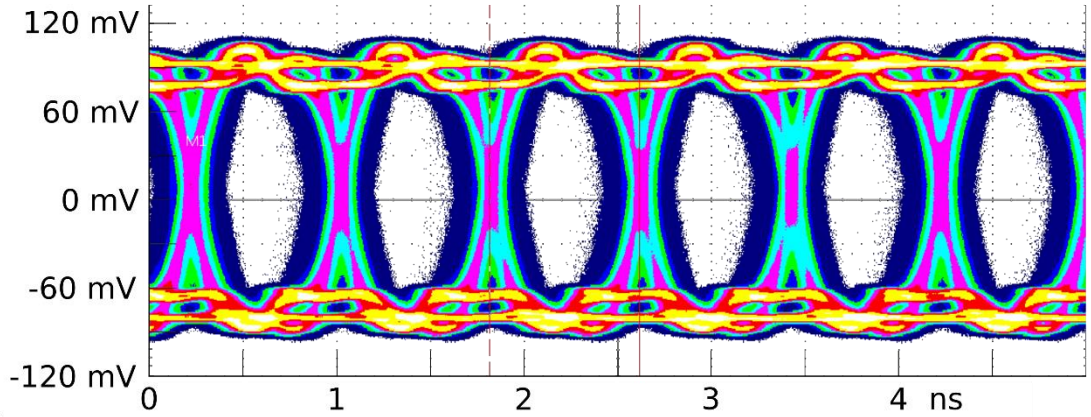


MuPix 7 – Serial Data Transfer

- 8b10b encoded data
- LVDS link up to 1.6 Gb/s, operated at 1.25 Gb/s
- Mu3e: Electrical connection between sensor and Front-end FPGA over aluminium interconnects

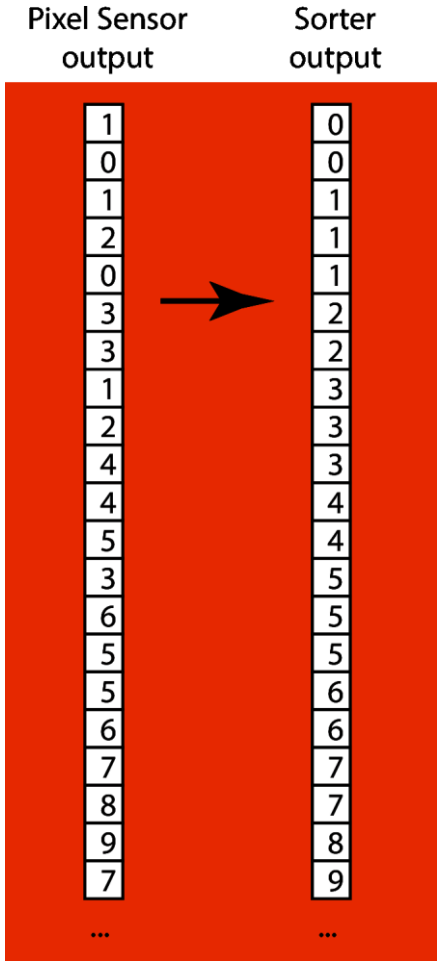
  T46.6: J. Kröger, Flexprint Design Studies for Mu3e
- MuPix8: 3 LVDS links per sensor

Eye diagram of MuPix7 after clock recovery (SMA cables)



Front-end FPGA

- Up to 45 LVDS links per FPGA
  ≙ 15 sensors with 3 links each
- Data decoding
- Time sorting of hits
- Packets of hits are sent using optical transceivers towards switching boards



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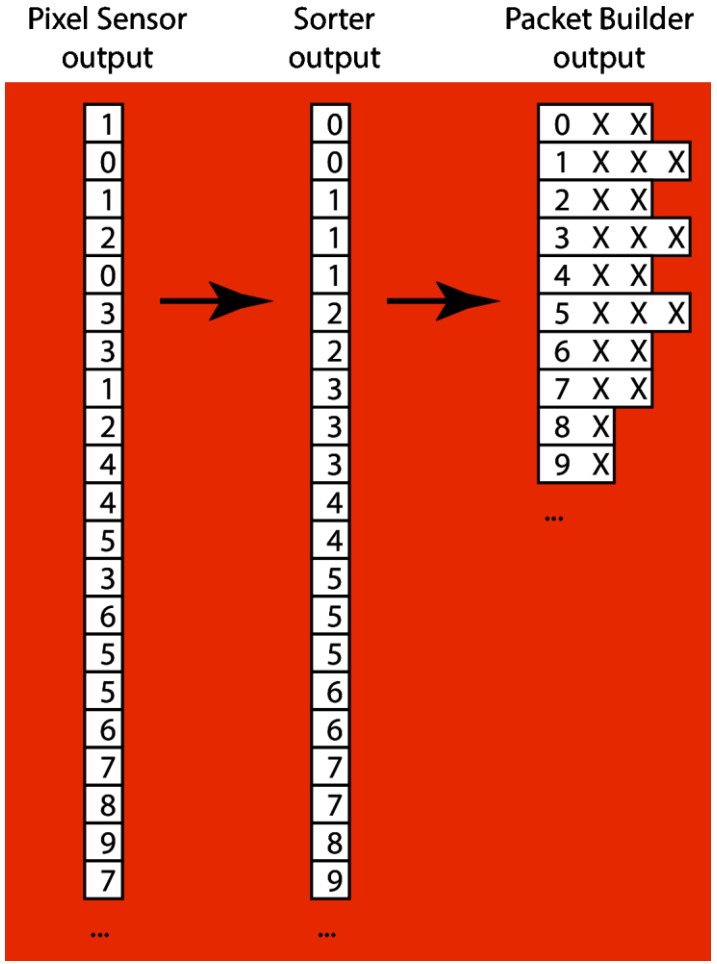
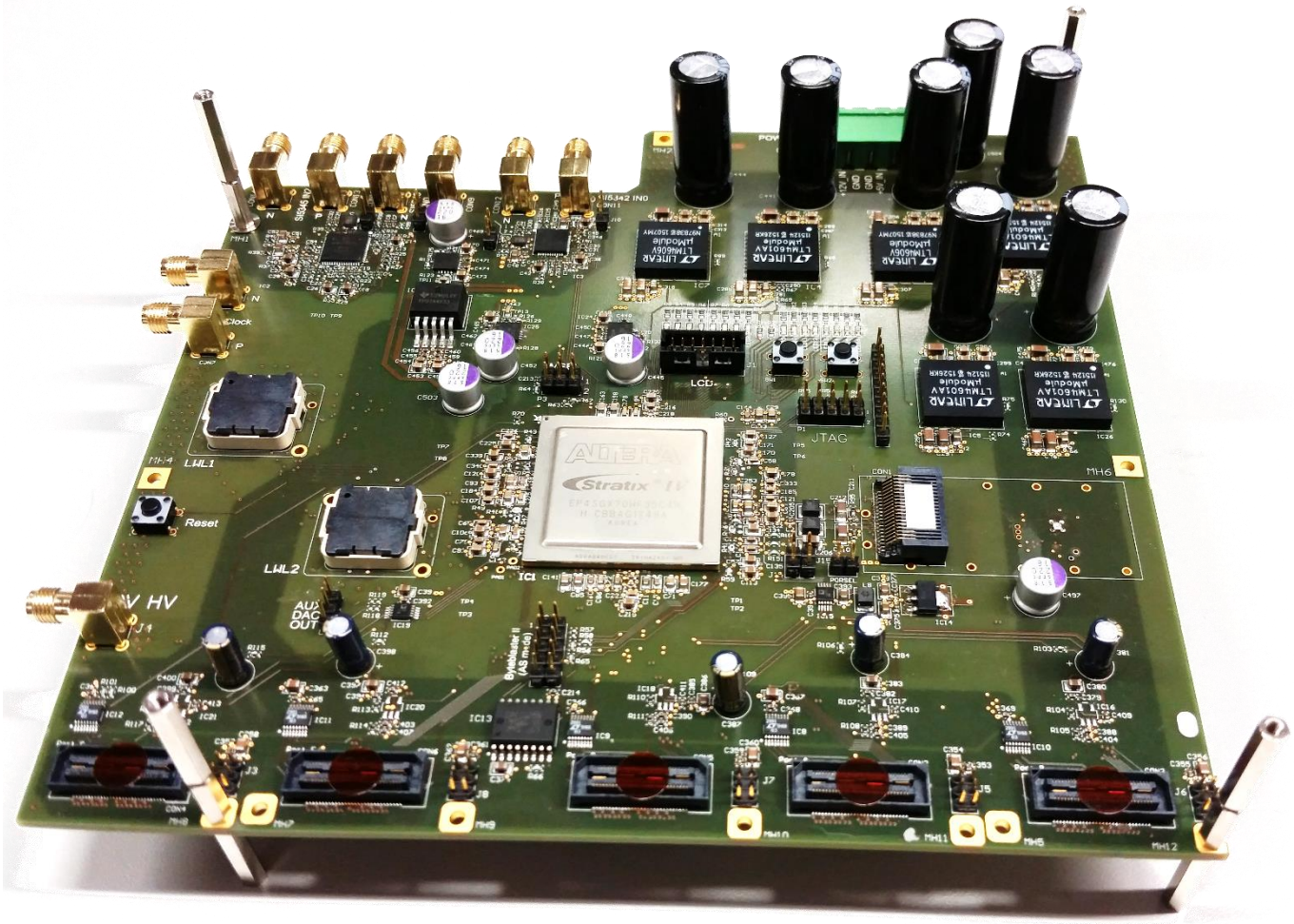


Front-end FPGA Board Prototype



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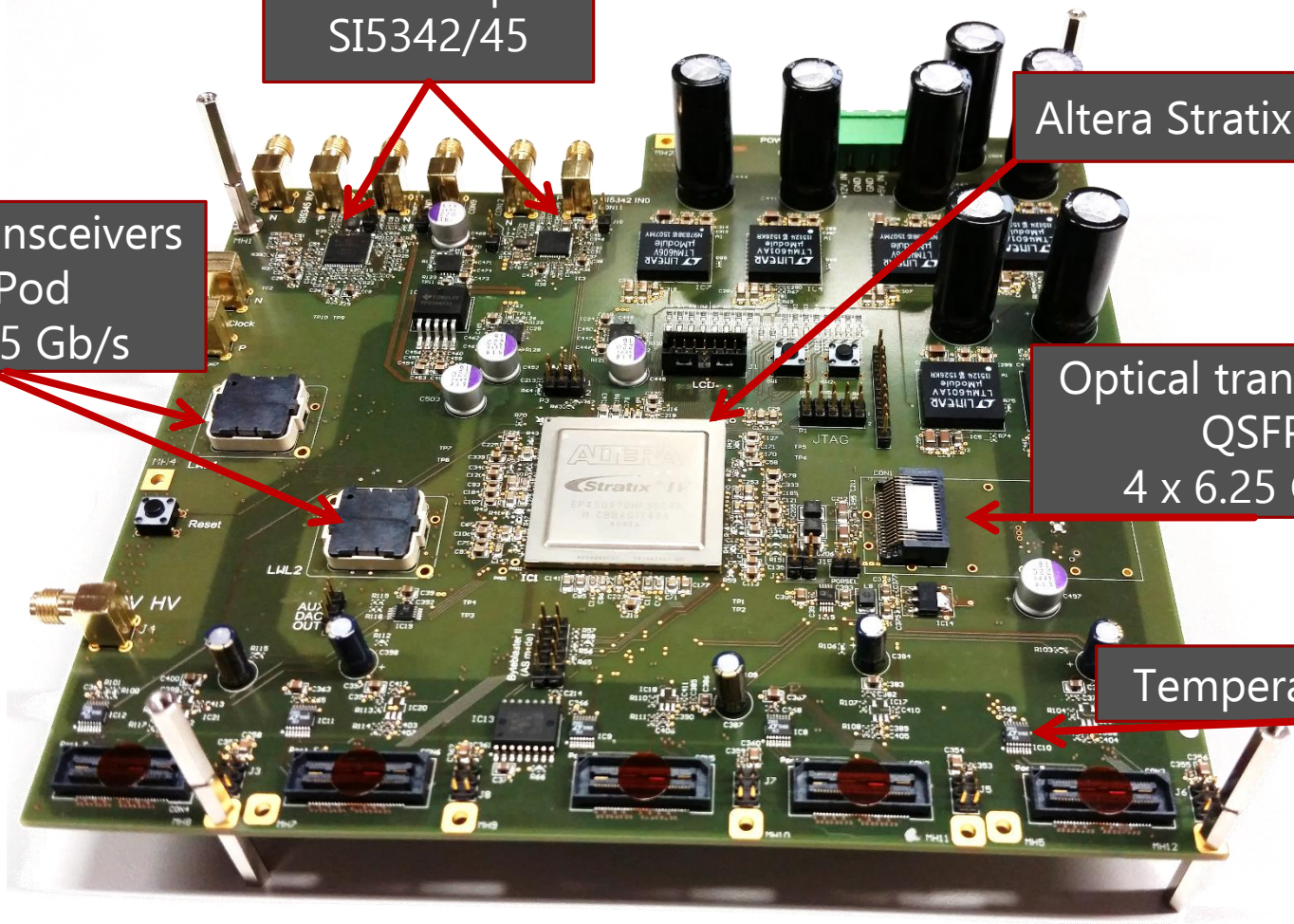
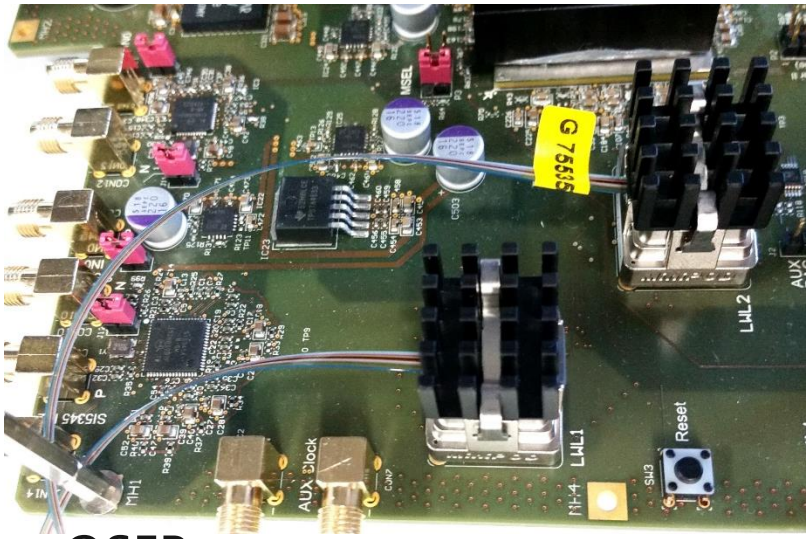
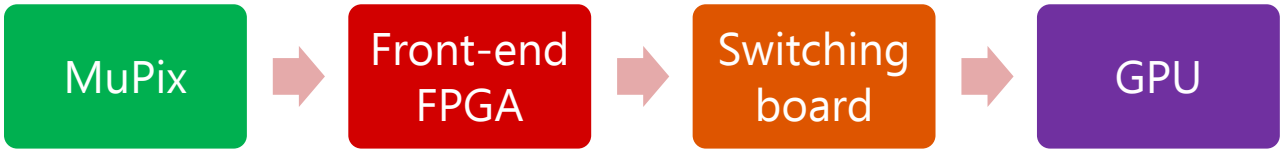


Optical Data Transmission

- Bit error rate tests
  8b10b encoded counter pattern



- MiniPod:
  - AFBR-811FH1Z / AFBR-812FH1Z
  - 1 m long multi-mode fibre
  - No bit errors observed
    on all 12 channels
  - **BER** $\leq 3.5 \cdot 10^{-16}$ @ 95% CL
    per channel
- QSFP:
  - Molex 106410-A-02
  - 3 m long single mode fibre
  - No bit errors observed
    on 3 of 4 channels
  - **BER** $\leq 1.9 \cdot 10^{-15}$ @ 95% CL
    per channel
  - 1 channel not responsive
    (soldering issue)

Summary and Outlook

- Three main layers of the triggerless Mu3e DAQ
  - Time sorting of hit data at the front-end FPGA
  - Data merging at the switching boards
  - Online event filtering on GPU filter farm
- Front-end FPGA prototype tested
  - Error-free optical data transmission at 6.25 Gb/s per channel
- Next step: Realization of the whole Mu3e readout chain