MuTRiG

- a Mixed-Signal SiPM Readout ASIC with High Timing Resolution and High Event Rate Capability

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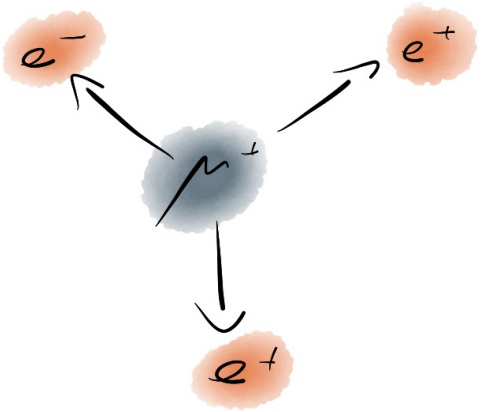
Mu3e Experiment

Search for $\mu^+ \rightarrow e^+e^+e^-$ at 10^{-16} level

- Forbidden in standard model (BR < 10^{-52})
- Clear sign for new physics



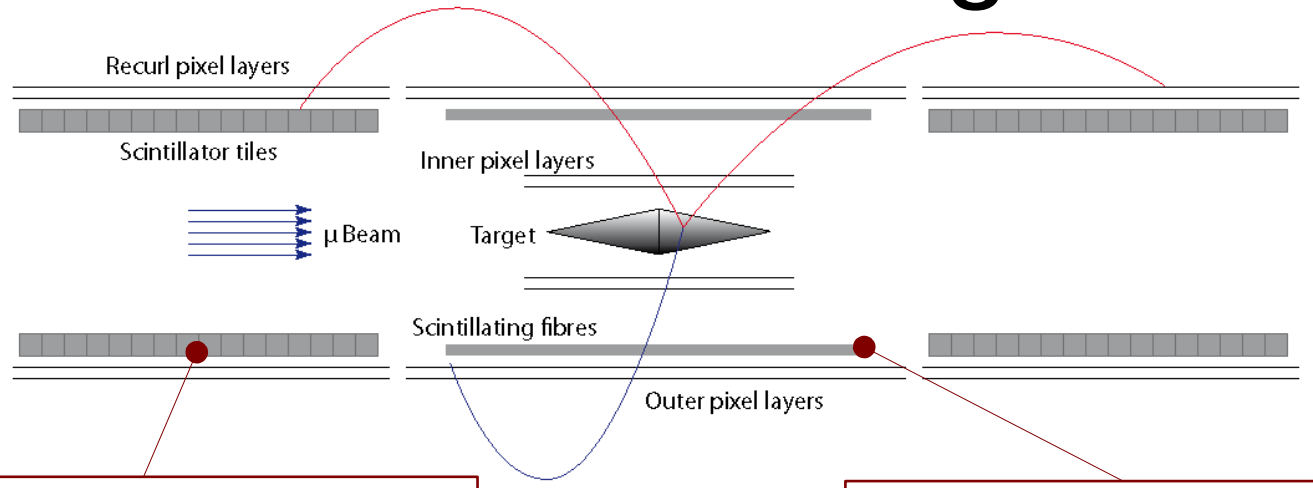
<u>Challenge</u>
Observe 1x10^{17} muon decay within a reasonable measurement time

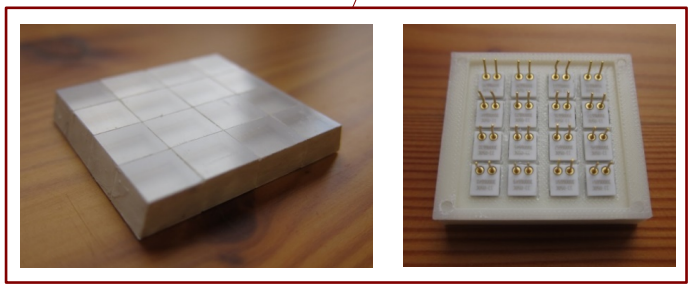
- Require high event rate, high geometrical acceptance and high efficiency

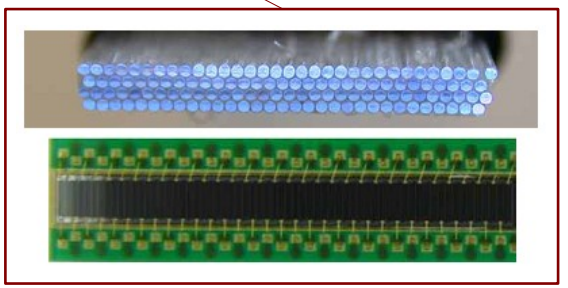
Suppress background to below a level Of 10^{-16}

- Require good momentum, vertex and timing resolution

Requirements for Timing Detector







Mu3e tile detectors
6272 SiPM channels
Requirements:

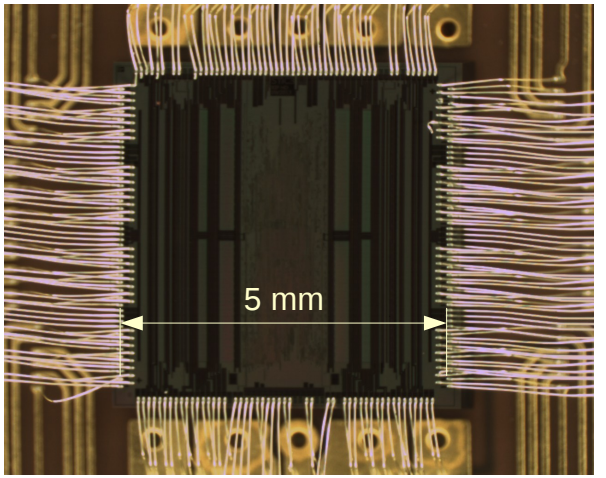
- Timing: 100 ps
- Event rate : 50 kHz/ch

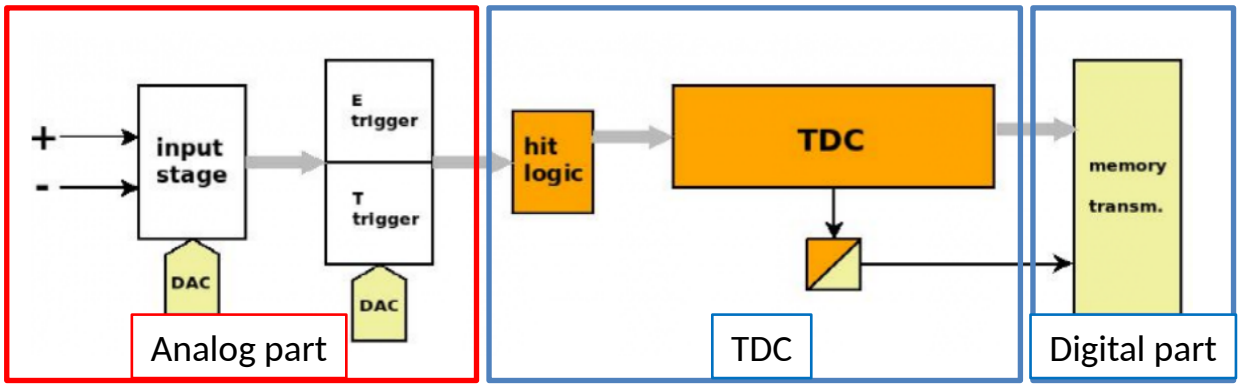
Mu3e fiber detectors
3072 SiPM channels
Requirements:

- Timing: 500 ps
- Event rate :
  700 kHz/ch - 1.3 MHz/ch

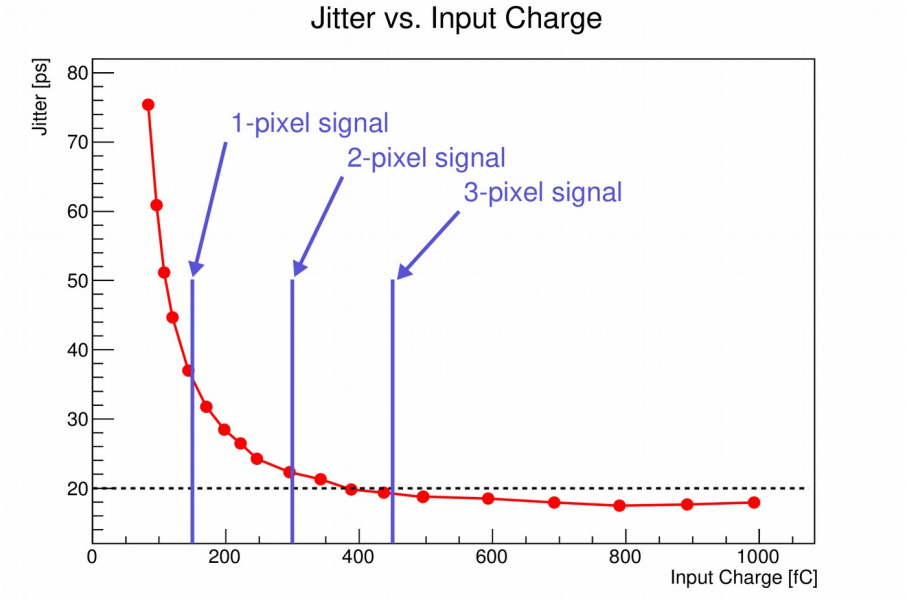
STiCv3 Chip

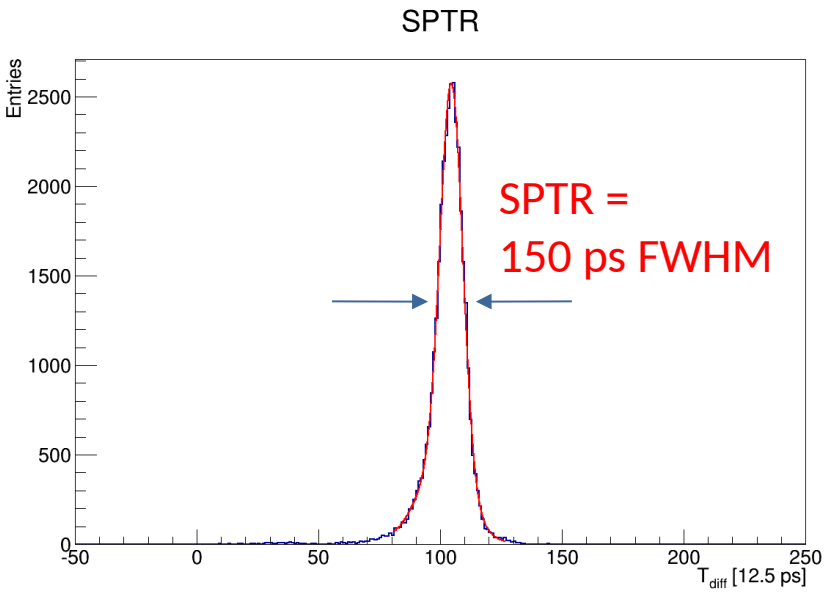
- 64-channel SiPM readout ASIC for Time-of-Flight applications
- Mixed-signal ASIC
  - Fully-differential analog front-end
  - 50 ps time binning TDC
  - On-chip digital circuit for event data processing and transferring to DAQ





Excellent Timing Performance of STiCv3





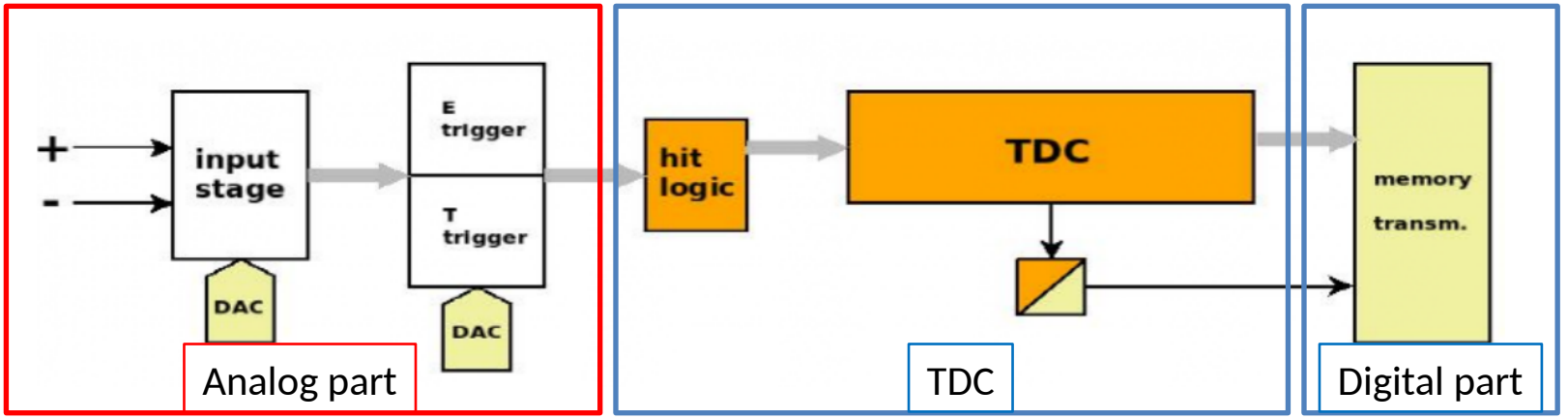
Charge injection measurement

- Analog front-end timing performance
- Time jitter < 20 ps for charge > 450 fC

Single photon timing resolution (SPTR)

- SPTR: 150 ps FWHM

Event Rate Limit on STiCv3



- Dead time depends on the input signal
- Almost no rate limit

- Dead time: 30 - 50 ns
- > 20 MHz/ch

- Serial data link, 160 Mbps per chip
- ~40 kHz/ch

MuTRiG: upgrade of STiCv3

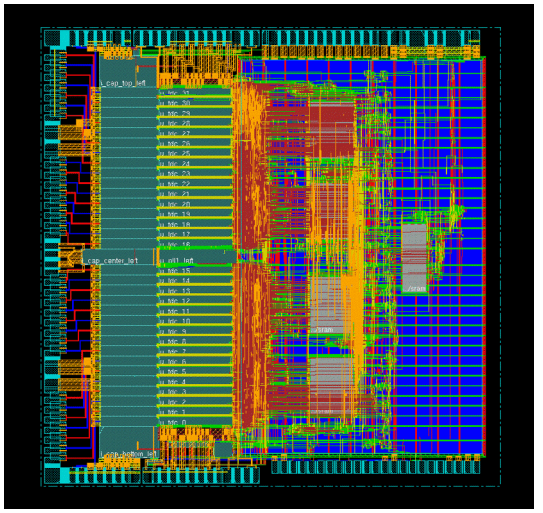
Keep the timing performance

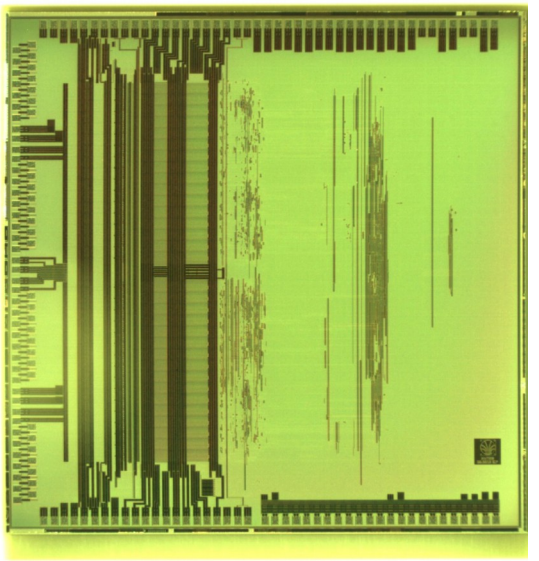
- Fully differential analog front-end
- 50 ps timing binning TDC

Increase the event rate capability

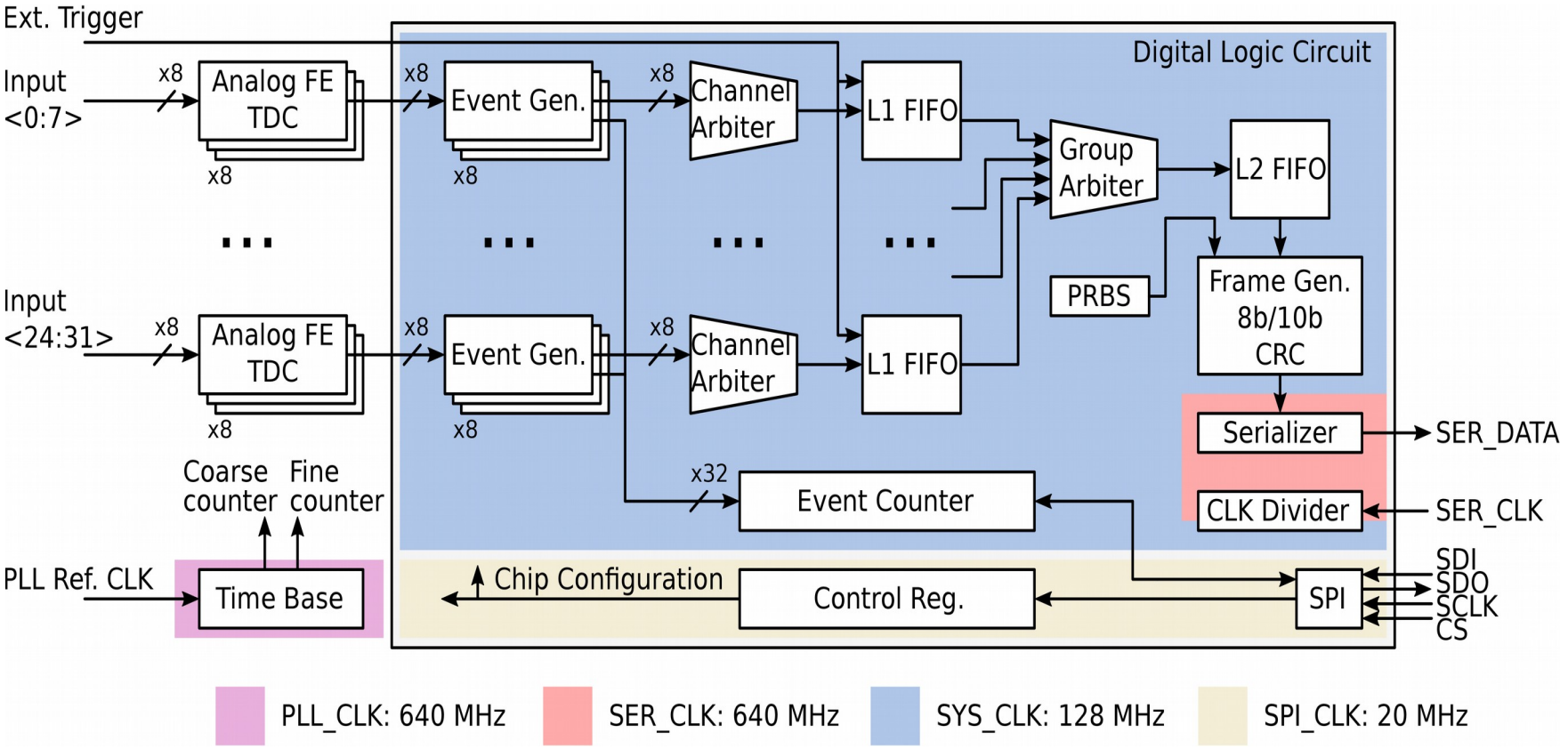
- Much higher serial link data rate:
  - 160 Mbps → 1.28 Gbps
- Switchable output event size:
  - Time + energy, full event (47 bits)
  - Timing + 1 bit energy info (27 bits)
- Less channels:
  - 64 → 32

Upgrade digital logic circuit



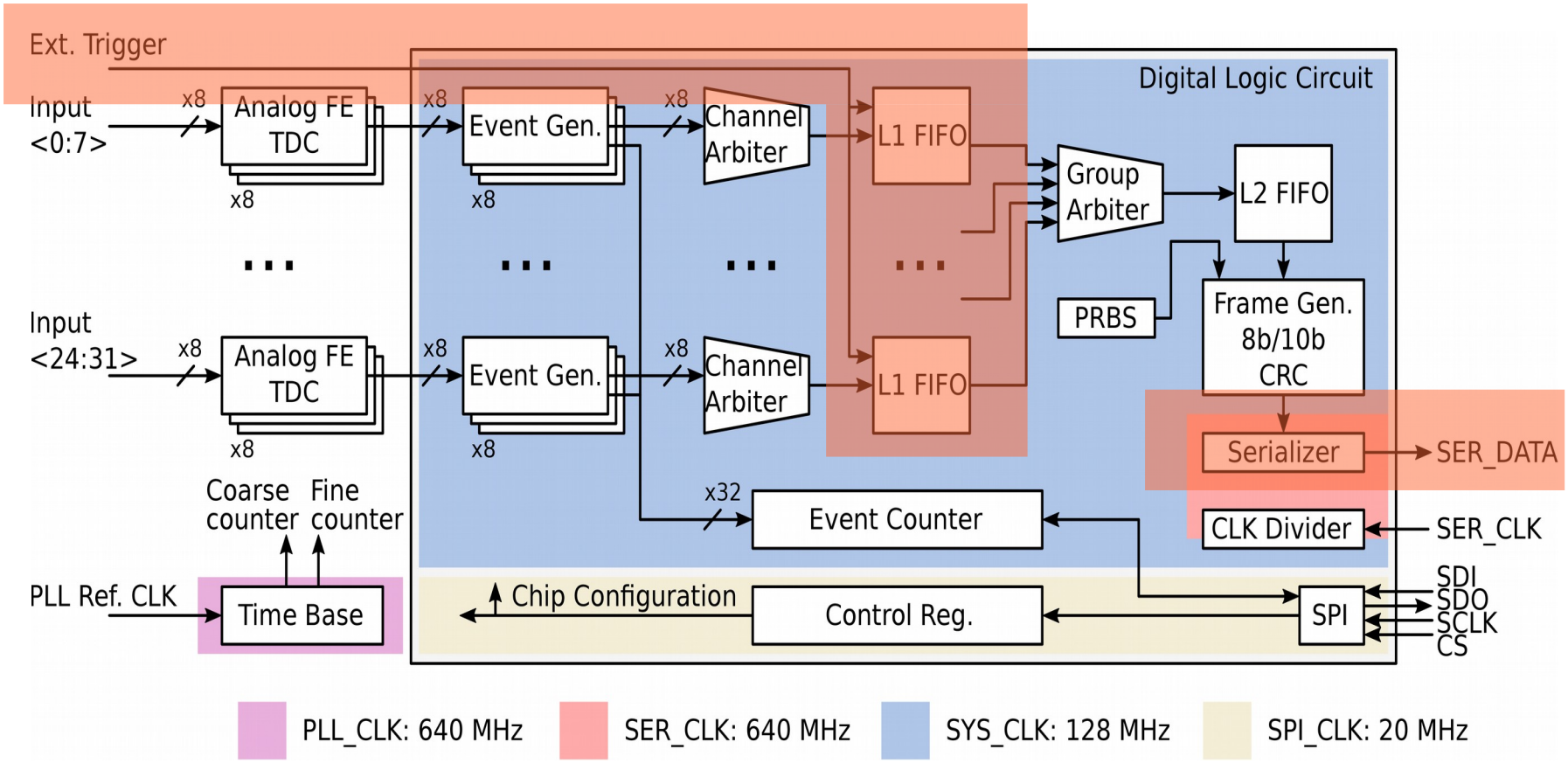


MuTRiG: Block Diagram



- Gigabit serial data link
- External trigger
- Channel event counter
- CRC for data transmission error detection
- PRBS

MuTRiG: Block Diagram



- Gigabit serial data link
- External trigger
- Channel event counter
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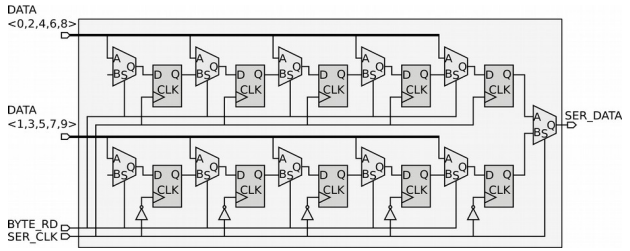
MuTRiG: Gigabit Serial Data Link

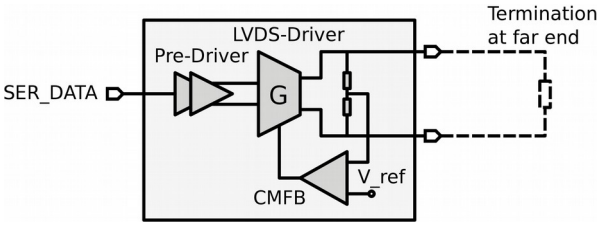
Double Data Rate Serializer

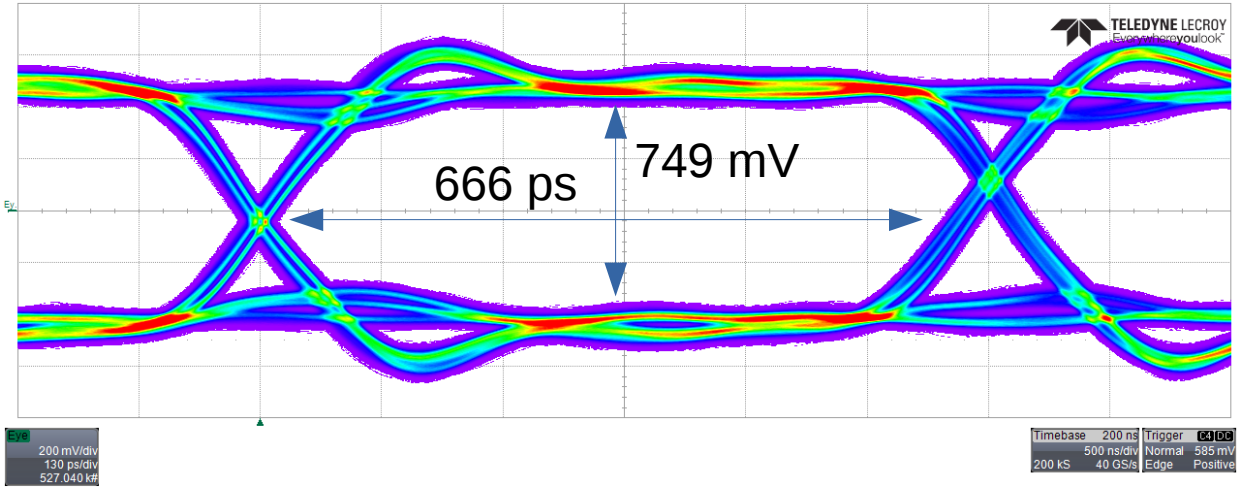
- Send data bits at both rising and falling edge of serial clock (640MHz): 1.28 Gbps data rate



Customized LVDS TX cell

- Driving serial data signal to far end receiver
- An opened eye diagram of PRBS data with 8b/10b encoding at 1.28 Gbps

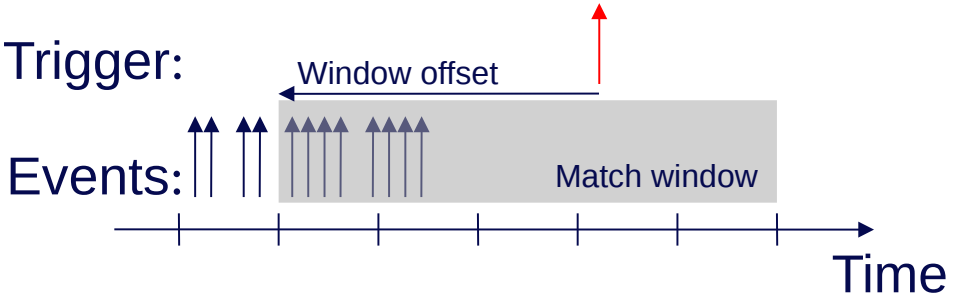


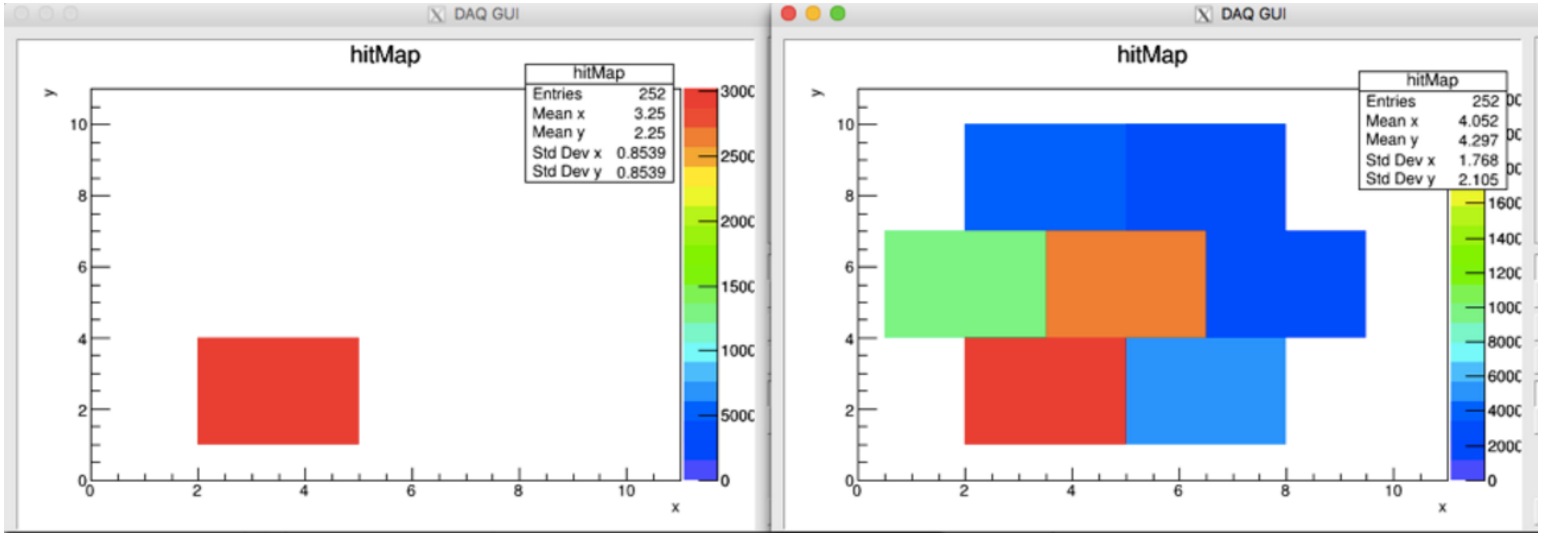


MuTRiG: External Trigger

Send out the events within the match window around the trigger signal

- Configurable match window size
- Tested on KLauS chip.





Summary

MuTRiG is

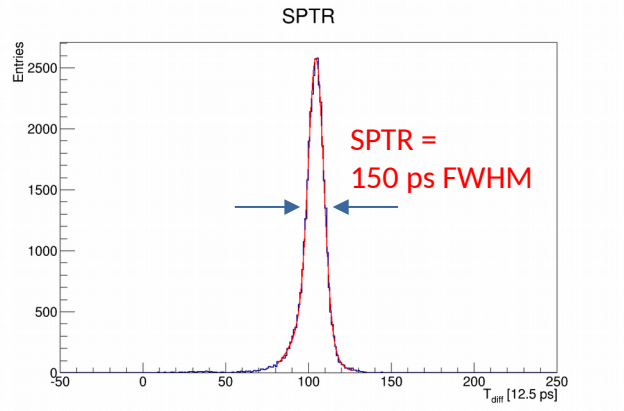
- a 32-channel **mixed-signal** SiPM readout ASIC

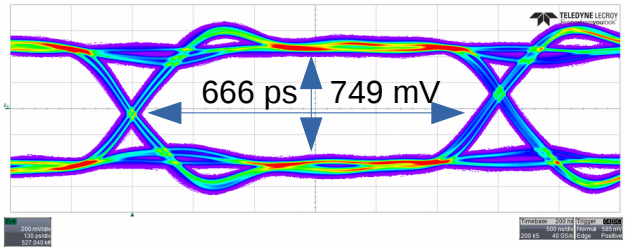
- **Fully differential analog front-end**
  + 50 ps timing binning TDC
  - Analog FE Jitter < 20ps; SPTR = 150 ps FWHM (STiCv3)

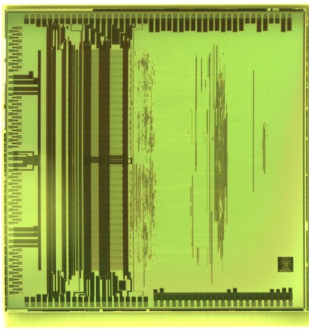
- **Gigabit serial data link**
  - Clearly opened eye diagram @ 1.28 Gpbs

- **External trigger** functionality tested on KLauS chip

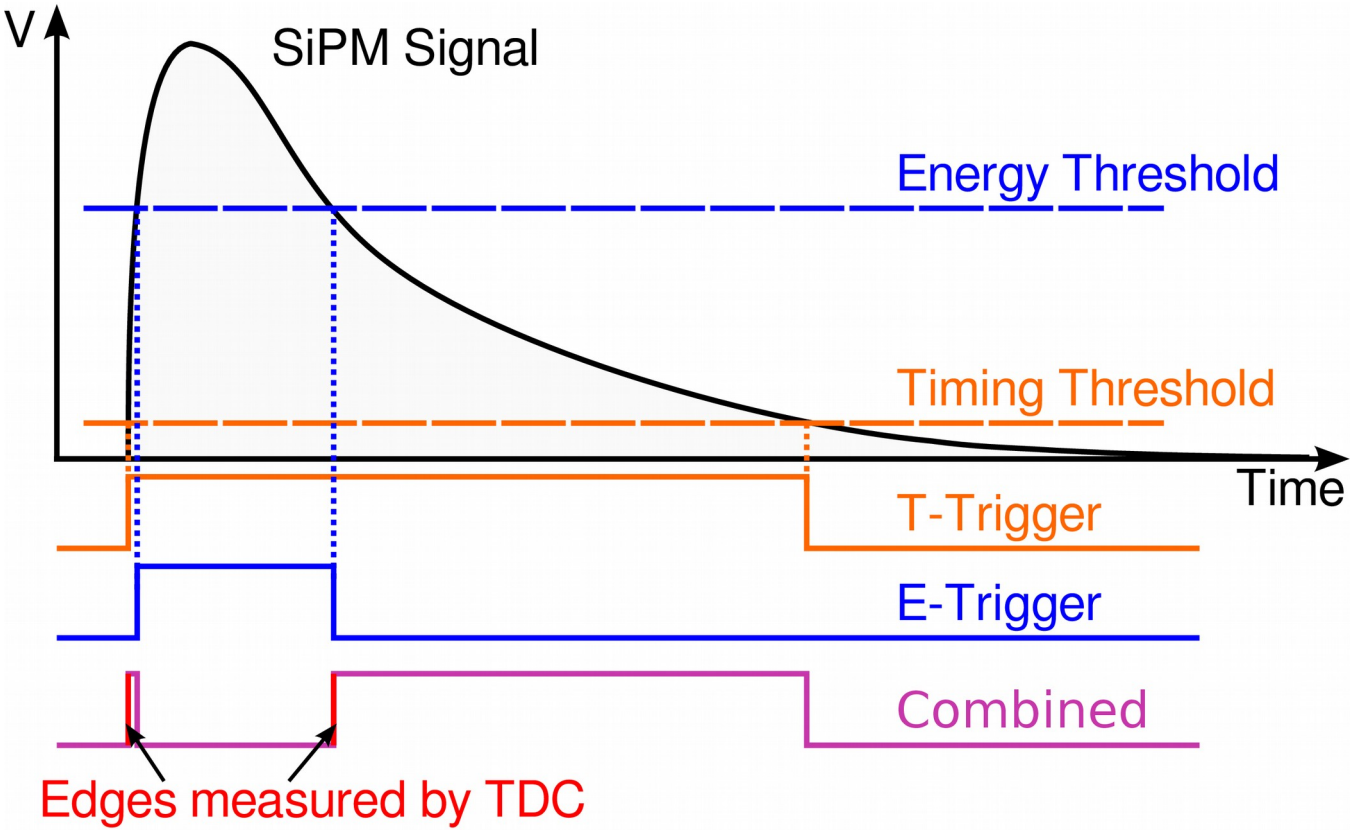
- Characterization setup is being prepared.







Backup – STiC readout principle



Backup – external trigger