The MuPix8 Chip
A monolithic large scale pixel sensor

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DPG Spring Meeting: HK 18.1
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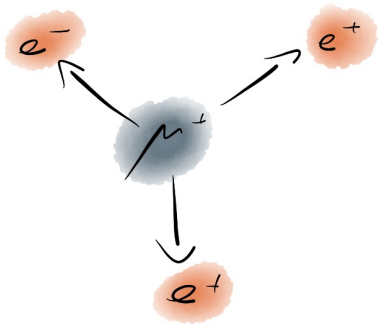
Mu3e



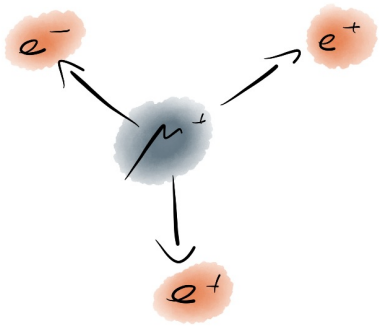
R.M.Djilkibaev and R.V.Konoplich,

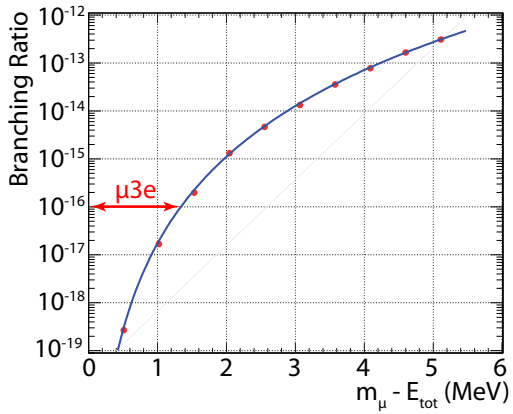
Phys.Rev., D79 073004, 2009

- $\mu^+ \to e^+e^-e^+$ (νSM: BR $< 10^{-54}$)
- current limit (SINDRUM) BR $< 10^{-12}$ @ 90% CL
- aiming for sensitivity of 1 in 10^{16} decays

- muons decay at rest: $\Sigma\vec{p} = 0$
- common vertex and coincident in time
- reconstruct invariant mass ($E_{tot} = m_\mu$)
- max momentum 53 MeV

Mu3e





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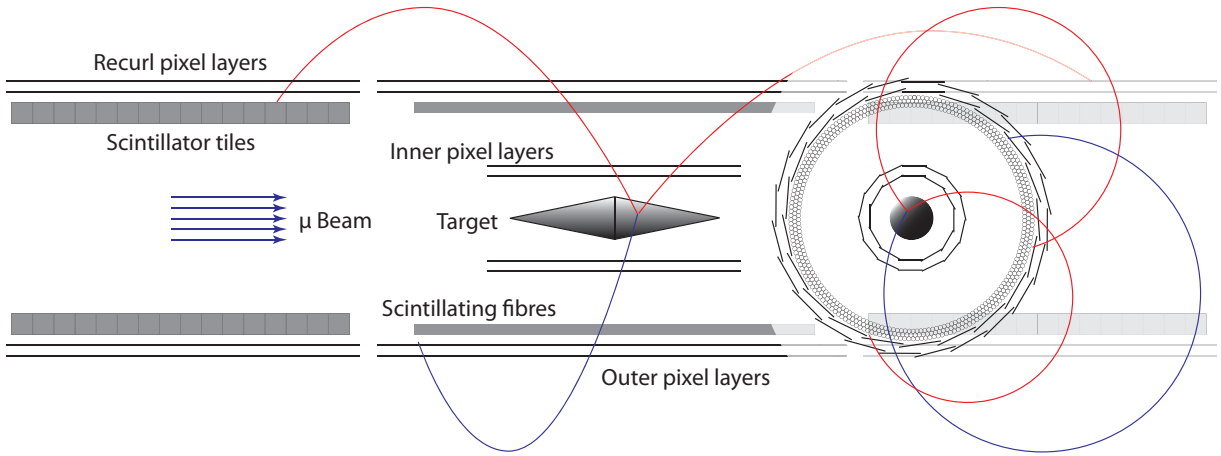
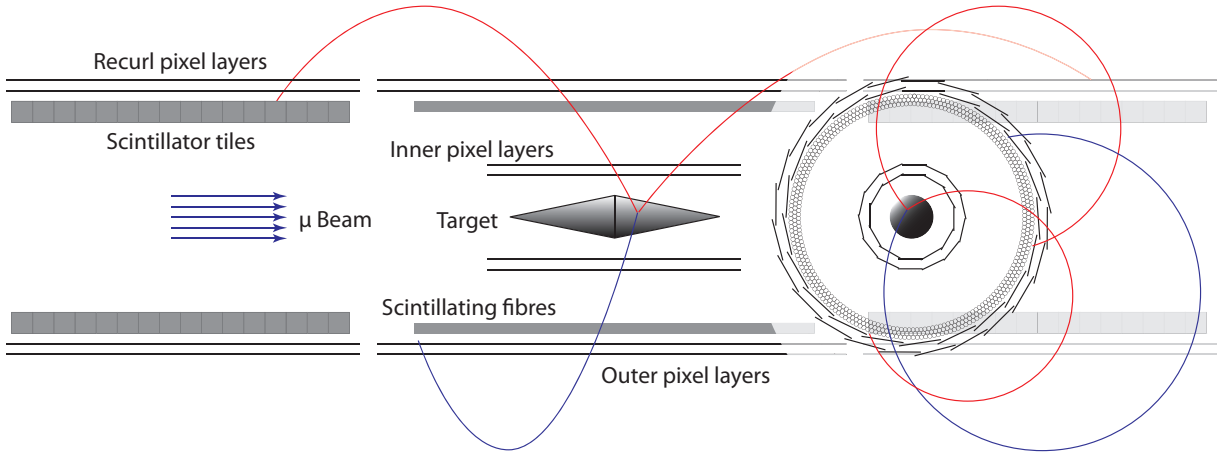
The Mu3e Experiment



- 10^9 muon decays per second
- good vertex & time resolution (100 μm & 500 ps)
- good momentum resolution (0.5 MeV)

The Mu3e Experiment



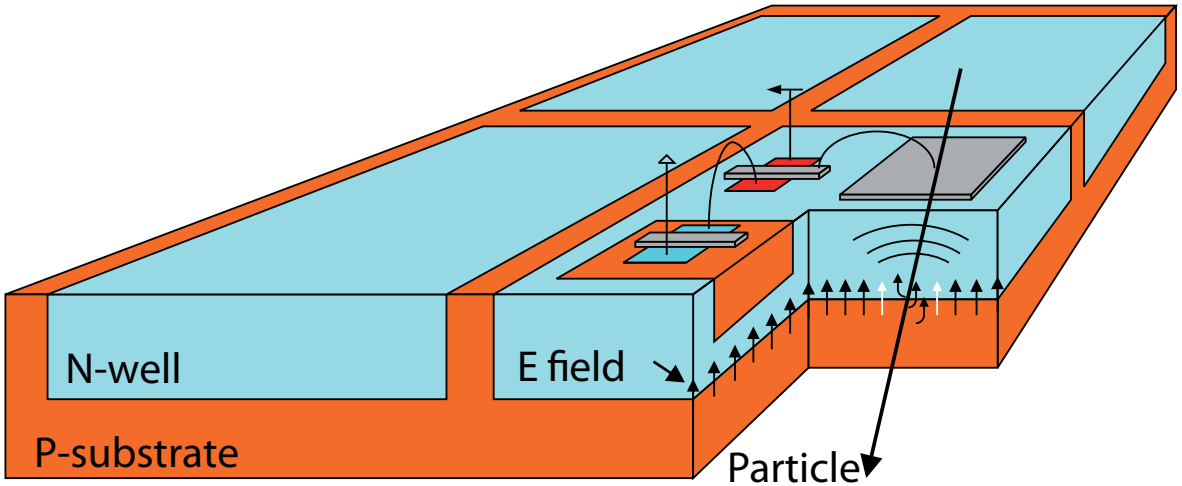
Multiple Coulomb Scattering:

$$\Theta \propto \frac{1}{p}\sqrt{x/X_0}$$

- optimize the material budget
- thin silicon sensors required $1‰ X_0$

$\rightarrow$ HV-MAPS

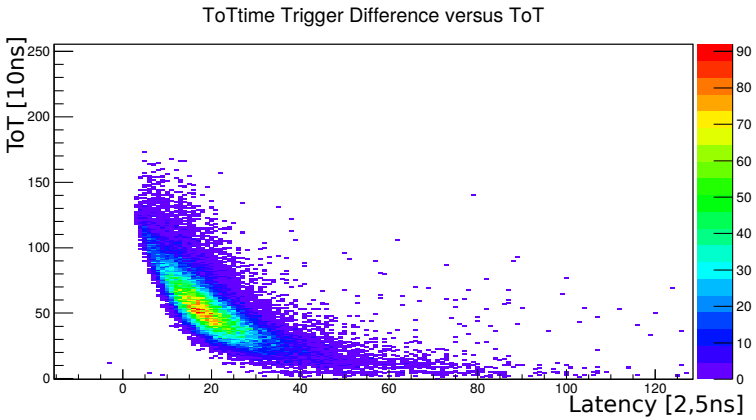
High Voltage - Monolithic Active Pixel Sensor (HV-MAPS)



I.Peric, P. Fischer et al., NIM A 582 (2007) 87

- low ohmic substrate (20 Ω cm)
- high voltage (100 V)
- AMS 180nm HV-CMOS
- depleted n-well diode
- charge collection via drift
- no additional readout chip

MuPix7 - Summary



- $80 \times 103\,\mu m^2$ pixel size
- $3.3 \times 3.3\,mm^2$
- full system on-chip
- $1.25\,Gbit\,s^{-1}$ data rate
- 99.5% efficiency
  with 14.3 ns time resolution
  @ $300\,mW\,cm^{-2}$

MuPix8 Design Features

- $80 \times 80\,\mu m^2$ pixel size
- $2 \times 1\,cm^2$ active area
- module building
- improve time resolution
- radiation hard design
- increase active volume ($80\,\Omega\,cm$ substrate)

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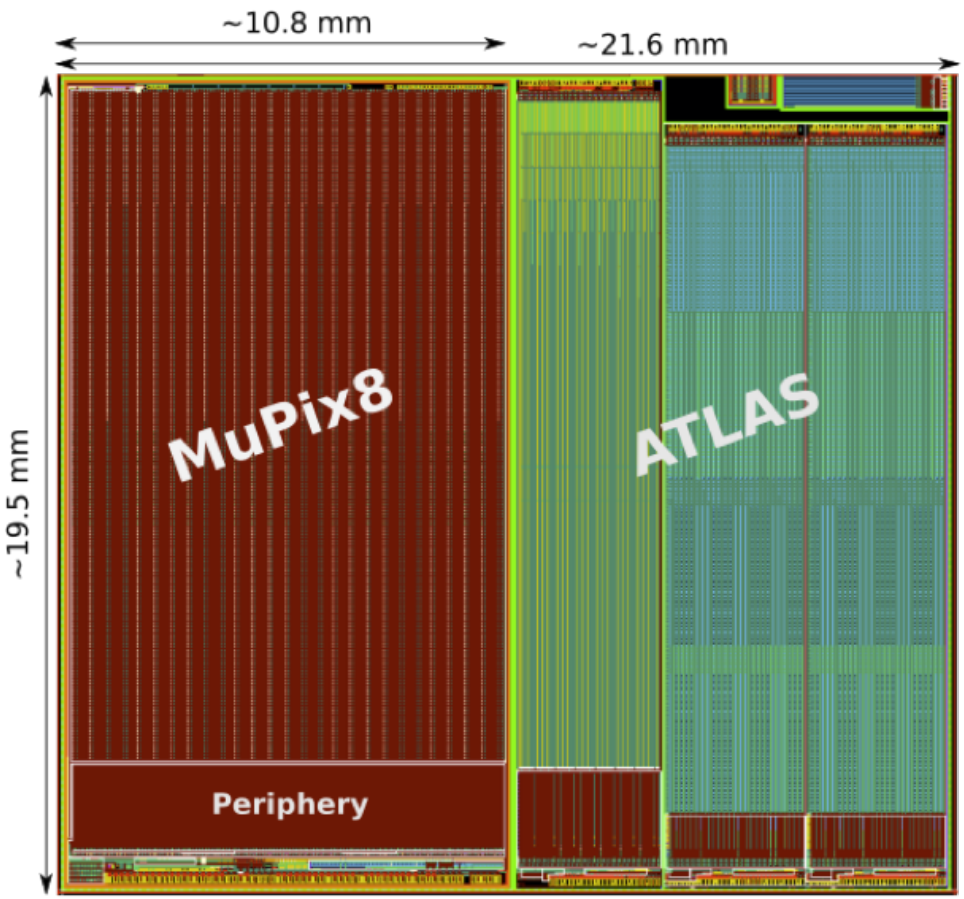
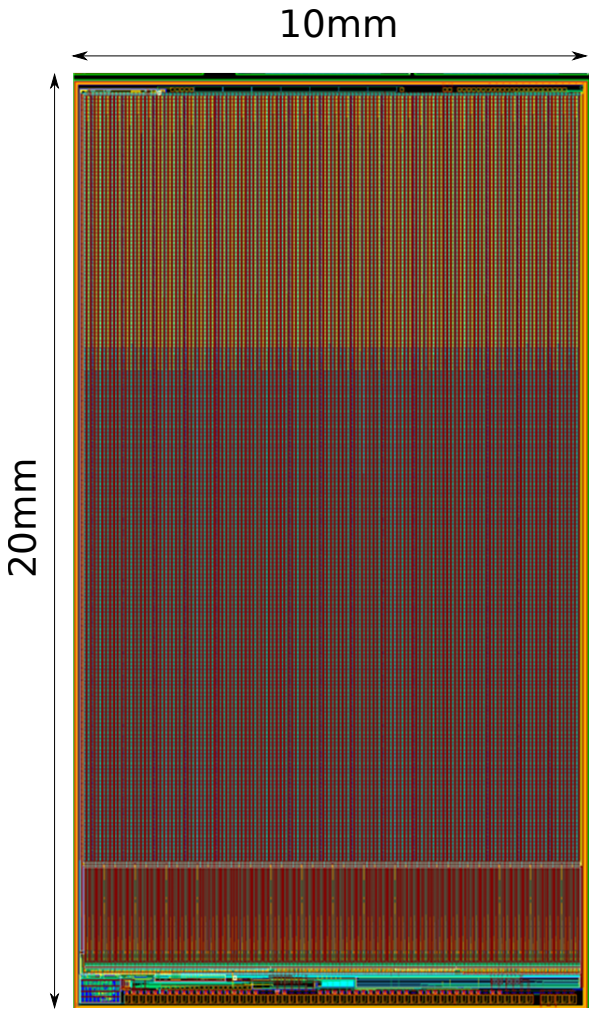
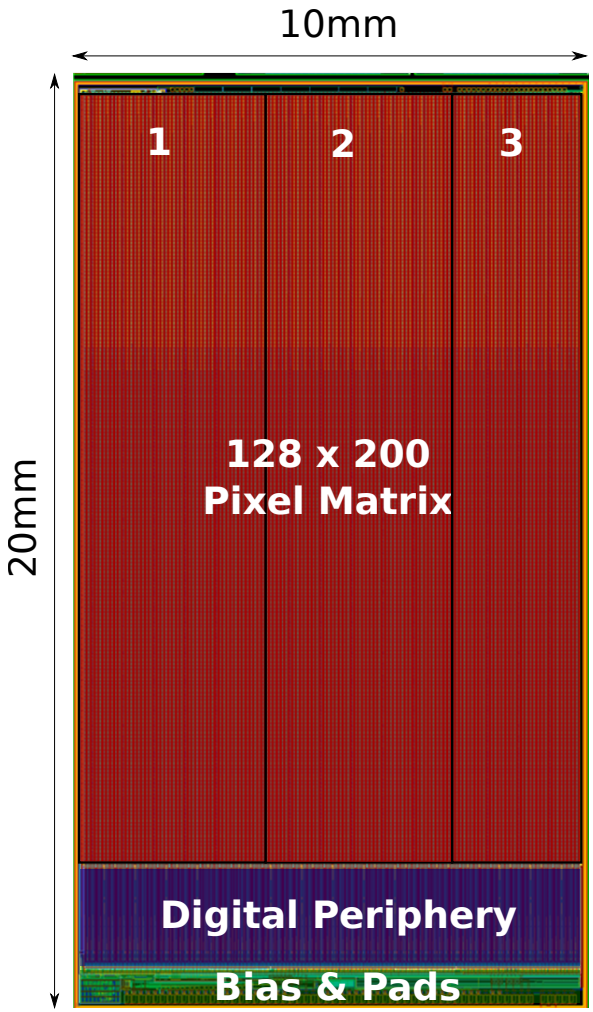


MuPix8 Chip



- $81 \times 80\,\mu m^2$ pixel size
- $17 \times 10\,mm^2$ active area
- 128×200 pixels
- 3 matrix partitions

MuPix8 Chip



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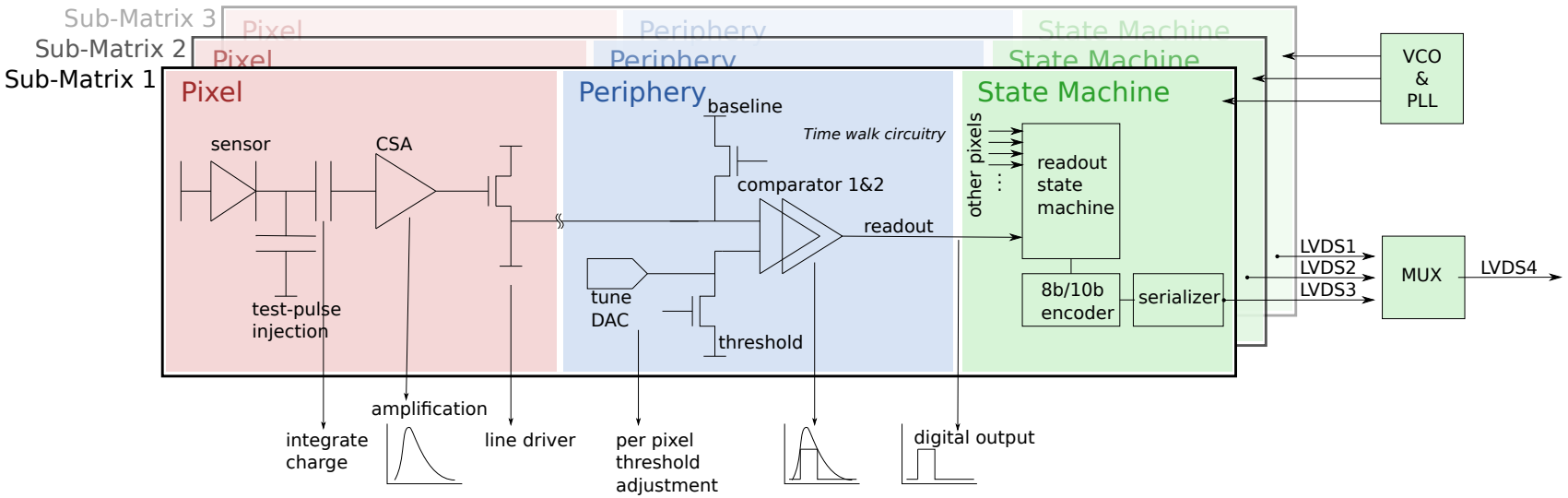
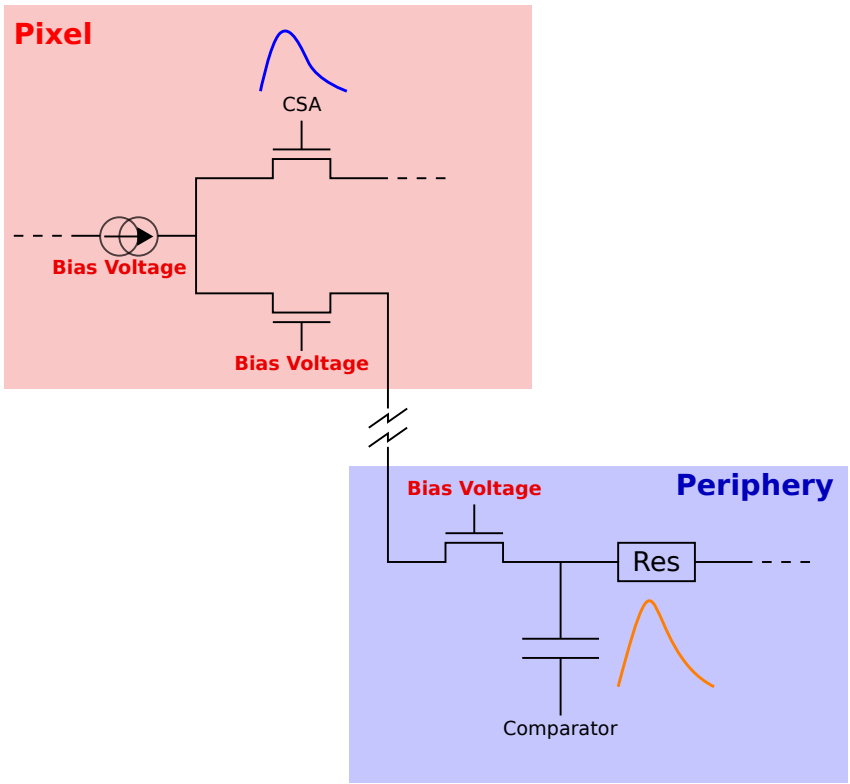
MuPix8 Electronics



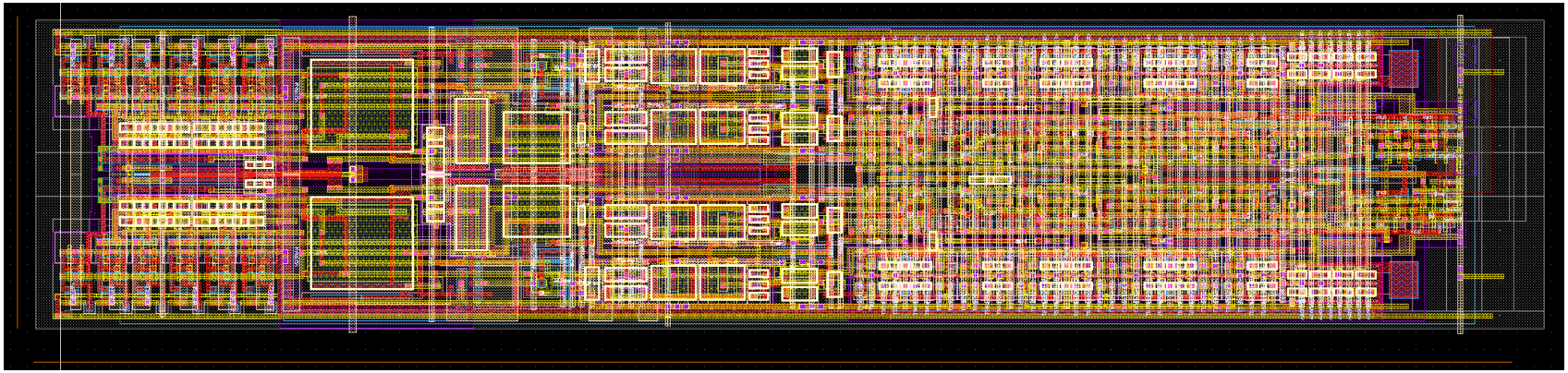
- timewalk reduction circuitry
- 3 sub-matrices with dedicated data output
- additional merged data output

Crosstalk and Signal Transmission



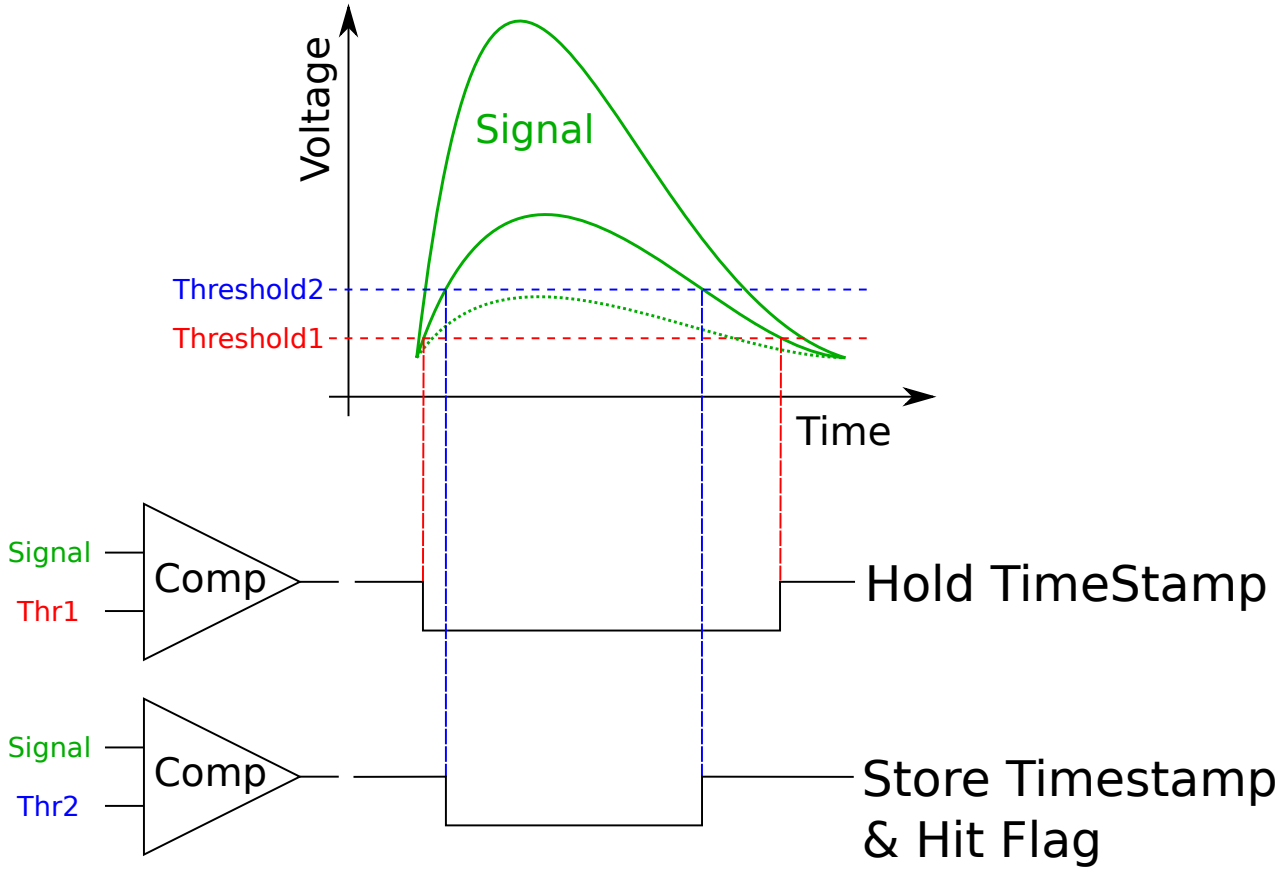
- very dense routing:
  2 metal layers, 200 signals
  300 nm spacing
- 1 sub-matrix source follower
- 2 sub-matrices current driven

Peripheral Cell



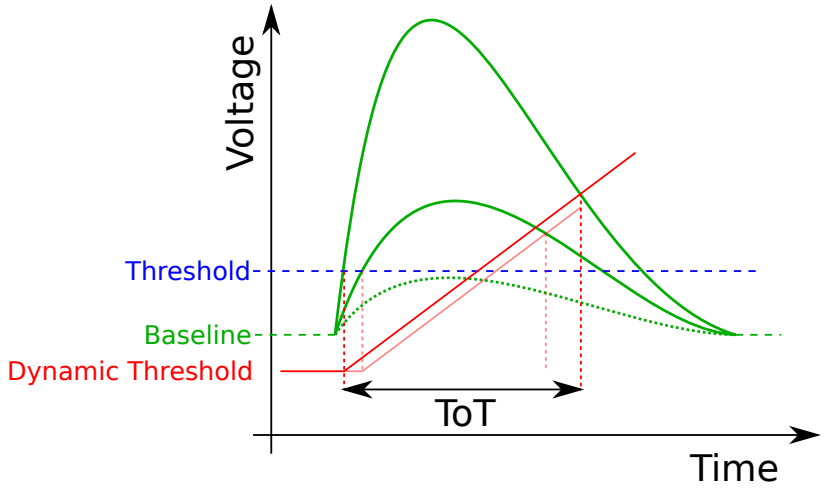
- 3 time walk correction approaches
- 2 comparators
- 10(+6) timestamp bits
- 3 Tune bits + pixel switch

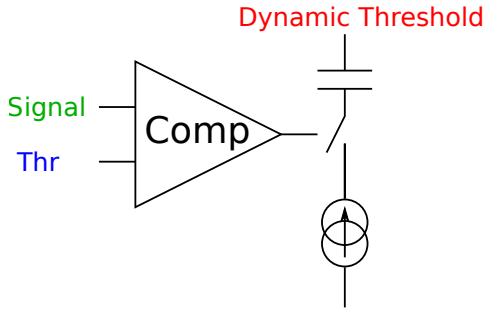
Timewalk Correction - Two Thresholds



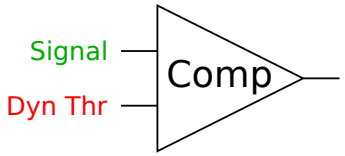
- simple
- timewalk suppression on-chip

Timewalk Correction - Two Thresholds





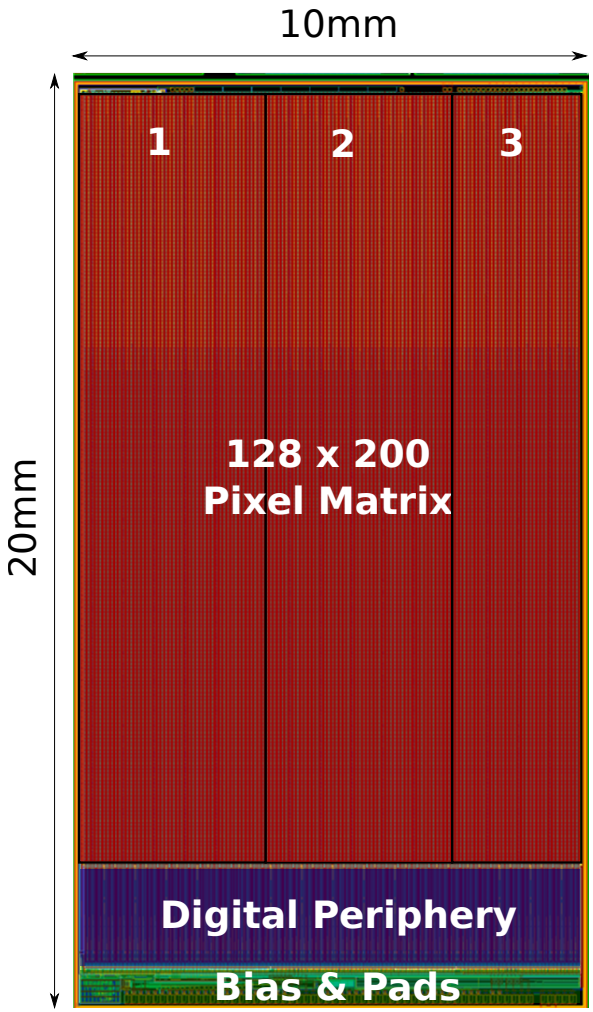
Start Ramp
& Store Timestamp



Store ToT Timestamp
& Hit Flag

- ToT sampling
- improve measurement with ramp
- off-chip timewalk correction necessary

Conclusion



- first large monolithic prototype
- expected in April
- module suitable
- exciting characterisation times ahead