MuPix8 – Large Area Monolithic HVCMOS Pixel Detector for the Mu3e Experiment

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Abstract

The requirements of the ultra thin pixel detectors for the Mu3e experiment at PSI can be achieved by the HVCMOS technology, which allows the design of fast monolithic detectors. The latest nearly full size prototype, MuPix8, has a size of about 1 x 2 cm^2. The pixel readout circuitry was fully redesigned in comparison to the previous MuPix versions. MuPix8's readout electronics implement a new concept with two comparators and two different operation modes. One mode uses two threshold voltages for time walk correction, the other is a ramp-ADC. First tests show a detection efficiency of 99.6% for 4 GeV electrons.

Keywords: HVCMOS, HVMAPS, High-voltage pixel detector, Monolithic Pixel Detector, Mu3e, Time Walk Correction

1. Introduction

A series of High Voltage CMOS (HVCMOS) sensor prototypes called MuPix has been designed for the Mu3e experiment at the Paul Scherer Institute in Switzerland. The latest nearly full size prototype is the MuPix8.

The Mu3e experiment is searching for the charged lepton flavor violating decay $\mu^+ \rightarrow e^+e^-e^+$ with an ultimate sensitivity of one in 10^{16} decays. The requirements for the pixel detector for Mu3e are a vertex resolution of about 100 µm, a time resolution of less than 20 ns for phase 1 and for phase 2 even better and a silicon sensor thickness of not more than 50 µm. The HVCMOS technology can fulfill these requirements. The final detector will have an instrumented area of about 2 m^2 [1]. HVCMOS sensors are depleted monolithic CMOS pixel sensors implemented in a standard commercial CMOS process. The MuPix8 is fabricated in the AMS aH18 technology with a minimum transistor gate length of 180 nm. The chips are produced on wafers with different substrate resistivities: 20 Ωcm, 50-100 Ωcm, 200-400 Ωcm, 600-1100 Ωcm. Monolithic pixel sensors unite the sensor and the readout electronics on a single die. This leads to a simplified fabrication process of modules, as well as a reduction of cost and material budget. The sensor element is the deep n-well/p-substrate diode. For fast charge collection and large active area, high voltage is used [2].

In the following, the new readout electronics, allowing for two different readout methods and measurements for the linearity of the ADC threshold voltage method, are presented.

2. Architecture of MuPix8

The MuPix8's pixel matrix consists of 128 columns with 200 pixels each (pixel size 80 µm x 81 µm). In the MuPix architecture the pixel sensor cell is separated from the readout cell including the comparators. On the MuPix8, two different line driver modes have been implemented: voltage driven and current driven. The following results were made with the voltage driven submatrix. Every pixel contains an amplifier and an output driver inside the deep n-well. This deep n-well is the charge collection electrode. Furthermore, every column contains one readout block, divided into 200 readout cells, one for each pixel, and one endof- column block (EOC). The readout cells in the periphery receive the output signals of the pixel drivers and generate the hit information. The readout of the 200 cells has a column-drain architecture. The area of the readout cells is ten times smaller than the pixel area. MuPix8 uses a scan logic, which allows a faster search for hits. MuPix8's scan logic works with pixel groups: If a hit has been detected in a

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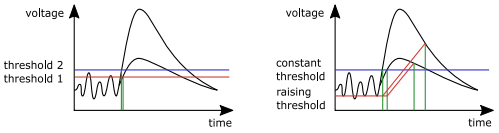


Figure 1: Left: Schematic of the readout mode with two threshold voltages. Right: Schematic of the readout mode with ADC threshold voltage.

group the subsequent groups are bypassed. The worst case execution time stays the same but average execution time is faster.

3. Readout Electronics with Several Readout Modes

A time walk correction can be applied to correct for amplitude dependent delays. The MuPix8 makes use of a two-comparator approach for time walk correction. With the second comparator, two new modes for the readout are possible. One comparator consumes approximately 1.8 µW, according to simulations. Therefore the increase of power consumption due to the second comparator is small. A typical value of the time walk of state-of-the-art HVCMOS detectors is about 60 ns.

3.1. Mode with two threshold voltages

The mode with two threshold voltages uses two different constant voltages. The lower threshold is close to noise level and thus delivers a timestamp with small time walk (see Fig. 1). Because this threshold is close to the noise level, the second threshold has to be higher to confirm that the first timestamp belongs to a signal (Fig. 1 left). In case of a confirmation, the timestamp from the lower threshold will be read out. The advantage is less time walk and a small noise rate.

3.2. Mode with ADC threshold voltage

The mode with ADC threshold voltage uses one constant threshold voltage and one linear rising threshold (Fig. 1 right). The constant threshold saves the timestamp and activates the linear rising threshold. The voltage of the ramp signal should start below the baseline of the chip. When the detected signal crosses the rising threshold, a second timestamp is saved. This timestamp provides amplitude information of the detected signal. The advantage is less noise and a better linearity as shown in the next section.

4. Measurement of the ADC Threshold Voltage

The following measurements show the linearity in the readout mode with ADC threshold voltage. The chip was operated at a readout speed of 400 MHz with timestamp width of 25 ns. Fig. 2 shows the ADC timestamp over the signal height for test signals of known charge. Fig. 2 shows a very good linearity. The calibration of this measurement was done by an X-ray fluorescence calibration. Four different targets, iron, zinc, molybdenum and silver were used. Fig. 3 shows the result.

In the case of a single comparator, the minimum threshold is about 6 sigma noise value above the base line. Simulated time walk for signals from 3000 to 7000 electrons is about 28 ns.

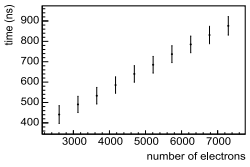
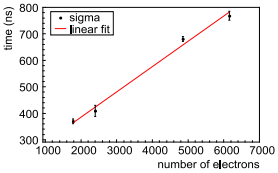


Figure 2: Test signal calibration of the mode with ADC threshold voltage.



Element	# e^- in Si
Fe	1778
Zn	2399
Mo	4855
Ag	6156

Figure 3: X-ray calibration with Fe, Zn, Mo, Ag targets.

In the case of two comparators, the threshold of the comparator that measures time can be lower, e.g. 3 sigma noise value above the base line because a possible noise hit will be not registered. In this case simulated time walk is about 14 ns. The ramp ADC can also indirectly improve the time resolution. Time delay is proportional to the amplitude and the ADC information can be used to compensate it. A good linearity of the ADC response, makes the delay compensation easier.

Furthermore, in 2017 first beam tests with MuPix8 at DESY and CERN were performed. The results show a uniformly high efficiency of 99.6 % for 4 GeV electrons (see figure 4).

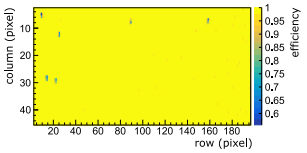


Figure 4: Efficiency beam tests at DESY for 4 GeV electrons

5. Conclusion

The MuPix8 is a large area monolithic HVCMOS pixel detector implementing several novel circuits as fast scan circuit, two comparators per pixel to allow for two threshold and a ramp ADC mode. All new circuits have been tested to work.

Acknowledgments

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