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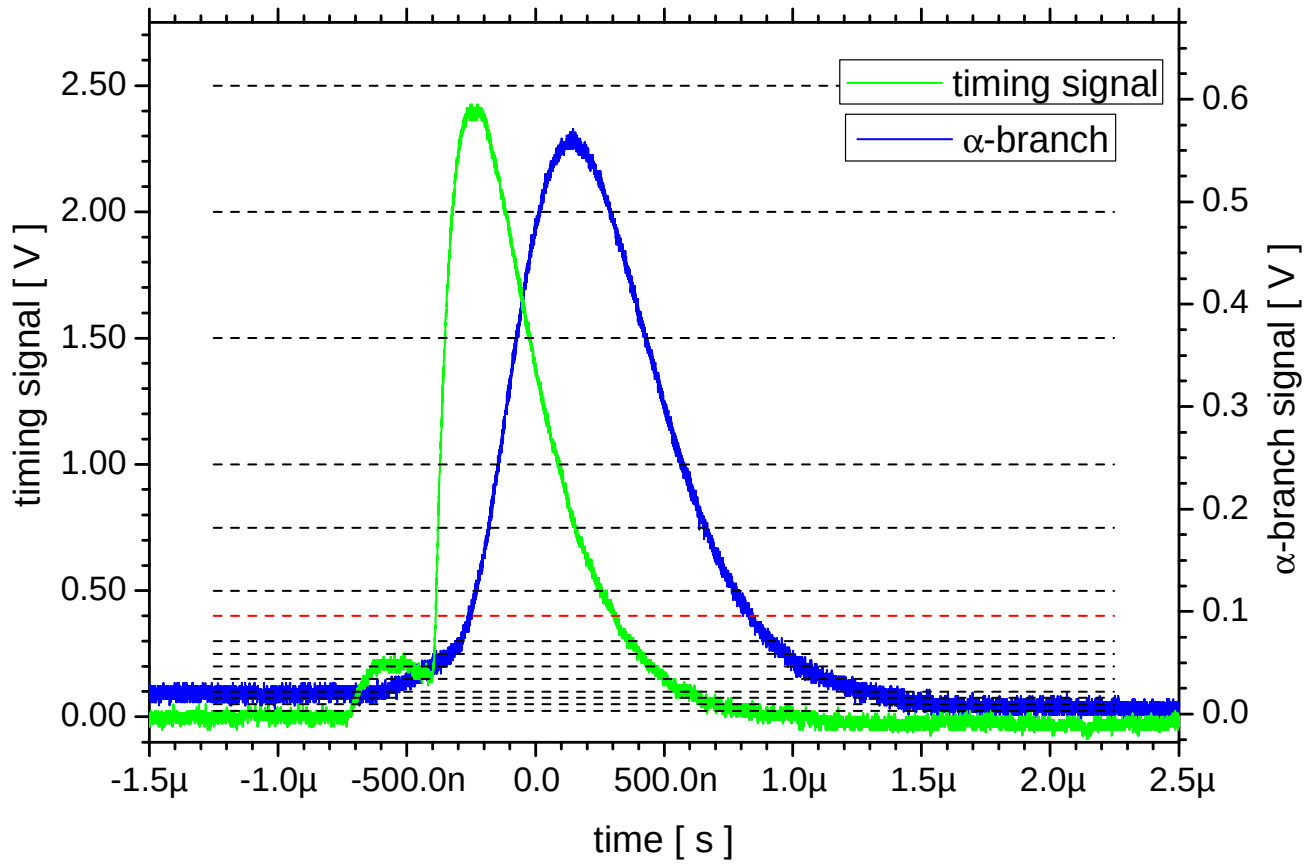
pure COLD: working principle

pile **u**p **r**ejection **e**lectronics for
Cryo **O**n-**L**ine **D**etectors
(heavy elements chemistry)



β → α pile up signals can reliably be measured in the „timing channel“ only

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pureCOLD: Comparator / ADC / FPGA stages

16 × fast comparators per timing channel

- 150 ps delay, 10ps jitter
- run-time matching via cable delay better 0.7 ps
- levels adjustable via DAC

8 phase sampling clock

- derived from a 250 MHz low jitter clock generator
- run-time matching via “cable” delay better 0.3 ps
- time resolution 0.5 ns

2 × 500 kSamples/s ADC per spectr. channel

- 16 bit conversion depth
- 2.5 V bipolar range
- 120 ns conversion time
- 1.8 µs serial read-out time

Spartan 3 FPGA

- 340 event FIFO
- 110 µs serial transfer to MB
- max. rate 9 kevents per sec
- time between consecutive events 4 µs
- 7x free programmable interconnection signals

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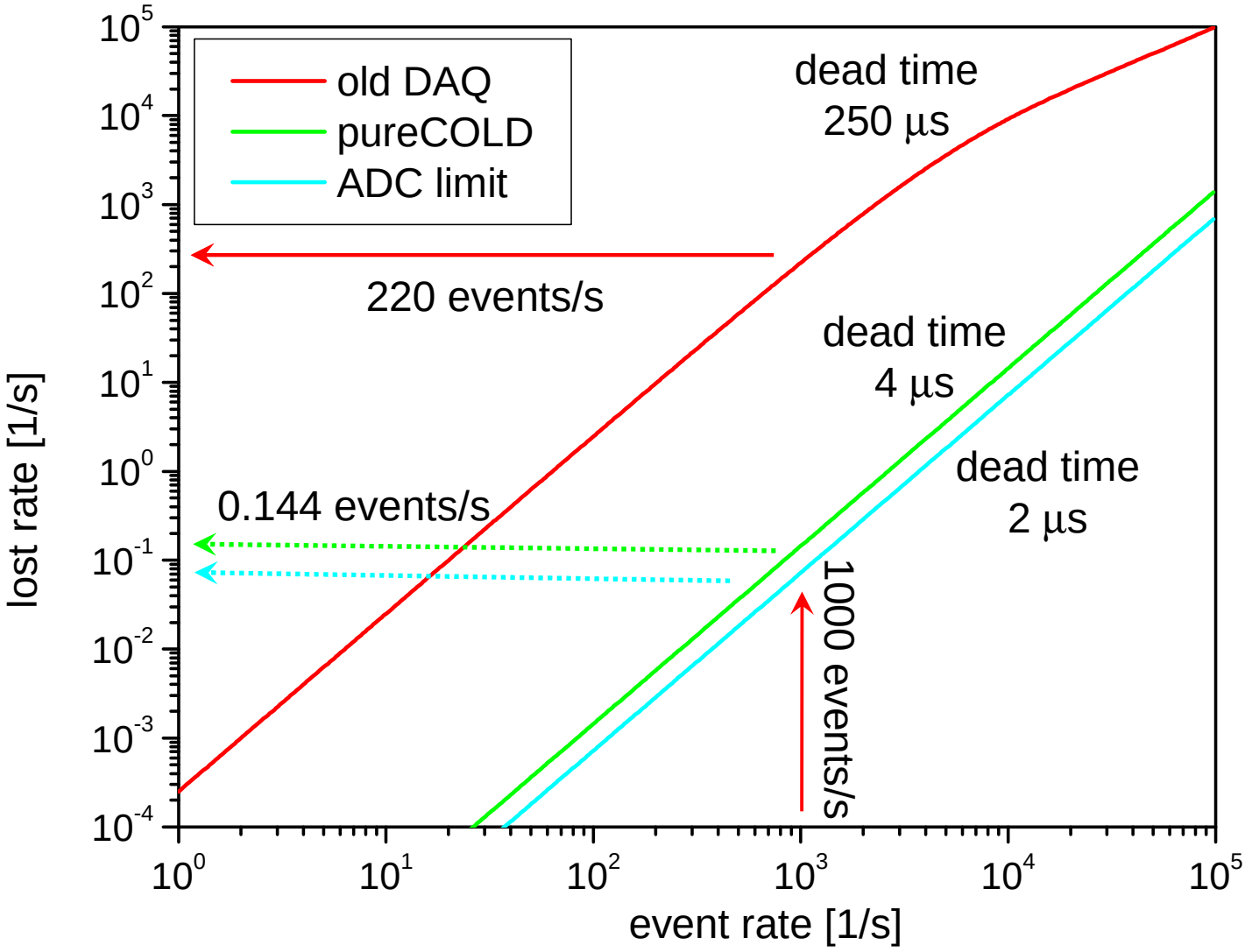
pureCOLD: missing event rate



major achievements:

- S/N optimized
- dead time / event minimized
- over all remote control implemented

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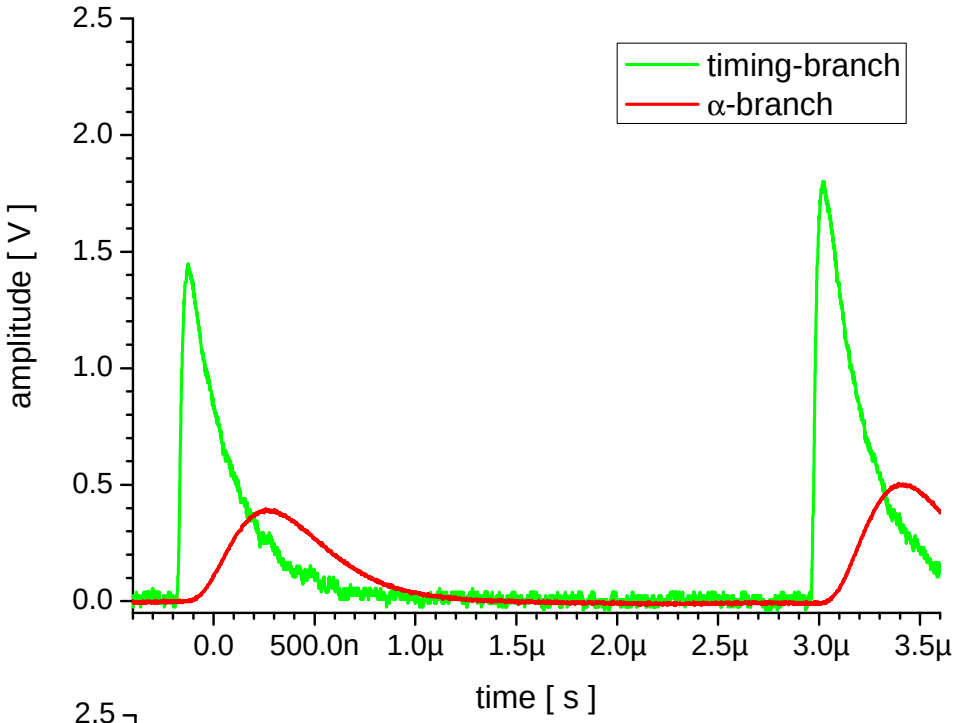
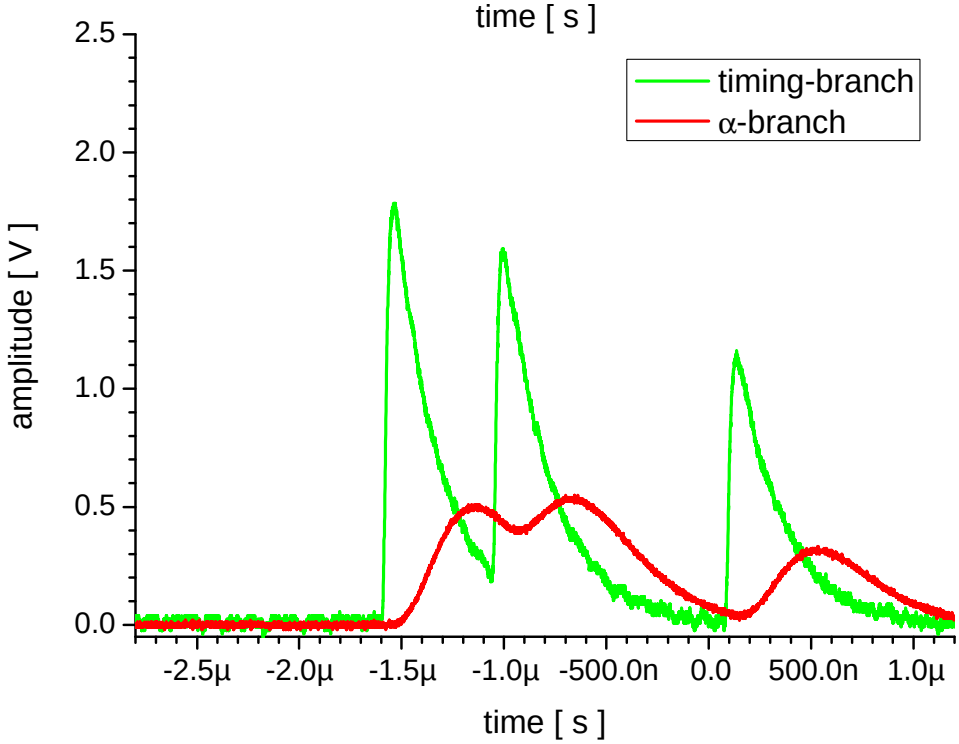
pureCOLD: typ. signals





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^{232}U - test-spectrum