PAUL SCHERRER INSTITUT

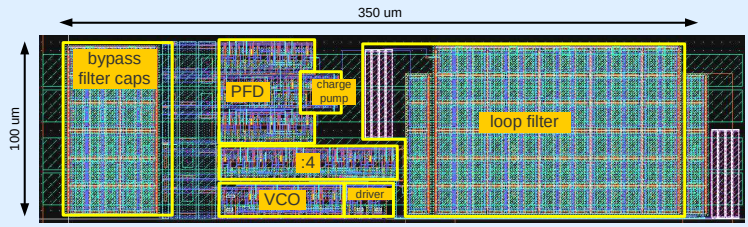
CMS Pixel Detector Electronics Upgrade

Goal for 2014-Upgrade : New readout frontend chip for higher luminosity with increased size of data buffers and digital data uplink

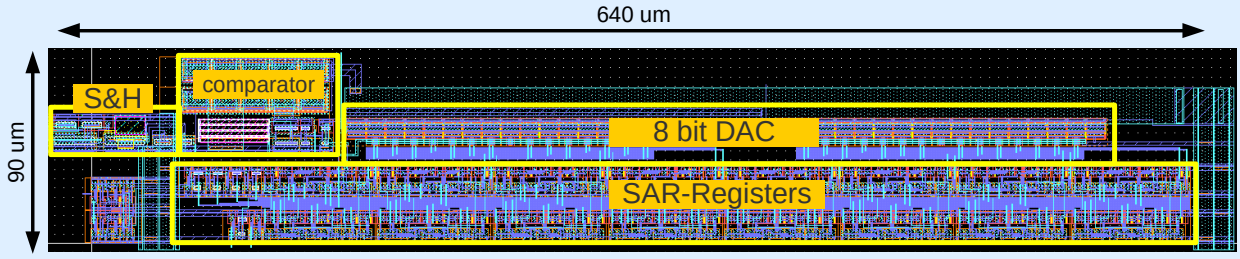
→ **higher data rate with the existing mass and power budgets !!!**

ASIC test structures for key components
(design finished, almost all tested):

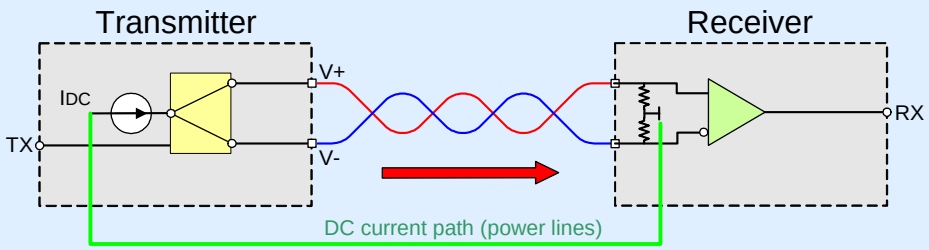
- **Fully integrated frequency multiplier PLL for clock generation**



- **8 bit successive approximation ADC**



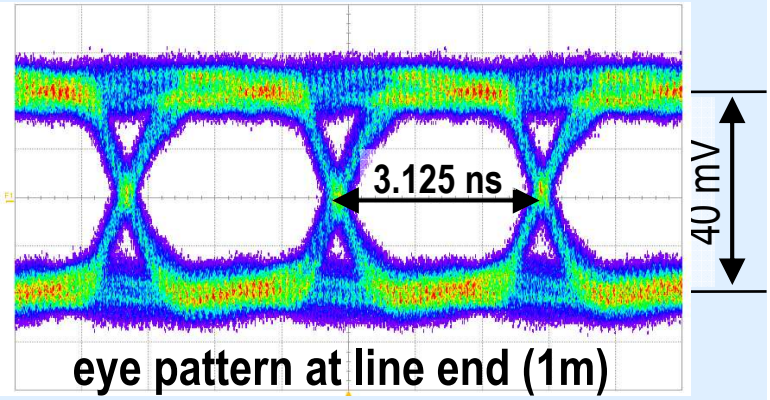
- **320 MBit / s driver and receiver**



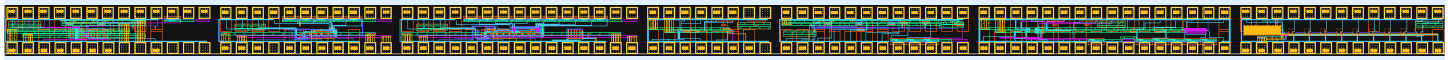
PAUL SCHERRER INSTITUT

New Data Link for CMS Pixel Detector

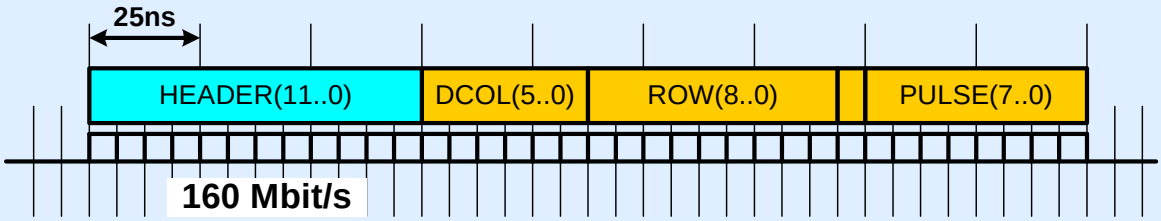
- 1216 links, each 320 MBit/s differential signal over 1 m cable
- **Low power:** 4 mW / Link (driver and receiver)
- **Low mass:** unshielded micro twisted pair cable (125 µm wire diameter)



- Custom ASIC design at PSI for driver and receiver



existing "analog" link: 2.5 bit / LHC clock



new digital data link: 8 bit / LHC clock
Link speed 320 Mbit/s (two frames multiplexed)