Requirements for new LEM/μSR facility hardware

T. Prokscha, 14-Jan-2003

- **time window:** **up to 20 μs**
- **time resolution:** **0.05 – 0.1 ns (high-field μSR), 0.25 – 1.0 ns others**
- **modules:** **TDC, ADC, Scaler applications; scaler information on single Detector rates as well as coincidences needed (presently, CAMAC scalers used)**
- **trigger logic:** **should be completely programmable**
  Present: - LEM: NIM electronics + coincidence steering by use of CAMAC IO units
  - μSR: most of instruments are using ORTEC pTA, completely programmable; limited flexibility
- **read out:** **LEM runs in event-by-event mode, total read out time must be less than 20 μs to handle 2000 trigger/sec with a few % dead time; other μSR instruments could use event-by-event mode for test purposes.**
- **detector rates:** **LEM + ALC beam counters have to measure > 10^7/s**
  → signal sampling (flash-ADC) would be very useful for pile up/rate determination
- **detector:** **pulse height information desirable**
- **future options:** **DAQ hardware should be extandable → position information with Si pixel/strip detectors**

“Desire”:

– a general purpose board (VME ?)
– send analog detector signals directly into board
– sample signals with 1 – 2 GHz flash ADC (NA48 at CERN uses 1 GHz, 8-bit flash ADC)
– send sampled signals to FPGA
– do everything what you want in the FPGA (TDC, ADC, logic…)

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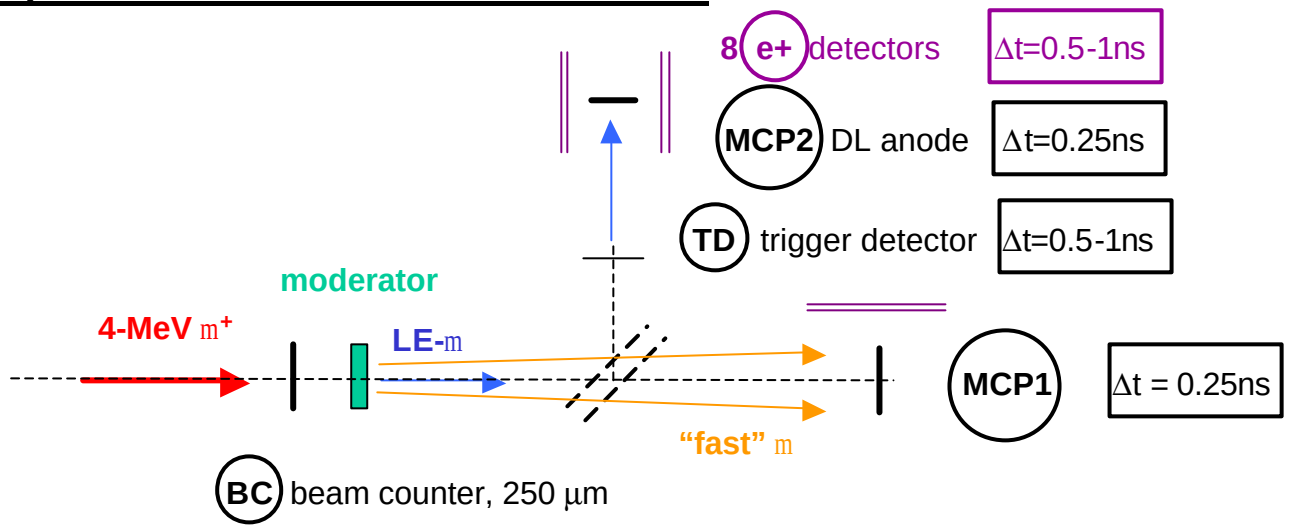
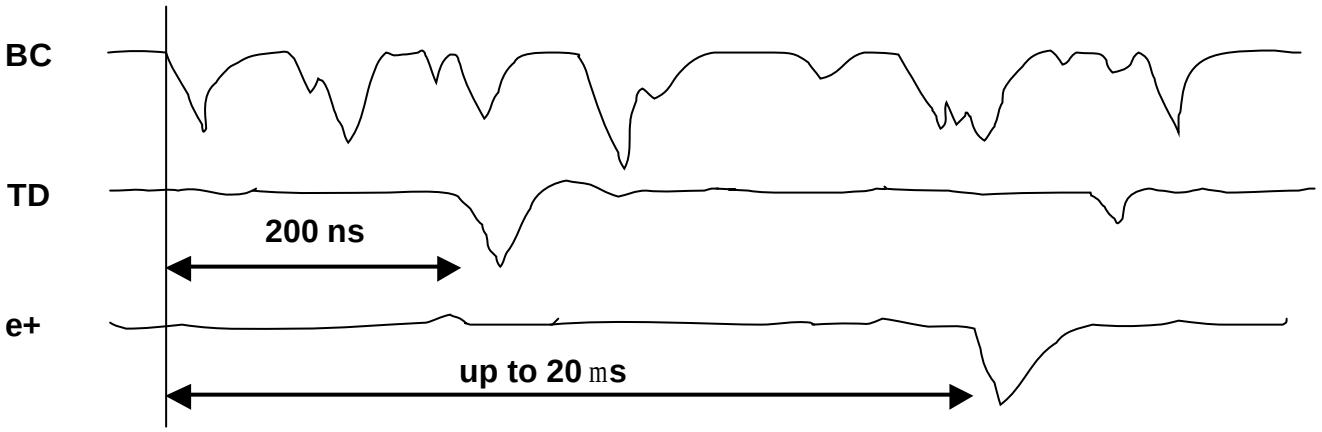


detector	present rates	future rates
BC	3×10^7/s	$8 \times 3 \times 10^7$/s 8 fold segmented
TD	1×10^4/s	7×10^4/s
MCP1	1×10^5/s	1×10^6/s
Sum of e+	4×10^2/s	3×10^3/s

Timing:



TDC measurements:

TDC Start: TD
TDC Stop: delayed BC for time-of-flight BC-TD
TDC Stop: decay e+ for µSR histograms

TDC Start: MCP2
TDC Stop: X1, X2, Y1, Y2 of MCP2 delay line anode

ADC:

TD pulse height distribution; future option: add BC, e+ scintillators