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Application of the DRS Chip for Fast Waveform Digitizing

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Abstract

The high demands of modern experiments in fast waveform digitizing led to the development of a whole family of switched capacitor arrays (SCA), called the Domino Ring Sampler (DRS). The most recent version, DRS4, is produced in a radiation hard 0.25 µm CMOS process, and is capable of digitizing 9 differential input channels at sampling rates of up to 6 Giga-samples per second (GSPS) with an analogue bandwidth of 950 MHz (-3 dB). The channel depth can be configured between 1024 and 8192 cells, and the signal-to-noise ratio allows a resolution equivalent to more than 11 bits. Using an interleaved sampling technique, sampling rates up to 48 GSPS are possible. Compared with the previous versions, the DRS4 chip contains several improvements such as an on-chip PLL for sampling-frequency stabilization and various mechanisms to readuce the read out dead-time. The high bandwidth, low power consumption and short readout time make this chip attractive for many experiments, replacing traditional ADCs and TDCs. This includes time-of-flight detectors, cosmic gamma ray observatories, PET scanners and industrial applications.

Keywords: Switched Capacitor Array; Waveform Sampling; DRS Chip

1. Introduction

In many fields there is a growing demand for high speed waveform digitizing in the GHz range. Nowadays, particle physics experiments, such as MEG [1], face the problem of pile-up at high rates, and in cosmic gamma-ray astronomy there is the need for pulse shape discrimination at high channel densities and low power consumption at affordable costs. An alternative to flash-ADCs is the usage of switched capacitor arrays (SCA). These chips store an analogue waveform from a photomultiplier or photodiode at multi-GHz sampling rates in a series of capacitors. The contents of these capacitors is then either digitized on-chip, typcially with a Wilkinson type ADC, or digitized off-chip with a commercial ADC. Serveral groups are currently active in this area [2][3]. While most of the developed chips are targeted for a specific experiment, the DRS chip developed at the Paul Scherrer Institute, Switzerland, has been designed for maximum flexibility and use in many different applications. A second goal was to minimize the drawbacks of the SCA technology, namely that of inherent dead-time during readout, the

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limited sampling depth and the non-linear timing behavior.

2. Theory of operation

Four versions of the DRS chip have been designed so far, each one improving the functionality and performance of the predecessor. The current version (DRS4) implements 8+1 channels each having 1024 sampling capacitors on a single chip (see Figure 1), fabricated using radiation hard layout techniques in the 0.25 μm 1P5M MMC process offered by UMC.

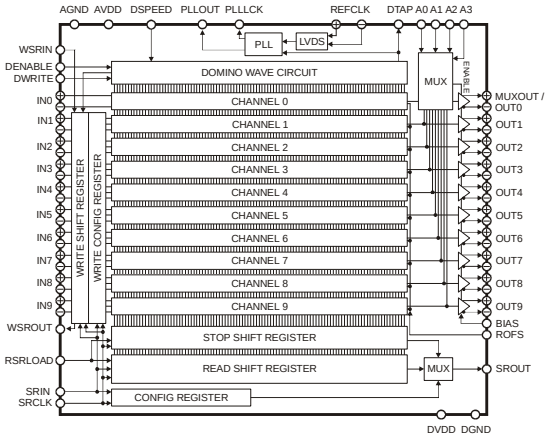

Figure 1. Functional Block Diagram of the DRS4 chip

A so-called “Domino Wave” circuit generates a short pulse which opens analogue switches at the input of sampling cells of each channel. The usage of input buffers for the analogue signals has been avoided, since they would either limit the bandwidth or the linear range. To minimize the bandwidth limiting effect of the bond wires in this passive input approach, a QFN-76 lead-less package has been chosen to house the chip, resulting in an analogue bandwidth of 950 MHz (-3dB).

The Domino Wave is generated by a series of inverters, whose speed is controlled by an analogue voltage. An on-chip PLL locks the generation of the Domino Wave to an external reference clock at a dividing ratio of 2048:1, and thus ensures a high stability over variations in temperature and power supply voltage. At 5 GSPS, the residual jitter is about 25 ps. Using this PLL, the sampling frequency can be configured in the range from 100 MSPS to 6 GSPS. For applications which require a timing precision better than 25 ps, the ninth channel can be used to digitize directly a precision sine wave or LVDS global reference clock. Using this technique, a timing precision of 4 ps has already been demonstrated in the laboratory. The total power consumption of the DRS4 chip is between 10 and 40 mW per channel, depending on the sampling speed and readout mode.

The Domino Wave can be stopped by an external trigger, after which the sampling capacitors are read out and digitized by a commercial ADC. The differential analogue output of the DRS4 chip matches the input of modern ADCs, so that the chip can be operated with a minimum of external components (Figure 2).

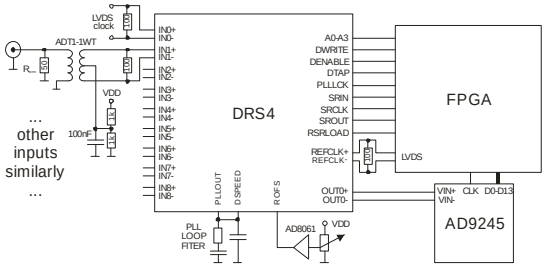

Figure 2. Typical Mode of Operation of the DRS 4chip

If dead-time is an issue, all eight data channels can be read out in parallel and digitized simultaneously, using modern octal ADCs such as the AD9222 from Analog Devices. Using a special Region-of-Interest readout mode, only the part of the stored waveform of interest can be read out and digitized. The digitization time is then $n \cdot 30$ ns, where n is the number of samples of interest. For short PMT pulses of 10 ns width sampled with 5 GSPS, the readout of all fifty samples takes then $50 \cdot 30\text{ns} = 1.5$ μs, allowing for acquisition rates of several 100 kHz.

A flexible cascading scheme has been implemented, with which one can configure the DRS4 chip to have deeper sampling depths at the cost of fewer channels. In the extreme case, the chip can be configured as a single channel with 8192 sampling cells. Furthermore, several DRS4 chips can be daisy-chained to form a channel with virtually unlimited sampling depth without compromising the

bandwidth, given that the analogue signal is externally split and fed to all channels of each chip in parallel. Another option is to have concurrent writing and reading. The chip can be configured as a single channel with eight analogue buffer segments of 1024 cells each. If a trigger occurs, the next segment is activated for writing while the previous segment is read out and digitized. For Poisson-distributed events, this technique can reduce the dead-time of the DAQ system significantly.

3. Application in the MEG Experiment

The MEG experiment at PSI, Switzerland, uses 3000 channels equipped with DRS chips to digitize all detector signals, including PMTs from the calorimeter and timing counters, as well as drift chamber anode and cathode signals. All pre-amplifiers used are voltage sensitive, so that the original waveforms from the detectors are preserved. This allows techniques such as shaping, filtering and integration to be applied offline, either by software in the analysis process or by firmware in the front-end FPGAs. The parameters of this waveform processing can be changed after the data has been recorded in order to optimize for example the signal-to-noise ratio by sophisticated baseline restoration (Figure 3). To determine the timing of a PMT pulse, methods such as cross-correlation with a template waveform are used. Precisions in the region of 10 ps have been achieved with this technique. It has also been shown that pile-up of events can be rejected if they are separated in time by at least the rise-time of the signals, which in the case of the liquid Xenon calorimeter of the MEG experiment is about 10 ns.

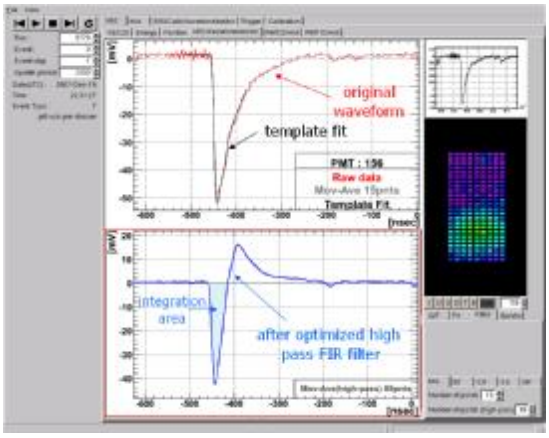

Figure 3: Online display of the MEG calorimeter PMT waveform. The original waveform (top) is processed with a software filter for optimal baseline restoration and integration

4. Availability for other experiments

Since the DRS chip might be suitable for other experiments, it has been decided to distribute the chip through the technology transfer programme of PSI on a non-profit basis. Groups considering building their own electronics around the DRS chip can benefit from the DRS4 evaluation board (Figure 4), which is available as well. Details can be found on the DRS home page [4].

Figure 4: DRS4 evaluation board with four input channels and USB 2.0 readout

The high channel density, fast readout speed and excellent electric characteristics of the DRS4 chip

make this device attractive for many other experiments. While several companies have announced production of VME and cPCI boards with the DRS4 chip, it is currently deployed at several cosmic gamma-ray observatories such as MAGIC [5] and VERITAS [6].

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