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Application of the 5 GS/s Waveform Digitizing Chip DRS4

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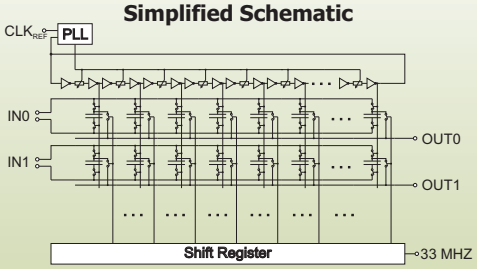
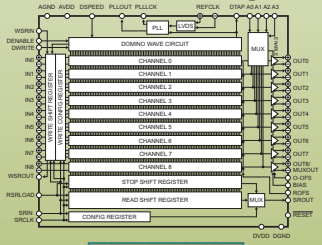
The DRS4 Chip

Simplified Schematic

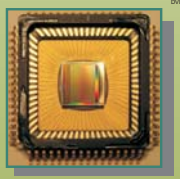


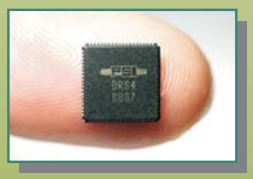
Functional Block Diagram



Basic Parameters

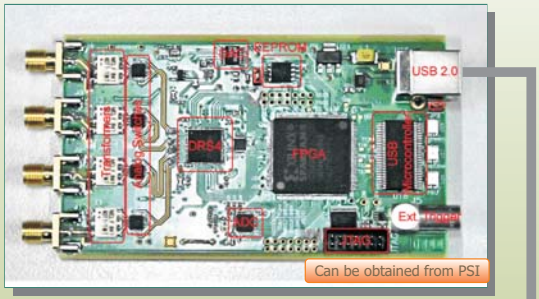
Technology:	UMC 0.25µm
Numer of Chn.:	9 with 1024 cells cascadable up to 8192
Power:	17.5 mW/chn. @ 2.5V
Sampl. Speed:	200 MSPS to 5 GSPS
Bandwidth:	950 MHZ (-3dB)
Readout time:	30 ns * $n_{samples}$
Nonlinearity:	$0.5*10^{-3}$ at 1V range
SNR:	69 dB after calibration
Aperture jitter:	4 ps at 5 GSPS after calibration



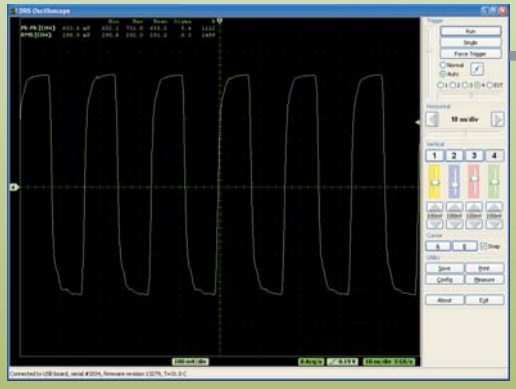


Evaluation Board

Four Channel Oscilloscope with USB power and readout



Can be obtained from PSI

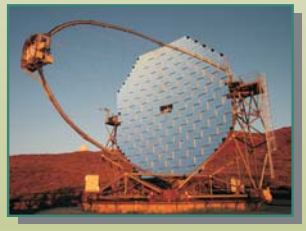


PC Oscilloscope Application (Windows and Linux)

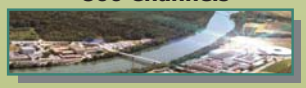
Experiments using DRS Chips

MEG (PSI)
3000 Channels

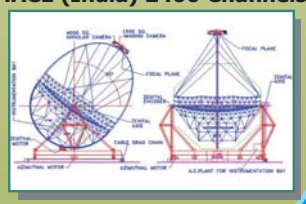
MAGIC-II (La Palma)
400 Channels



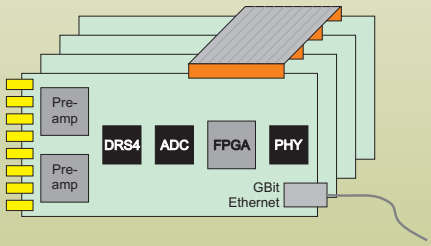
XFEL BPM (PSI)
800 Channels



MACE (India) 2400 Channels



Ethernet Board (planned)



- 8 Channel board to be mounted directly on detector electronics 50 mm x 100 mm
- Preamplifier for PMTs, APDs, SiPMTs
- Read out through Gigabit Ethernet
- Local LVDS bus for cascading and synchronization
- Event rate: 100 kHz (50 Samples/chn.)
- Goal: < 40 €/channel

http://drs.web.psi.ch