Design and Performance of the 6 GHz Waveform Digitizing Chip DRS4

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***Abstract*– The high demands of modern experiments in fast waveform digitizing led to the development of the DRS4 chip, which is a radiation hard switched capacitor array (SCA) fabricated in a 0.25 µm CMOS process. It is capable to digitize 8+1 input channels at sampling rates up to 6 Giga-samples per second (GSPS) with an individual channel depth of 1024 bins and a effective range of 11.5 bits. A novel cascading scheme allows the combination of several channels or even chips to deliver very deep sampling depths or interleaved sampling with up to 48 GSPS. An on-chip PLL ensures high timing accuracy over a wide temperature range. The high analog bandwidth of 850 MHz, low power consumption of 40 mW/channel and fast readout time make this chip attractive for many experiments, replacing traditional ADCs and TDCs.**

I. Introduction

In many fields there is a demand of high speed waveform digitizing in the GHz range. Particle physics faces the problem of pile-up at high rate experiments such as the MEG experiment [1], and in cosmic gamma ray astronomy there is the need for pulse shape discrimination at high channel densities and low power consumption at affordable costs. An alternative to flash-ADCs is the usage of switched capacitor arrays (SCA). These chips store an analog waveform from a photomultiplier or photodiode at multi-GHz sampling rates in a series of capacitors. These capacitors are then either read out and digitized externally or digitized directly on the chip. The DRS4 chip is the fourth version in a series of developments at the Paul Scherrer Institute, Switzerland. Originally targeted for the MEG experiment, this chip finds now applications in several other fields.

II. Architecture

A. Theory of Operation

The DRS4 chips implements 9 channels each having 1024 sampling capacitors on a single chip (see Figure 1), fabricated in the 0.25 µm 1P5M MMC process by UMC (Figure 2).

A so-called Domino Wave Circuit generates a write pulse which opens analog switches at the sampling cells of each channel. The inputs are differentially to reduce the inter-channel crosstalk. The usage if input buffers has been avoided, since they would either limit the bandwidth or the linear range with current chip technologies. To minimize the bandwidth limiting effect of the bond wires, a QFN-64 lead-less package has been chosen as a chip housing. Alternatively, the DRS4 chip can be mounted in a flip-chip assembly, avoiding bond wires completely.

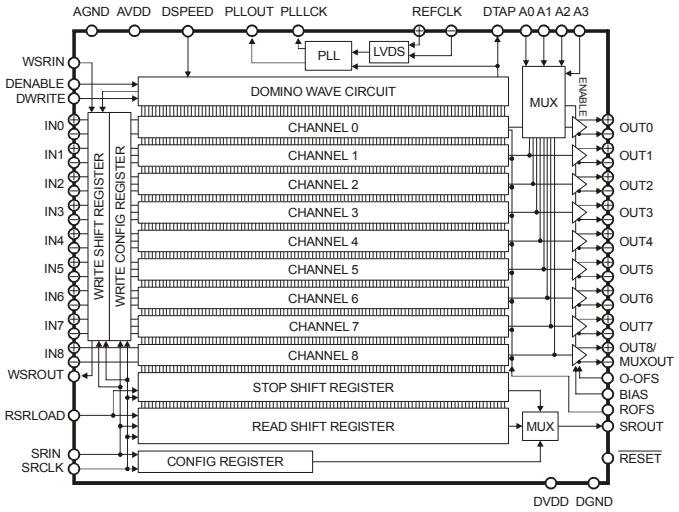

Figure 1 Functional Block Diagram of the DRS4 chip

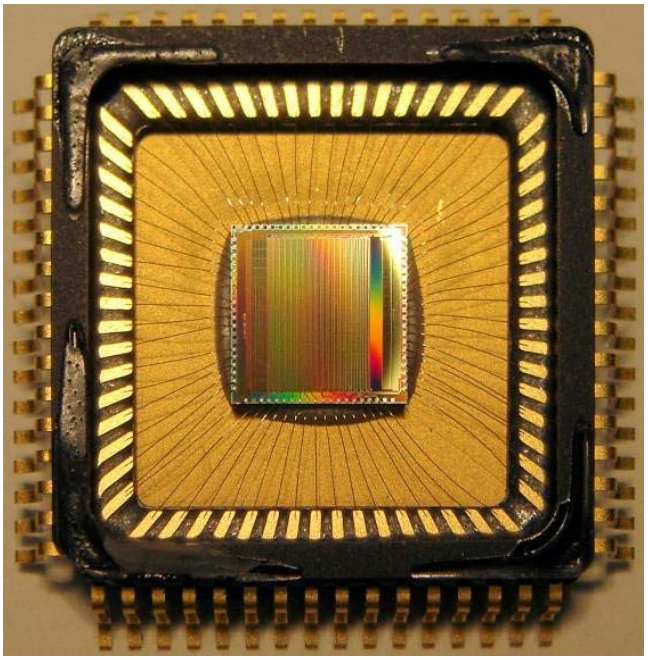

Figure 2 Image of the 4.2 mm × 4.2 mm DRS4 chip inside a prototype package.

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For applications which require a timing accuracy below 100 ps, the ninth channel can be used to digitize directly a precision global reference clock for calibration.

The Domino Wave is generated by a series of inverters, whose speed is controlled by an analog voltage. An on-chip PLL locks the generation of the Domino Wave to an external reference clock at a dividing ratio of 2048:1, and thus insures a high stability over variations in temperature and power supply voltage. Using this PLL, the sampling frequency can be configured in the range from 500 MSPS to 6 GSPS with a residual PLL jitter below 100 ps.

An external trigger stops the sampling, after which the capacitors are read out and digitized with an external ADC at a speed of 33 MHz and a resolution of 12 bits. For cost sensitive applications all nine channels can be digitized with a single external ADC through an internal multiplexer, while for experiments requiring small dead time all nine channels can be digitized in parallel.

B. Improvements of the DRS4 chip

The DRS4 chip is the fourth version of a series of chips developed for high speed waveform digitization. Many lessons have been learned and led to major improvements in this version of the chip. A careful layout of the passive input bus together with a smaller packaging increases the bandwidth by about a factor of two compared to the previous chip DRS3 which had 450 MHz. A special clear-before-write cycle ensures that all sampling cells are free of residual charge from the previous revolution of the Domino Wave, a common problem to most SCA chips currently on the market [2].

The differential analog output of the DRS4 chip matches the input of modern ADCs, so that the chip can be operated with a minimum number of external components required (Figure 3).

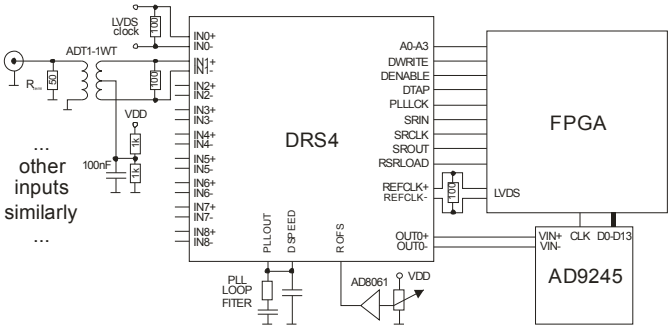

Figure 3 Typical Mode of Operation of the DRS 4chip

A flexible cascading scheme has been implemented, with which one can configure the DRS4 chip to have deeper sampling depths at the price of fewer channels. It can be configured as 8 channels with 1024 cells, 4 channels with 2048 cells, 2 channels with 4096 cells or one channel with 8192 cells. Furthermore, several DRS4 chips can be daisy-chained to form a channel with virtually unlimited sampling depth without compromising the bandwidth.

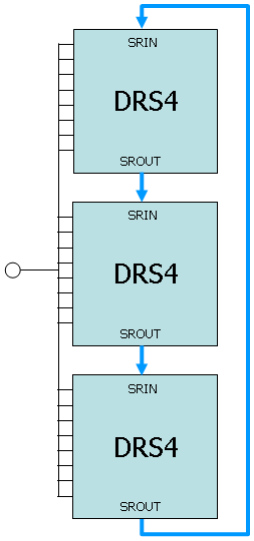

Figure 4 Cascading several DRS4 chips to for a very deep sampling channel by connecting their shift register outputs (SROUT) to the shift register inputs (SRIN) of the next chip.

Another option is to have concurrent writing and reading. The chip can be configured as a single channel with eight analog buffer segments of 1024 cells each. If a trigger occurs, the next segment is activated for writing while the previous segment is read out and digitized. For Poisson-distributed events, this technique can reduce the dead time of the DAQ system significantly with the penalty of some cross-talk between the write and read operations of a few mV.

Since new compact octal ADCs operating at 65 MSPS are now available from industry, a special "transparent mode" has been implemented. During acquisition, the input signals are sampled at high speed inside the DRS4. At the same time, these signals are visible at the analog outputs, where they can be digitized continuously by the external ADC. The attached FPGA can then make a trigger decision based on some threshold or channel multiplicity. Upon a trigger, the FPGA stops the DRS4 waveform digitizing and then reads out the stored waveform through the same octal ADC. This allows both triggering and waveform digitizing with the same electronics, eliminating the need of traditional splitter-trigger-DAQ branches.

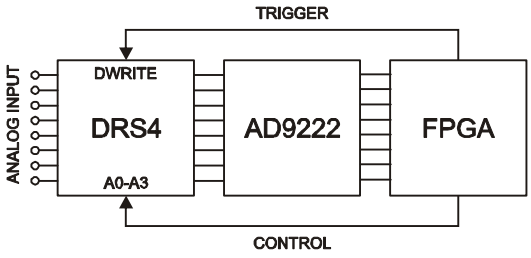

Figure 5 Simultaneous triggering and waveform digitizing in the "transparent mode" of the DRS4 chip

III. Test Results

First test results have been obtained with a DRS4 test board (Figure 6). A PC oscilloscope application has been written using the wxWidgets library [3], which runs under Windows and Linux (Figure 7) and connects to this board. Due to the low power consumption of the DRS4 chip, the board can be powered completely from USB. Using the USB 2.0 standard, a sustained data rate of 20 MB/sec. can be achieved, which is enough to read a single channel at a rate of 10 kHz.

Figure 6 USB powered DRS4 evaluation board with four 2048 cells deep input channels

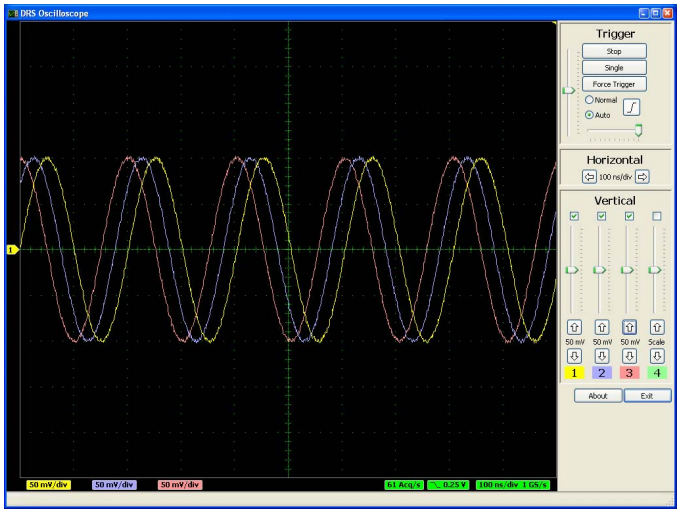

Figure 7 PC based oscilloscope application for the readout of the evaluation board

A. Analog Bandwidth

First samples of the DRS4 chip have been shipped on August 2008 and most characterization tests have been accomplished in meantime. Since the prototype samples are packaged in a ceramic QFP-64 package for accessibility (Figure 2), the final analog bandwidth which depends on the length of the bond wires cannot be determined precisely, since the final QFN-76 packages will have shorter bond wires. The QFP-64 package gave an analog bandwidth of 850 MHz (-3 dB) and it is expected that the QFN-76 package will give a slightly higher value. It should be noted however that the DRS4 input is completely passive, so the external signal source must be able to load the internal sampling capacitors, which can lead to a current of up to 800 µA.

B. PLL performance

The newly implemented internal PLL has been proven to work very nicely. It uses the DTAP output of the domino circuit, which toggles on each revolution of the domino wave and has therefore a frequency which is the sampling frequency divided by 2048. The PLL implements a phase detector between the DTAP signal and an externally produced LVDS reference clock. Figure 8 shows the locking behavior. The domino wave starts at 6 GSPS and is then throttled to lock at a sampling frequency of 1 GSPS in this case.

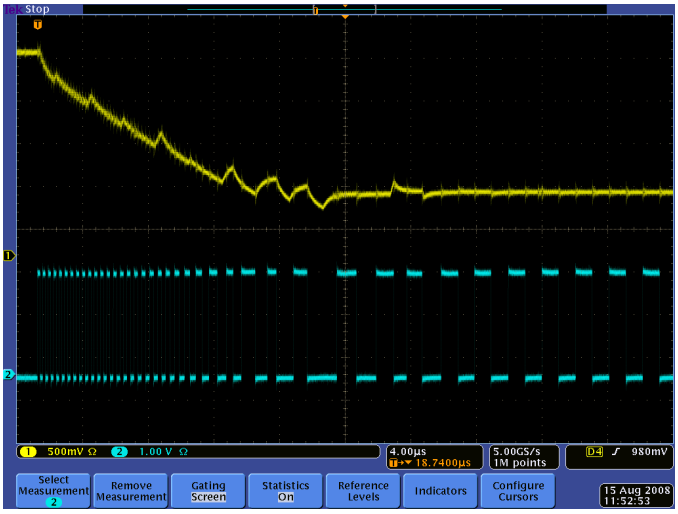

Figure 8 Locking of the internal PLL. The upper trace is the analog PLL output and the lower trace is the DTAP output indicating a start-up at 6 GSPS and locking at 1 GSPS

The loop filter of the PLL is implemented off-chip, so it can be optimized for various sampling frequencies. As can be seen from Figure 8, the PLL locks after approximately 30 µs on the external reference clock and is insensitive to higher harmonics. It is dead-band free in order to minimize the residual PLL jitter. In a first quick test, the jitter has been measured to be roughly 100 ps, which was limited by the reference clock jitter of 150 ps coming from the fact that the reference clock was produced in the FPGA by a PLL itself (Xilinx DCM). A measurement with a low jitter reference clock is planned.

C. Timing Jitter

A well-known issue in SCAs is the fact that the delay produced by the inverter chain shows a cell-by-cell variation, mainly caused by the mismatch of the inverter transistors. This variation causes a jitter of the sample time, commonly referred to as *aperture jitter*. This aperture jitter is composed of a part which is constant over time (fixed pattern jitter) and a part which varies from one event to the next (random pattern jitter). To measure this jitter, a precise 500 MHz sine wave with random phase was sampled 500 times. Then a global fit was performed, with the amplitude, phase and frequency of

each waveform left as a free parameter as well as an "effective cell width" for each sampling cell. The effective width is the nominal value (e.g. 200 ps for 5 GSPS) plus the fixed pattern jitter. It was kept as a free fit parameter for each cell, but constant over all 500 waveforms. The resulting effective cell width is therefore a good measure of the fixed pattern jitter, while event-by-event deviations of this value give the random pattern jitter. The value for the fixed pattern jitter has been determined using this method for the DRS3 chip running at 5 GSPS in a previous work [4] to be 50 ps (RMS) and the random pattern jitter to be 3 ps (RMS). The random jitter in this case is the average deviation in time of a sampling point from the fitted sine wave. It is expected to be slightly better in the DRS4 chip since some internal signals have steeper edges. If waveform sampling is applied to individual pulses from photomultipliers or photodiodes, the achievable timing resolution depends on the rise time of the signal. For fast detectors, rise times below 1 ns are possible. Having ~5 samples on the rising edge of such a pulse, the random jitter of these cells can be averaged, which should yield in a timing resolution below the above quoted value of 3 ps. Further tests to verify this are currently going on.

Another possibility is the interleaved sampling of a single signal with all eight channels of a DRS4 chip. If the same signal is fed to channel i with a delay of t_i = 1/6GHz * i/8, an effective sampling speed of 6 GHz*8=48GHz can be achieved, improving the timing resolution even further (Figure 9). Studies are currently underway with the goal to achieve a timing resolution for individual pulses in the order of one picosecond.

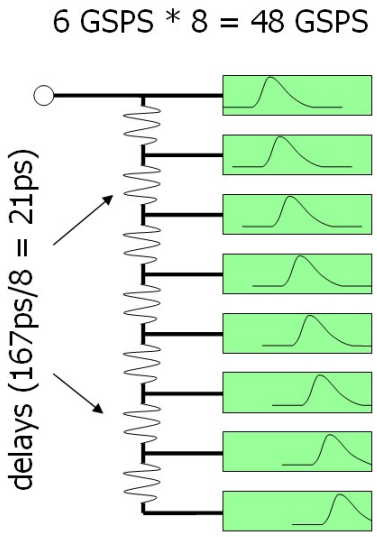

Figure 9 Interleaved sampling using a fixed delay between channels

IV. Summary

The high channel density, fast readout speed and excellent electrical characteristics of the DRS4 chip make this device attractive for many applications. While several companies have announced to produce VME or cPCI boards with the DRS4 chip, it is currently deployed at several cosmic gamma ray observatories such as MAGIC [5] and VERITAS [6]. The chip is available for other experiments together with the USB evaluation board from our institute [7].

Acknowledgment

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