THE WaveDAQ SYSTEM FOR THE MEG II UPGRADE

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DRS4 Chip

- Switched Capacitor Array (Analog Memory) developed at PSI
- 5 GSPS / 11.5 bits SNR, 9 channels on 5 mm x 5 mm chip, 40 mW / chn.
- Used at ~200 locations worldwide
- 2012: “Gigahertz Waveform Sampling: An Overview and Outlook”

- Pile-up rejection \(O(~10 \text{ ns})\)
- Time measurement \(O(10 \text{ ps})\)
- Charge measurement \(O(0.1\%)\)
MEG & MEG II

MEG Experiment 1999-2013
- Separated DAQ & Trigger
- 3000 Channels DRS4
  (0.8 GSPS / 1.6 GSPS)
- 1000 Channels Trigger
  (100 MSPS)
- 5 Racks

MEG II Experiment 2014-
- 9000 Channels
- Same rack space
  ➔ Combine
  DAQ & Trigger

S2: M. de Gerone: An extreme high resolution Timing Counter for the MEG II Experiment
S2P: M. Simonetta: Test and characterization of SiPMs intended as detector for the MEG timing counter
S5P: D. Nicolò: An FPGA-based trigger for the MEG II Experiment
S5P: A. Pepino: A high performance Front End Electronics for Drift Chamber readout in the MEG II Experiment
S7P: M. Grassi: A new cylindrical drift chamber for the MEG II Experiment
S7P: G. Rutar: A Dedicated Calibration Tool for the MEG and MEG II Positron Spectrometer
S7P: L. Galli: MEG II drift chamber prototype characterization with the silicon based cosmic ray tracker at INFN Pisa
S7P: M. Venturini: Ageing tests for the MEG II drift chamber
S9P: D. Nicolò: A liquid hydrogen target for the calibration of the MEG and MEG II liquid xenon calorimeter
S9P: K. Ieki: Upgrade of the MEG liquid xenon calorimeter with VUV-light sensitive large area SiPMs

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### Crate Options

<table>
<thead>
<tr>
<th>Feature</th>
<th>VME</th>
<th>ATCA</th>
<th>???</th>
</tr>
</thead>
<tbody>
<tr>
<td>Transfer speed (O(100 \text{ MB/s}))</td>
<td>✔</td>
<td>✔</td>
<td>✔</td>
</tr>
<tr>
<td>Dual-Star Topology with Gbit links</td>
<td>✗</td>
<td>✔</td>
<td>✔</td>
</tr>
<tr>
<td>Shelf management</td>
<td>✗</td>
<td>✔</td>
<td>✔</td>
</tr>
<tr>
<td>Fast trigger distribution</td>
<td>✗</td>
<td>✗</td>
<td>✔</td>
</tr>
<tr>
<td>Low-jitter precision clock (O(\text{ps}))</td>
<td>✗</td>
<td>✗</td>
<td>✔</td>
</tr>
<tr>
<td>200 V SiPM biasing</td>
<td>✗</td>
<td>✗</td>
<td>✔</td>
</tr>
<tr>
<td>&lt; 2000 EUR per crate including power</td>
<td>✗</td>
<td>✗</td>
<td>✔</td>
</tr>
</tbody>
</table>

WaveDAQ System

- Fans blow from back to front
- Crate Management Board:
  - Power supply 24V / 300W
  - Fan / Temp. control
  - Power cycle each slot
  - FPGA Firmware upload
  - Ethernet remote control
- Data Concentrator Board
- Trigger Concentrator Board
- 16 WaveDREAM boards (256 channels)
WaveDREAM Board (WDB)

Drs4 based REAdout Module
Preamp

Gain | $BW_{3\text{db}}$ (MHz) | Noise (mV)
--- | --- | ---
1 | 940 | 0.37
10 | 880 | 0.40
100 | 300 | 1.2
100 | 500 | 1.7
100 | 800 | 3.3

Different compensations

3.3 mV at output = 33 $\mu$V at input
WaveDREAM2 HV

~ 5 EUR / channel

+1...+85 V

+/- 1mV
Ripple < 10 µV
Temperature Sensor Extension

DESCRIPTION
The DS18B20 digital thermometer provides 9-bit to 12-bit Celsius temperature measurements and has an alarm function with nonvolatile user-programmable upper and lower trigger points. The DS18B20 communicates over a 1-Wire bus that by definition requires only one data line (and ground) for communication with a central microprocessor. It has an operating temperature range of -55°C to +125°C and is accurate to ±0.5°C over the range of -10°C to +85°C. In addition, the DS18B20 can derive power directly from the data line (“parasite power”), eliminating the need for an external power supply.

Each DS18B20 has a unique 64-bit serial code, which allows multiple DS18B20s to function on the same 1-Wire bus. Thus, it is simple to use one microprocessor to control many DS18B20s distributed over a large area. Applications that can benefit from this feature include HVAC environmental controls, temperature monitoring systems inside buildings, equipment, machinery, and process monitoring and control systems.

FEATURES
- Unique 1-Wire® Interface Requires Only One Port Pin for Communication
- Each Device Has a Unique 64-Bit Serial Code
- accuracy ±0.5°C, 3 EUR / sensor
- 1-16 sensors per WD2 board with only one coaxial cable
- Automatic HV adjustments with temperature changes

DS18B20 Programmable Resolution 1-Wire Digital Thermometer
- User-Definable Nonvolatile (NV) Alarm Settings
- Alarm Search Command Identifies and Addresses Devices Whose Temperature is Outside Programmed Limits (Temperature Alarm Condition)
- Available in 8-Pin SO (150 mils), 8-Pin µSOP, and 3-Pin TO-92 Packages
- Software Compatible with the DS1822
- Applications Include Thermostatic Controls, Industrial Systems, Consumer Products, Thermometers, or Any Thermally Sensitive System
Trigger Concentrator Board (TCB)

- Receives serial links (SERDES) from WD boards
- Computes crate local trigger
- Send trigger via serial links to global trigger in dedicated crate
- FCI Densishield cables
Ancillary system

- Contains master clock
- Distribute clock (jitter < 12 ps measured)
- Distribute trigger
- 4 diff. pairs for
  - Clock
  - Trigger
  - Busy
  - (Sync)

Clock 100 MHz

Trigger

Busy

Digitization and Readout

optional: Error

Spare (Sync)
DAQ Concentrator Board (DCB)

- Receive Gbit links from WDB
- Use SERDES instead GTX (lower latency)
- Waveform preprocessing in Zynq CPU
- Output via Gbit Ethernet (10 Gbit optional)
- Board under design
- Tests with Zed-Board and “Backplane Simulator”
Half Height Backplane
SPI configuration

```
0 1 ... 7 8 ... 14 15

MOSI / MISO / SCLK

SSx

DCB  TCB  CMB

10 GBit Ethernet

SPI Master
SCLK MOSI MISO SS

SPI Slave
SCLK MOSI MISO SS

SS

SCLK

MSB LSB MSB

MOSI R/W A6 A5 A4 A3 A2 A1 A0
D31 D30 D29 D28 D27 D26 D25 D24 D21 D20

... LSB
```
Gbit links for DAQ & Trigger

0  1  ...  7  8  ...  14  15

3 x GBit 8 x GBit

10 GBit Ethernet

Event Builder PC  Global Trigger

DCB  TCB  CMB
Trigger Bus & HV

0 1 ... 7 8 ... 14 15

Trigger Sync Busy

DCB TCB

Global Trigger

High Voltage

CMB
WaveDAQ Clock Distribution

Goal: < 5 ps clock jitter at system level
Minimal System

Power-over-Ethernet
One-crate system

Up to 256 Channels

Detector

Gbit Ethernet

Power Supply 24V

220 V
MEG II System

35 crates x 256 channels = 9000 channels
WaveDAQ Performance

- Trigger resolution 10 ns (100 MHz clock)
- Trigger bandwidth 8 Gbit / s
- Trigger latency <380 ns *) (9000 channels)

- DAQ bandwidth 2 Gbit / s
- DAQ time measurement 10 ps *)
- DAQ dead time 3 - 35 μs / event

- MEG II: 7 x 10^7 μ/s, DAQ eff. > 95% @ 30 Hz *)

*) projected
Conclusions

• WaveDAQ system has been designed to fulfill needs of MEG II experiment
• System has huge potential for many others (costs: ~130 EUR / channel)
• Status: Crate fully working, trigger board and WaveDREAM board successfully tested, firmware to be finished, DCB under design
• First full crate test end of 2015, full system (35 crates) in 2016
• DRS5 chip (no dead-time) planned for 2017+