The MuPix 10 – the current state of design

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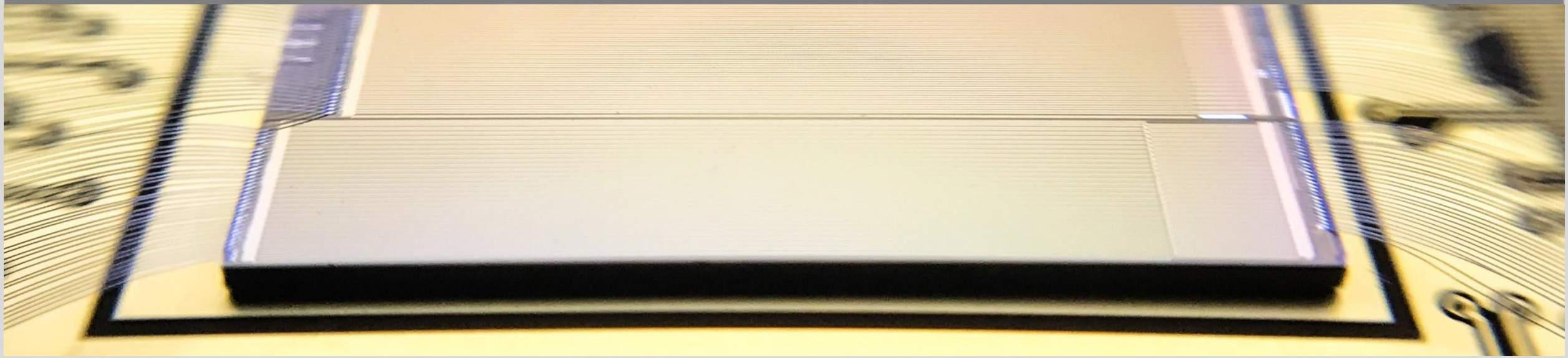
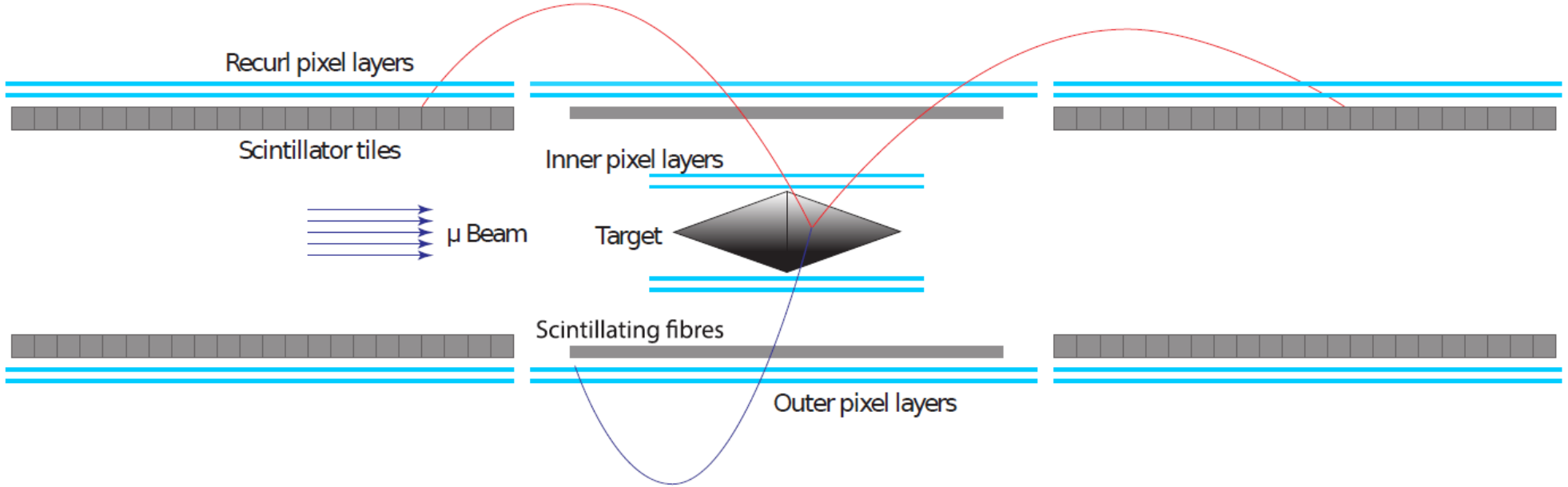


The Mu3e Experiment

- Searching for $\mu^+ \rightarrow e^+e^-e^+$
- Main requirements of the detector:
  - Precise tracking
  - Minimal material budget

- High Voltage Monolithic Active Pixel Sensors (HV-MAPS) fulfil requirements
- Chosen for tracking layers

→ On track to the final chip

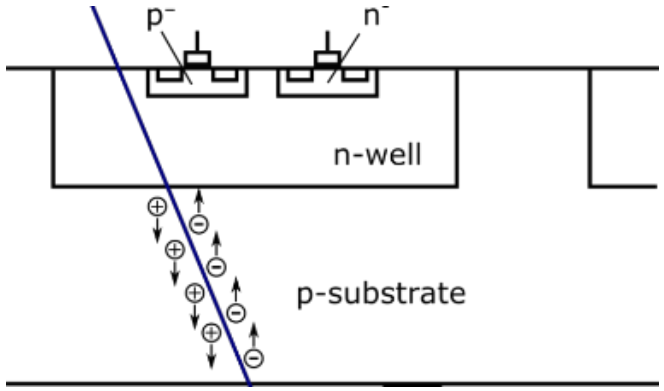


HVCMOS

= **H**igh **V**oltage **C**omplementary **M**etal **O**xide **S**emiconductor

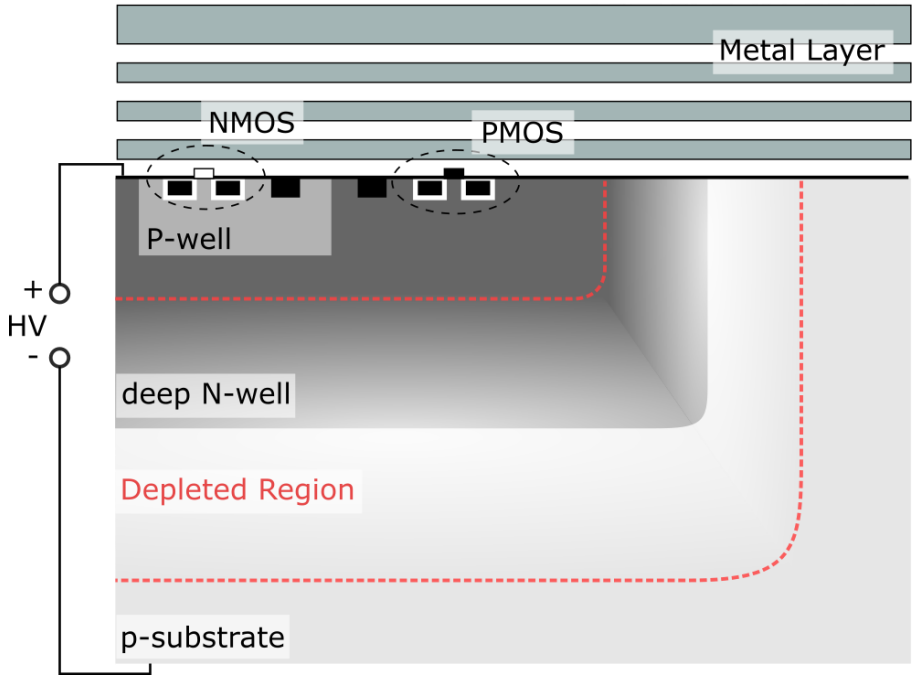
Features

- Fast and efficient charge collection by drift
- Sensor and electronics on the same die
  → monolithic
- Low cost
- Thinned to 50 µm

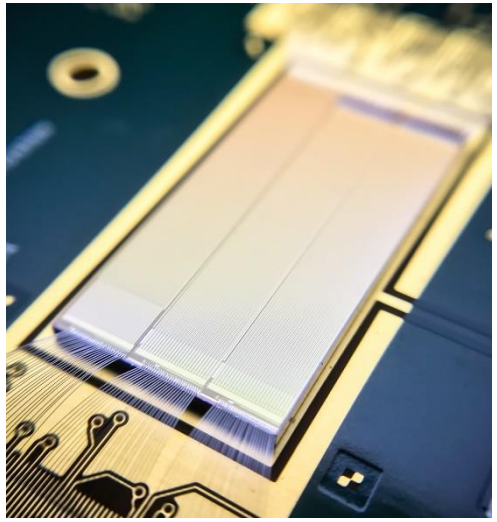


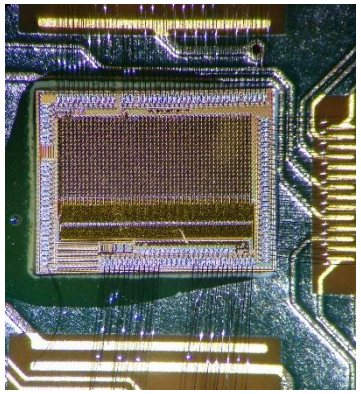
Properties

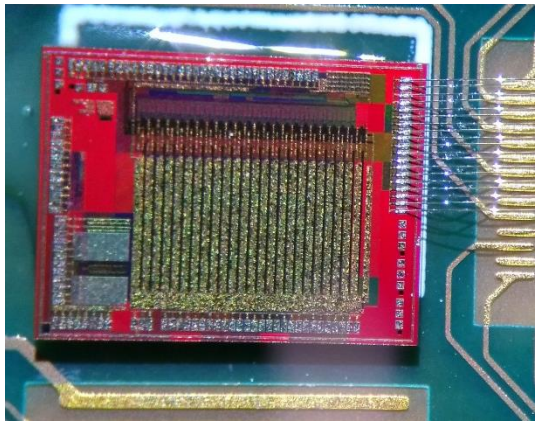
- High depletion voltage ≈ -150 V
- 30 µm depletion depth
- Standard process

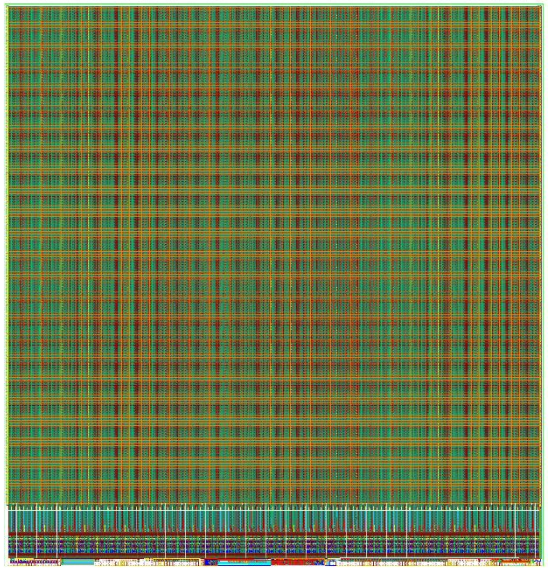


Overview of the latest MuPix and ATLASPix sensors









MuPix 8 January 2017

ATLASPix 1 January 2017

MuPix 9 September 2017

ATLASPix 2 September 2017

ATLASPix 3 March 2019

MuPix 10

Main Challenges

Surrounding

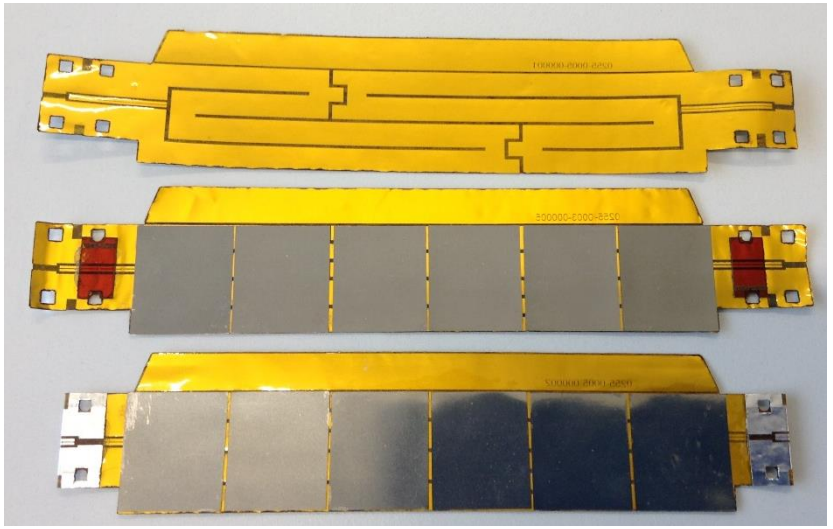
- Full size: active sensor size ≈ 2 x 2 cm²
- Move to new technology
  From AMS to TSI
- One single supply voltage

Design Challenges

- Fully functional
- Operate multiple chips on flexprint
- Limited routing possibilities on flexprint

Aim

Provide a chip for building functional Mu3e modules



Parts of the existing mockup

Design transfer to another technology

AMS ah18

- Used for several prototypes > 10
- 6 metal layers

TSI 180 nm HVCMOS

- First use in our group in 2018
- Submitted three chips
- Verification by comparison of MuPix7 in AMS and in TSI
- 7 metal layers

Chances

- One metal layer more:
  will be used for optimized routing
- Similar technology

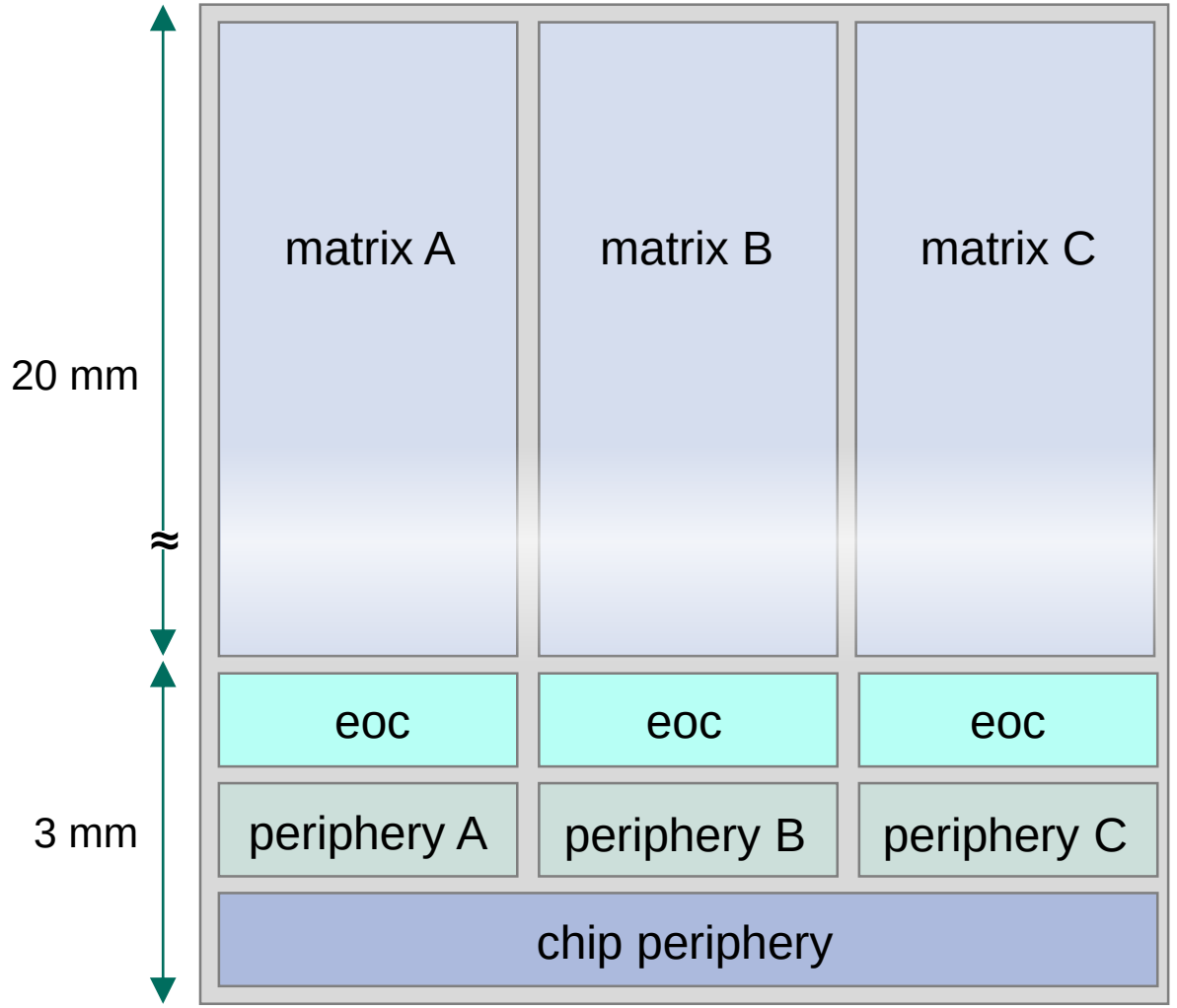
Challenges

- Layout has to be redone for a few circuits
- Design rules different from metal 5 to the top
- Process similar but not the same

Chip overview

Main parts

- Pixel matrix divided in three submatrices
- Pixel periphery with end of column (eoc)
- Submatrix periphery
- Chip periphery



Matrix Design – three submatrices

Common features

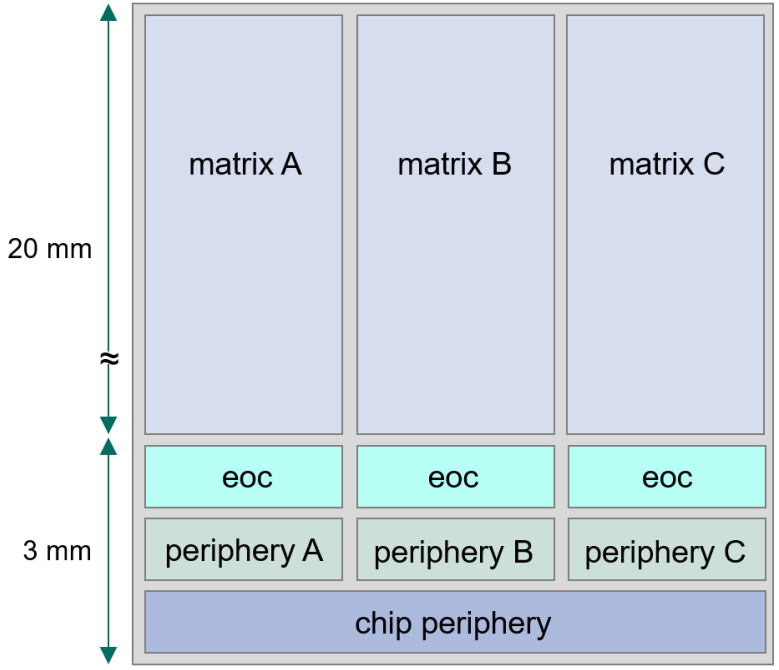
- Pixel size 80 x 80 µm²
- 250 pixels per column, in total 250 columns
- Same state machine but one for every matrix
- Chip periphery

Separated parts and differences

- Configuration bits can be set individually
- Pixel amplifiers
- Signal transmission

Challenges

Operate all matrices at the same time with corresponding configuration and shared chip periphery



Pixel Cell - Diode

Properties

- Pixel size 80 x 80 µm²
- Diode formed by the deep n-well and p-substrate
- New geometry of n-well

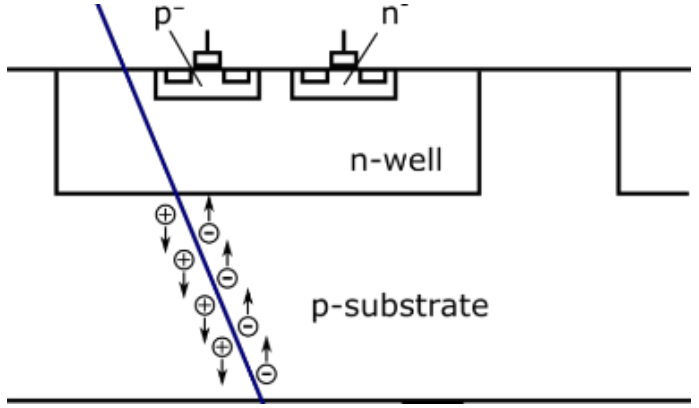
Optimization

- Geometry of charge collection diode will be optimized with TCAD simulations

  → studies ongoing
- Goal: homogeneous electrical field distribution

Implementation and Verification

- One optimized geometry chosen for all matrices
- In first columns of matrix A different pixel geometries will be implemented to allow studies and verification



Pixel Cell - Amplifier

Properties

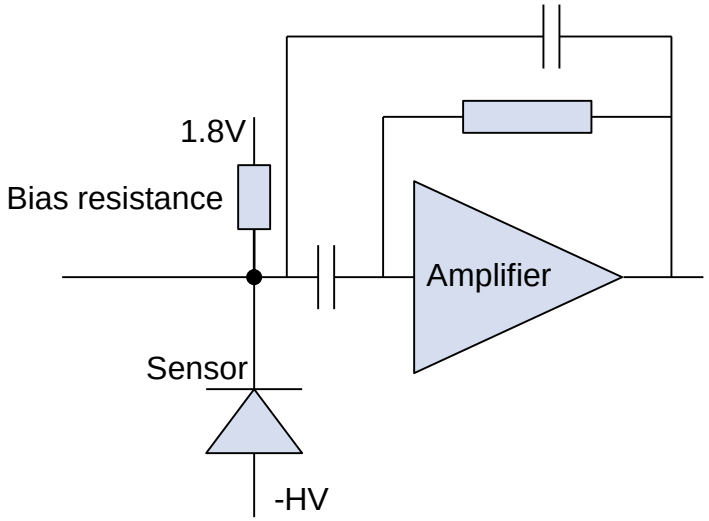
- Amplifier in pixel
- Every pixel maskable

CMOS Amplifier

- Implemented in ATLASPix 3
- Uses vdda = 1,8 V
  no additional voltage needed
- Matrix C

PMOS Amplifier

- Implemented in MuPix 8
- Vssa needed = 0,9 V
- Used successfully in many chips
- Matrix A and B



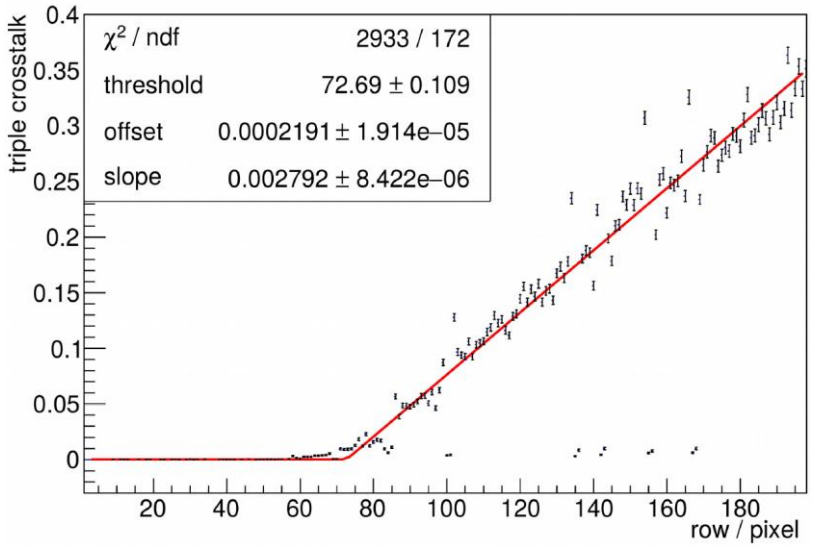
Signal Transmission

Source follower

- Implemented in MuPix 8 matrix A

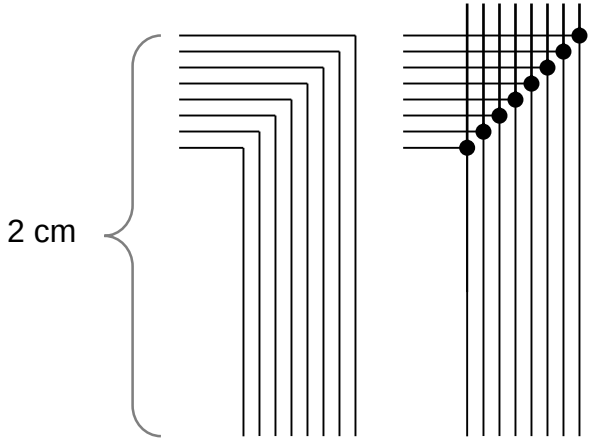
Current driver

- Implemented in MuPix 8 matrices B and C
- Small design modifications needed



Routing

- For routing in total 3 metal layers
- Routing scheme similar to ATLASPix 3
  - same line length
  - all lines with same shape
  - requires more time for routing
  - suppression of row-dependent change of pulse shape
  - more homogeneous time resolution



Readout Cell

2 Threshold Method

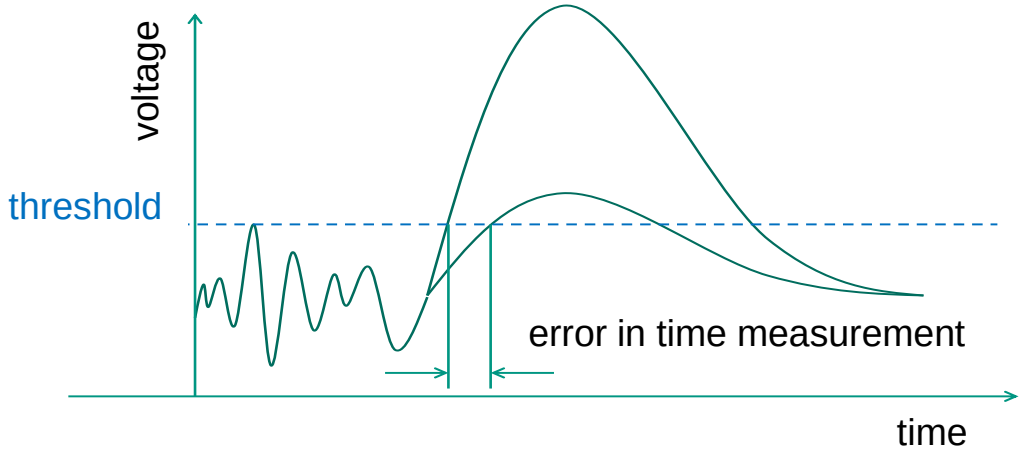
- 2 Comparators per pixel
  like MuPix 8
- 3 bits per readout cell for threshold tuning
- Lower threshold voltage provides timestamp with less timewalk
- Higher threshold confirms signal

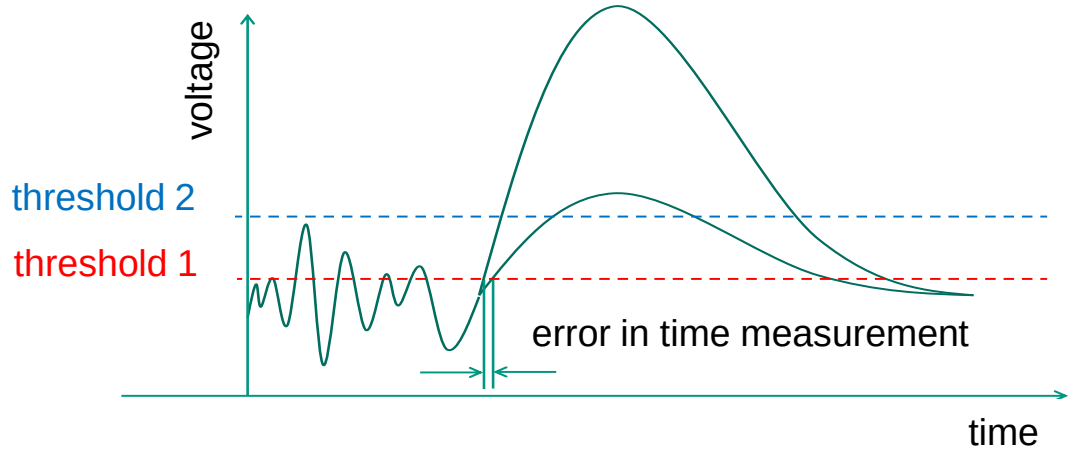
Data Rate

- 11 bits for timestamps
  1 bit more then MuPix 8
- 5 bits for TOT
  one bit less then MuPix 8

→ same data format like MuPix 8

- sampling frequency 250 MHz





Chip Readout and Pads

Readout

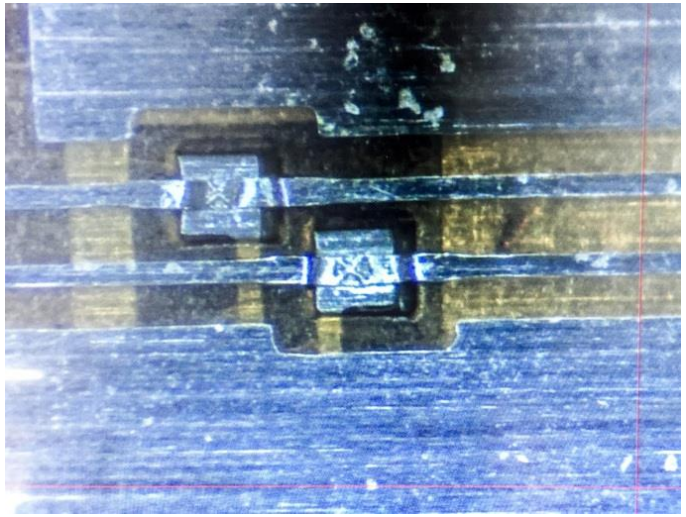
- 3 LVDS links (one for every matrix)
- 1 LVDS link with multiplexed signals
- Max. LVDS data rate 1.6 Gbit/s

Pads

- Minimized number of inputs and outputs to run the chip
- All pads at the bottom
- Enough space for test to monitor internal signals
- Suitable for TAB-bonding

Monitor internal signals

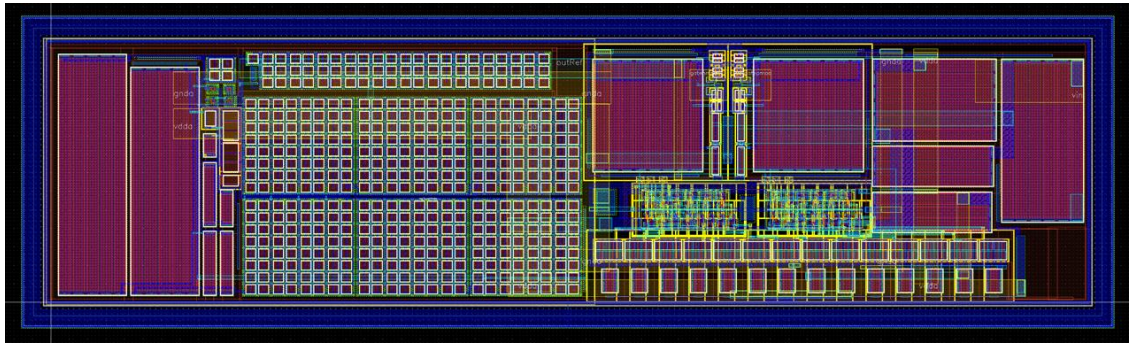
- Temperature
- Amplifier output
- Hitbus
- Bandgap voltage
- Power regulated voltages
- …



Power Regulator

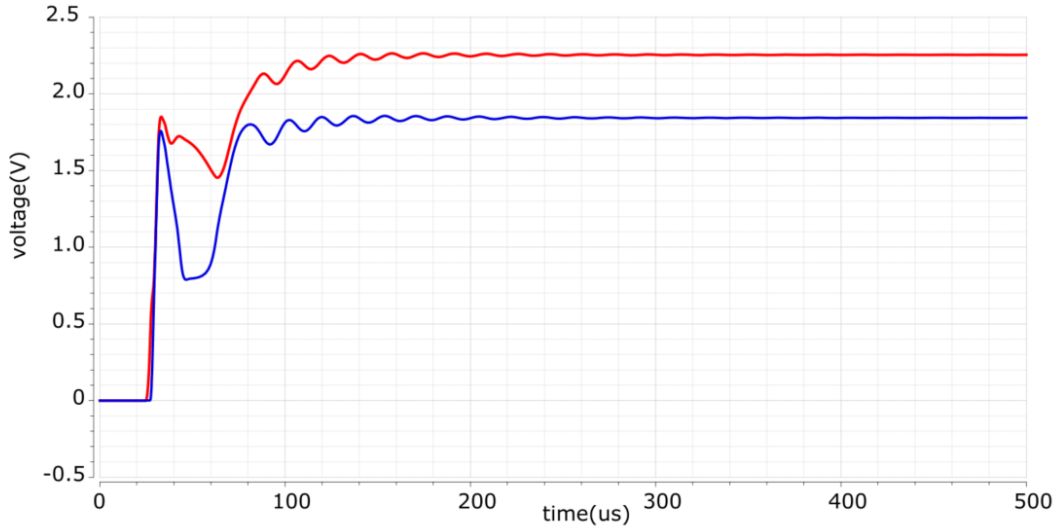
Properties

- In Mu3e: one supply voltage: 2.0 – 2.2 V
- Generates stable 1.8 V and 0.9 V
- Controlled by slow control
- Power separated:
  - Analogue and digital part separated
  - Capacitively coupled
  - Allow different voltage levels for optional serial powering with different schemes



Status

- Power regulator designed for ATLASPix and MuPix
- Actual design submitted with ATLASPix 3



Simulation of 4 chips with power regulator connected in parallel

Summary

Opportunities

- Full size
- Suitable for module building
- A lot of features in one chip – old ones, improved ones, new ones
- Different options in one chip – including the final MuPix design
- Last prototype
- Final chip based on MuPix 10

Photo of the existing mockup

BACKUP

Important features from other chips for MuPix 10

- 2 threshold mode – MuPix 8
- 3 submatrices – MuPix 8
- Pixels with PMOS amplifier – MuPix 8
- Slow control – MuPix 9
- Analog and digital power supply separated and capacitive coupled – MuPix 9
- Power Regulator – MuPix 9 and ATLASPix 3
- Pixels with CMOS amplifier – ATLASPix 3

Power Regulator

- Only one supply voltage: 2.0 – 2.2 V
- Similar Power Regulator developed and implanted on ATLASPix 3, submitted in March
- Based on the results of the measurements of this power regulator the circuit will be optimised for MuPix 10
- Power Regulators controlled by slow control
- Power Regulators can be bypassed
- Power Up Reset with max 1 ms length
  - chip in standby
  - chip can be configured → slow control is the only powered part
  - power regulators disabled
  - single chips tests without cooling possible
- Analogue and digital part separated regarding to power and capacitively coupled

  → allow different voltage levels for optional serial powering with different schemes → implemented in MuPix 9 ✓