Power distribution for the Mu3e experiment

Frederik Wauters
on behalf of the Mu3e collaboration

Johannes Gutenberg Universität Mainz
The Mu3e experiment

- Standard Model branching ratio $5 \times 10^{-55}$
- Mu3e aims for a single event sensitivity of $1 \times 10^{-16}$ (Phase II)
  of $2 \times 10^{-15}$ (Phase I = this talk)
  → Search for new physics
  → Previous limit $1 \times 10^{-12}$ (SINDRUM, 1988)

Signal:
- $\sum E = m_\mu$
- $\sum \vec{p} = 0$

Background:
- Internal conversion
- Combinatorial
The Mu3e detector

- Mu3e detector:
  - $1 \times 10^8 \mu^+$ at the Paul Scherrer Institute
  - Stop muons inside a 1T magnet
The Mu3e detector: power hungry ASICs

- **Mu3e detector:**
  - $1 \times 10^8 \mu^+$ at the Paul Scherrer Institute
  - Stop muons inside a 1T magnet
  - HV-MAPS Si pixel tracker

**MuPix chip:**
- High Voltage Monolithic Active Pixel Sensors
- $< 0.1\%$ of a radiation length/layer
- 2x2 cm, 50 um thick
- 1.25 Gb/s LVDS readout
- 1.8 VDC, $< 1.6 W$, He gas cooled
The Mu3e detector: power hungry ASICs

• Mu3e detector:
  - $1 \times 10^8 \mu^+$ at the Paul Scherrer Institute
  - Stop muons inside a 1T magnet
  - HV-MAPS Si pixel tracker
  - Outer tracker and timing detectors

MuTrig ASIC:
  - SiPM readout
  - 1.25 Gb/s LVDS
  - 1.8 VDC, < 1W

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The Mu3e experiment

Mu3e detector:
- $1 \times 10^8 \mu^+$ at the Paul Scherrer Institute
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- Frontend board with FPGA to merge data and send data out via optical links

112 x Frontend board:
- ArriaV FPGA
- LVDS in, optical out
- $1.1 \rightarrow 3.3$ VDC @ $\approx 15$ W

- 3304 detector ASICs
- 5 kW @ 1.8 VDC
- 100 Gb/s @ 1.25 Gb/s
The Mu3e experiment

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  - Frontend board with FPGA to merge data and send data out via optical links
  - Power distribution & DC-DC conversion
The Mu3e experiment

- **Mu3e detector:**
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  - Frontend board with FPGA to merge data and send data out via optical links
  - Power distribution & DC-DC conversion
  - Very limited space for electronics
Power distribution

12 x 12 20VDC

High density feedthrough
~ 10 kW

Outside

He volume

Frontend boards

Power crate

DC-DC converters in magnetic field

2x18 cm flex with tap bonded 2x2 cm chips

! 2 x 14 μm Al for signal and power!

Cu bars along the beamline

Mupix chips

Flex

Outside He volume

‘no space’ region

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DC-DC converters

- Requirements DC-DC converters
  - $V_{in} = 20$ VDC
  - Efficiency $> 75\%$
  - Ripple of $V_{out} <$ few mV
  - Compact

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- Design concept
  - Buck convertor topology
  - Commercial controller / switch +
  - Custom aircoil because B Field

\[
V_{\text{out}} = \text{Duty cycle} \times V_{\text{in}}
\]

$\Delta V = \Delta Q / C \ (\text{in theory})$

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+ We don`t have to invent the wheel (e.g. FEAST modules of Atlas & CMS)

- Specs of existing CERN boards ≠ Mu3e requirements
DC-DC convertors

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- Status:
  - Aircoil design ready: 2 x 1 cm
  - Prototype for each type
  - Currently: testing / noise study

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10 mV Pk-PK

Efficiency vs. load current

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  - Mechanical/durability testing
  - Feedback stability → load transients

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**Conclusion**
- Mu3e under construction (2021)
- Powering scheme
- DC-DC converter prototypes
  - High $I$
  - B field
  - Compact