

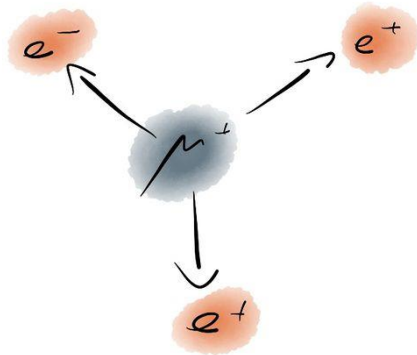


# Power distribution for the Mu3e experiment

Frederik Wauters  
on behalf of the Mu3e collaboration  
Johannes Gutenberg Universität Mainz

# The Mu3e experiment

SM background free  
new physics search



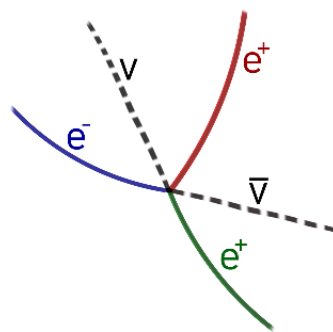
- Standard Model branching ratio  $5 \cdot 10^{-55}$
- Mu3e aims for a single event sensitivity of  $1 \cdot 10^{-16}$  (Phase II) of  $2 \cdot 10^{-15}$  (Phase I = this talk)
  - Search for new physics
  - Previous limit  $1 \cdot 10^{-12}$  (SINDRUM, 1988)

## Signal:

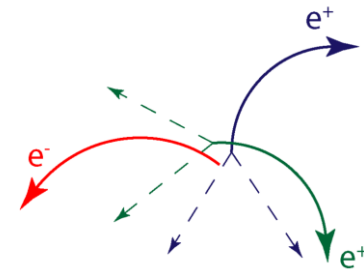
- $\sum E = m_\mu$
- $\sum \vec{p} = 0$

## Background:

Internal conversion



Combinatorial

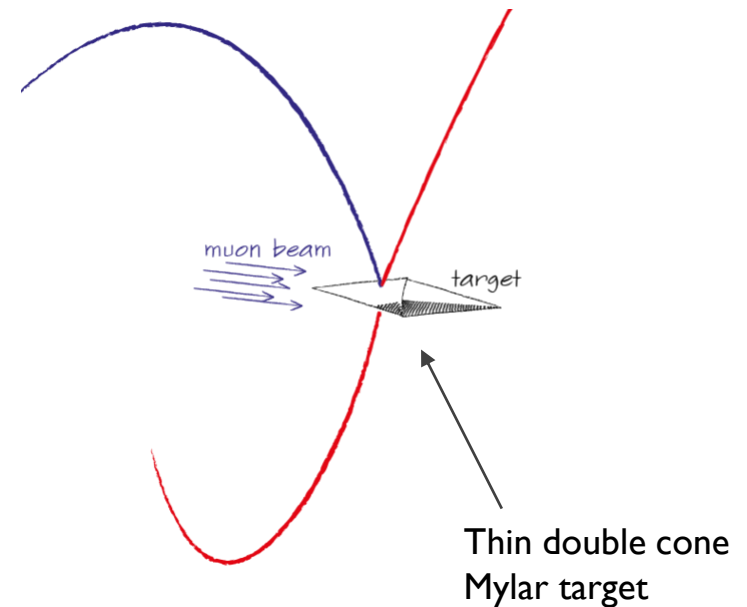
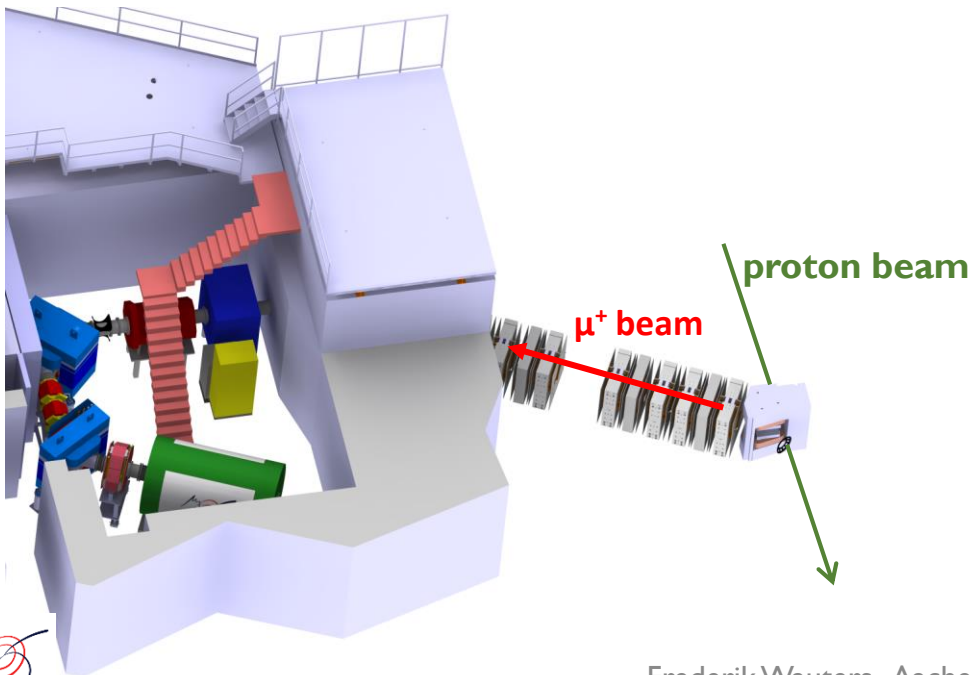


# The Mu3e detector

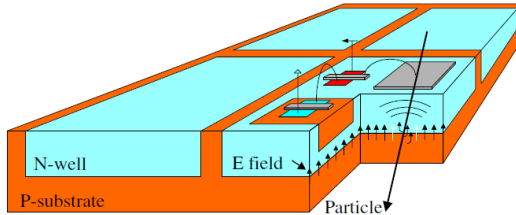


- Mu3e detector:

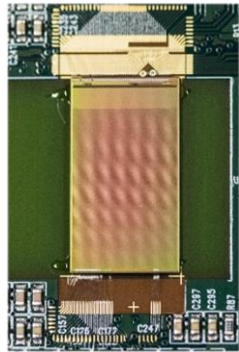
- $1 \cdot 10^8 \mu^+$  at the Paul Scherrer Institute
- Stop muons inside a IT magnet



# The Mu3e detector: power hungry ASICs



T 27.1, T 27.2, T 27.3,  
T 45.6, T 54.1

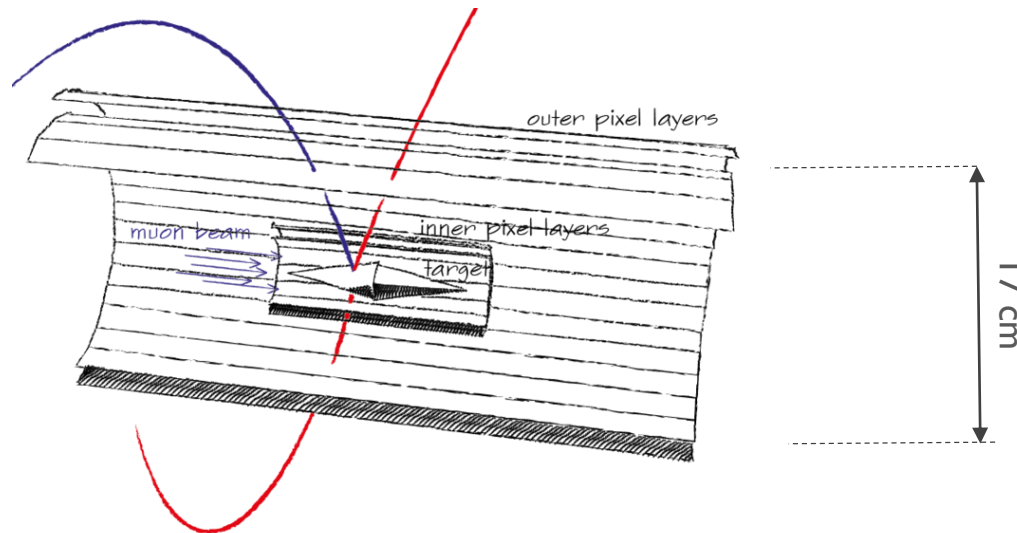


## MuPix chip:

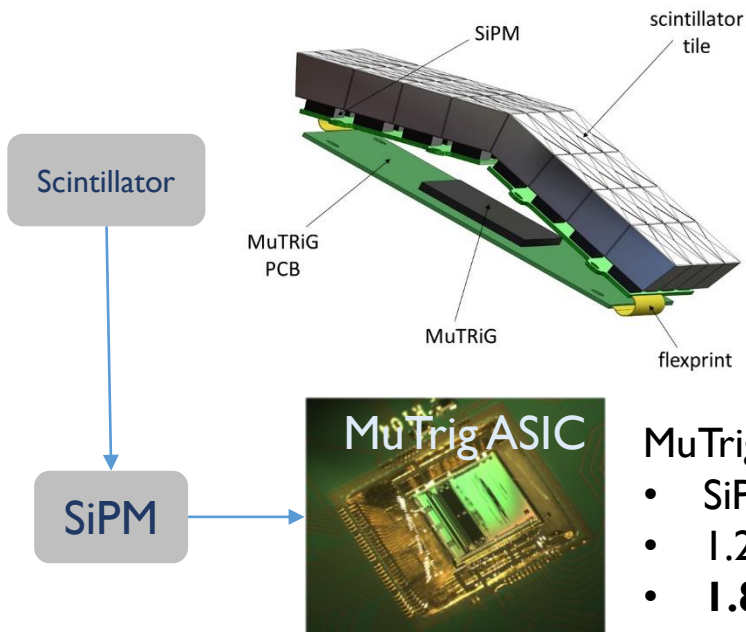
- High Voltage Monolithic Active Pixel Sensors
- $< 0.1\%$  of a radiation length/layer
- 2x2 cm, 50  $\mu\text{m}$  thick
- 1.25 Gb/s LVDS readout
- **1.8 VDC**,  **$< 1.6 \text{ W}$** , He gas cooled

## • Mu3e detector:

- $1 \cdot 10^8 \mu^+$  at the Paul Scherrer Institute
- Stop muons inside a IT magnet
- HV-MAPS Si pixel tracker



# The Mu3e detector: power hungry ASICs



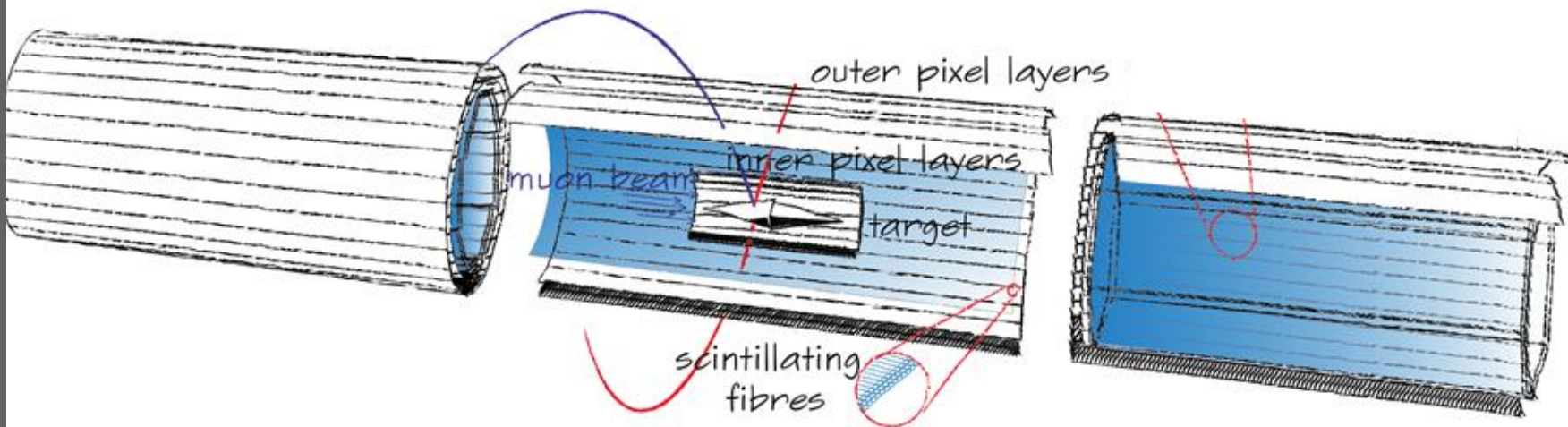
T 94.4

## • Mu3e detector:

- $1 \cdot 10^8 \mu^+$  at the Paul Scherrer Institute
- Stop muons inside a IT magnet
- HV-MAPS Si pixel tracker
- Outer tracker and timing detectors

### MuTrig chip:

- SiPM readout
- 1.25 Gb/s LVDS
- **1.8 VDC, < 1W**



# The Mu3e experiment

OUTSIDE

MAGNET BORE

optical fibres

112 x Frontend board:

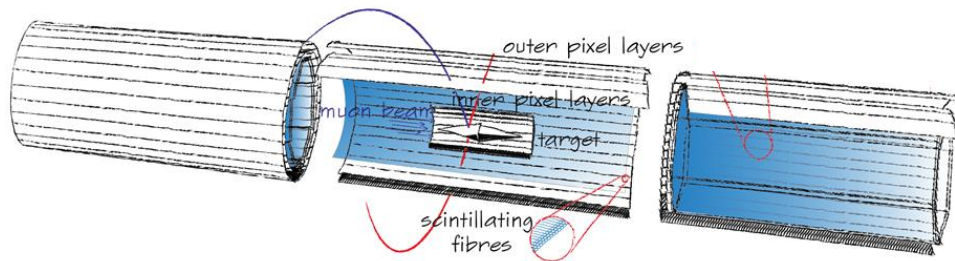
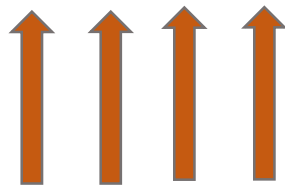
- ArriaV FPGA
- LVDS in, optical out
- **1.1→3.3 VDC @ ≈15 W**



• Mu3e detector:

- $1 \cdot 10^8 \mu^+$  at the Paul Scherrer Institute
- Stop muons inside a IT magnet
- HV-MAPS Si pixel tracker
- Outer tracker and timing detectors
- Frontend board with FPGA to merge data and send data out via optical links

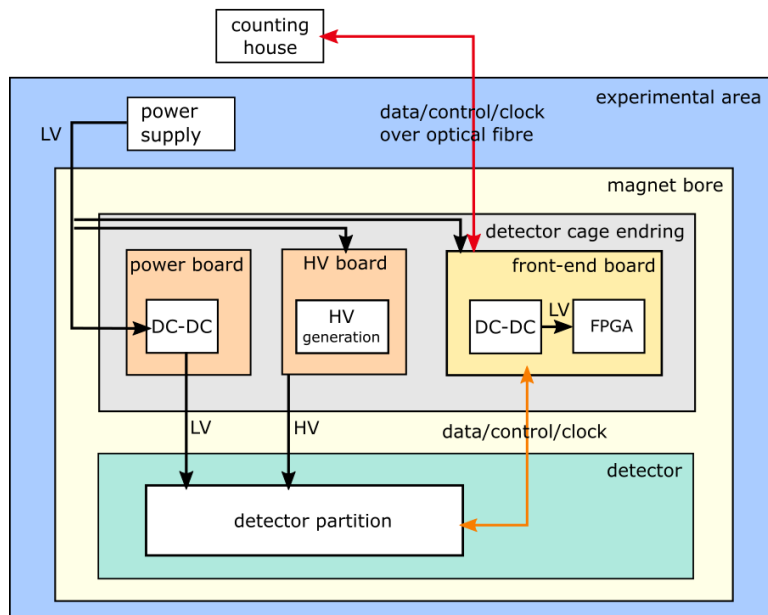
- 3304 detector ASICs
- 5 kW @ 1.8 VDC
- 100 Gb/s @ 1.25 Gb/s



# The Mu3e experiment

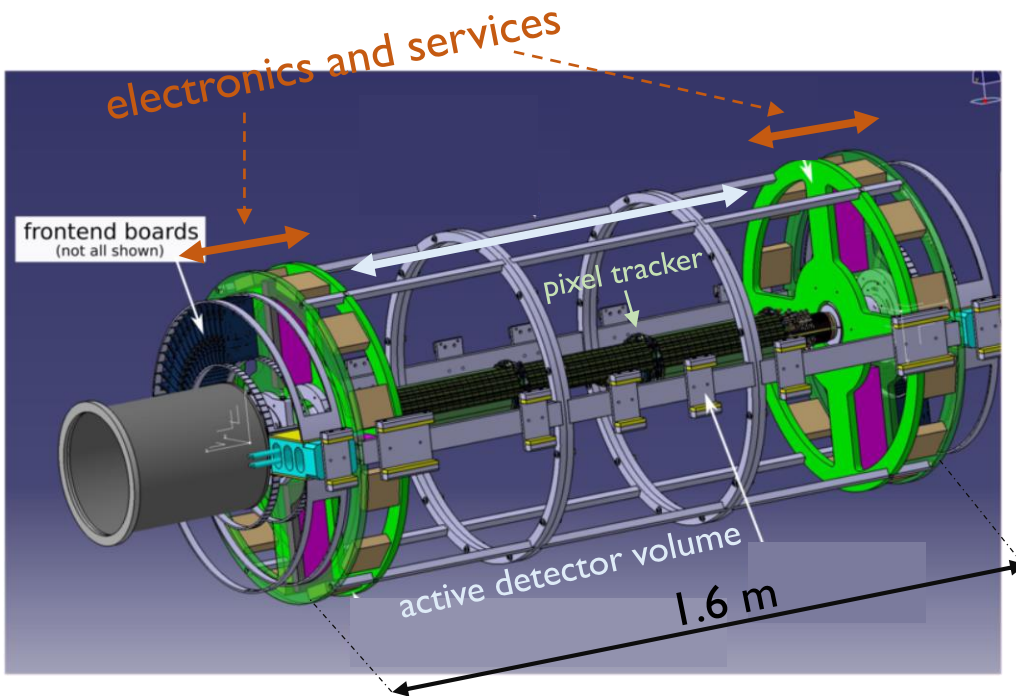
- Mu3e detector:

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- Frontend board with FPGA to merge data and send data out via optical links
- Power distribution & DC-DC conversion



# The Mu3e experiment

- Mu3e detector:



- $1 \cdot 10^8 \mu^+$  at the Paul Scherrer Institute
- Stop muons inside a IT magnet
- HV-MAPS Si pixel tracker
- Outer tracker and timing detectors
- Frontend board with FPGA to merge data and send data out via optical links
- Power distribution & DC-DC conversion
- Very limited space for electronics



# Power distribution

12 x 12 20VDC



high density feedthrough  
~ 10 kW

Outside

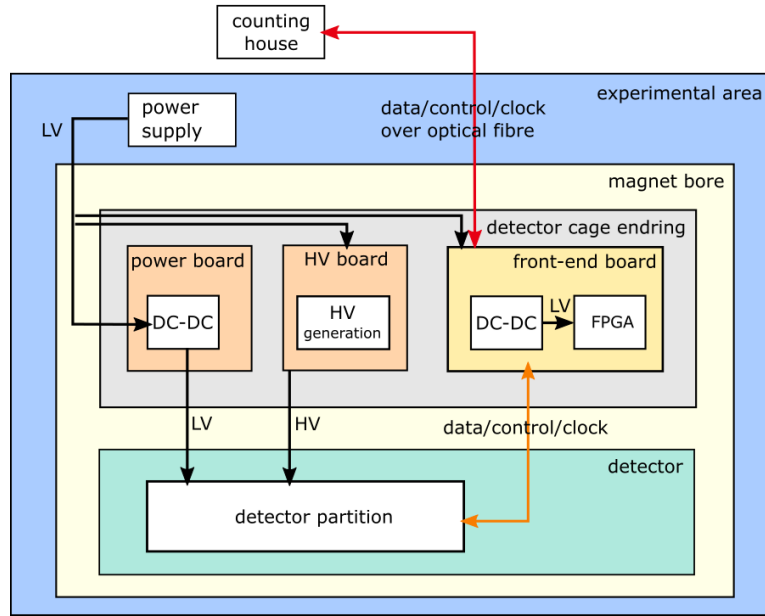


He volume

Frontend boards

power crate

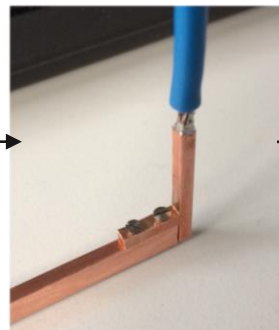
DC-DC converters in magnetic field



- 2x18 cm flex with tap bonded 2x2 cm chips
- ! 2 x 14  $\mu\text{m}$  Al for signal and power !

Al 14 $\mu\text{m}$
PI 10 $\mu\text{m}$
Glue 5 $\mu\text{m}$
PI 25 $\mu\text{m}$
Glue 5 $\mu\text{m}$
Al 14 $\mu\text{m}$
PI 10 $\mu\text{m}$

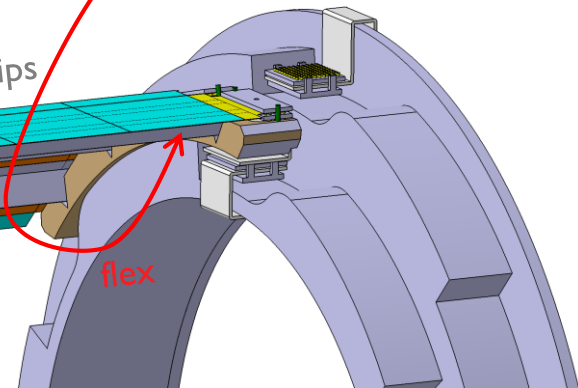
'no space' region



Cu bars along the beamline

Mupix chips

flex



# DC-DC converters

- Requirements DC-DC converters

- $V_{in} = 20\text{VDC}$
- Efficiency  $> 75\%$
- Ripple of  $V_{out} < \text{few mV}$
- Compact

Number	Device	Vout (V)	Current (A)
112	Frontend board	1.1	2
112	Frontend board	1.8	2
112	Frontend board	3.3	2.5
112	Detector ASIC	2.2	10-27

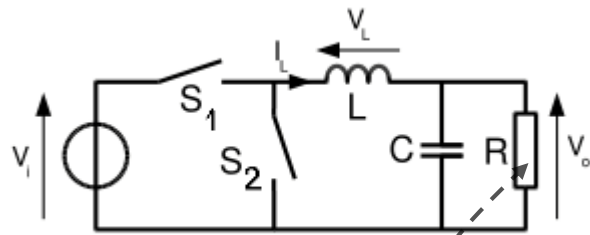


# DC-DC converters

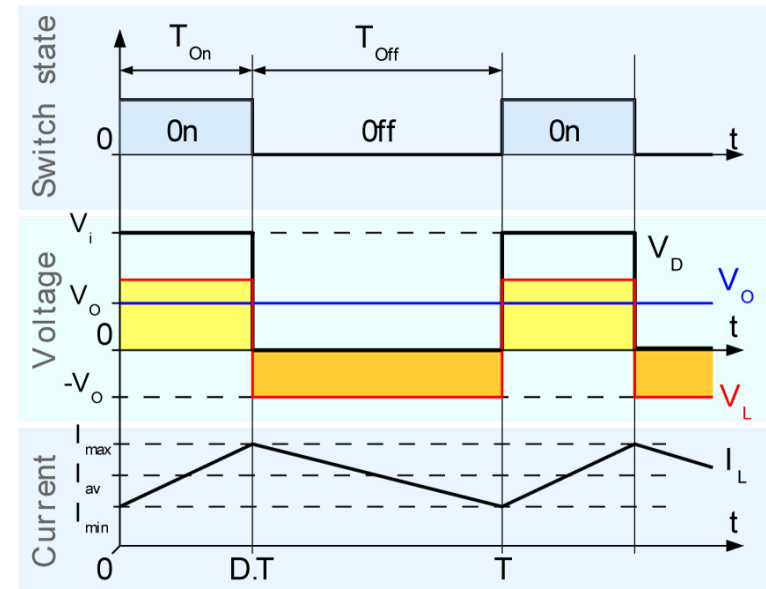
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  - Compact
- Design concept
  - Buck convertor topology
  - Commercial controller / switch +
  - Custom aircoil because **B Field**

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$$V_{out} = \text{Duty cycle} \times V_{in}$$



$$\Delta V = \Delta Q / C \text{ (in theory)}$$



# DC-DC convertors

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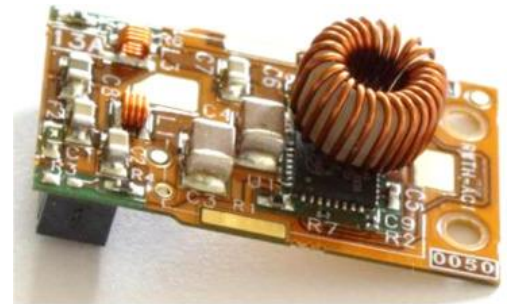
- Design concept

- Buck convertor topology
- Commercial controller / switch +
- Custom aircoil because **B Field**

+ We don't have to invent the wheel  
(e.g. FEAST modules of Atlas & CMS)

- Specs of existing CERN boards  
 $\neq$  Mu3e requirements

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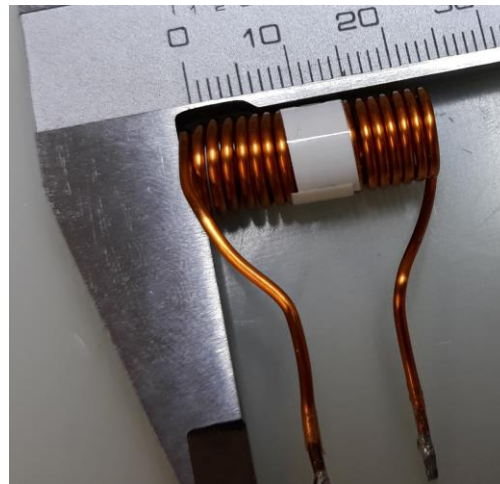
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- Status:

- Aircoil design ready:  $2 \times 1\text{ cm}$
- Prototype for each type
- Currently: testing / noise study

Number	Device	Vout (V)	Current (A)
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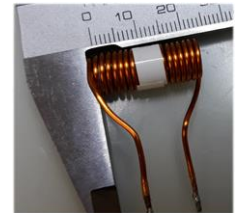
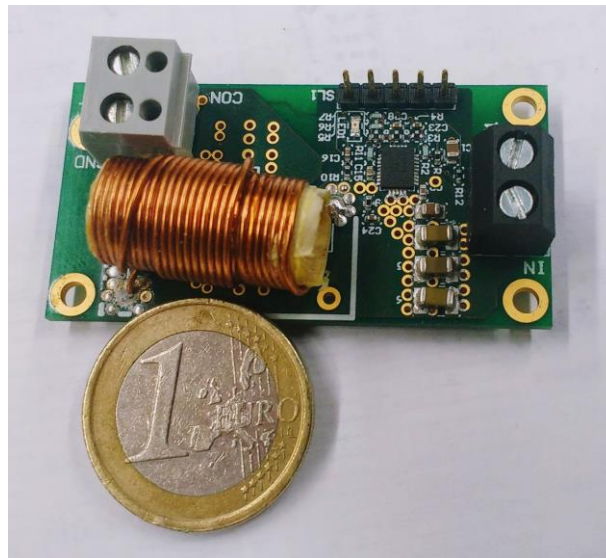
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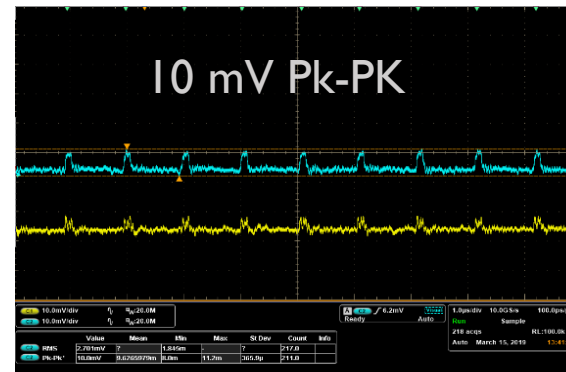
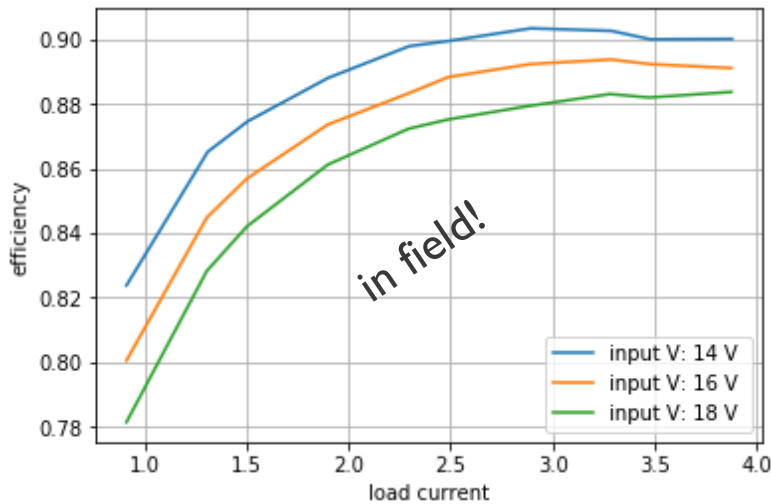
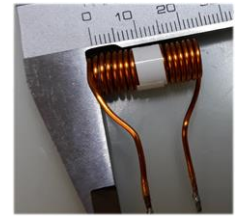
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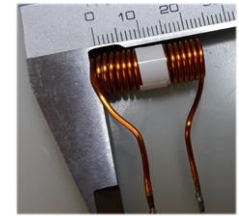
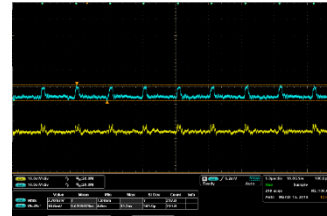
- Requirements DC-DC convertors

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- Compact

Number	Device	Vout (V)	Current (A)
I12	Frontend board	1.1	2
I12	Frontend board	1.8	2
I12	Frontend board	3.3	2.5
I12	Detector ASIC	2.2	10-27

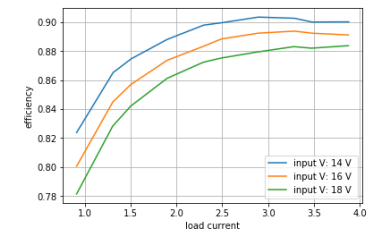
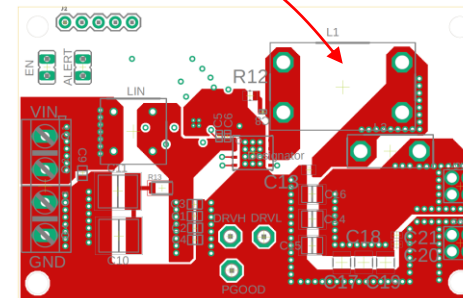
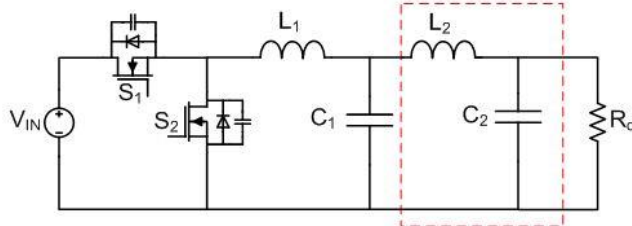
- Status:

- Aircoil design ready: 2 x 1 cm
- Prototype for each type
- Currently: testing / noise study



- Testing program:

- Noise study: second filter? + shielding
- Mechanical/durability testing
- Feedback stability  $\rightarrow$  load transients





# DC-DC convertors

## Requirements DC-DC convertors

- $V_{in} = 20\text{VDC}$
- Efficiency  $> 75\%$
- Ripple of  $V_{out} < \text{few mV}$
- Compact

## Status:

- Aircoil design ready:
- Prototype for each t
- Currently: testing / n

## Testing program:

- Noise study: second
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- Feedback stability →

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		2.2	10-27

## Conclusion

- Mu3e under construction (2021)
- Powering scheme
- DC-DC converter prototypes
  - High I
  - B field
  - Compact

