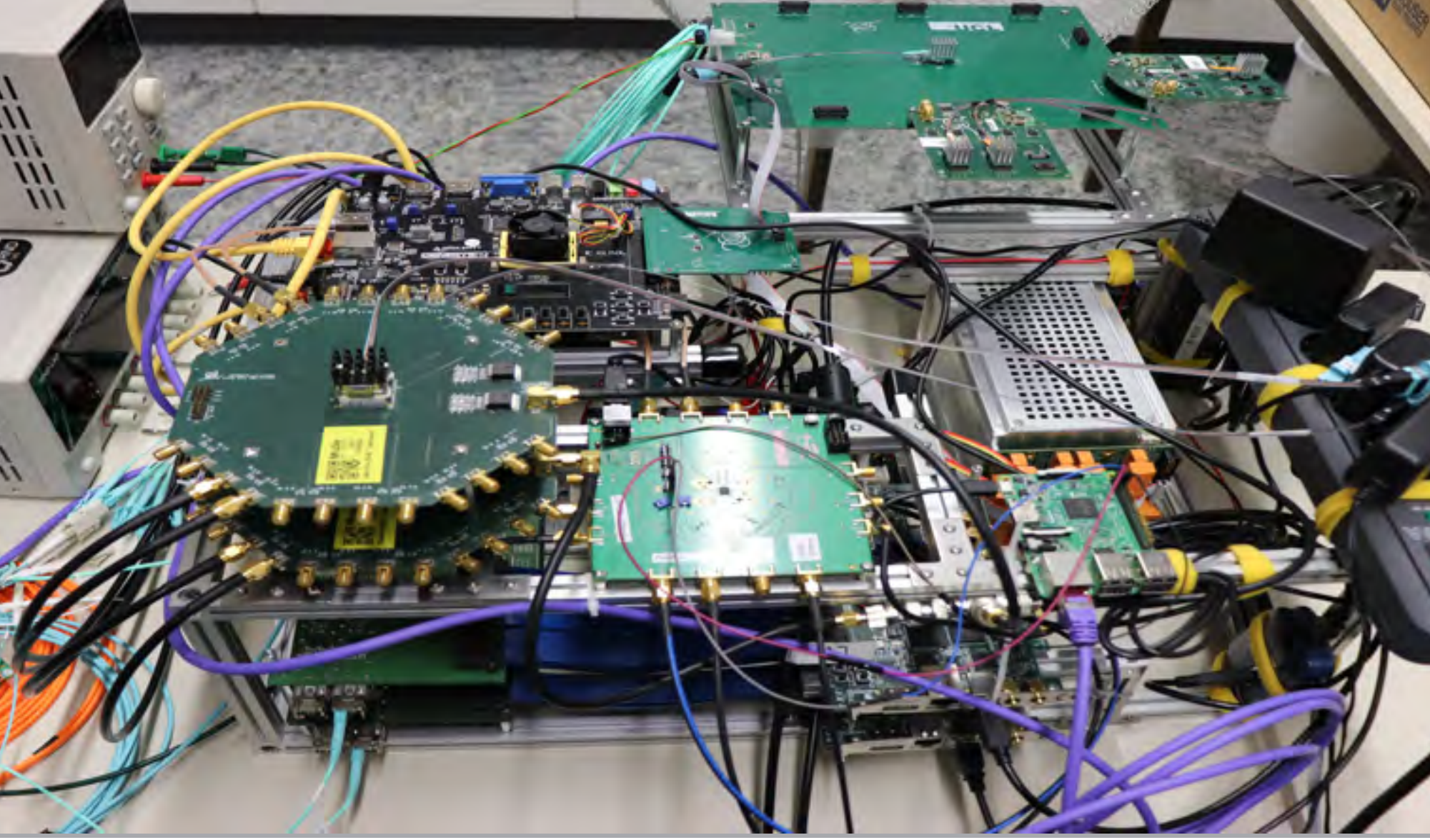


JG|U

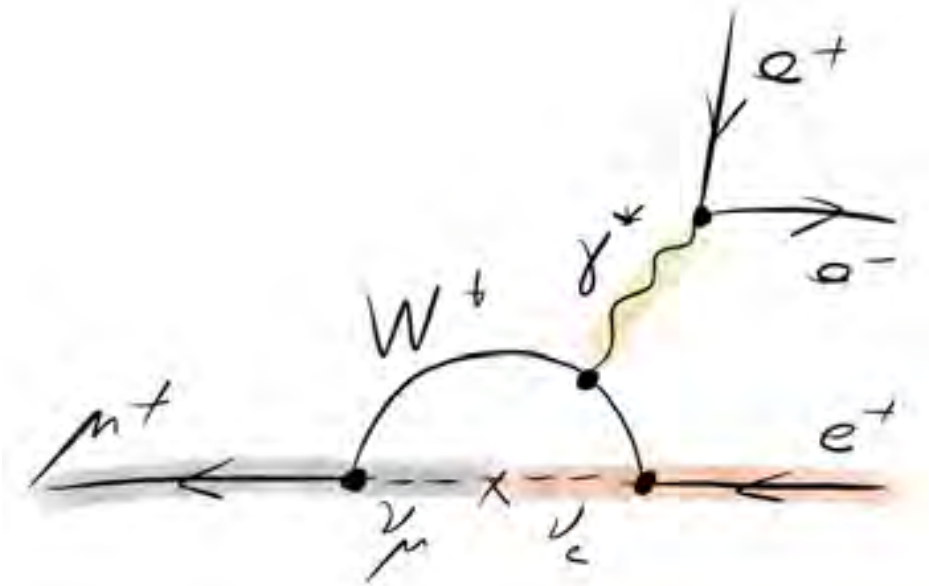
JOHANNES GUTENBERG UNIVERSITÄT MAINZ

A Control System for the Mu3e DAQ

Martin Müller, DPG Spring Meeting 2019 Aachen

Mu3e

$\mu^+ \to e^+ e^- e^+$



Mu3e

- search for the decay $\mu^+ \to e^+ e^- e^+$
- allowed in the SM via internal neutrino oscillation
- predicted branching ratio of 10^{-54} (not observable)
- observation of $\mu^+ \to e^+ e^- e^+$ would be a clear sign for new Physics
- previous upper limit: BR$= 10^{-12}$ SINDRUM (1988)
- Mu3e will aim for 10^{-15}

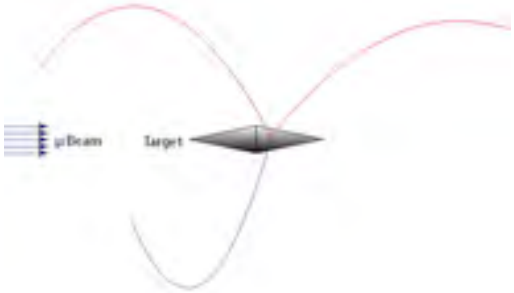
The Mu3e Experiment

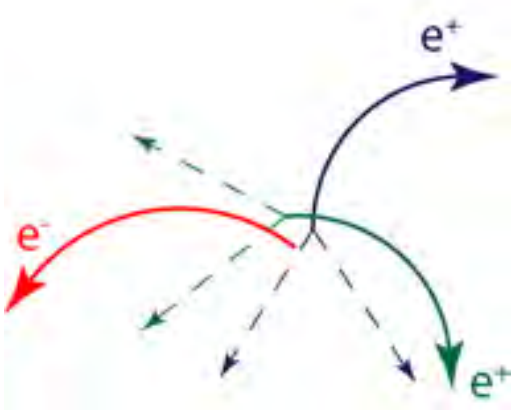
https://www.psi.ch/media/the-psi-proton-accelerator

- Mu3e will be located at the Paul Scherrer Institute (PSI)
- world's most powerful proton accelerator (HIPA)
- 590 MeV, 2 mA
- $10^8 \mu/s$ in a secondary beamline
- muons stopped in a target
- Inside a 1 T magnetic field

The Mu3e Experiment

Background processes:





Background processes

- combinatorical
- ...

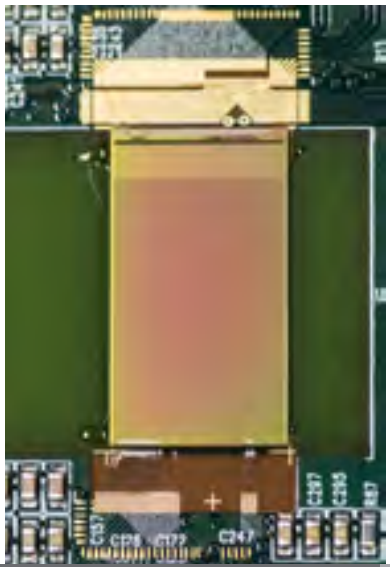
- for **signal** events: $\sum \vec{p} = 0$, $\sum E = m_\mu$, $\Delta t = 0$
- $\rightarrow$ need good momentum, vertex and time resolution
- multiple scattering $\rightarrow$ material budget

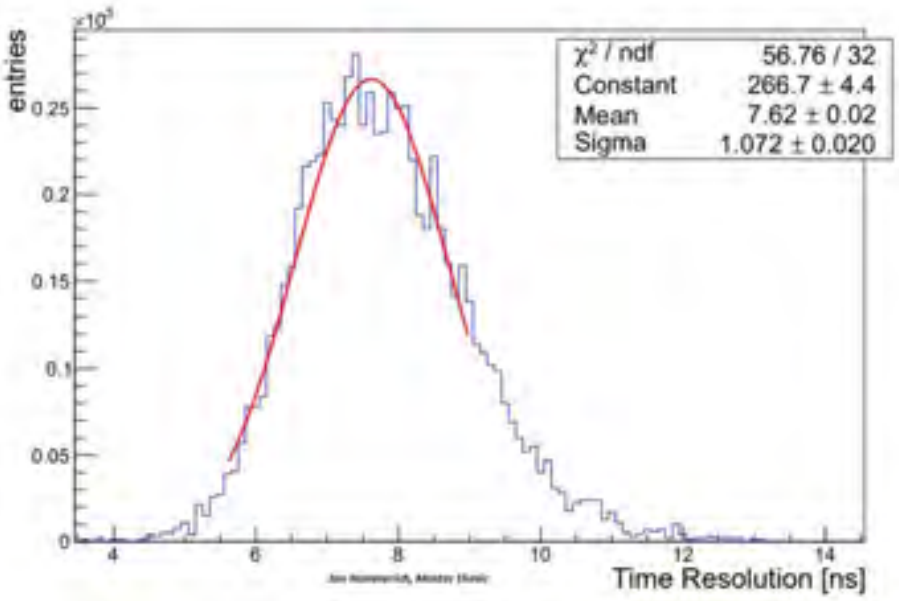
The Mu3e Experiment

The MuPix

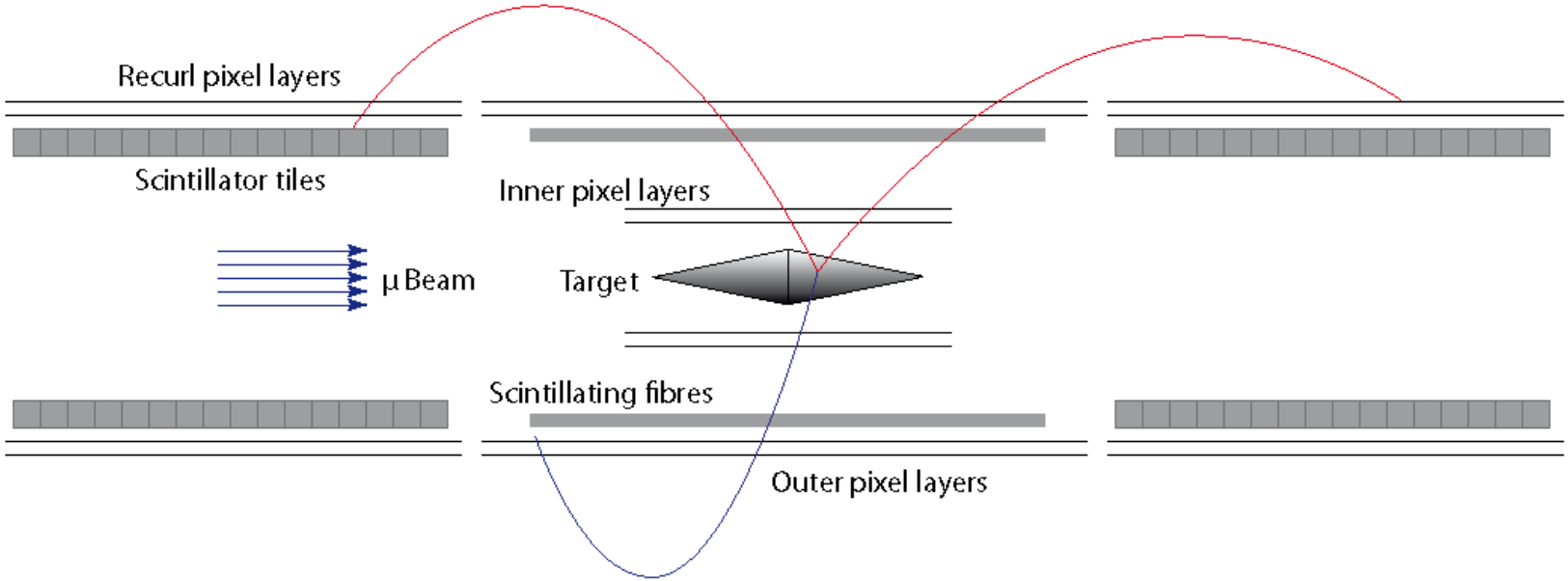
Development of a pixel sensor for the Mu3e experiment

- pixel size of 80x80 μm^2, can be thinned down to 50μm
- includes analog and digital readout electronics on chip
- high voltage bias $\rightarrow$ "HV-MAPS"
- prototype efficiency $> 99\%$
- time resolution < 10 ns



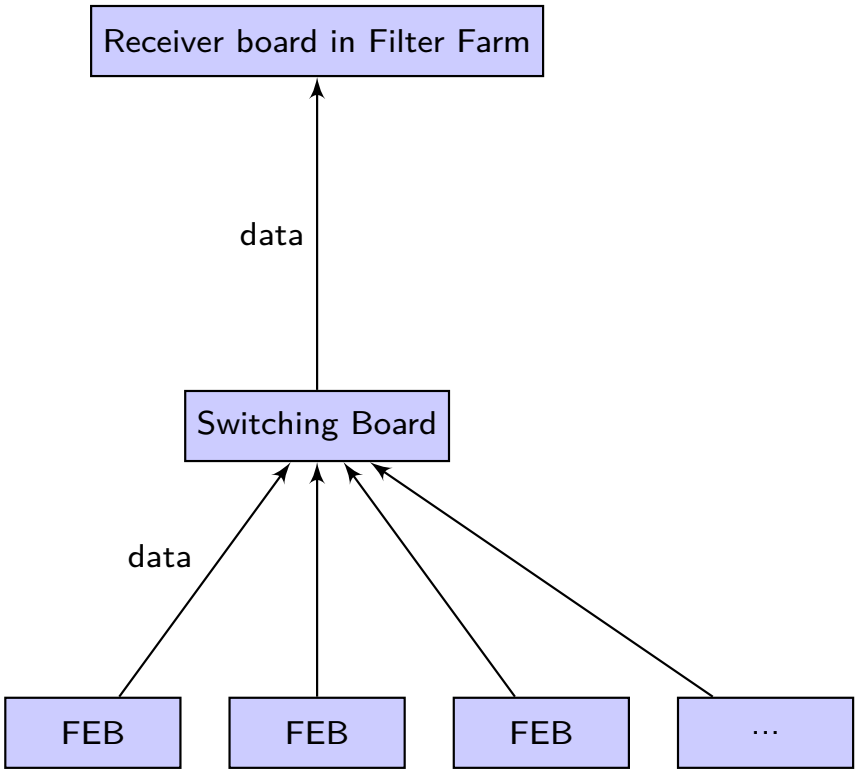


The Mu3e Experiment



- pixel sensors mounted in 4 layers on kapton strips
- scintillating fibres (Δt =500 ps) & tiles (Δt =70 ps) to increase timing precision
- $\rightarrow$ need time synchronization (clock and reset) to a precision of $\mathcal{O}$(10 ps)
- expected data rate of up to 1 TBit/s

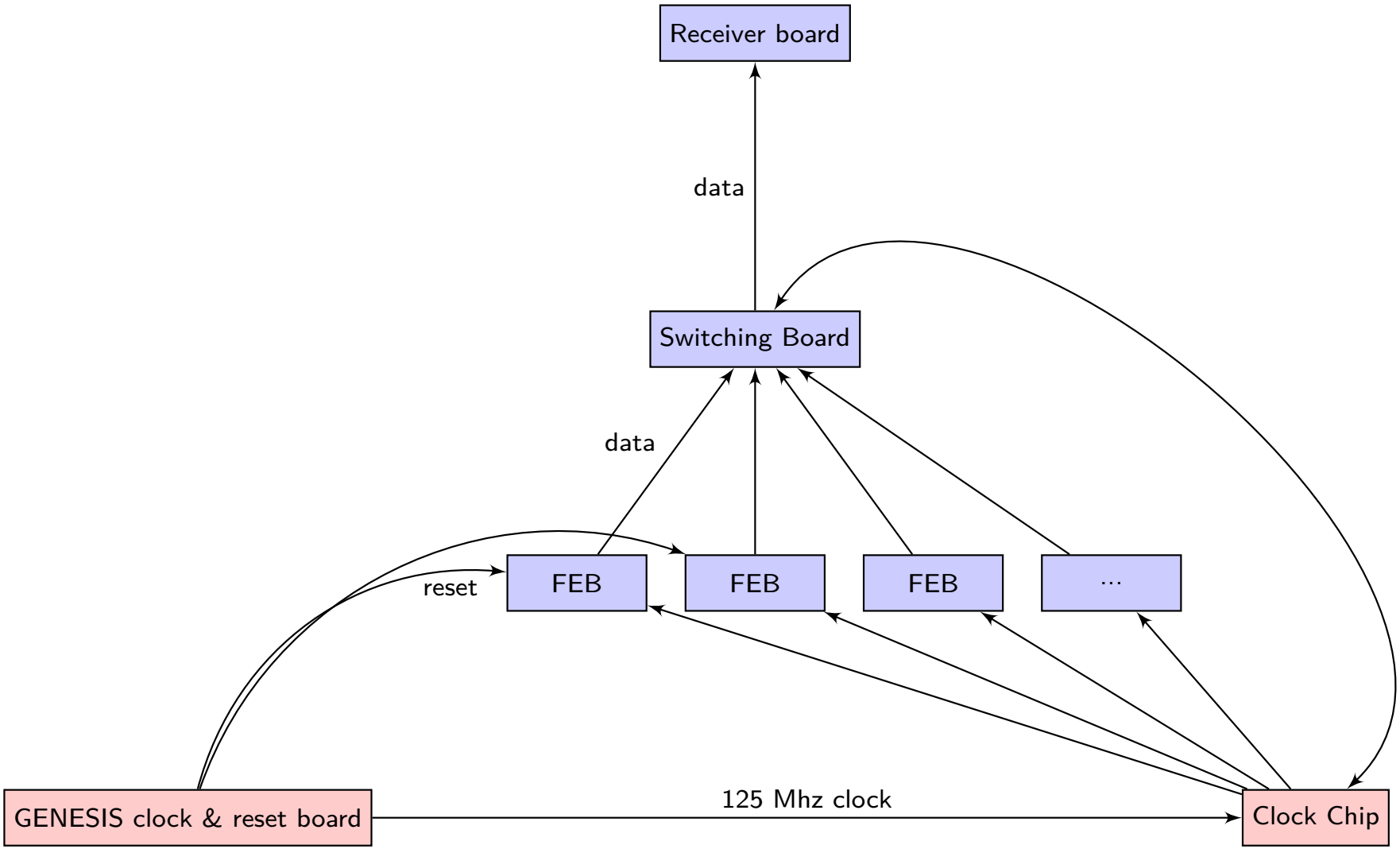
3 Layer DAQ system



- 3 Layer system
- 112 Frontend boards (FEB) connected to Pixel sensors and scintillators
- fast optical connection to 4 Switching boards
- daisy Chain of GPUs with Arria10 development boards as optical receiver
- more in the next two talks ...

Mu3e DAQ

clock & reset distribution



Clock Transmission Boards

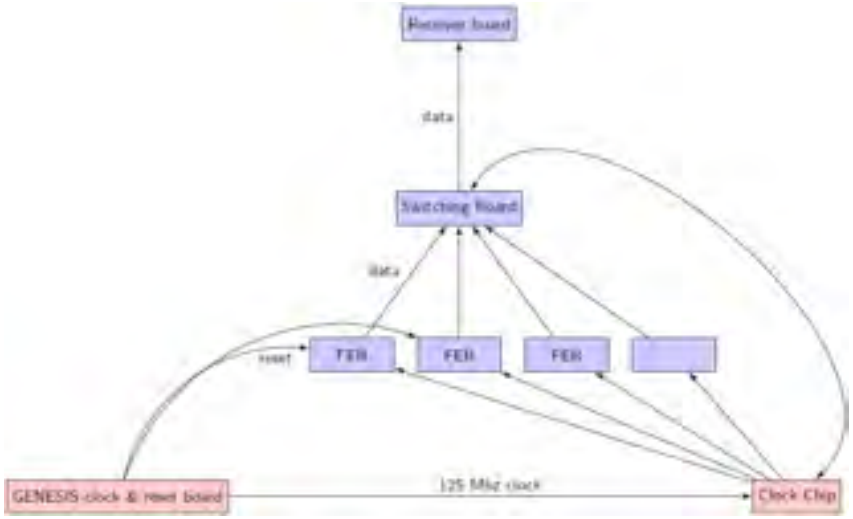
- clock & reset distribution board
- provides 144 copies of a optical clock and 144 copies of a optical reset signal
- FEB's have optical receivers for clock and reset
- other components need electrical input ...

Clock Transmission Boards

- converts the optical clock to electrical signal
- used inside the filter farm PCs
- programmable via SPI with the receiver board
- designed by a bachelor student (Tobias Wagner)

Clock & reset distribution

test results



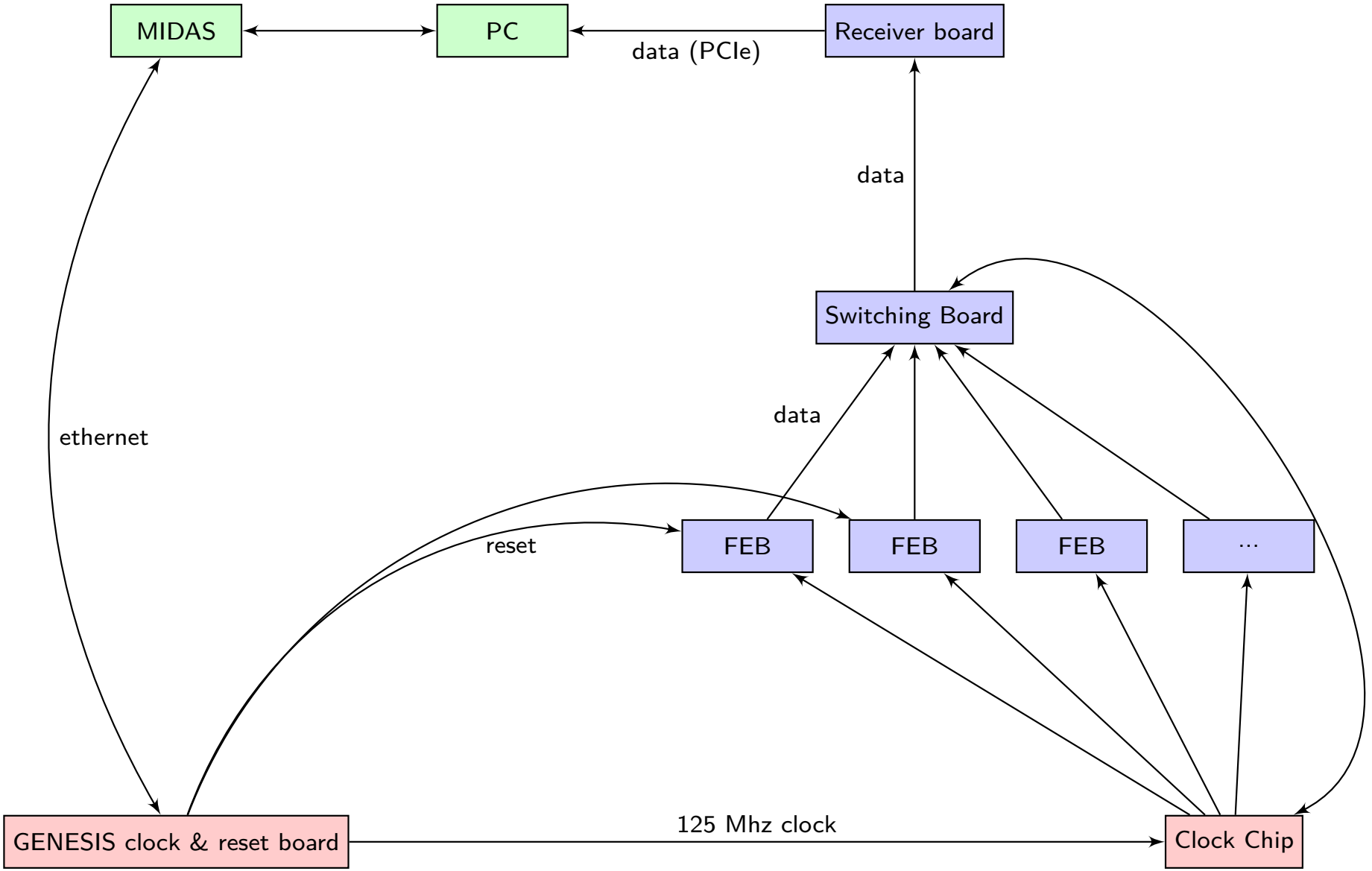
- synchronisation test results:
- 10 ps relative delay (with clock chip corrections and reset synchronised in firmware)
- jitter < 2 ps
- can be maintained across the system
- using MIDAS to control reset signals

MIDAS

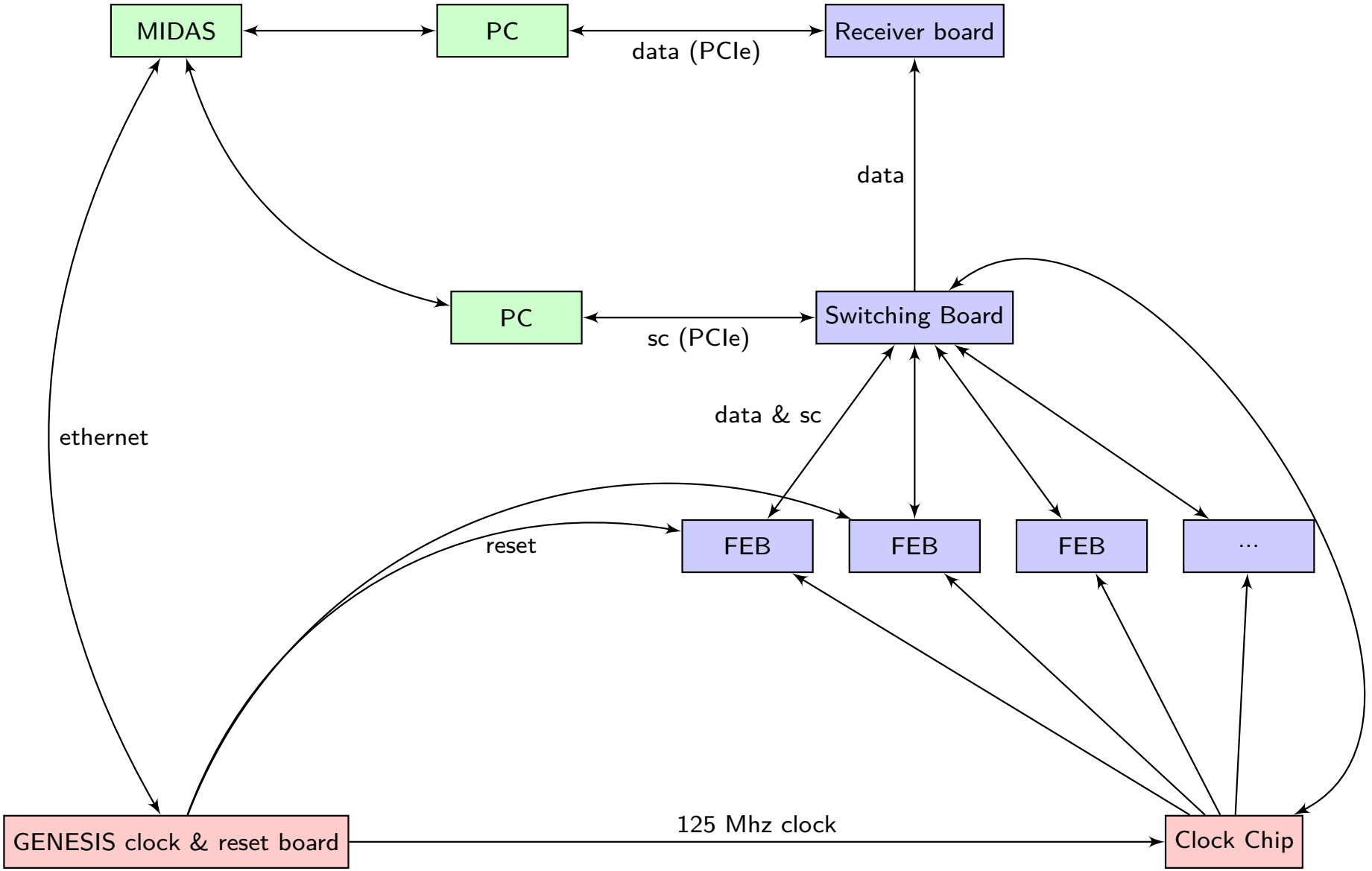
Maximum Integrated Data Acquisition System

- continuous development since 1988
- control of fast and slow data
- integrates all parts of a DAQ into a single system with an online database
  - data logger
  - custom device drivers
  - alarm system
  - history system
  - electronic logbook (ELOG)
  - ...
- user interface: MIDAS Web Server
- more information: https://midas.triumf.ca

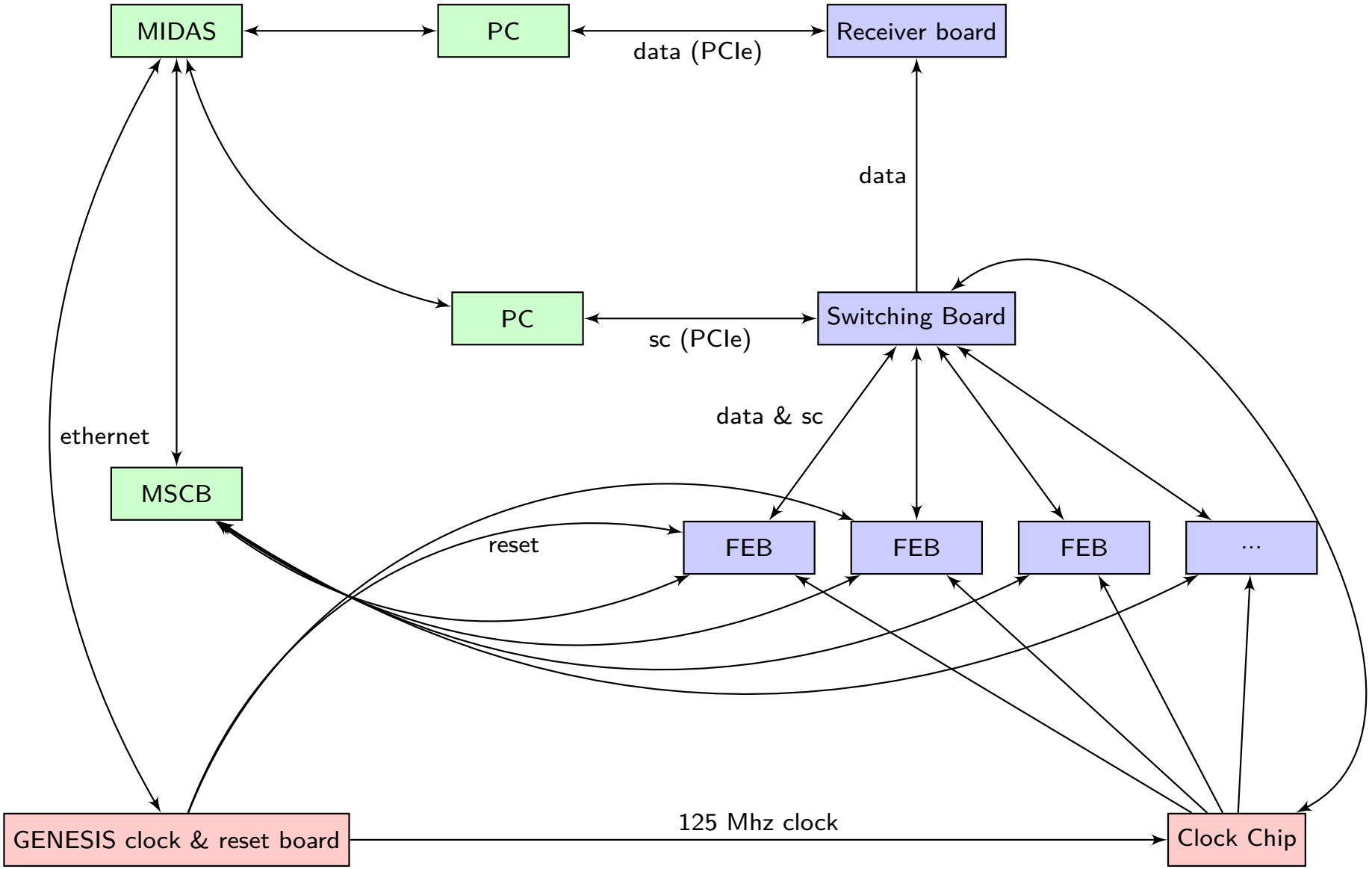
Mu3e DAQ
MIDAS



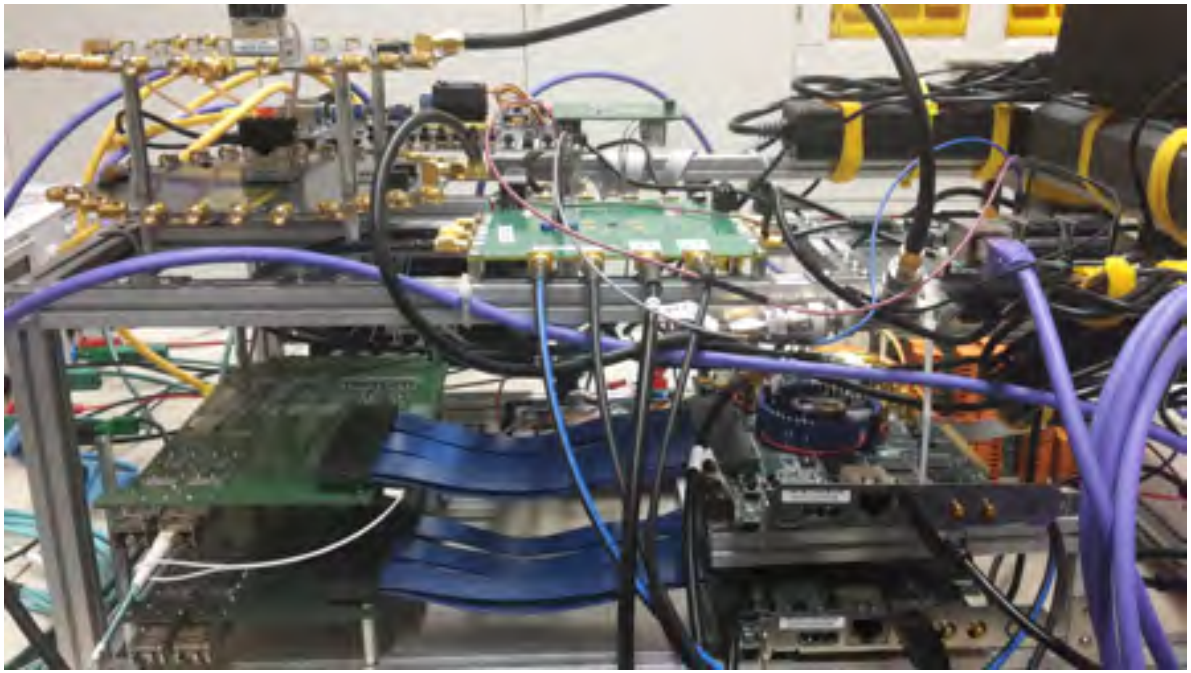
Mu3e DAQ
Slowcontrol (sc)



Mu3e DAQ
MSCB (Midas Slow Control Bus)



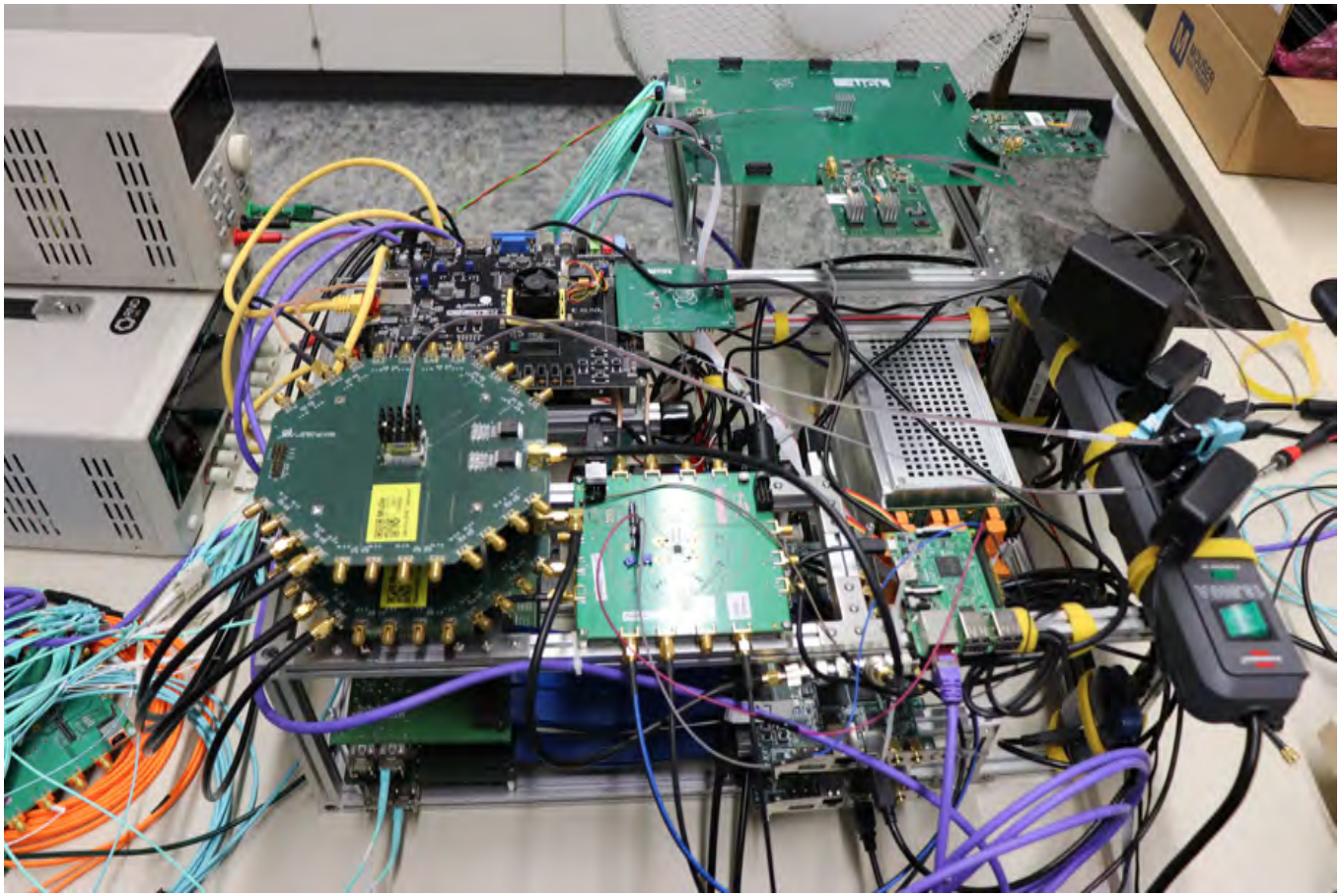
DAQ test setup



Outlook

- user interfaces
- horizontal scaling (more FEB's)
- replacing preliminary parts with the final components
- integrating the real pixel, fibre and tile detector

DAQ test setup



Questions ?

Backup

FEB States
and Data send to SWB

FEB State	Data→SWB	Comment
Idle	Slowcontrol	
Run Prepare	Slowcontrol Active signal	 only once
Sync	–	
Running	Slowcontrol MuPix data	
Terminating	Slowcontrol MuPix data Run tail	 "leftovers" from running only once
Link Test	BERT's	bit error rate tests
Sync Test	Timing measurements	
Reset	–	
Out of DAQ	Slowcontrol	

- use reset link to distribute control signals from GENESIS

Reset signals

Command	Code	Payload	Comment
Run Prepare	0x10	32 bit run number	
Sync	0x11	-	
Start Run	0x12	-	
End Run	0x13	-	
Abort Run	0x14	-	
Start Link Test	0x20	To be specified	
Stop Link Test	0x21	-	
Start Sync Test	0x24	To be specified	
Stop Sync Test	0x25	-	
Test Sync	0x26	To be specified	
Reset	0x30	16 bit mask	
Stop Reset	0x31	16 bit mask	
Enable	0x32		
Disable	0x33		
Address	0x40	16 bit address scheme to be defined	

Reset control singals

- Implemented in hardware, including ...
  - Payload
  - Addressing
  - synchronisation across multiple FEB's
- MIDAS frontend communicating with GENESIS

MIDAS

How to connect MIDAS with the different layers ?

3 categories of control data:

- default (optical)
  - large amounts of data
  - pixel configuration
  - firmware updates
  - ...
- safety-related data (MSCB)
  - temperatures
  - pressure
  - ..
  - redundancy for some measurements required
- time critical signals (optical reset)
  - timestamp synchronisation