Development and simulation of the Mu3e tile detector prototype

DPG Spring Meeting Aachen

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HighR

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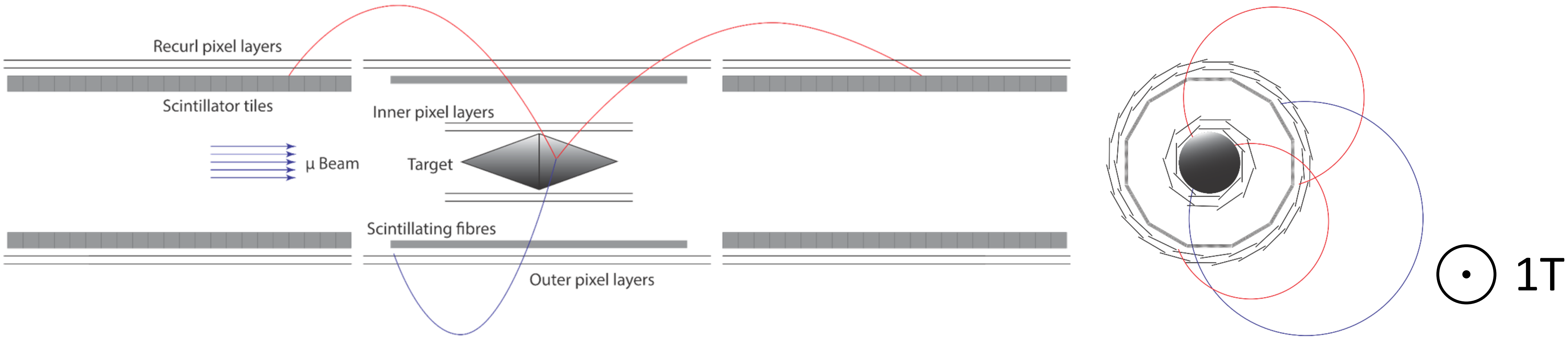
The Mu3e tile detector

The Mu3e experiment

- search for decay $\mu^+ \rightarrow e^+e^+e^-$
- current upper limit: $B_{\mu\rightarrow 3e} < 10^{-12}$ (SINDRUM experiment, 1988)

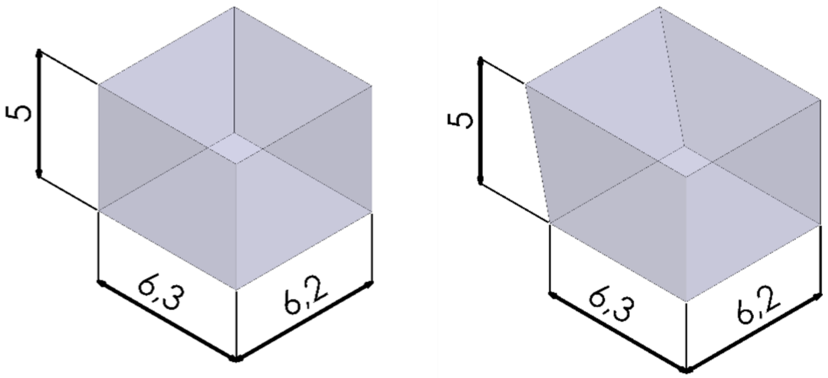
  → aim of Mu3e: $\mathbf{B_{\mu\rightarrow 3e} < 10^{-16}}$
- fixed-target experiment at the Paul Scherrer Institute, Switzerland
- pixelated tracking detectors + scintillating fibre/**tile detector**

position time

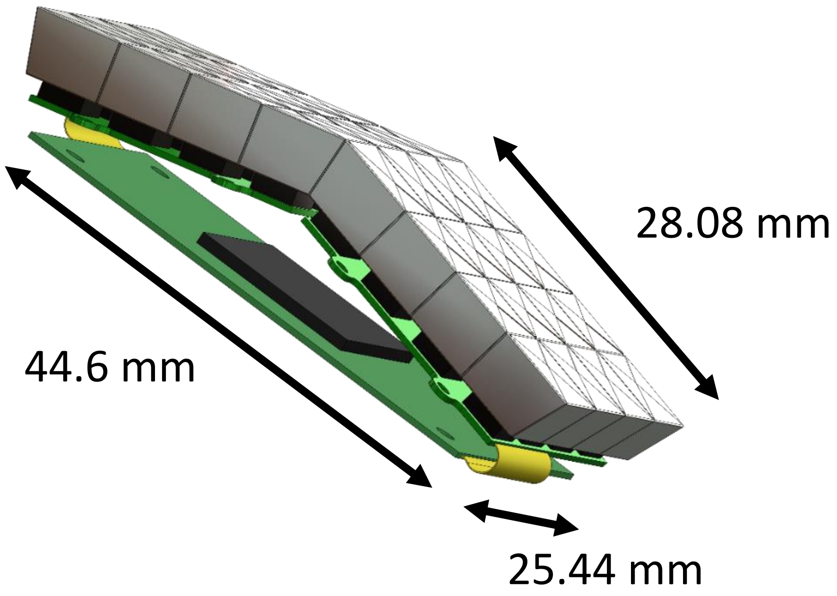


The tile detector

- suppression of accidental background
  - requires timing resolution **≤ 100 ps** at close to 100% efficiency
  - maximum rate: 60 kHz per channel
- plastic scintillator + silicon photomultipliers (SiPMs)
- MuTRiG: custom-designed ASIC to fulfil timing and rate requirements

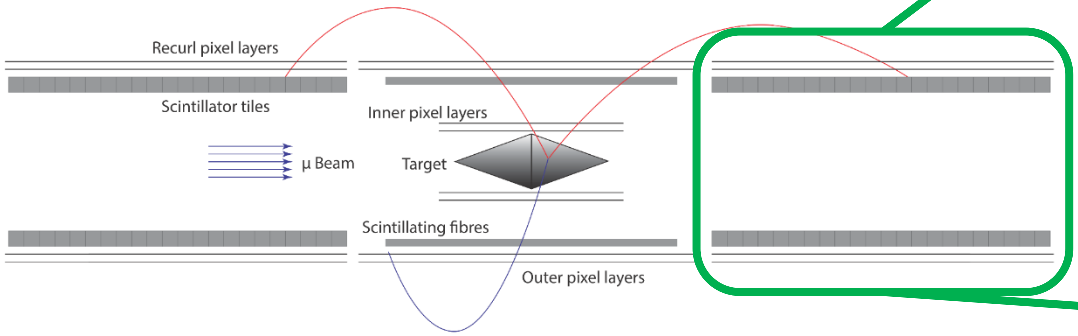


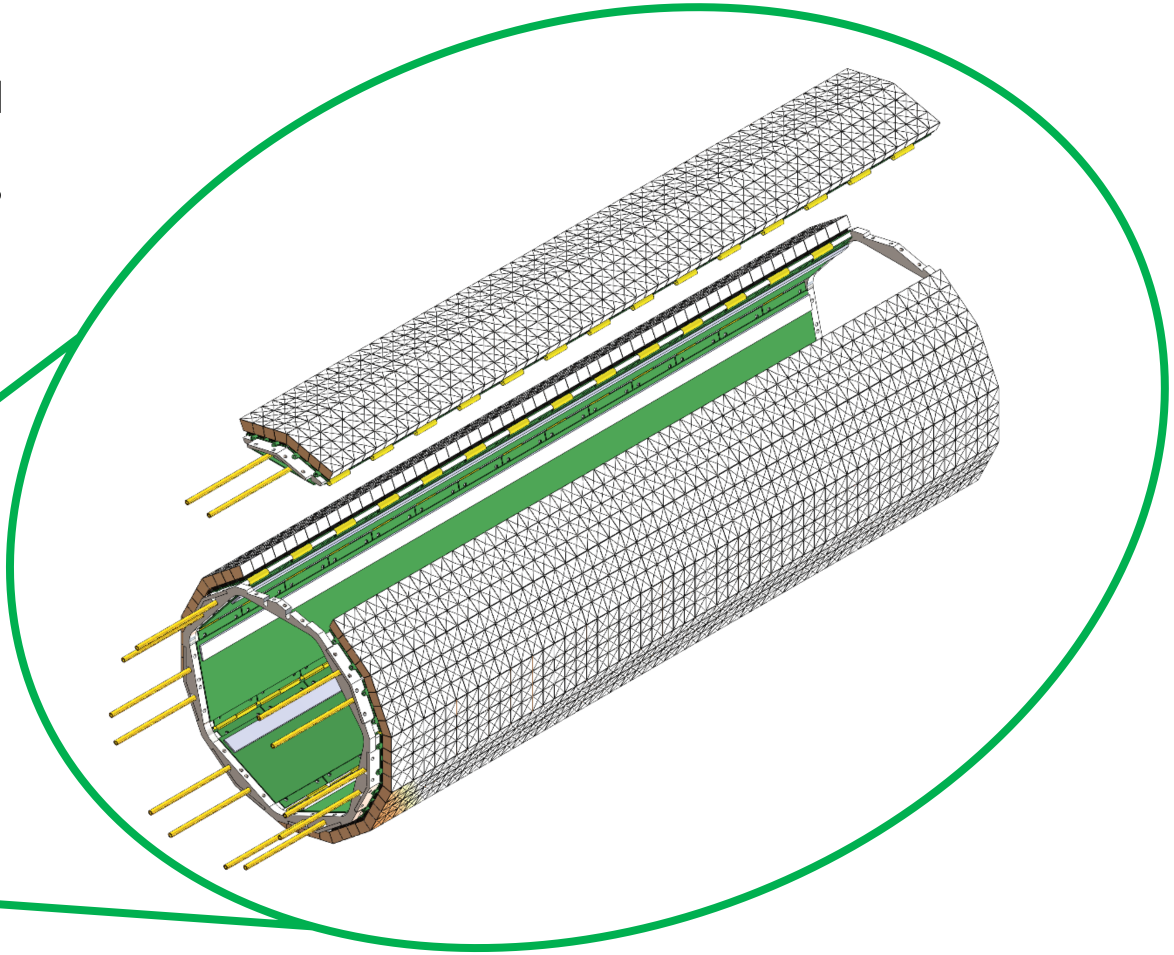
→ resulting base-unit: **submodule**
  - 32 channels (tiles + SiPMs)
  - custom-designed PCB with flex-print
  - two tile types: centre and edge



From submodule to module to full detector

- **module**: 14 submodules assembled on aluminium support/cooling structure
  - water-cooled
  - read-out of all 14 ASICs by one long mezzanine board
- **full detector**: 7 modules assembled on two endrings
- Mu3e phase I: two detectors in recurl stations





Technical prototype

Prototype production

- first technical prototype: **three submodules**
  - two submodules assembled on detector cooling structure
  - one additional submodule on custom-made cooling block (serving as reference during testbeam)
- to produce one submodule, we need:
  - assembled PCB (SiPM, ASIC, components) → electronic workshop
  - two types of tiles cut to the desired dimensions
  - reflective foils for tile wrapping

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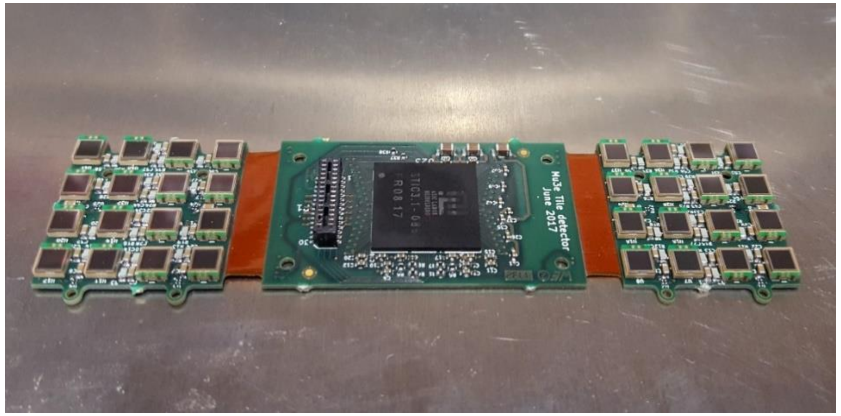

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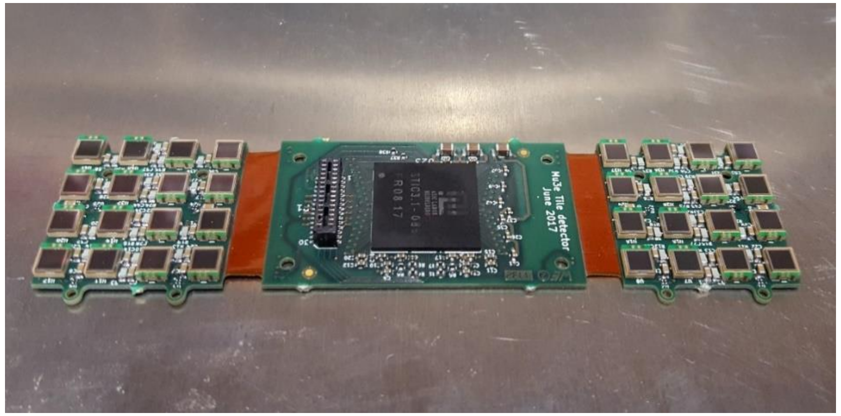

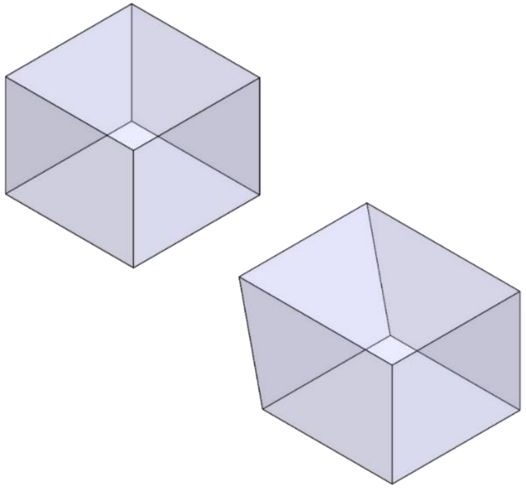

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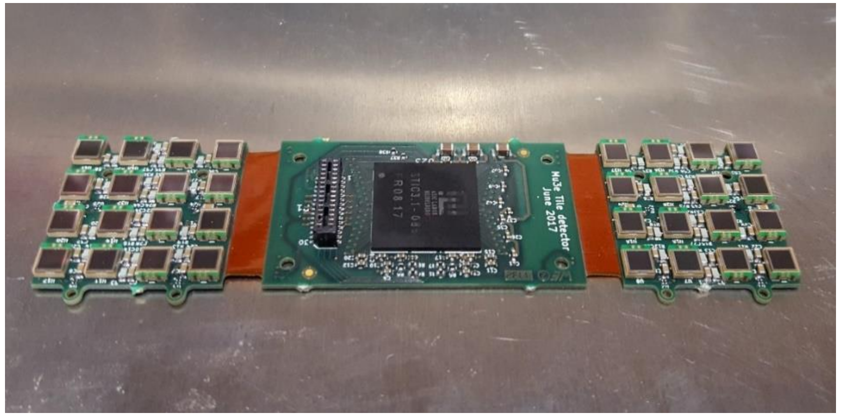
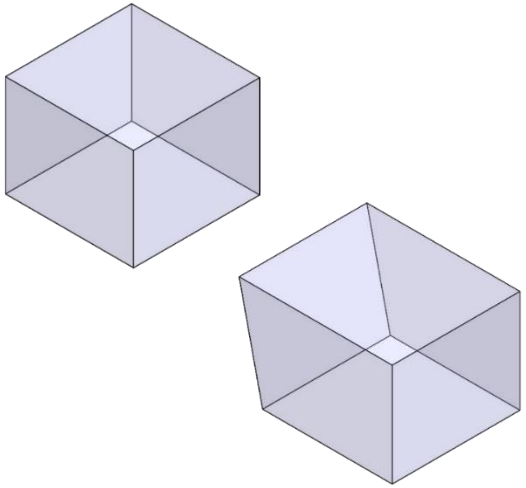
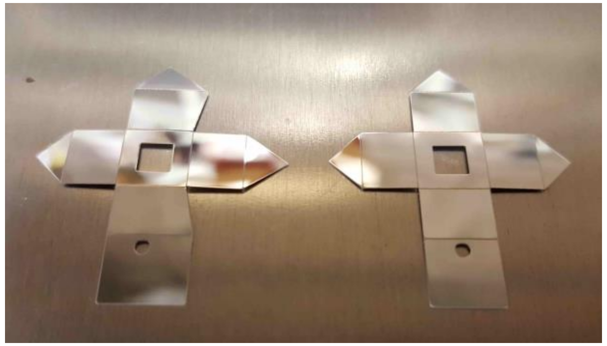


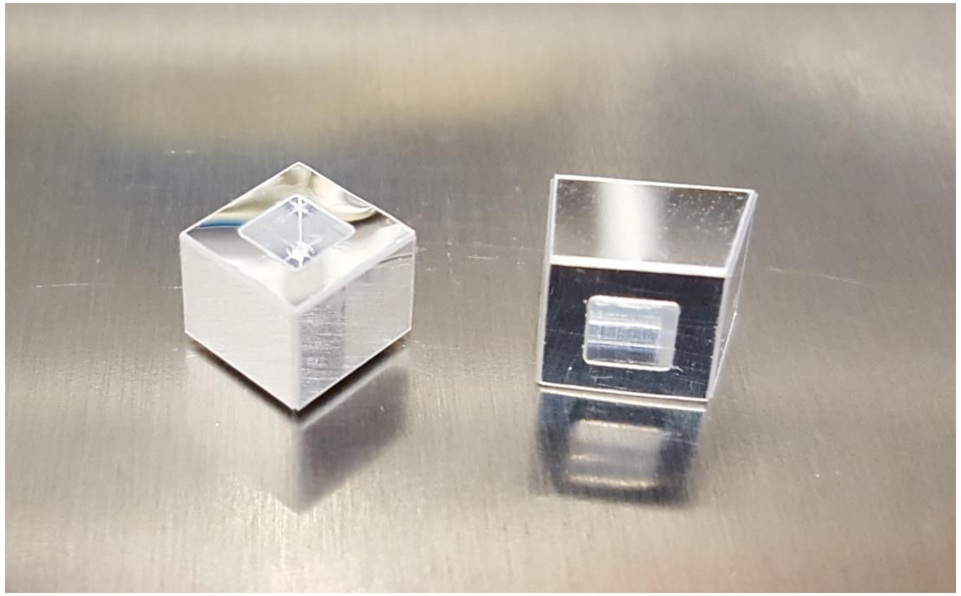


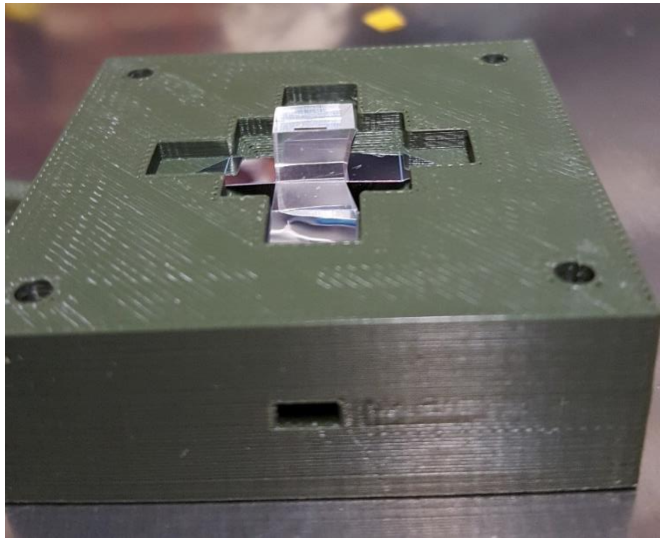


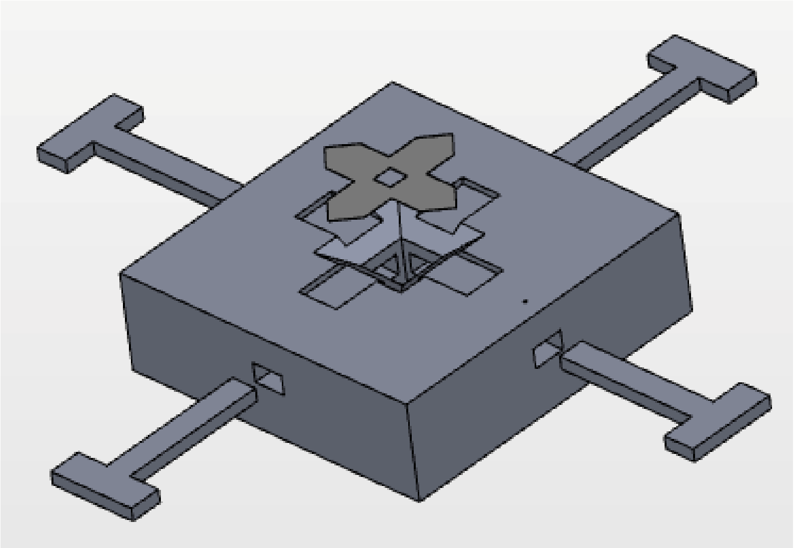
Tile wrapping

- wrapping of tiles with reflective foil to reduce optical cross-talk
- wrapping tool design using CAD software

  → 3D-printed

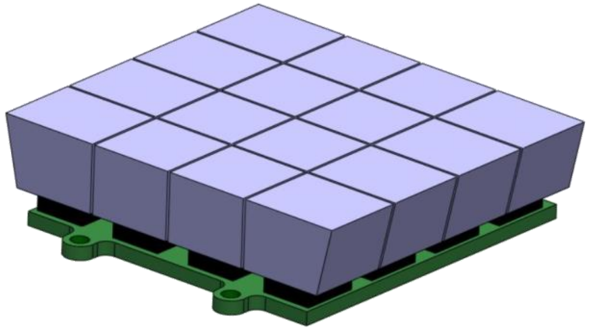






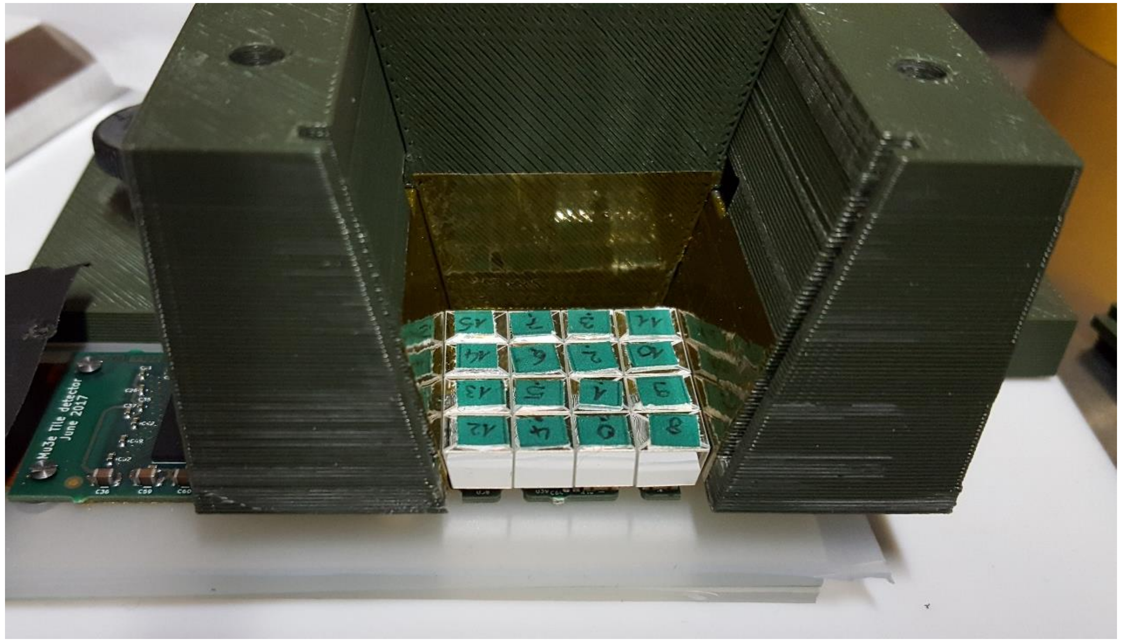
Gluing the tiles to the SiPMs

- need to attach tiles to SiPMs → light-transmitting glue
- some things to consider:
  - small tolerances (200 µm between tiles, without foils)
  - glue curing time of the order of a day
  - avoid bubbles → once tile is glued, it must not be moved (up) again

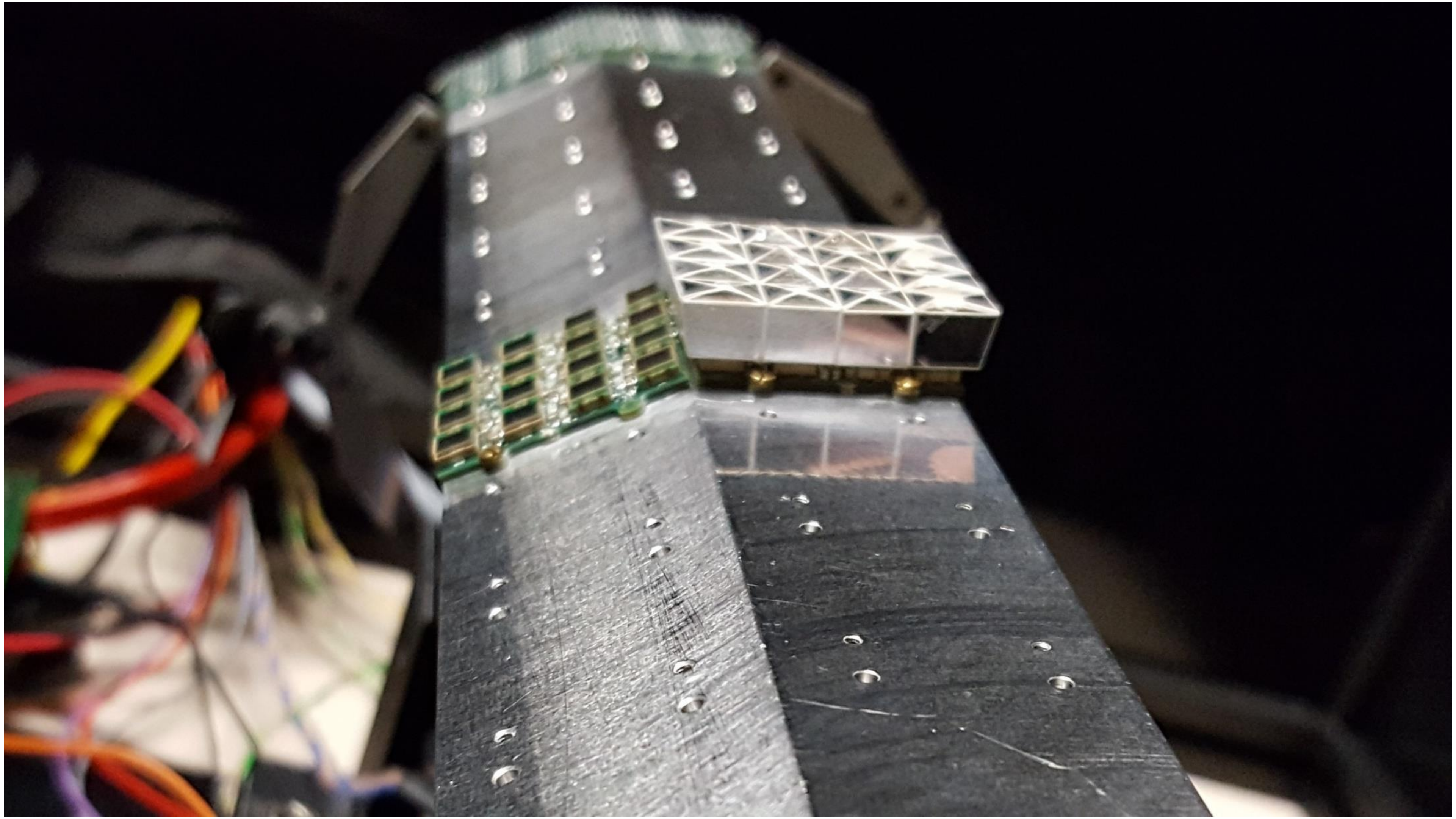


→ glue full tile matrix (4 x 4 tiles) all at once

→ dedicated 3D-printed tool

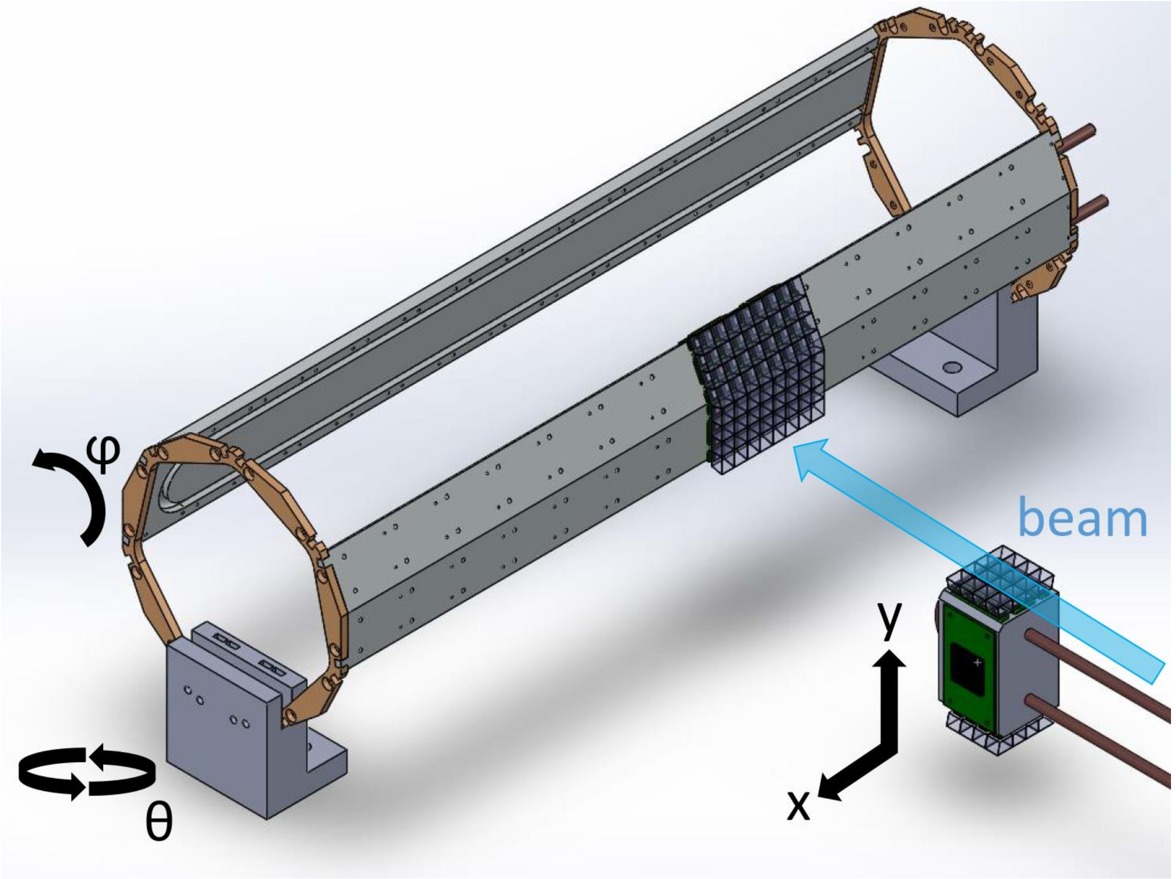


Assembled submodule with one tile matrix



Testing the technical prototype at DESY

- two testbeam campaigns in 2018 (February and June/July)
- measuring/testing:
  - general functionality of the technical prototype
  - calibration/optimisation (w.r.t. timing performance)
  - data acquisition
  - time resolution



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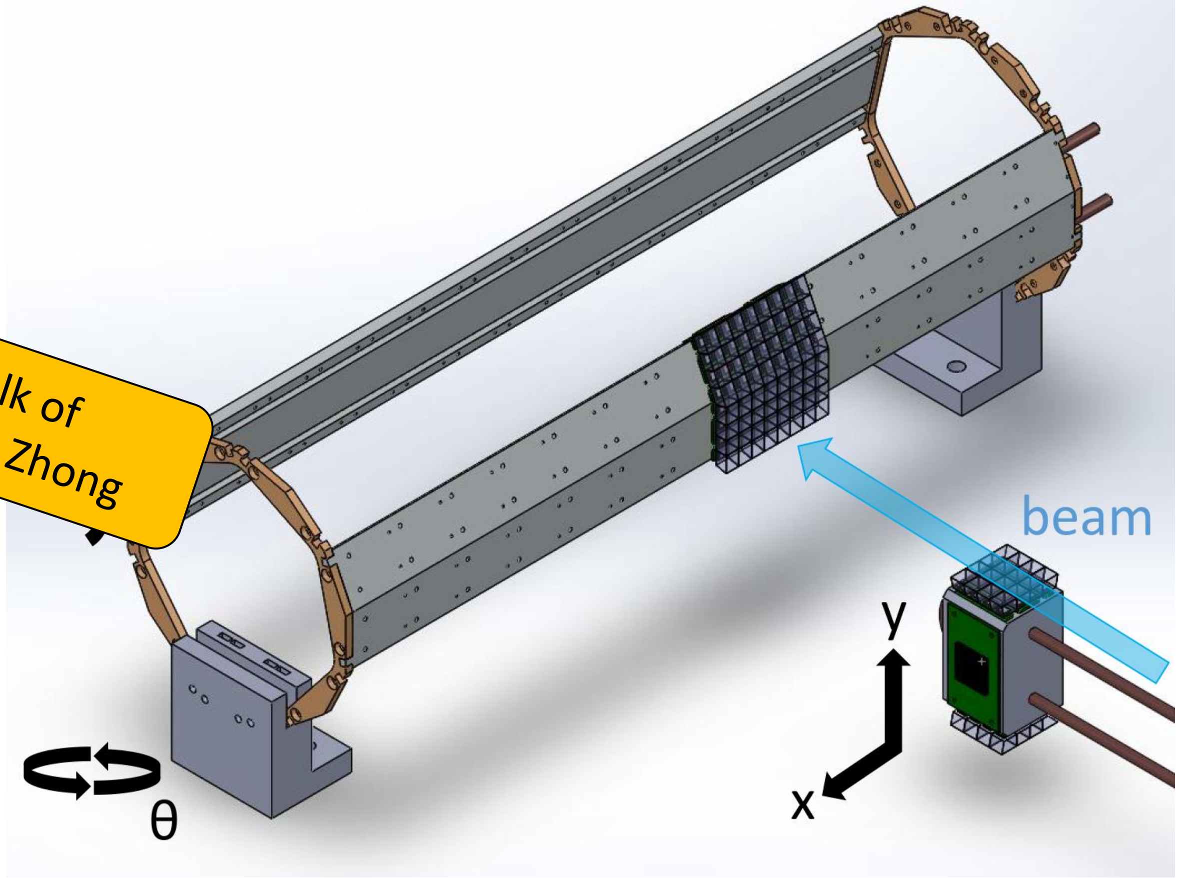
↓

average single channel timing resolution: ≈ **47 ps**

See talk of Tiancheng Zhong

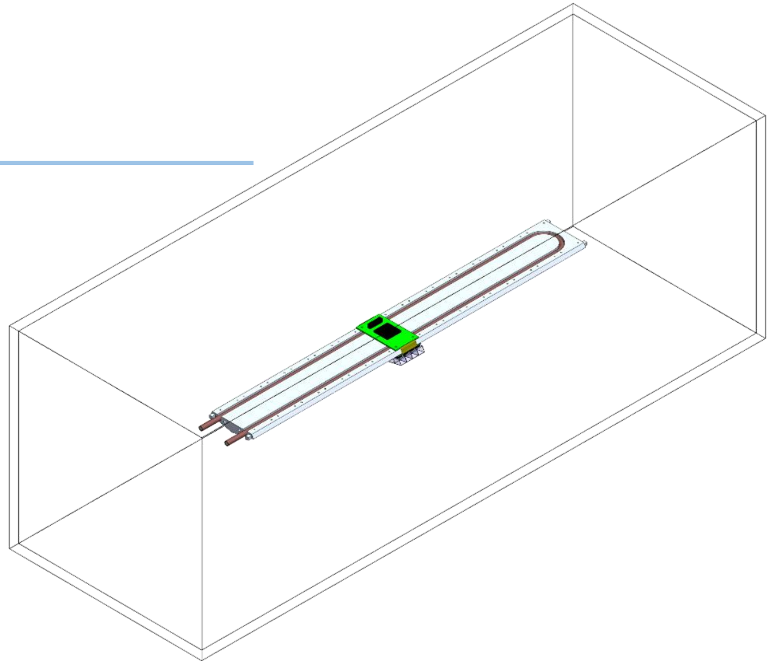


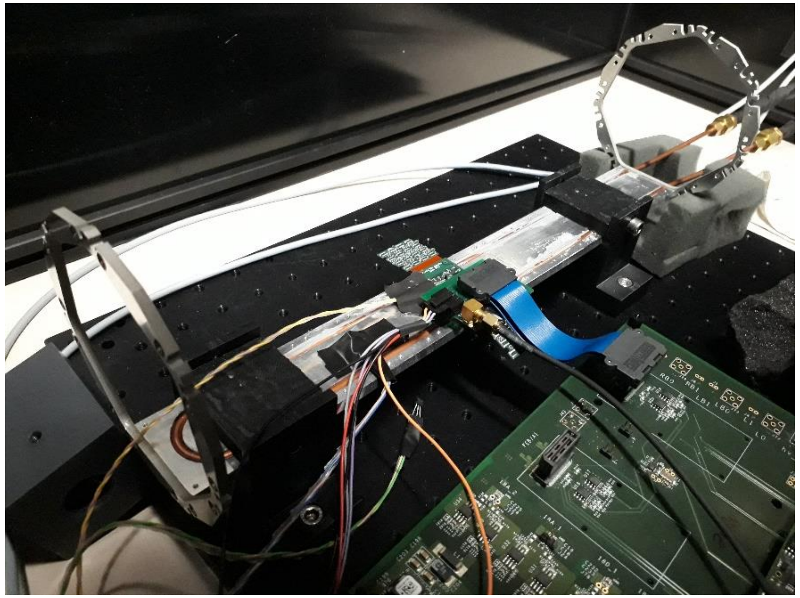
Thermal simulation

Thermal simulation concept

- CAD software also offers simulation add-ins
  → **flow simulation** (simulation of heat conductance, cooling system, water flow)
- idea: replicate prototype setup in simulation
- input from laboratory:
  - water temperature and volume flow
  - enviroment temperature
  - ASIC power consumption as heat source (3 different configurations)

→ comparison with lab measurements



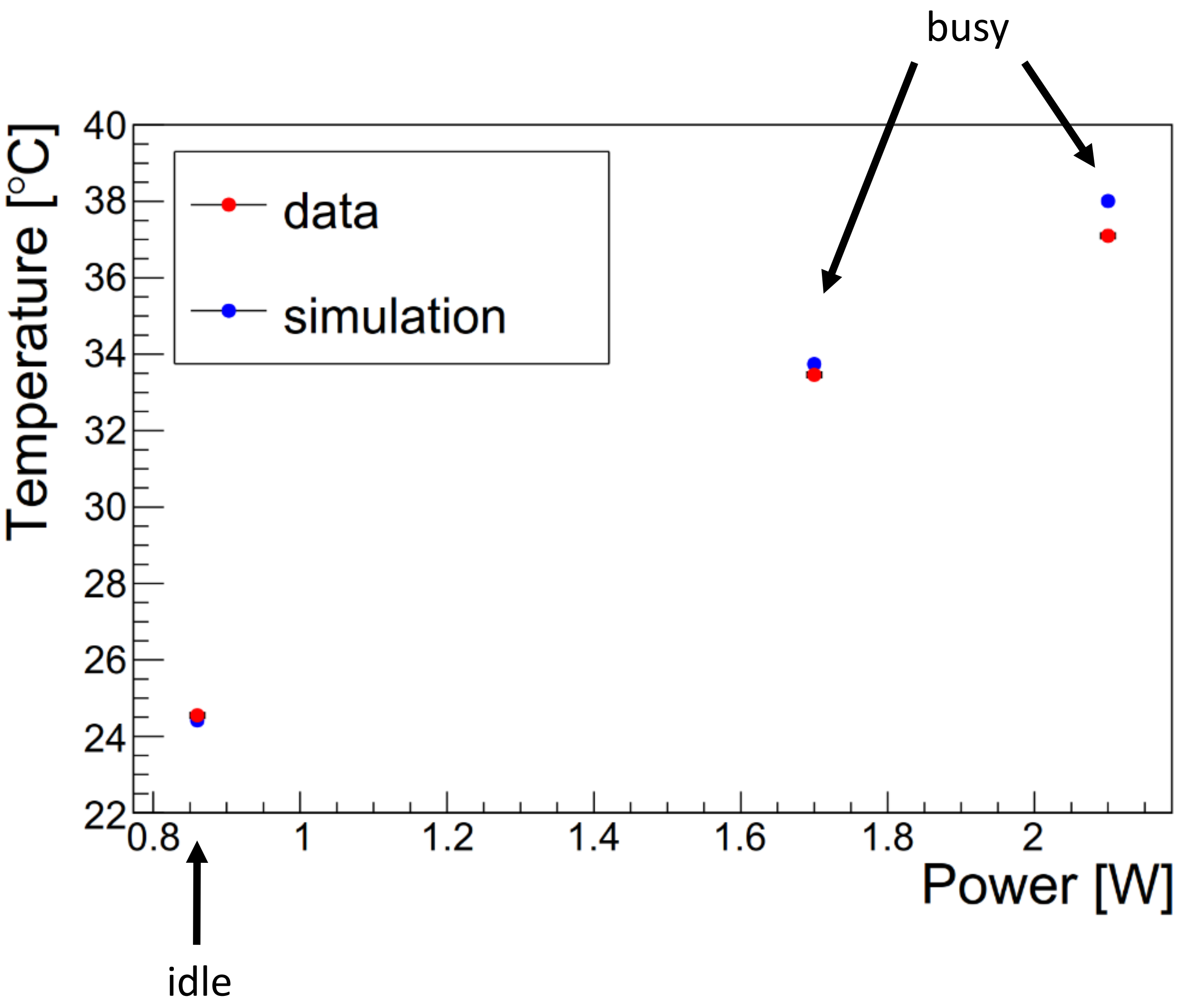


First results

- comparison of lab data and simulation
  - lab: temperature sensor on top of ASIC package
  - simulation: average temperature of sensor area
- good agreement of data and simulation

→ reliable simulation

→ can be enhanced and/or modified



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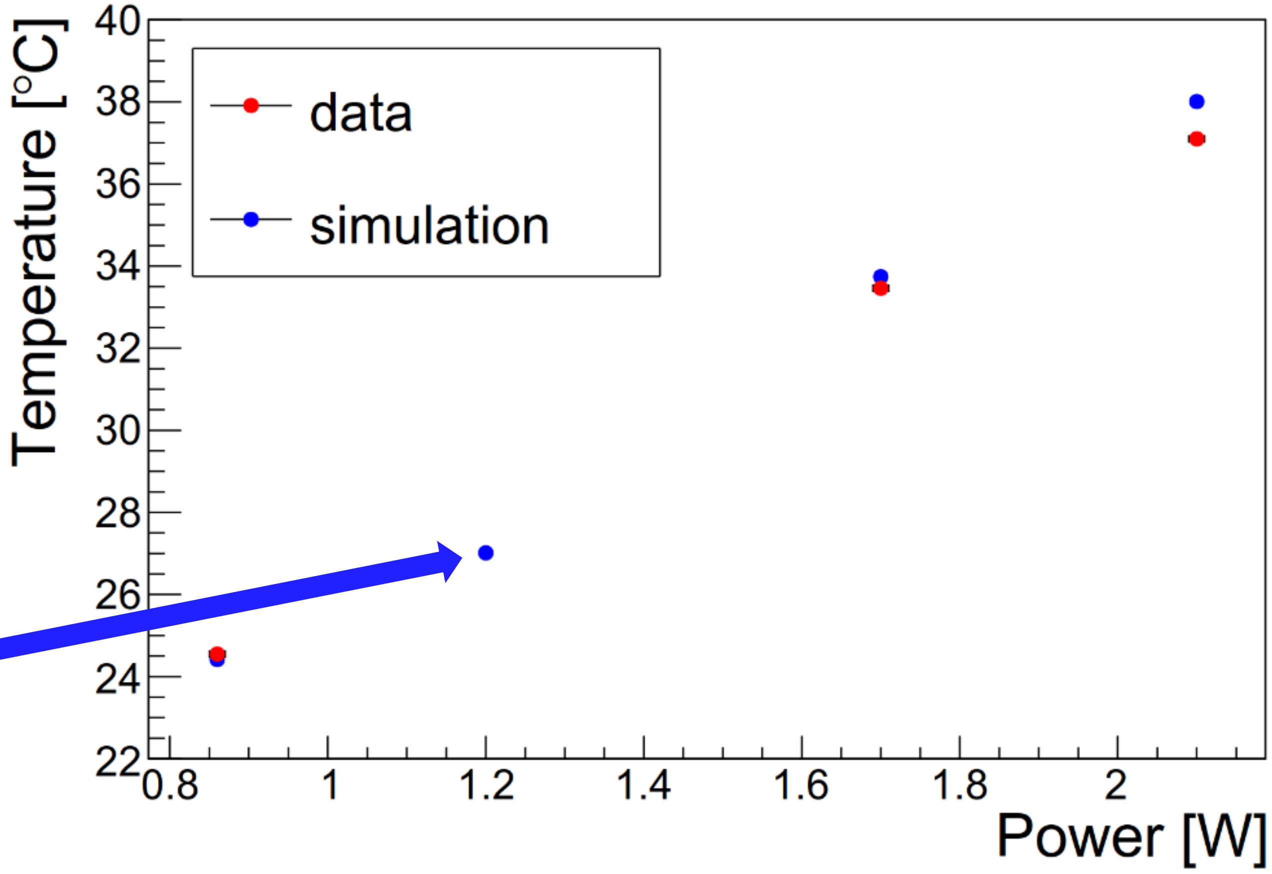
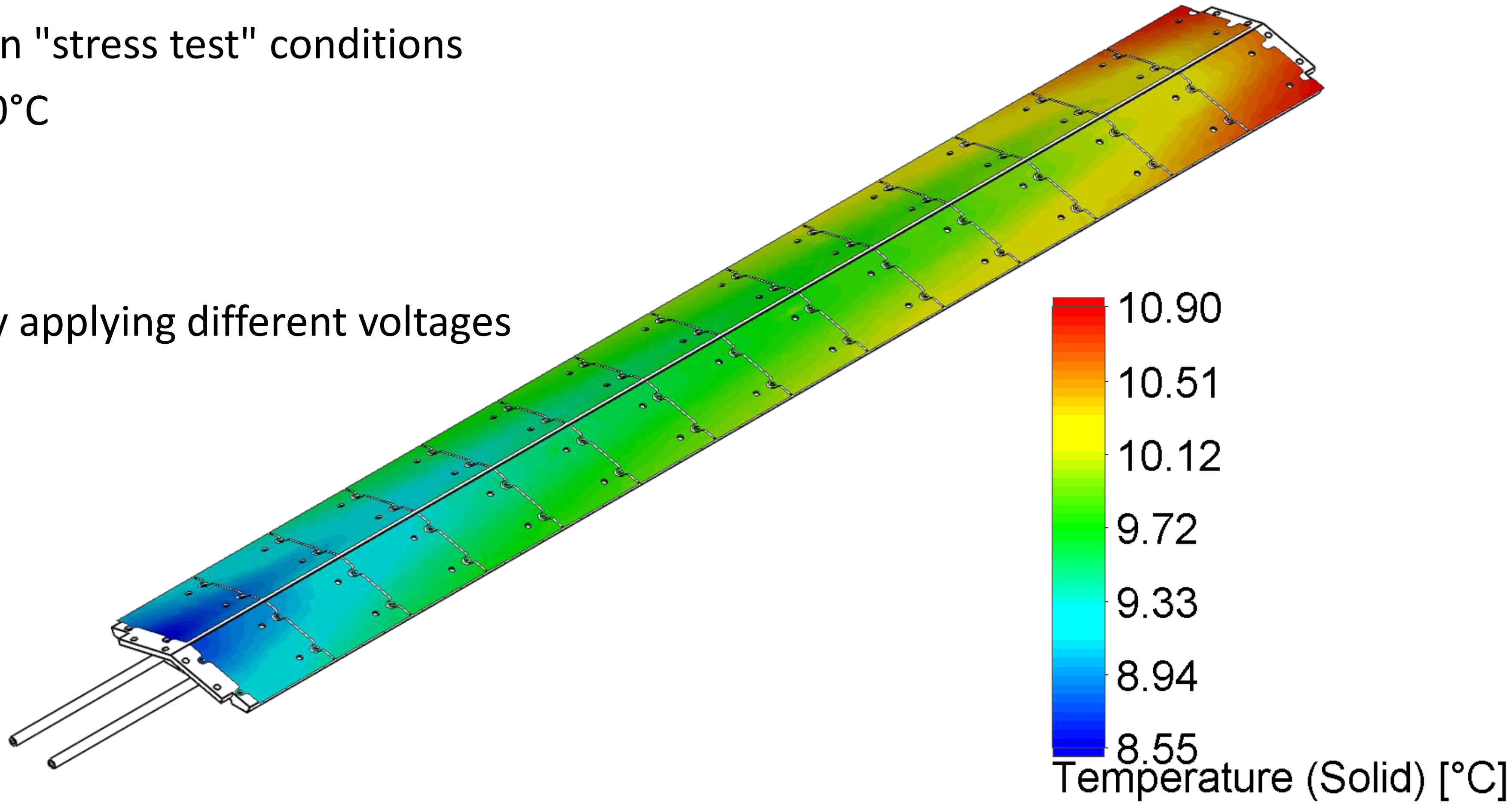
… e.g. to simulate power consumption expected during normal operation



Pre-study for experimental conditions

- SiPM performance depends on temperature
- shown here: SiPM PCBs in "stress test" conditions
  - → environment: T = 50°C
  - → water: T = 1°C
- temperature range ~ 2°C
  - → could be adjusted by applying different voltages



Summary and outlook

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- tile detector prototype is fully functional
  - production and assembly procedures developed
  - cooling system tested
- testbeam results show excellent timing performance well below requirement of 100 ps
- thermal simulation provides insights into cooling performance

next steps:

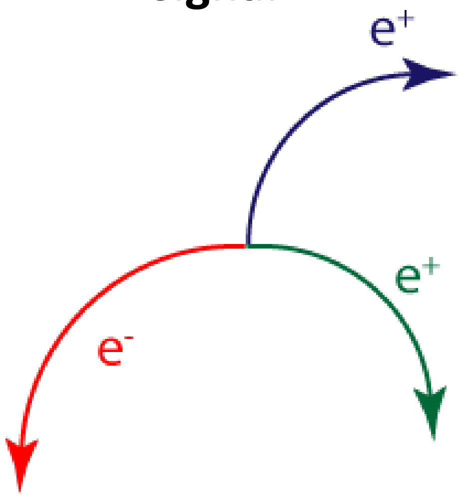
- assembly line for submodule production
  - must be easy to operate, yet precise (alignment)
  - also need to think about quality assurance procedures
- enhancement of thermal simulation
  - implement expected environment of the Mu3e experiment

Appendix

Tile detector requirements

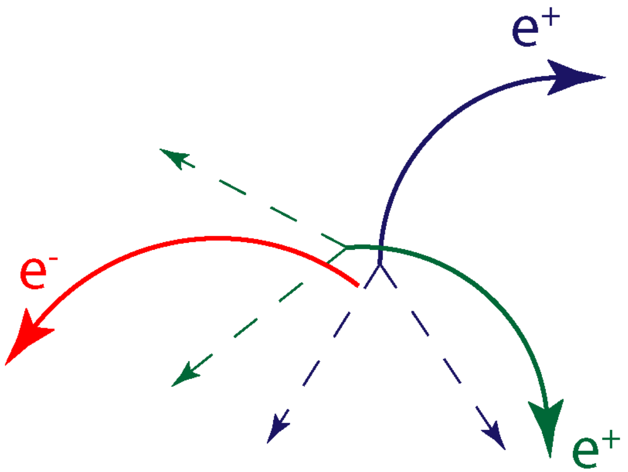
- suppression of combinatorial background
  - e.g. Michel decays + scattered electron, Michel decay + internal conversion, …
- requires 100 ps timing resolution at close to 100% efficiency
- maximum rate: 60 kHz per channel

signal



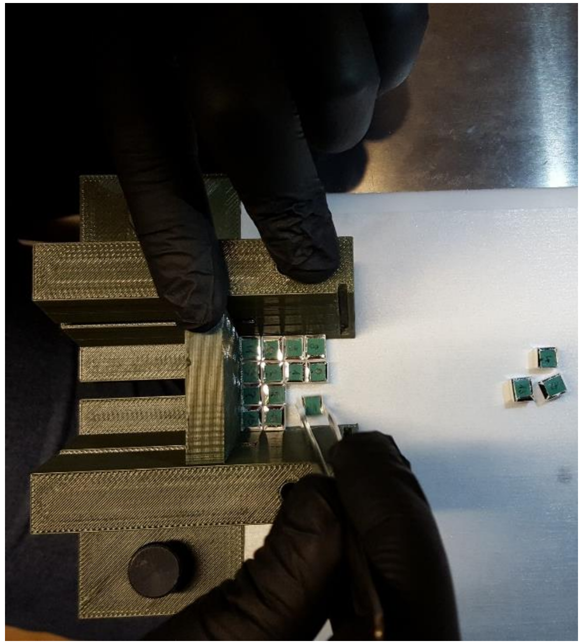
$\sum E_e = m_\mu,\ \sum \vec{p}_e = \vec{0}$

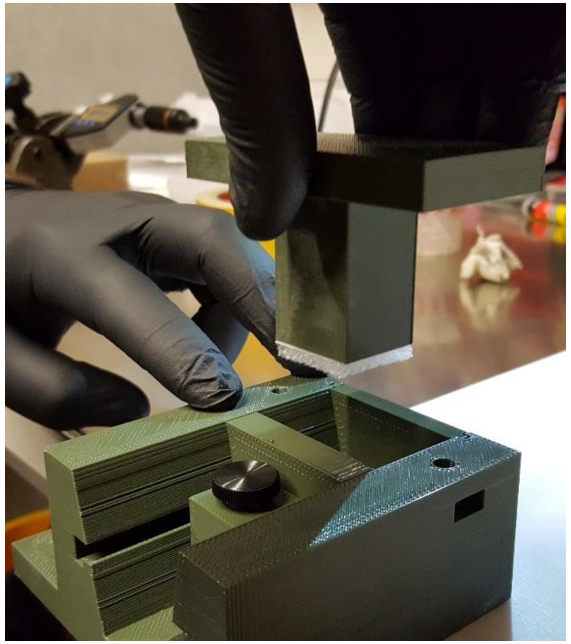
combinatorial background

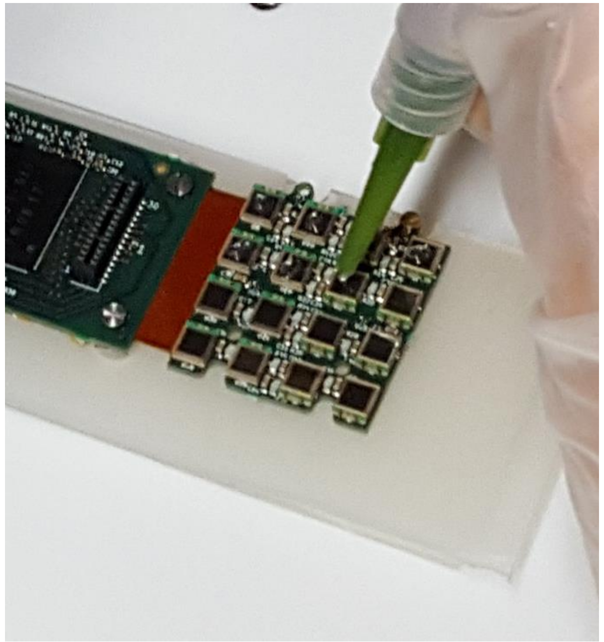


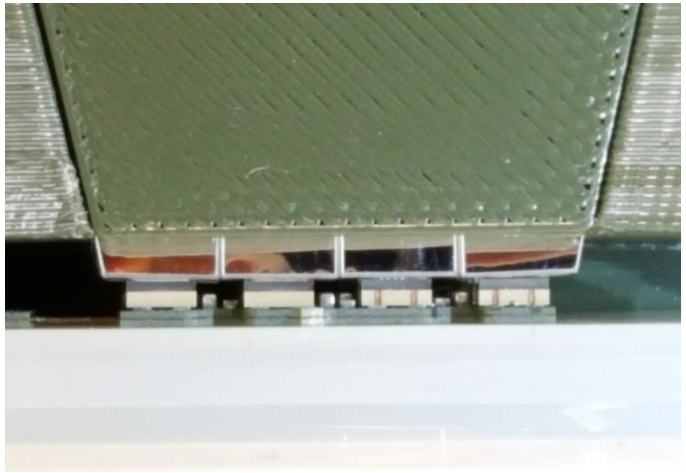
$\sum E_e \neq m_\mu,\ \sum \vec{p}_e \neq \vec{0}$

Gluing procedure









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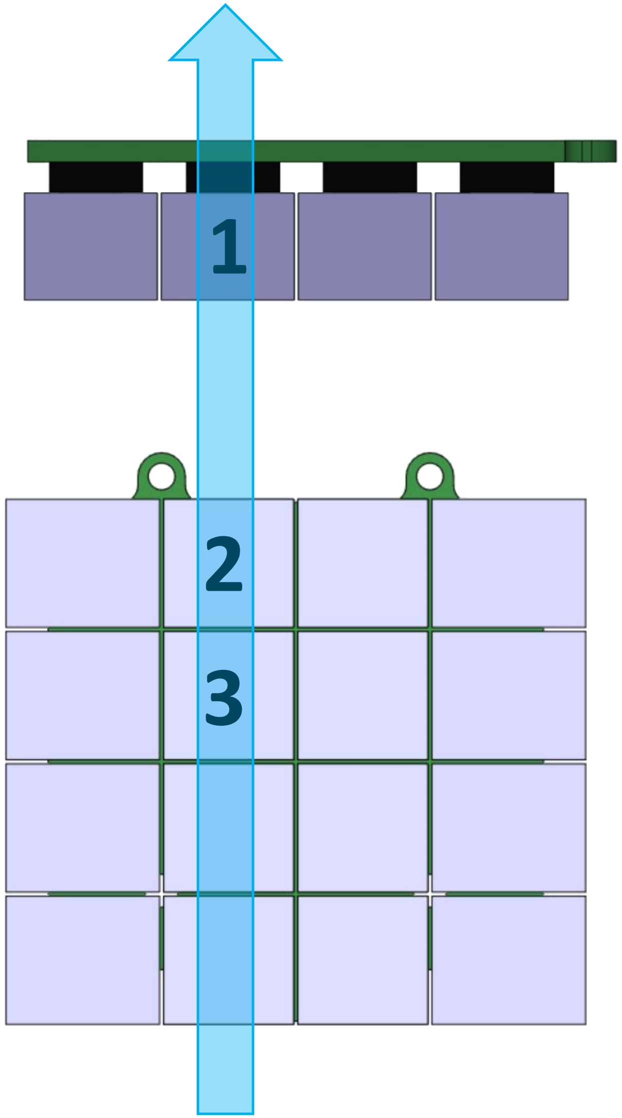
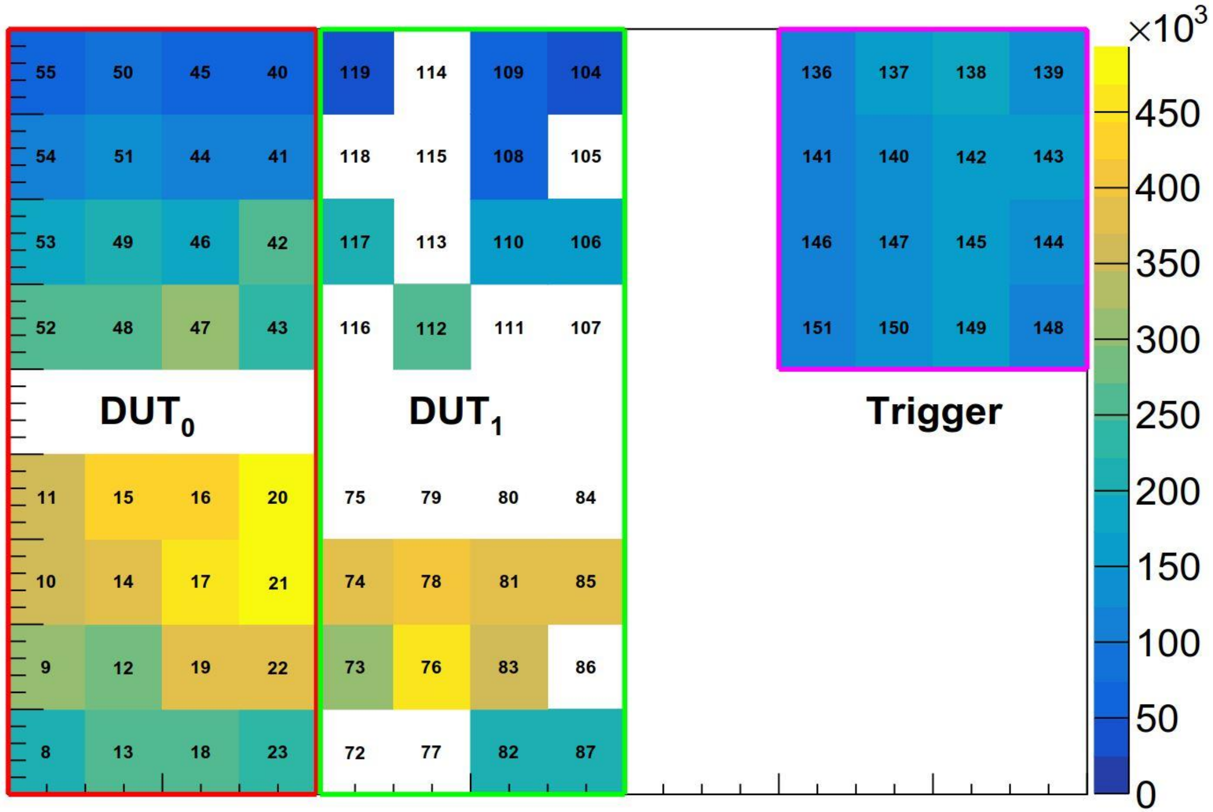
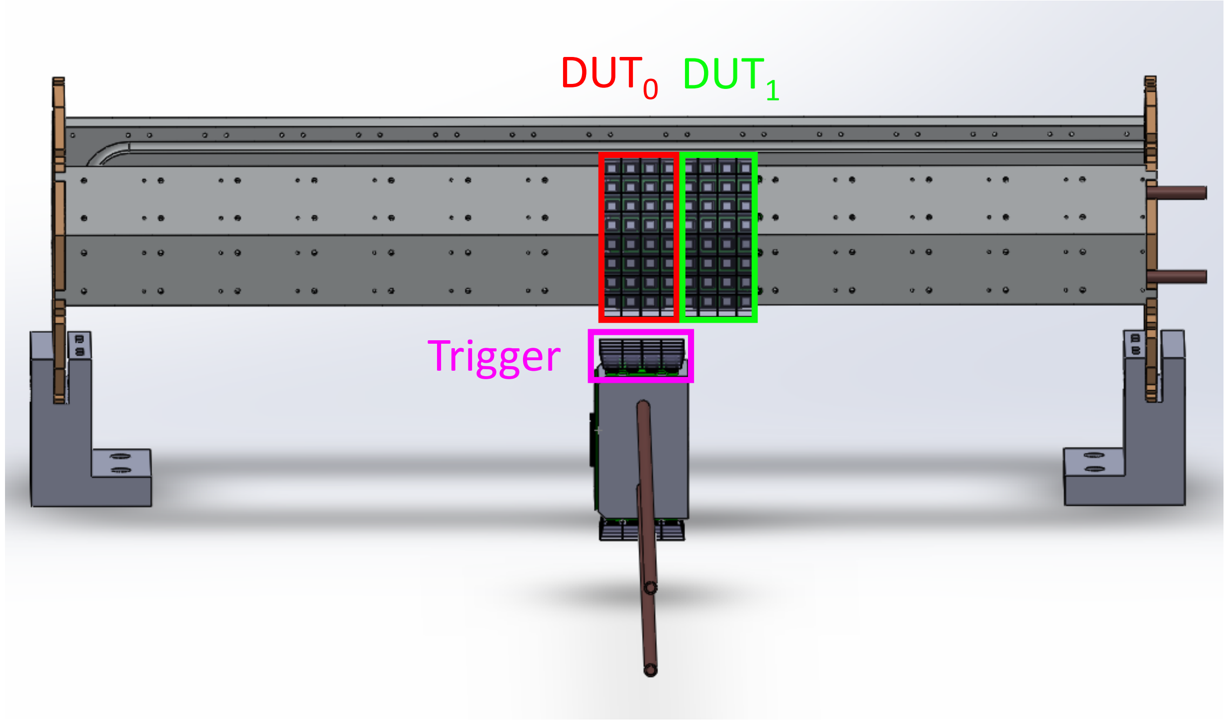


Channel hitmap





- DUT$_0$ fully functioning (32 channels)
- DUT$_1$ only partially recovered → only limited time available
- All trigger channels working (only one matrix used)

Single-channel timing resolution

See talk of Tiancheng Zhong (→T94.2)

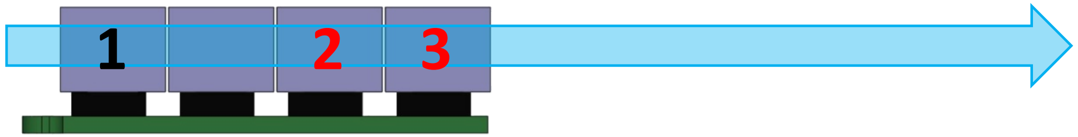
- coincidence time resolution (CTR):

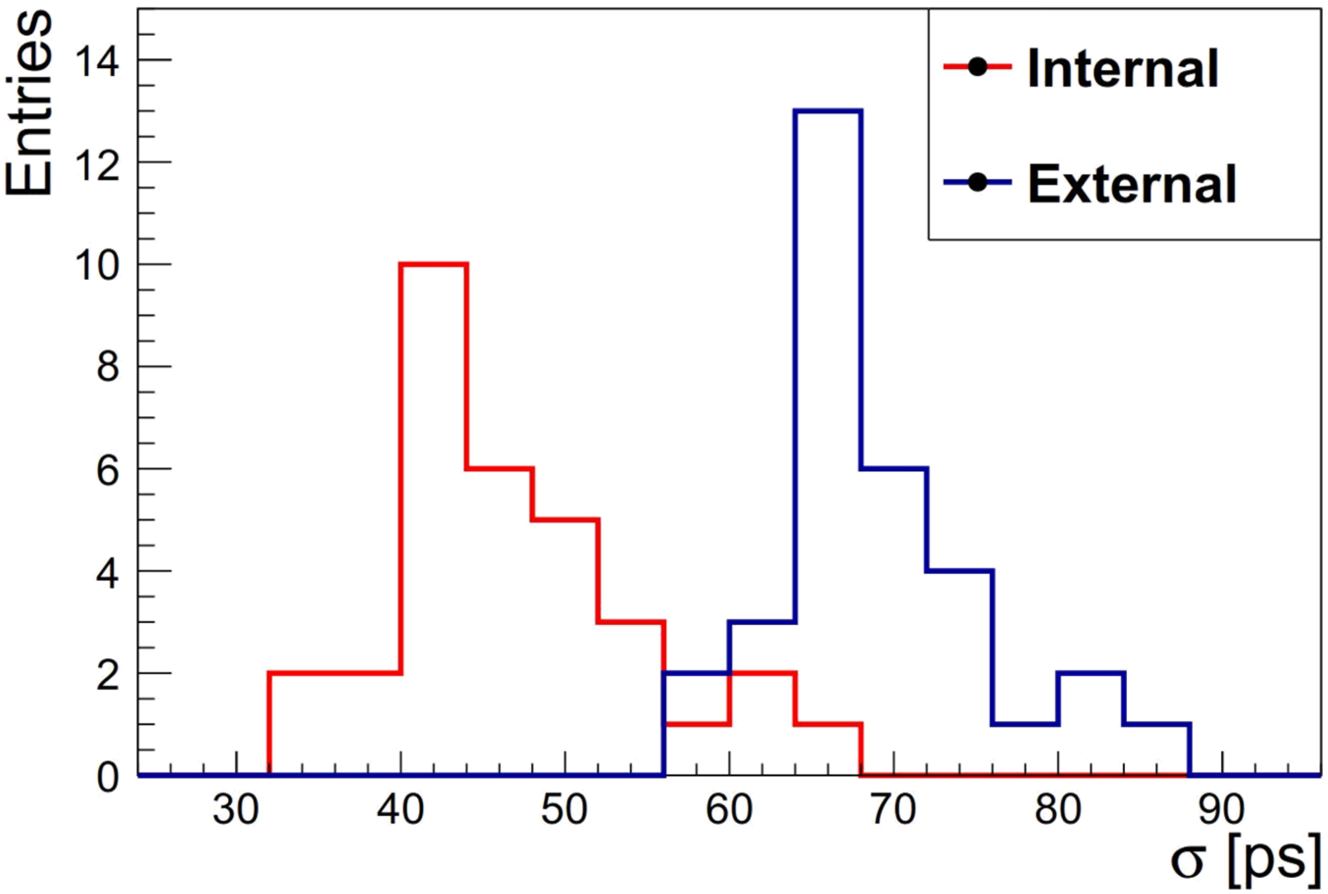
$$\sigma^2_{ij} = \sigma^2_i + \sigma^2_j$$

- single channel resolution using three channels 1, 2, 3:

$$\sigma_1 = \frac{1}{\sqrt{2}}\sqrt{\sigma^2_{12} + \sigma^2_{13} - \sigma^2_{23}}$$

- internal timing resolution: ≈ 46.8 ps





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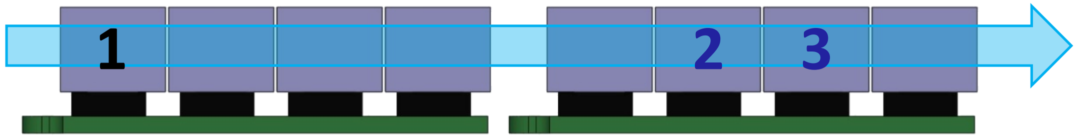
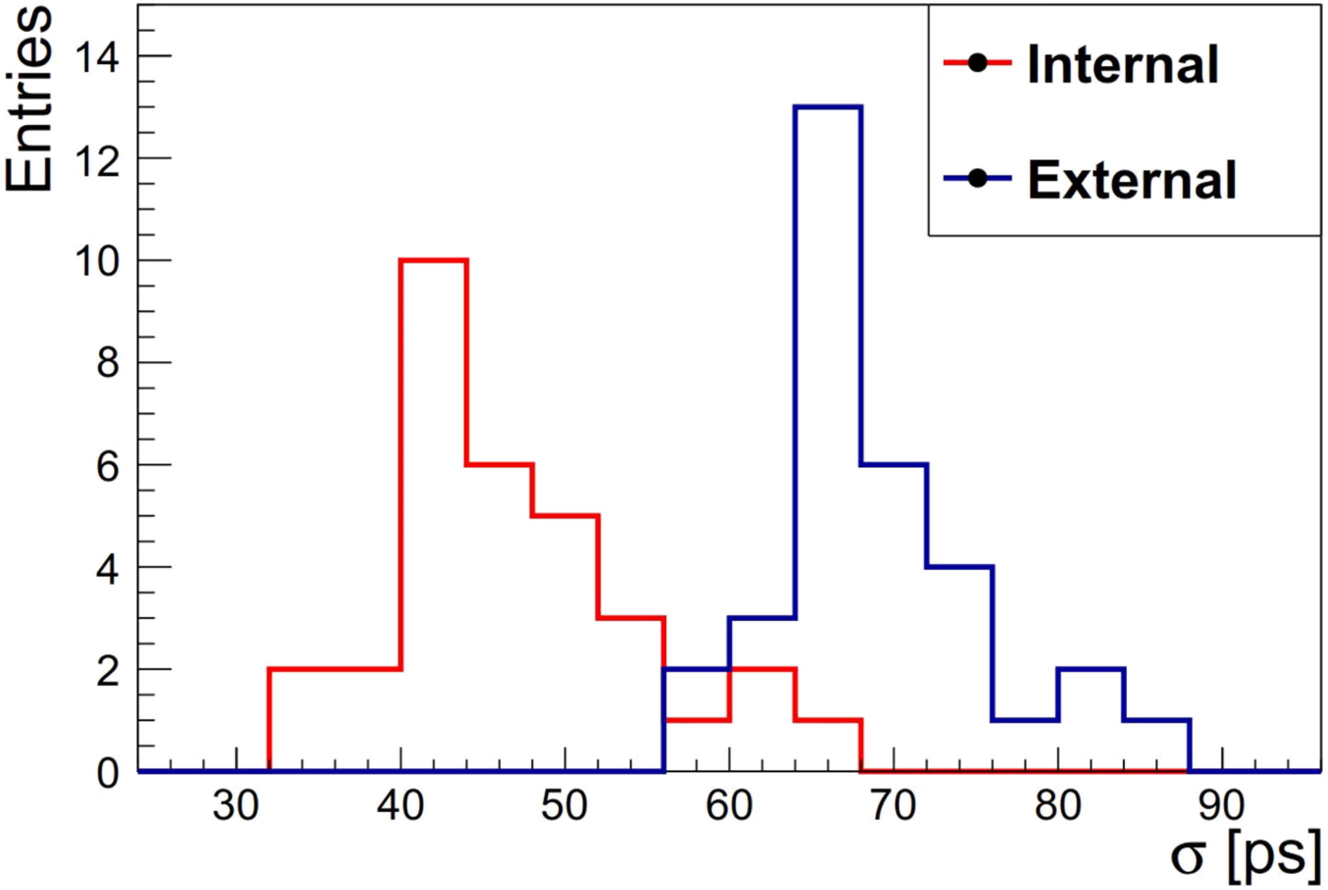
- external timing resolution: additional jitter of the order of 50 ps





Time-over-threshold spectrum

See talk of Tiancheng Zhong (→T94.2)

- different contributions to ToT spectrum
  - → blue: particle fully traversing the tile
  - → red: crosstalk
  - → green: particle grazing tile