On the Path to Module Integration with the HV-MAPS prototype MuPix9



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The Mu3e Detector





- Search for $\mu^+ \rightarrow e^+e^-e^+$
- 10⁹ decays per second
- $p_{max} = m_{\mu}/2$
- Multiple Coulomb Scattering
- Good vertex and time resolution (100 µm & 500 ps)
- Good momentum resolution (0.5 MeV)

The Mu3e Detector

Pixel detector requirements:

Pixel Size	Time Resolution	Material Budget	Efficiency
80 x 80 µm ²	< 20 ns	0.1% X ₀ /layer	> 99 %

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High Voltage - Monolitic Active Pixel Sensors



- Low ohmic substrates (10-200 Ωcm)
- High voltage > 100V
- Deep N-well diode
- ~ 30 µm depletion
- Charge collection via drift

- In-pixel electronics
- Monolithic design: Detection and Readout combined in one chip
- Commercially available processes: AMS 180nm TSI 180nm
- Chips are thinned to 50 µm

The Road Map to the Mu3e Pixel Chip MuPix8



Detector Integration

The Road Map to the Mu3e Pixel Chip MuPix8



Detector Integration

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The MuPix9 Chip



Standalone Slow Control Statemachine

- AMS aH18 (MPW)
- 20 Ωcm substrate
- Test of new NMOS in-pixel
 amplifier
- Test of serial powering infrastructure: shunt regulator
- Slow control statemachine

The MuPix9 Chip



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MuPix9 – Pixel Matrix



- Pixel matrix is fully functional
- Breakdown at -60V reverse bias (design -120 V)
- Performance out-of-the-box: Time resolution: $\sigma < 9$ ns Efficiency: ~86 %

MuPix9 – NMOS amplifier





MuPix8 PMOS Amplifer 80 Ωcm

- Efficiency reduced by resistivity 80 → 20 Ωcm
- Limited by noise
- PMOS amplifier is preferred

MuPix9 - Requirements for Module Integration



- Ultra-low material design (0.1% X₀)
- Powering, configuration and readout via a 2 layer aluminum flexprint
- Up to 9 chips per flexprint
- Power distribution is challenging \rightarrow minimisation of per chip signals

Flexprint Constraints



- 12 differential lines per flexprint
- Use bus for common signals
- → 1 differential bus for slow control (SIN)
- MuPix8 shift register requires 5 inputs



MuPix9 - Slow Control Statemachine



- Synthesized verilog code
- I²C like protocol
- Slow control data parser
- 32 bit data words:
 4 bit chip address (bus)
 4 bit command
 24 bit payload

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- Synthesized verilog code
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- 32 bit data words:
 4 bit chip address (bus)
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 24 bit payload
- Broadcast: synchronous reset

MuPix9 – Synchronous Reset





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IN				\int		syn	c reset									
slow clk1	 			1				1								
slow clk2																
slow clk3						ΓL								l		

- Phase of the state machine clock undefined on power up
- Synchronisation to control FPGA
- Synchronisation of all chips on the bus
- Successfully tested in the lab

Summary and Outlook



- First step towards module integration
- MuPix9 is in the lab
- Focus on slow control
- Expansion of the MuPix9 slow control interface:
 - 64 bit input
 - more broadcast commands
- → Crucial input for MuPix10

Thank you!

Questions?

On-chip Power Domains



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