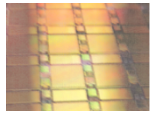
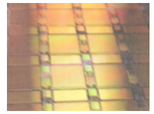
Seminar, February 22, 2018



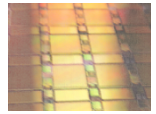
The ALICE ITS (Inner Tracking System) Upgrade – Monolithic Pixel Detectors for LHC

Petra Riedler, CERN EP-DT

Outlook

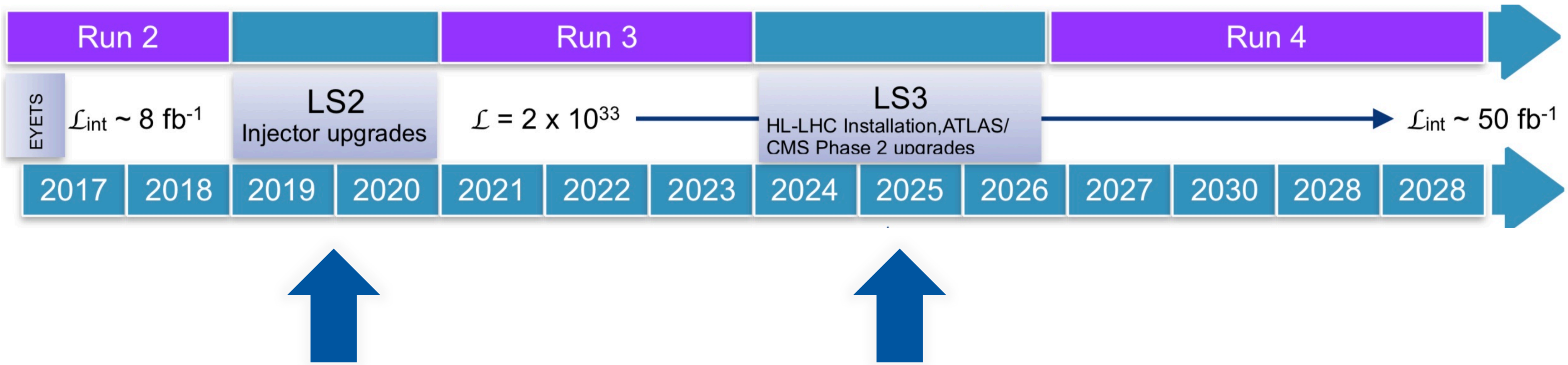


- Introduction
- Pixel detectors - hybrid and monolithic
- Examples of monolithic pixel detectors in HEP
- The ALICE ITS
- Future developments
- Summary



We live in interesting times…

…for silicon detectors



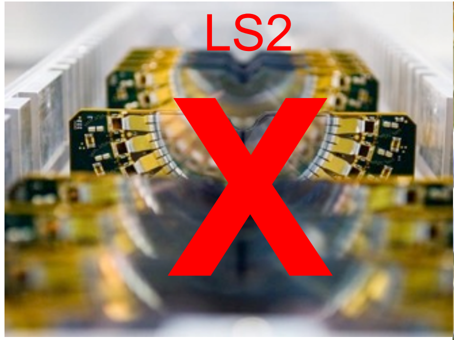
ALICE LHCb

ATLAS EXPERIMENT CMS

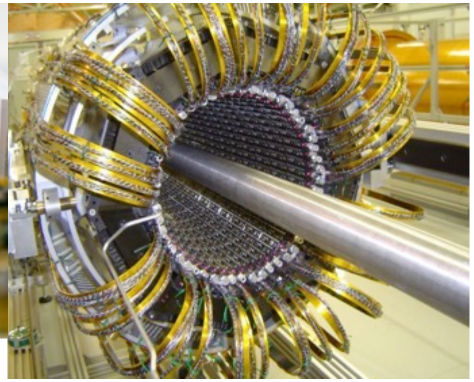
Silicon Tracking Detectors

- Complex systems operated in a challenging high track density environment
- Innermost regions usually equipped with pixel detectors

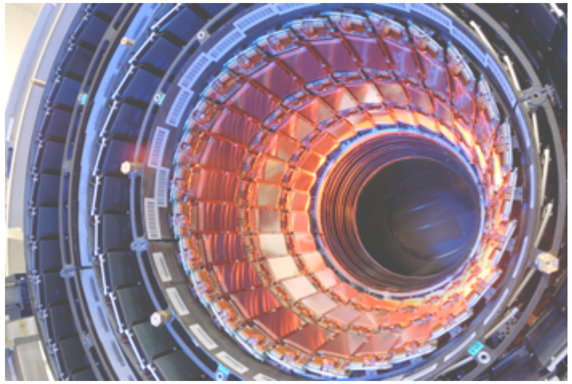
ALICE **Pixel** Detector



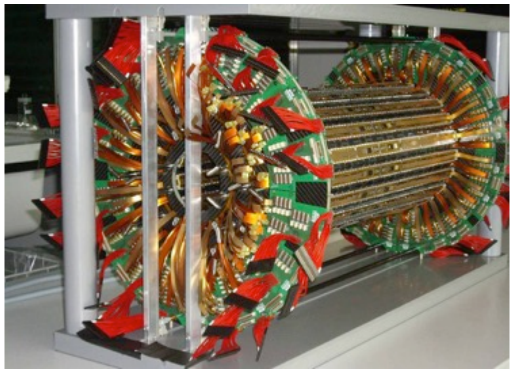
LHCb VELO



ATLAS **Pixel** Detector

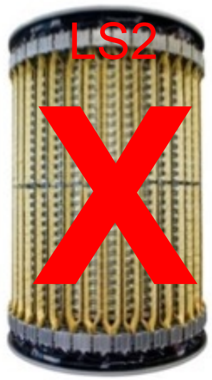


CMS Strip Tracker IB

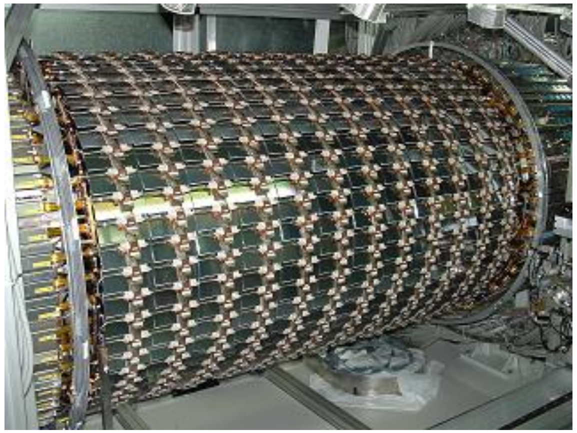


CMS **Pixel** Detector

ALICE Drift Detector

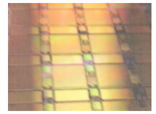


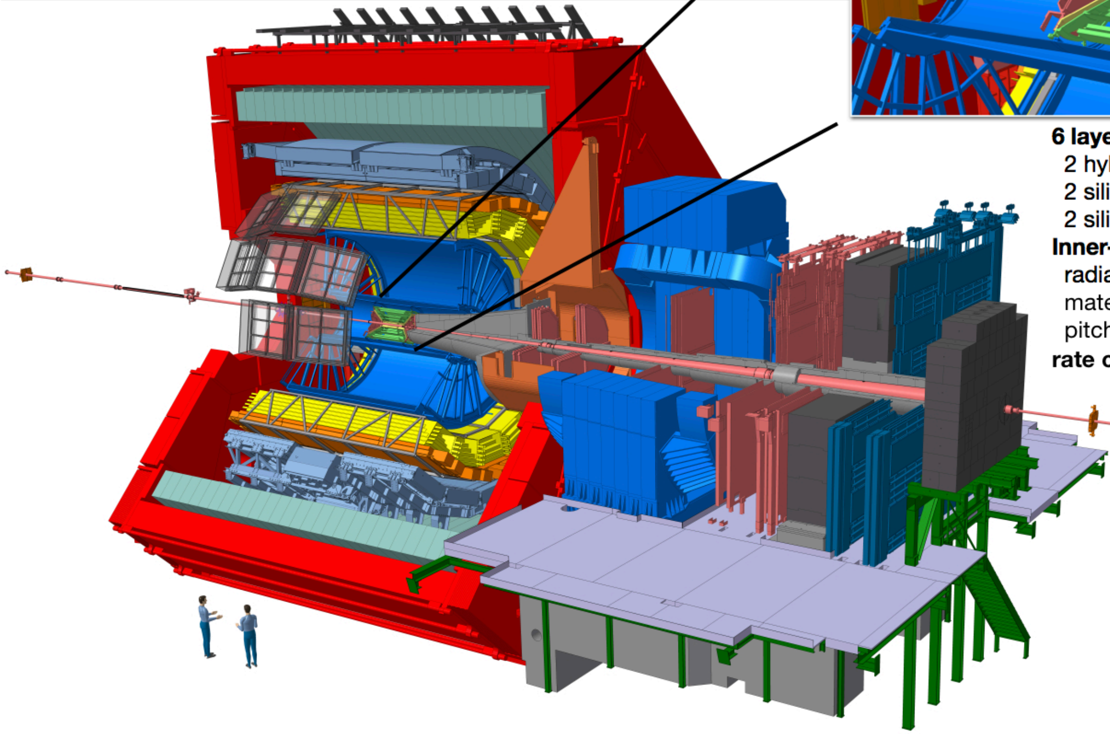
ALICE Strip Detector

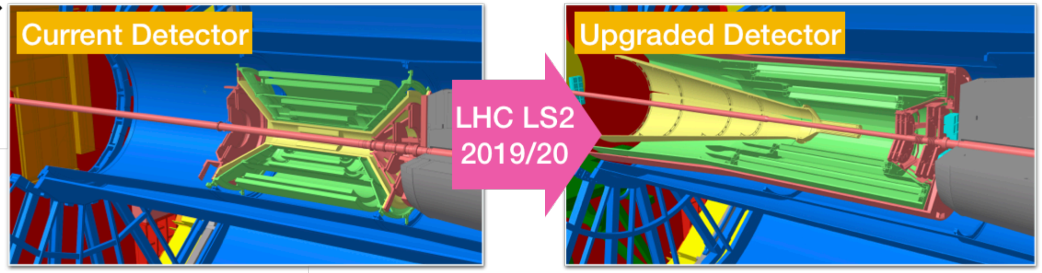


ATLAS SCT Barrel

ALICE Inner Tracking System







6 layers:
- 2 hybrid silicon pixel
- 2 silicon drift
- 2 silicon strip

Inner-most layer:
- radial distance: 39 mm
- material: $X/X_0 = 1.14\%$
- pitch: $50 \times 425\ \mu m^2$

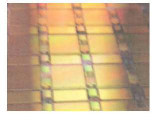
rate capability: 1 kHz

7 layers:
- all Monolithic Active Pixel Sensors

Inner-most layer:
- radial distance: 23 mm
- material: $X/X_0 = 0.3\%$
- pitch: $O(30 \times 30\ \mu m^2)$

rate capability: 100 kHz (Pb-Pb)

LoI: 2012
ITS CDR: 2012
ITS TDR: 2013

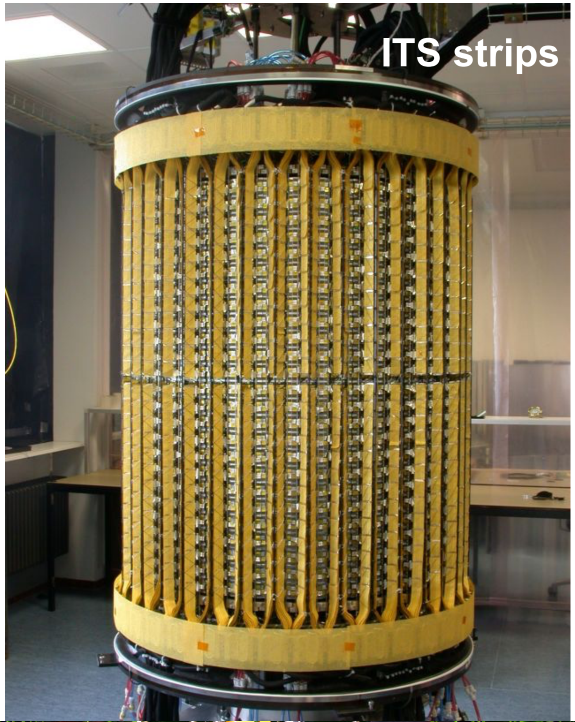


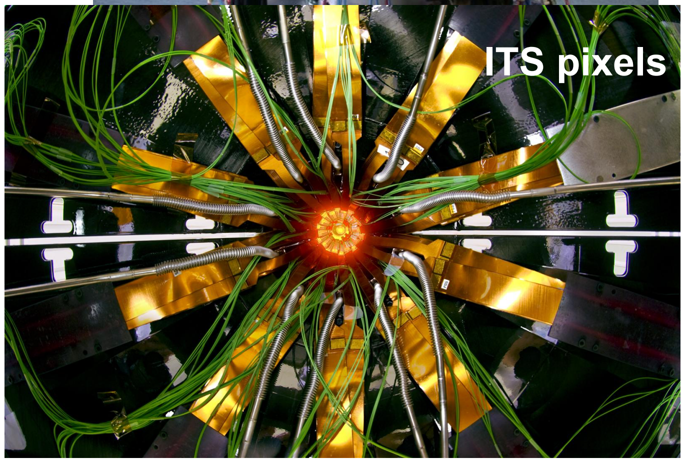
ALICE ITS upgrade

- Complete removal of the **present inner tracking system and installation of a new tracker based on monolithic silicon pixel** sensors (~ $10m^2$)

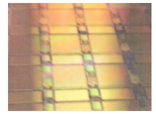
- **Change of technology** compared to the present system: hybrid pixels silicon drift, silicon strips → **monolithic CMOS sensors**

- **First use of monolithic pixel detectors in an LHC experiment.**

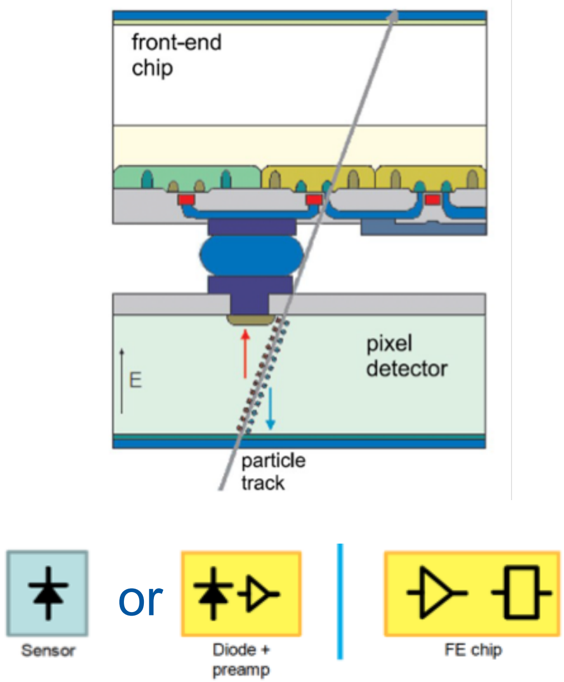


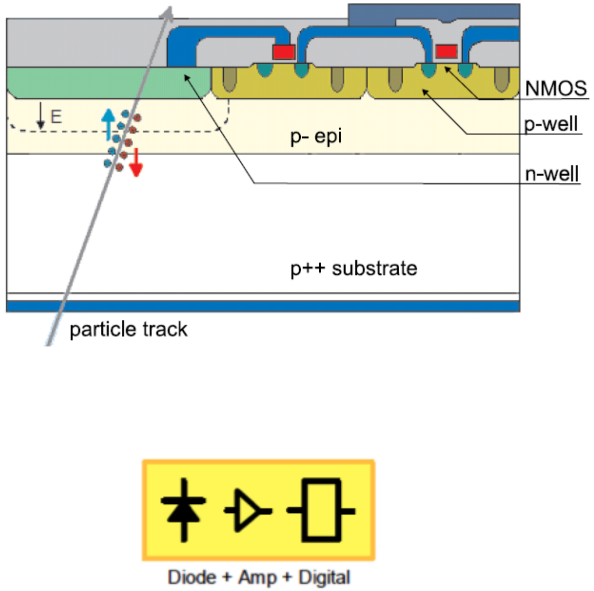


Pictures: CERN.http://cds.cern.ch/



Hybrid and Monolithic Pixels

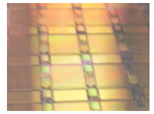




- Separately optimize sensor and FE-chip
- Fine pitch bump bonding to connect sensor and readout chip

- Charge generation volume integrated into the ASIC, but many different variants!
- Thin monolithic CMOS sensor, on-chip digital readout architecture

Hybrid Pixels



Offer a **number of advantages due to the split functionality** of sensor and readout:

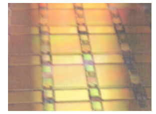
- complex signal processing in readout chip
- zero suppression and hit storage during L1 latency
- radiation hard chips and sensors to $>10^{15}$ n_{eq}/cm^2
- high rate capability (~MHz/mm^2)
- spatial resolution ≈10 – 15 µm

There are also **some other aspects:**

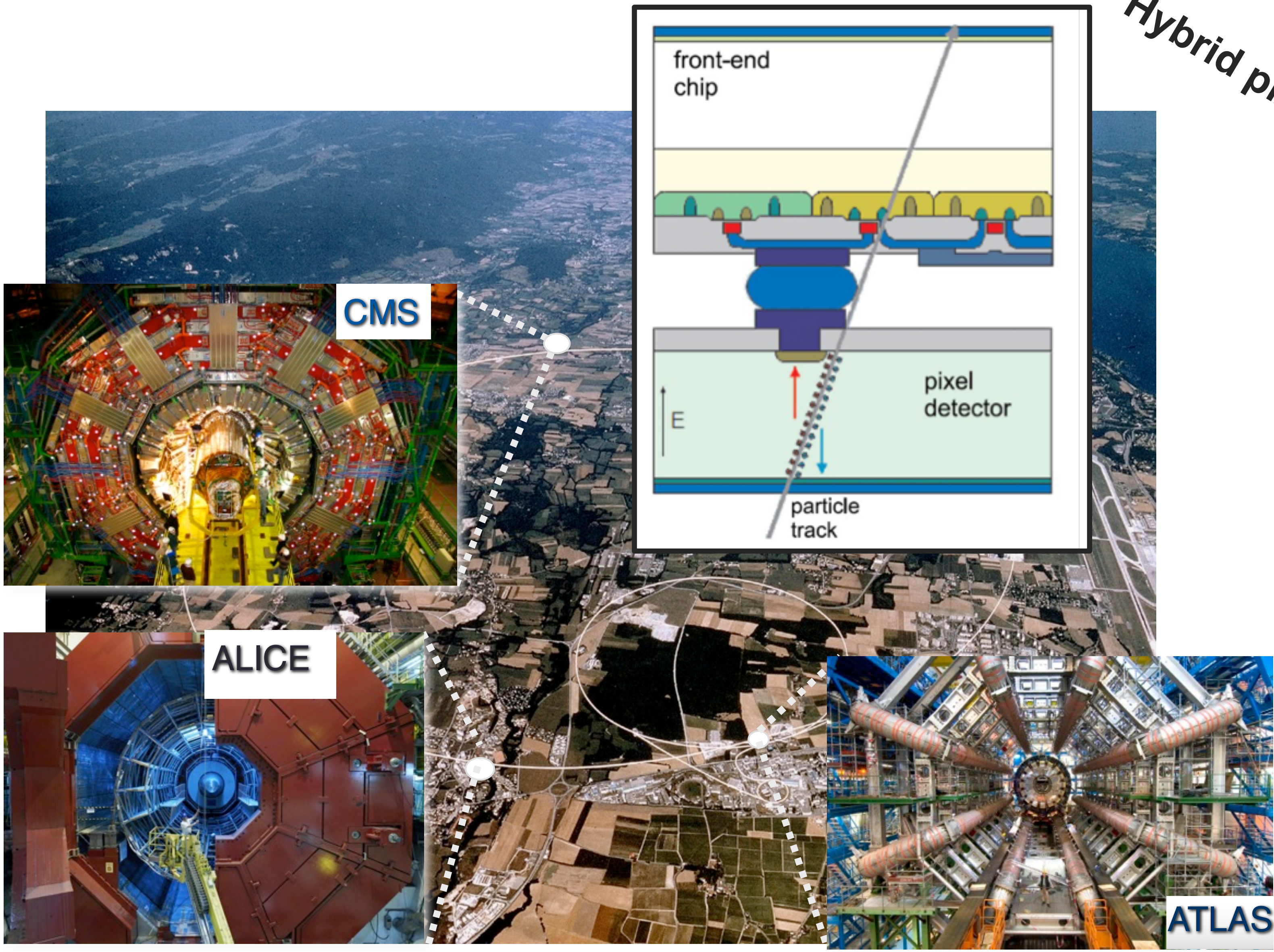
- relatively large material budget: >1.5% X_0 per layer
- resolution could be better
- complex and laborious module production
- bump-bonding / flip-chip
- many production steps
- expensive

But hybrid pixels are extremely successful and if you look at today's LHC experiments...

Pixel Detectors at LHC

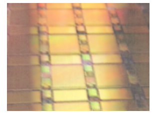


Hybrid pixels!



Installation process for new pixel detector

https://www.ethz.ch/en/news-and-events/eth-news/news/2017/03/new-heart-for-cerns-cms.html

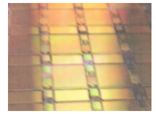


CMOS Image Pixel Sensors

- CMOS active image pixel sensor developed by NASA/JPL (patents by Caltech) in 1992, plus proposals in HEP*
- Used (vanilla) CMOS process available at many foundries → easily accessible
- First versions contained in-pixel source follower amplifier for charge gain, low noise Correlated Double Sampling, basis for camera-on-chip
- Though specialized fab processes are required, the market has driven developments leading to CMOS sensors dominating the field.

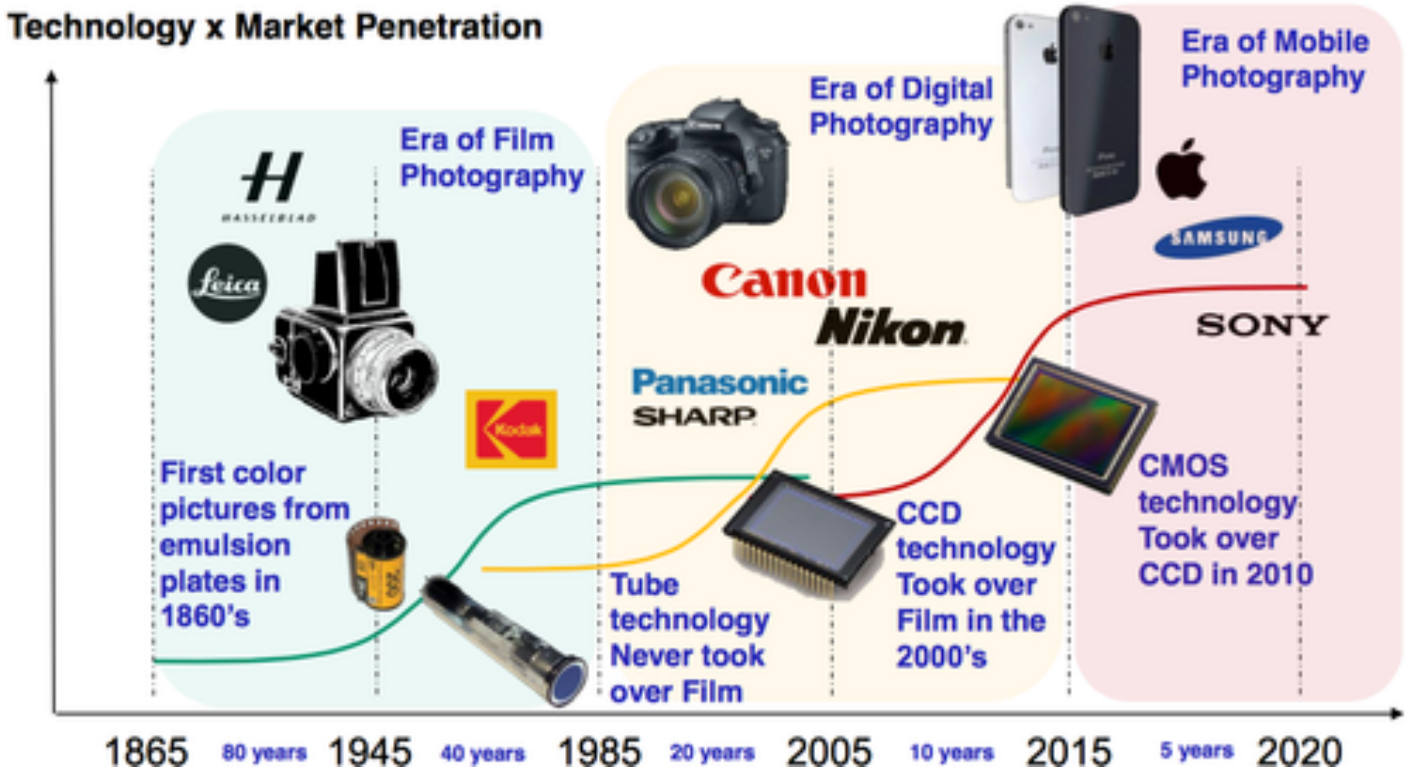
ER Fossum, CMOS Active Pixel Sensors – Past, Present and Future, 2008
https://pdfs.semanticscholar.org/6d85/af67a846d13b7e7502f7fa96c0729c972590.pdf

*In HEP, e.g.
S. Parker, A proposed VLSI pixel device for particle detection
NIMA 275 (1989), 494-516



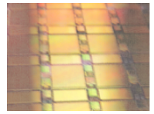
CMOS Image Pixel Sensors

- While 1980s were dominated by CCDs (camcorder market)
- The 1990s/2000s have shown an increasing demand for CMOS imaging sensors due to the camera phone market



http://www.eetimes.com/document.asp?doc_id=1325655&image_number=1

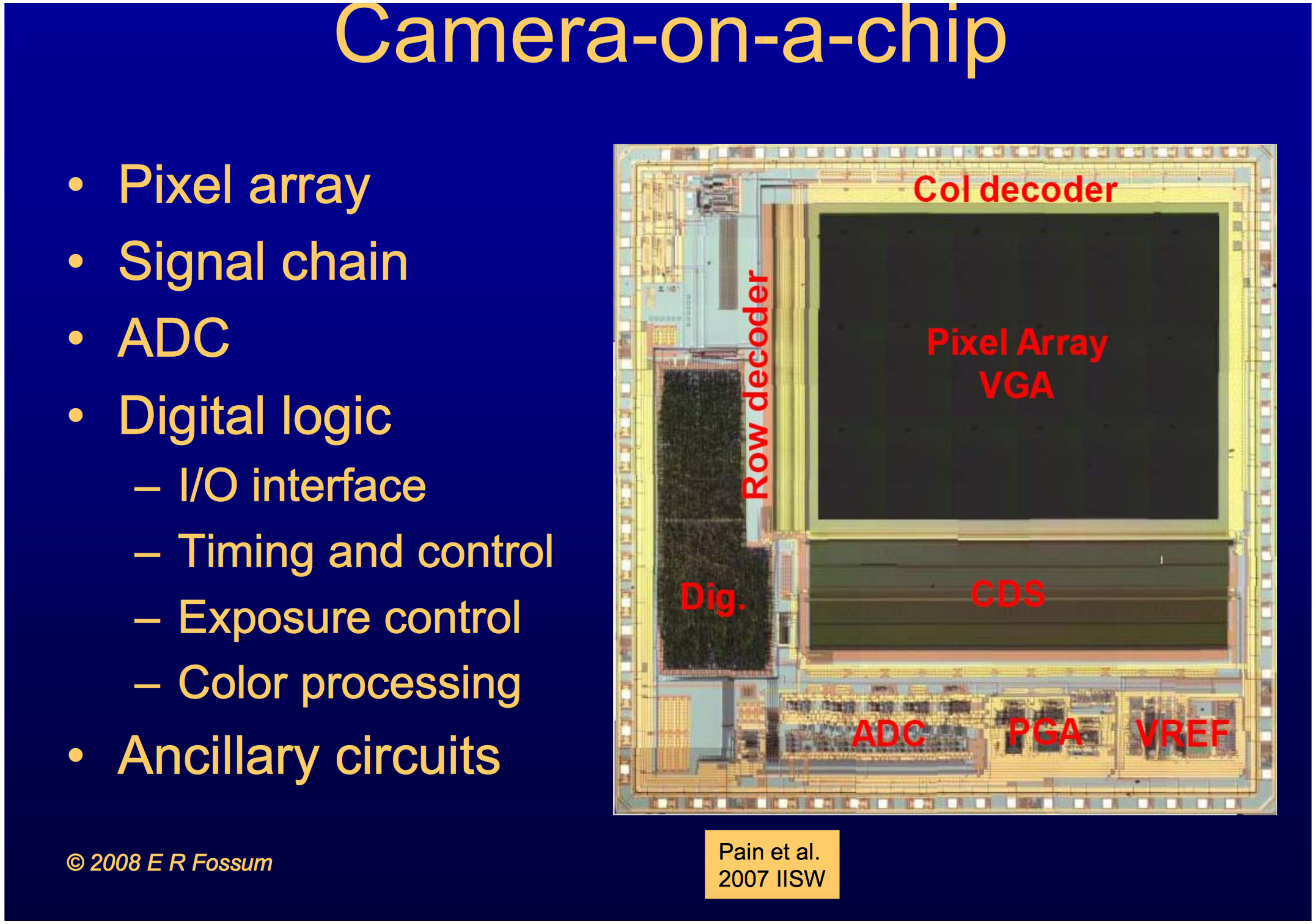
CMOS Image Pixel Sensors



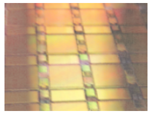
What are the advantages of CMOS imaging sensors (camera-on-chip) in industry? For example:

- Low power, important for portable devices
- Compact cameras due to system-on-a-chip
- Fewer components needed

ER Fossum, CMOS Active Pixel Sensors – Past, Present and Future, 2008
https://pdfs.semanticscholar.org/6d85/af67a846d13b7e7502f7fa96c0729c972590.pdf

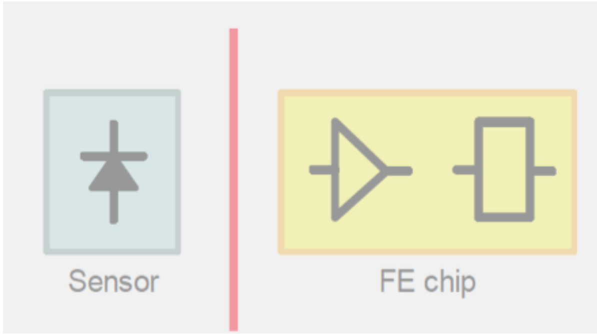


Monolithics in HEP?

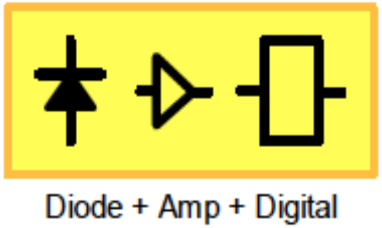


Silicon trackers are part of the core tracking systems of all present LHC experiments.

Monolithic pixel detectors can offer a number of interesting advantages for HEP experiments:

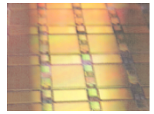


- Commercial process (8” or 12” wafers)
- Multiple vendors
- Potentially cheaper interconnection processes available
- Thin sensor (50-100 um) have less material and reduce cluster size at large eta
- ..



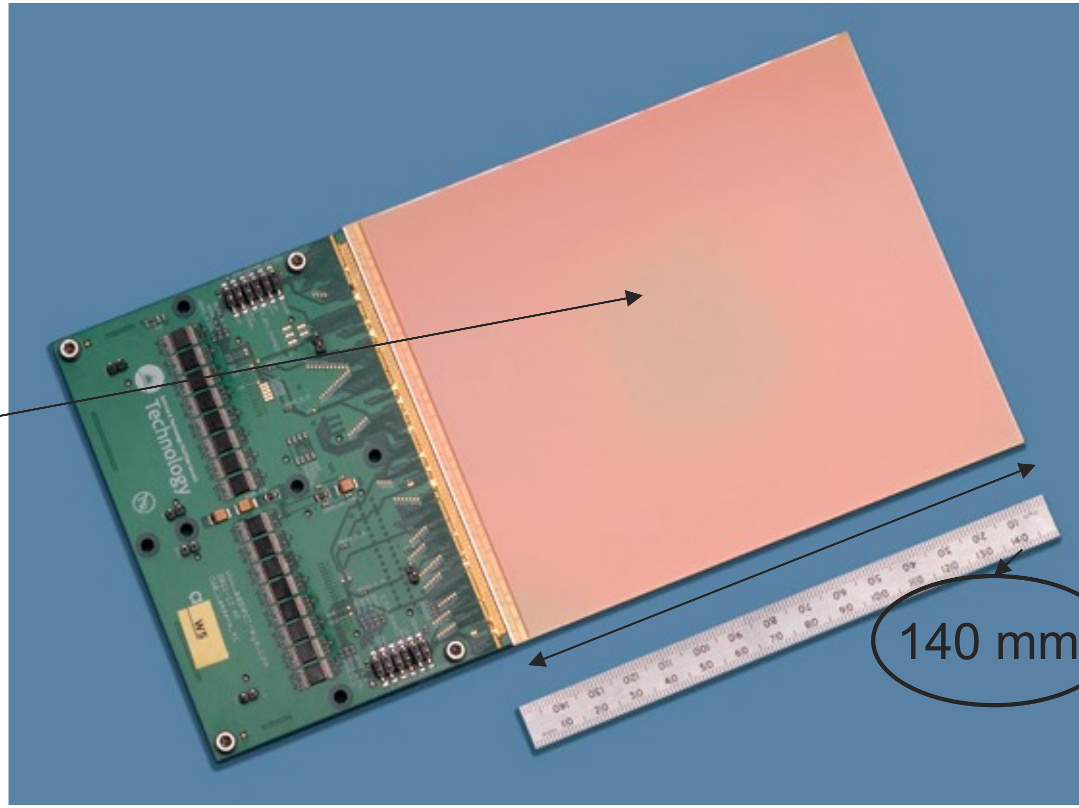
Strong interest in monolithic pixels, with many different variants!

MAPS (Monolithic Active Pixel Sensors) for Imaging and More



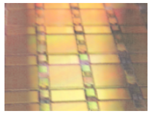
Many developments in the field of CMOS imaging sensors and MAPS in general within the community!

Example:
Wafers scale (8”) imaging sensor developed by the RAL team (stitched)



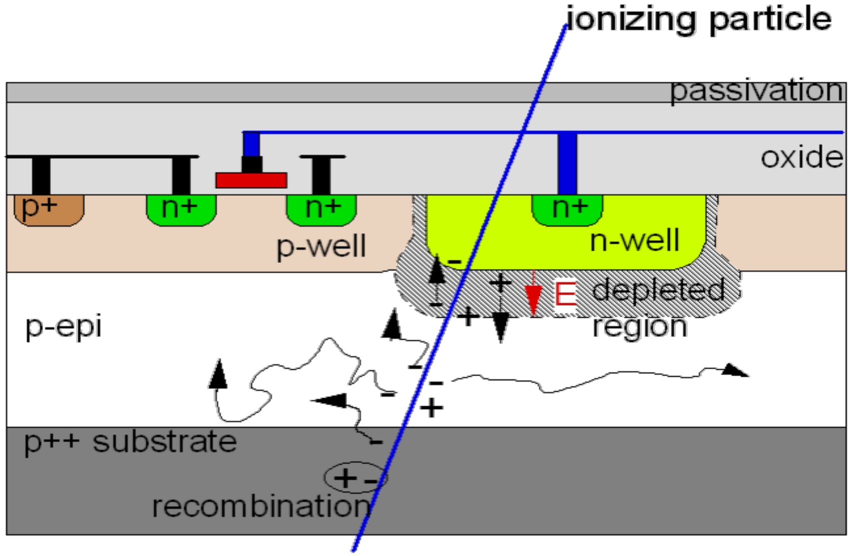
N. Guerrini, RAL, 5th school on detectors, Legnaro, April 2013

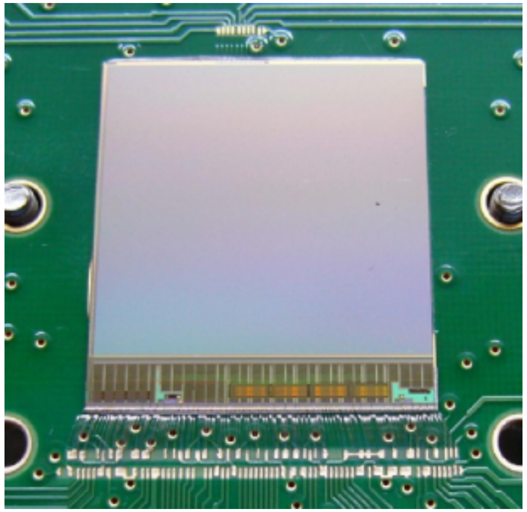
MAPS



Developments lead by IPHC created a number of monolithic pixel sensors of the MIMOSA family:

- Epitaxial wafers with collection diode and few transistors per cell (size ~ 20 x 20 μm^2)
- 0.35 μm CMOS technology with only one type of transistor (NMOS)
- Rolling shutter architecture (readout time O(100 μs))
- **Charge collection mostly by diffusion**
- Limited radiation tolerance (< 10^{13} n_{eq} cm^{-2})

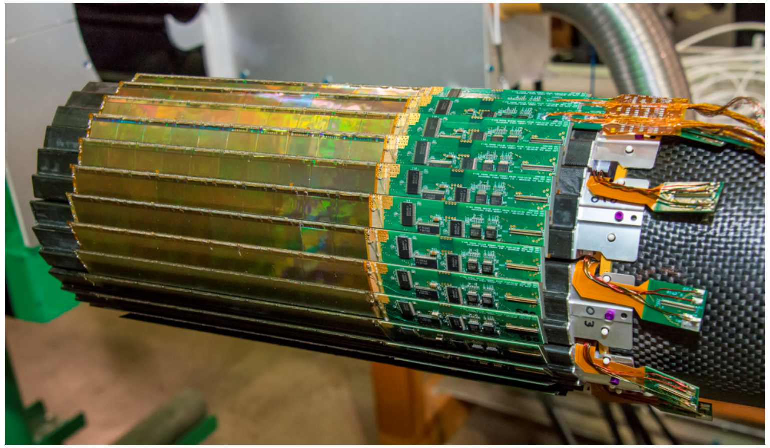




ULTIMATE chip for STAR HFT (IPHC Strasbourg)

STAR Heavy Flavour Tracker

The upgrade of the STAR HFT included also the installation of the **first MAPS based vertex tracker at a collider experiment.**



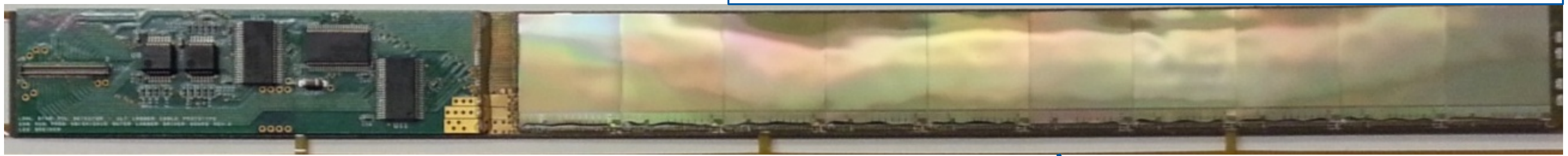
DCA Pointing resolution	(10 ⊕ 24 GeV/p·c) μm
Layers	Layer 1 at 2.8 cm radius Layer 2 at 8 cm radius
Pixel size	20.7 μm X 20.7 μm
Hit resolution	3.7 μm (6 μm geometric)
Position stability	5 μm rms (20 μm envelope)
Material budget first layer	X/X_0 = 0.39% (Al cond. cable)
Number of pixels	356 M
Integration time (affects pileup)	185.6 μs
Radiation environment	20 to 90 kRad / year $2*10^{11}$ to 10^{12} 1MeV n eq/cm^2
Rapid detector replacement	< 1 day

After R&D and prototyping the construction of 3 trackers started in 2013.

STAR HFT

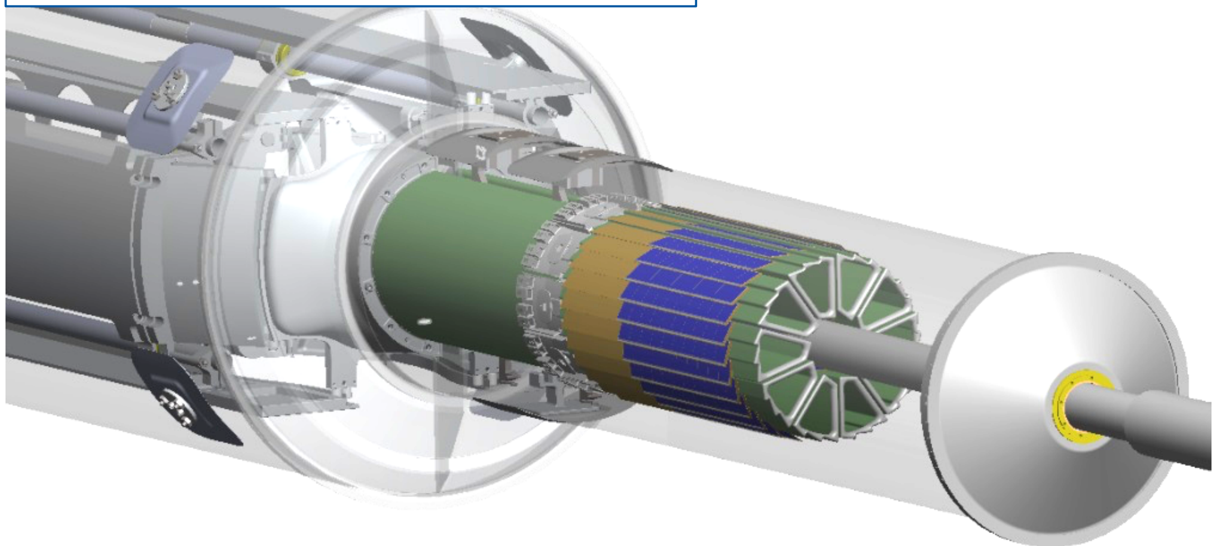
Basic Detector Element

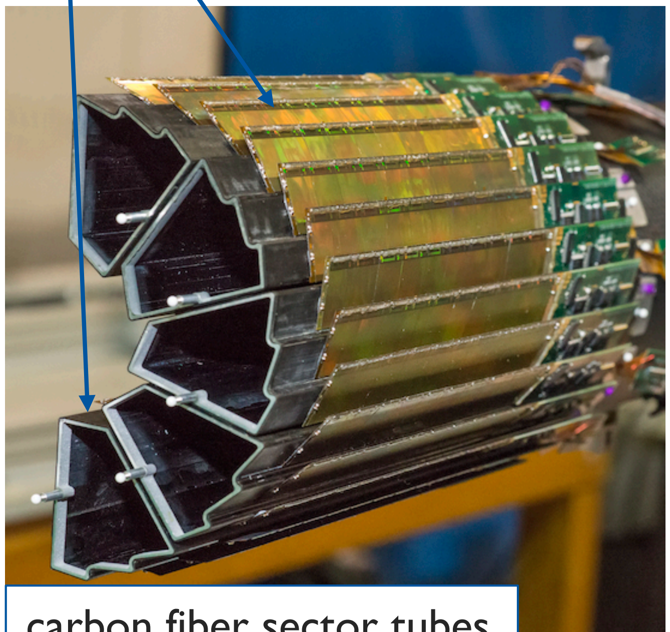
Ladder with 10 MAPS sensors (~ 2×2 cm each)



10 sensors / ladder
4 ladders / sector
5 sectors / half
10 sectors total

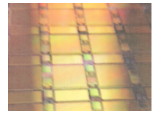
Mechanical support with kinematic mounts (insertion side)



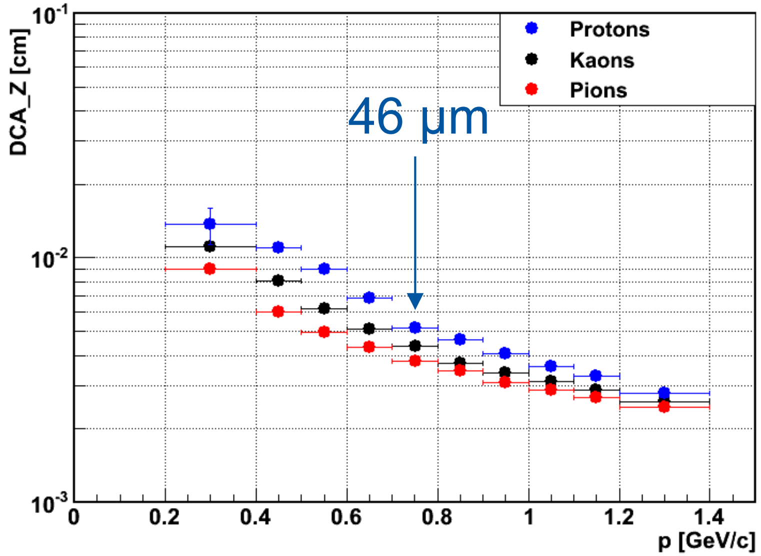


carbon fiber sector tubes (~ 200 µm thick)

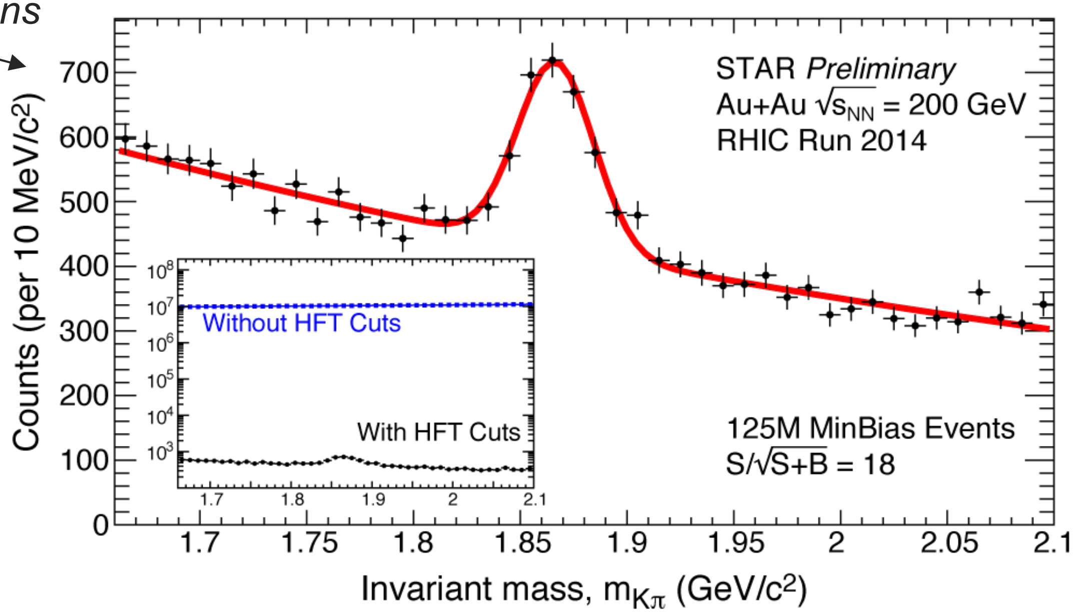
STAR HFT



- DCA pointing resolution
  - Design requirement exceeded: 46 µm for 750 MeV/c Kaons for the **2 sectors** equipped **with aluminum cables on inner layer**
  - ~ 30 µm for p > 1 GeV/c
  - From 2015: all sectors equipped with aluminum cables on the inner layer

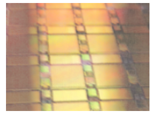


***$D^0 \rightarrow K\,\pi$ production** in*
$\sqrt{s_{NN}}$ = 200GeV Au+Au collisions
(partial event sample)



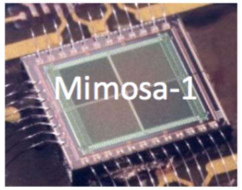
- Physics of D-meson productions
  - High significance signal
  - Nuclear modification factor R_{AA}
  - Collective flow v_2
- First Λ_c^+ signal observed in HI collisions (QM 2017)!

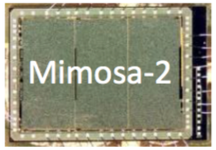
MAPS Evolution

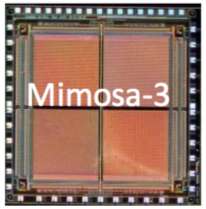


L. Musa, 30 years HI Forum
November 2016

Owing to the industrial development of CMOS imaging sensors and the intensive R&D work (IPHC, RAL, CERN)







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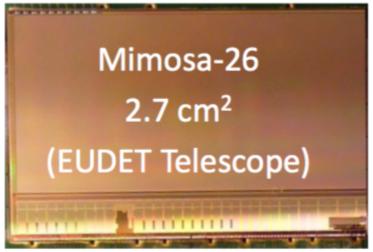
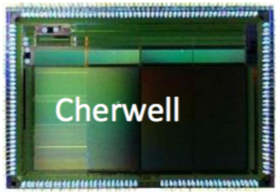
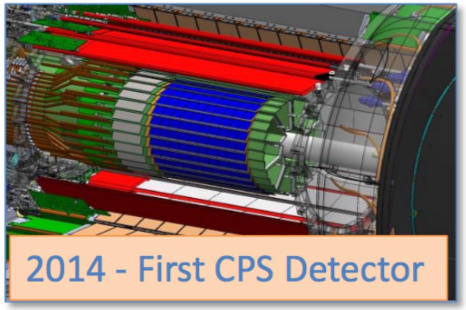
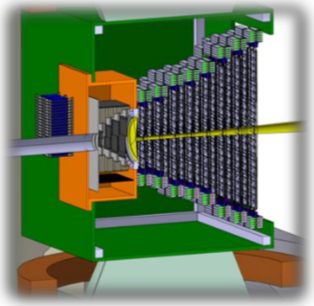




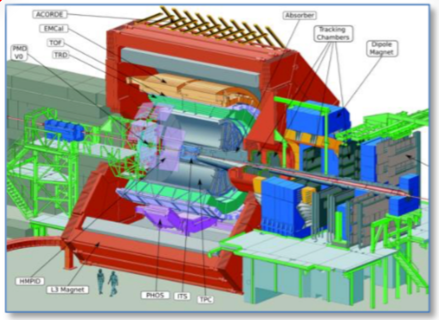
... several HI experiments have selected CMOS pixel sensors for their inner trackers



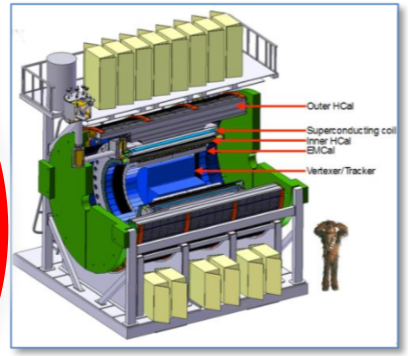
STAR HFT
$0.16\ m^2$ – 356 M pixels



CBM MVD
$0.08\ m^2$ – 146 M pixel



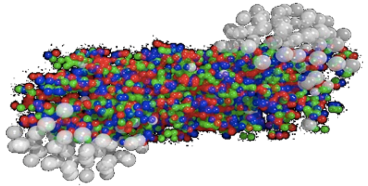
ALICE ITS Upgrade (and MFT)
$10\ m^2$ – 12 G pixel



sPHENIX
$0.2\ m^2$ – 251 M pixel

30

ALICE Upgrade



Motivation: QGP precision study

- High precision measurement of heavy flavour hadrons over a large range in p_T and rapidity and multi-differentially in centrality and reaction plane.

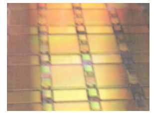
Requirements:

- Excellent tracking efficiency and resolution at low p_T
- Large statistics with minimum bias trigger to gain a factor 100 over present program
  - Pb-Pb recorded luminosity $\geq 10\ nb^{-1}$ plus p-p and p-A data
- Preserve PID capability at high rate

Strategy:

- **Readout all Pb-Pb interactions** at max. rate (50 kHz) with minimum bias trigger
  - Upgrade of the detector readout and online and offline systems
- Large improvement of **vertexing and tracking capability**
  - **New Inner Tracking System (ITS)** and Muon Forward Tracker (MFT)

ALICE ITS Upgrade Design Requirements



Improve impact parameter resolution by factor of ~3 in (r-ϕ) and ~5 in (z)

- Get closer to IP: 39 mm → 21 mm (layer 0)
- Reduce beampipe radius: 29 mm → 18.2 mm
- Reduce material budget: 1.14 % X_0 → 0.3 % X_0 (inner layers)
- Reduce pixel size: (50 μm x 425 μm) → O(30 μm x 30 μm)

High standalone tracking efficiency and p_T resolution

- Increase granularity and radial extension → 7 pixel layers

Fast readout

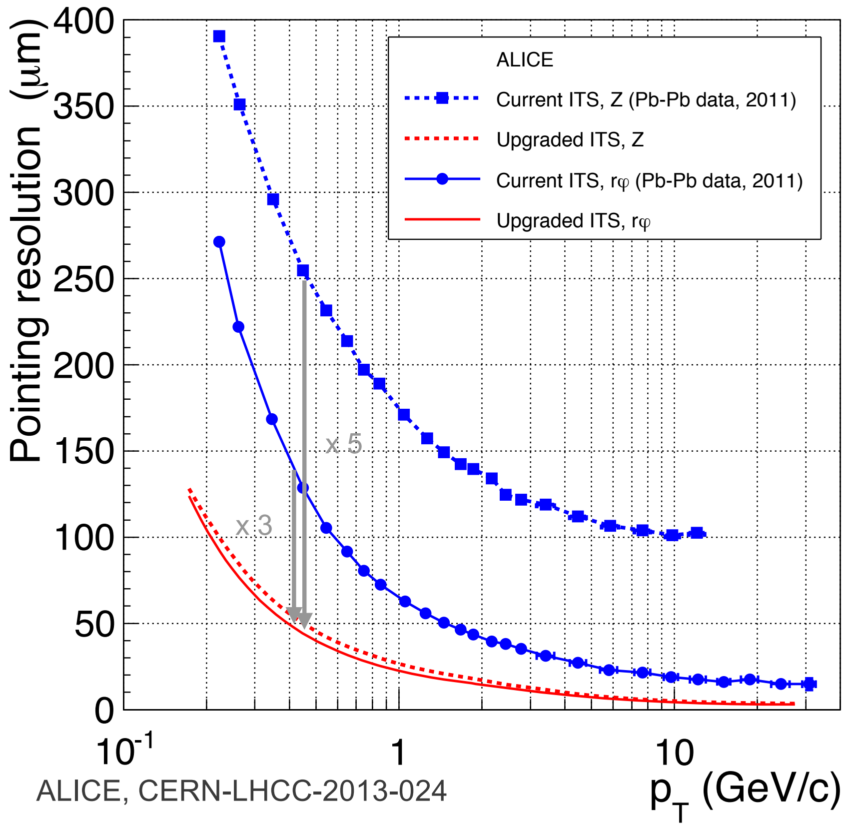
- Readout of Pb-Pb interactions at 50 kHz (presently 1kHz) and 400 kHz in p-p interactions

Fast insertion/removal for yearly maintenance

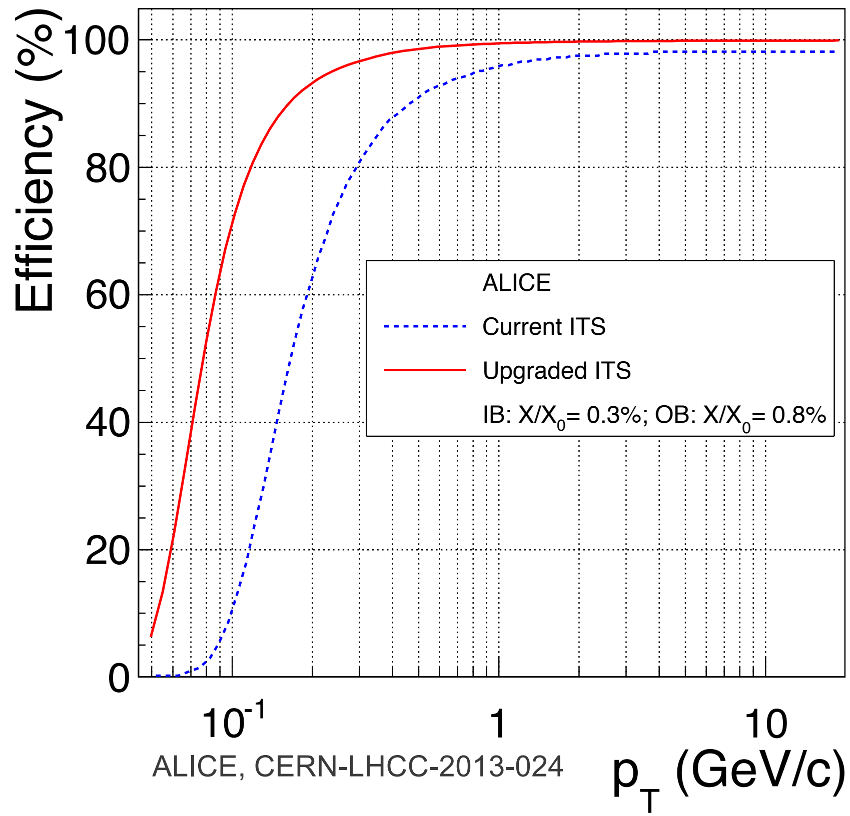
- Possibility to replace non functioning detector modules during yearly shutdown

ALICE ITS Upgrade Performance Studies

Impact parameter resolution



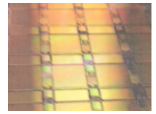
Track reconstruction efficiency



Improved impact parameter resolution

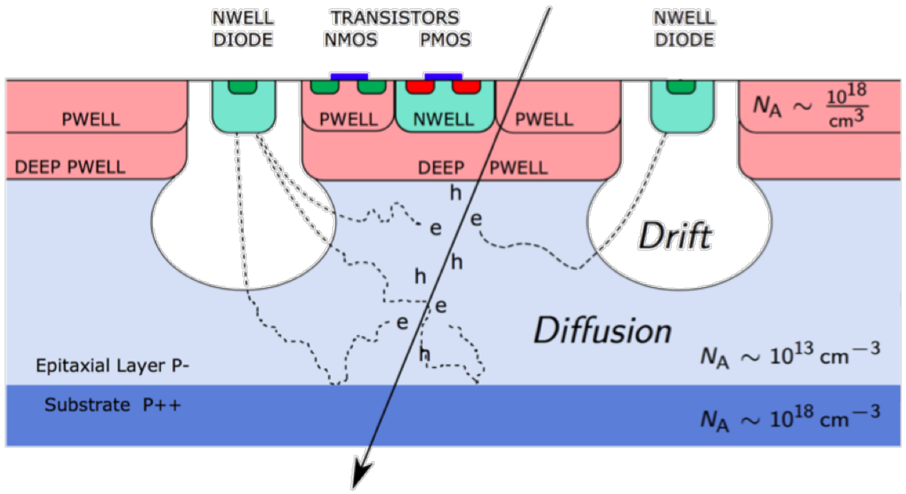
High standalone tracking efficiency

ALICE ITS Upgrade Pixel Technology

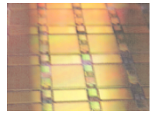


TowerJazz 0.18μm CMOS imaging process

- N-well collection electrode in high resistivity epitaxial layer
- Present state-of-art based on **quadruple well allows full CMOS**
- **High resistivity (> 1kΩ cm) epi-layer** (p-type, 20-40 μm thick) on p-substrate
- **Moderate reverse bias => increase depletion region** around Nwell collection diode to collect more charges by drift



ALICE ITS Upgrade



Based on high resistivity epi layer MAPS

3 Inner Barrel layers (IB)
4 Outer Barrel layers (OB)

Radial coverage: 21-400 mm

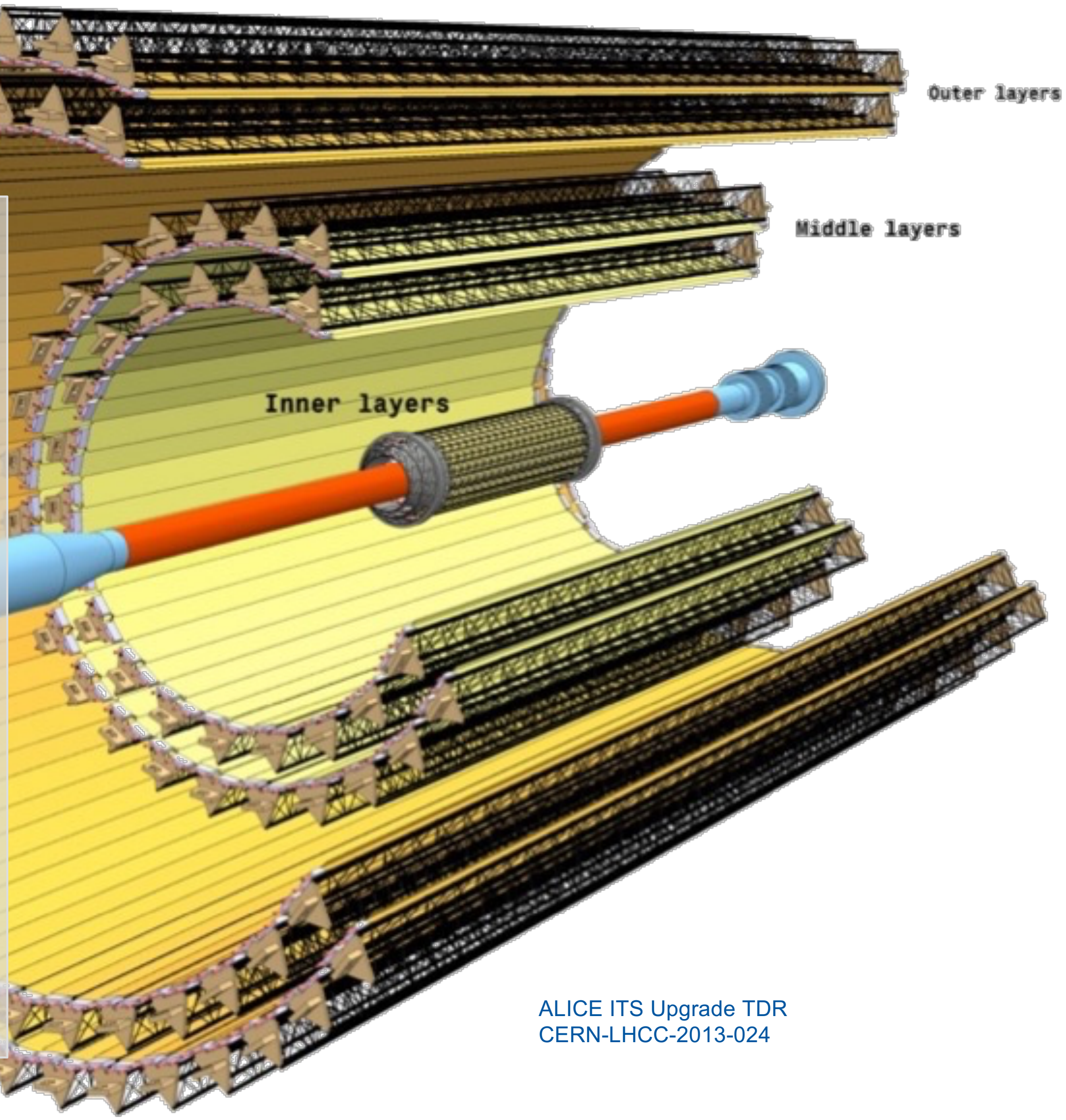
~ 10 m^2

|η|<1.22 over 90% of the luminous region

0.3% X_0/layer (IB)
0.8 % X_0/layer (OB)

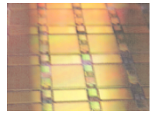
Radiation level (IB, layer 0): TID: 2.7 Mrad, 1.7 x 10^{13} 1 MeV n_{eq} cm^{-2}

Installation during LS2

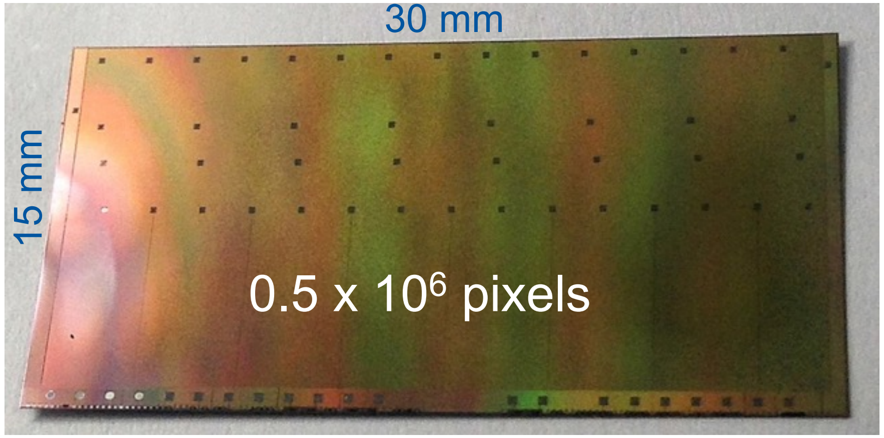


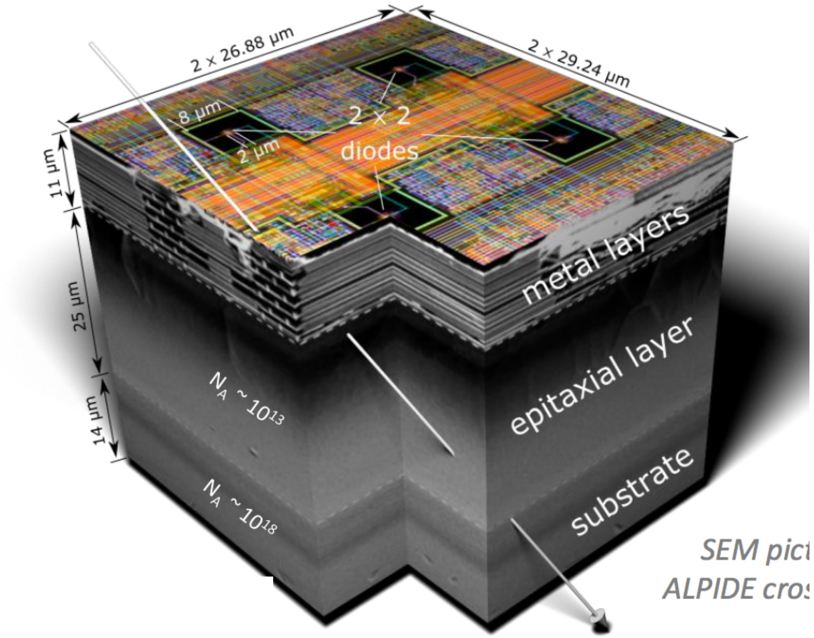
ALICE ITS Upgrade TDR
CERN-LHCC-2013-024

ALPIDE Chip

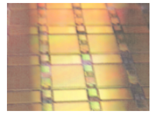


- Pixel size: 29 x 27 µm² with low power front-end (40 nW)
- Small n-well diode (2 µm diameter), ~ 100 times smaller than pixel size
- Asynchronous sparsified digital readout
- **Power density ~300 nW/pixel**
- Minimized inactive area on the edge due to pads-over-matrix design (~ 1.1 x 30 mm²)
- Full size prototypes produced on different epitaxial wafers
- **Partial depletion of the sensitive region due to back bias**





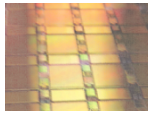
Chip Development

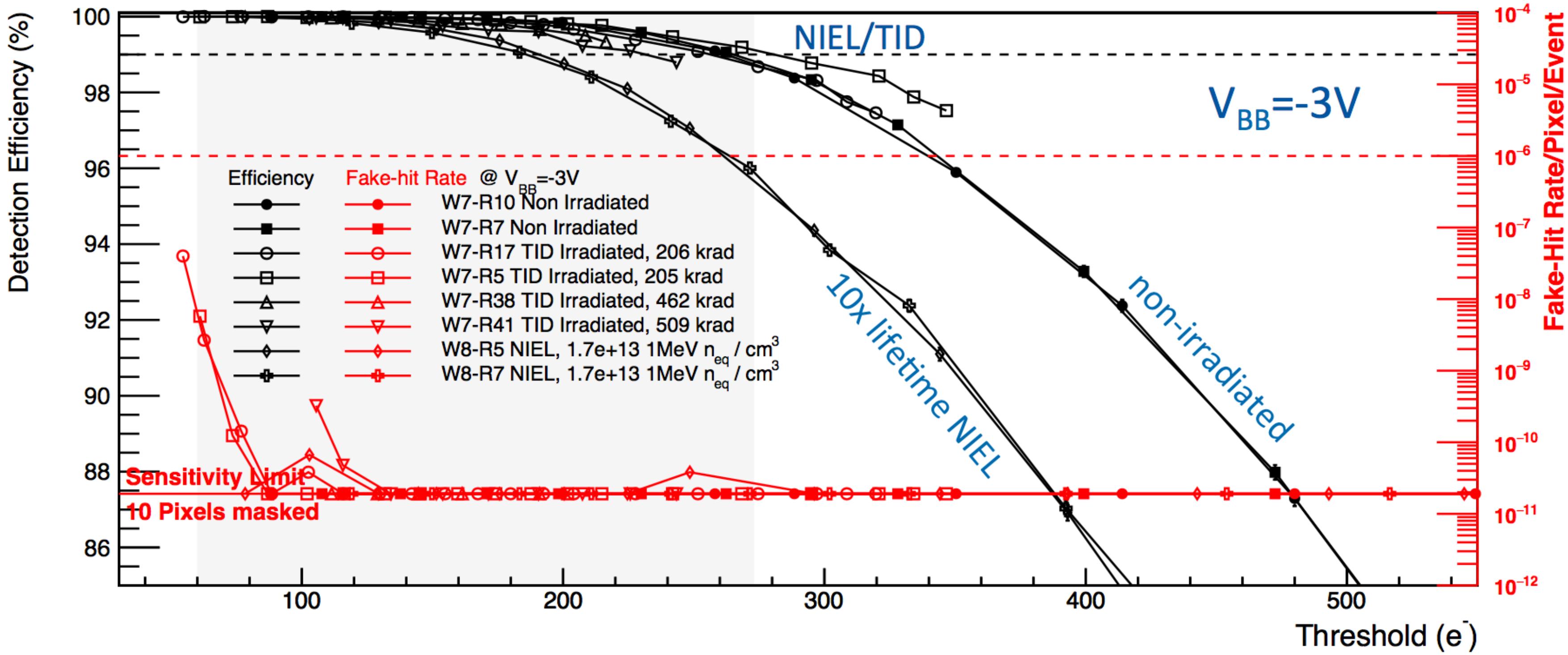


Design team from CERN, INFN, CCNU, YONSEI, NIKHEF, IRFU, IPHC

2012	Explorer	20 µm x 20 µm and 30 x 30 µm pixels (analogue readout) 1.8 x 1.8 mm^2, study of pixel geometry, starting material, radiation
2013	pALPIDEss-0	Matrix with 64 columns x 512 rows, 22 µm x 22 µm pixels, 11 x 1.8 mm^2, in-pixel discrimination and buffering, zero suppression
2014	pALPIDE-1	**First full scale prototype!** 28 µm x 28 µm pixels, 15 x 30 mm^2, four sectors with variants, 1 register/pixel, no final interface
8/2015	pALPIDE-2	**Full scale prototype,** four sectors with variants, optimisation of circuits, integration in modules, no high speed serial output
10/2015	pALPIDE-3	**Full scale prototype,** eight sectors with variants, all communincation features, no ADC, no temperature sensor)
8/2016	ALPIDE	**Final chip**

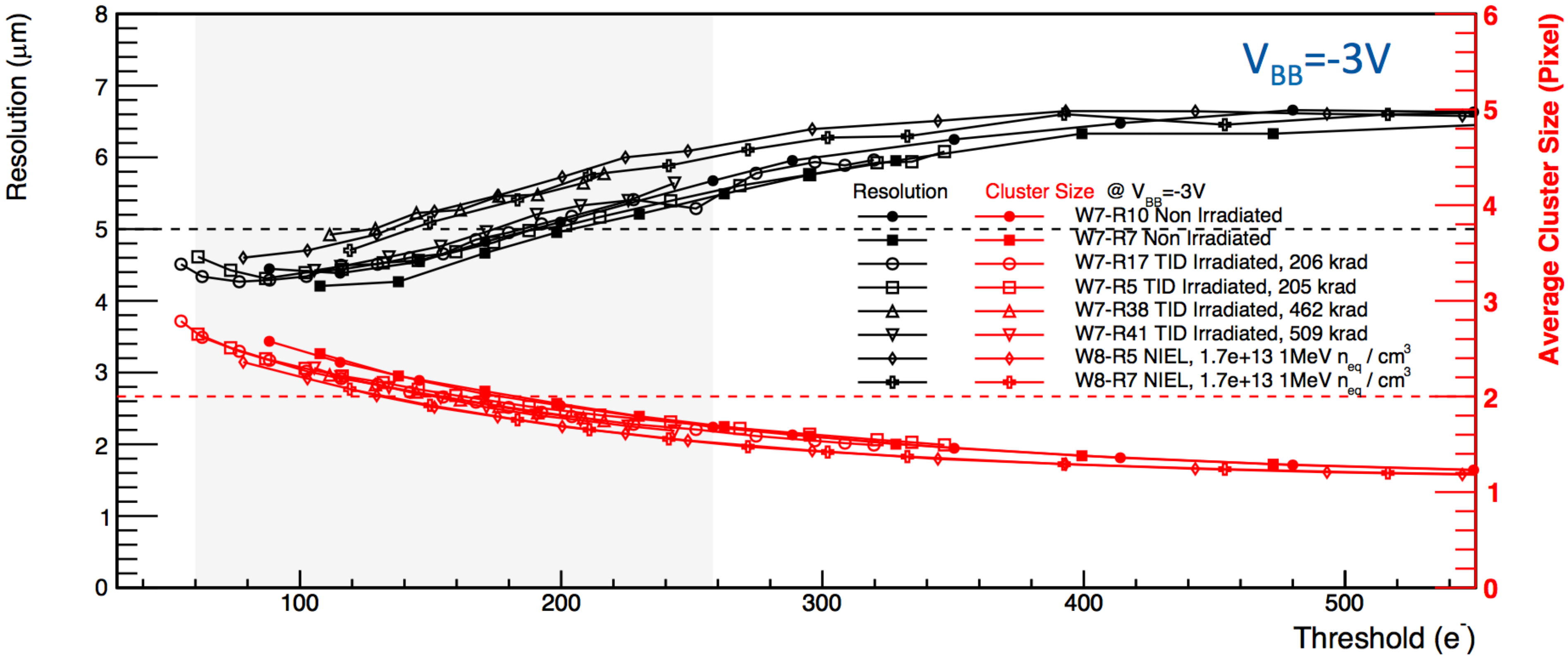
ALPIDE Chip Performance





- Large operational margin before and after irradiation up to 10 x lifetime NIEL
- Chip-to-chip fluctuations negligible
- Fake hit rate << 10^{-5}

ALPIDE Chip Performance



- Similar performance before and after irradiation
- Chip-to-chip fluctuations negligible
- Resolution of 4-6 µm up to ~ 300 electrons threshold range

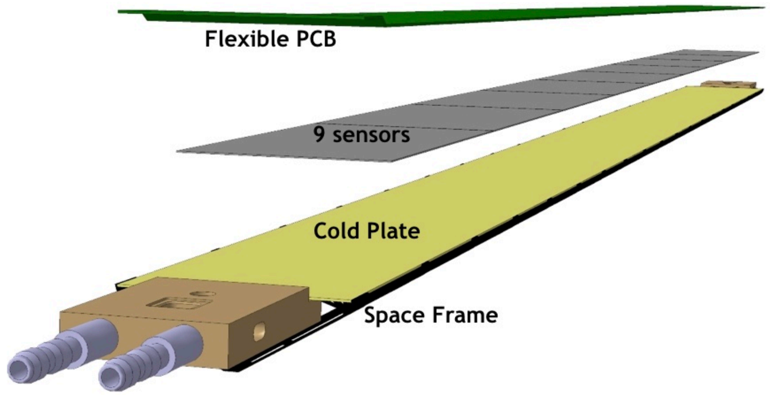
ALICE ITS in Numbers

Inner Barrel

3 Inner Layers: 12+16+20 Staves
1 Module / Stave

9 sensors per Module

108 Modules to produced
(2 Inner Barrels + spares)

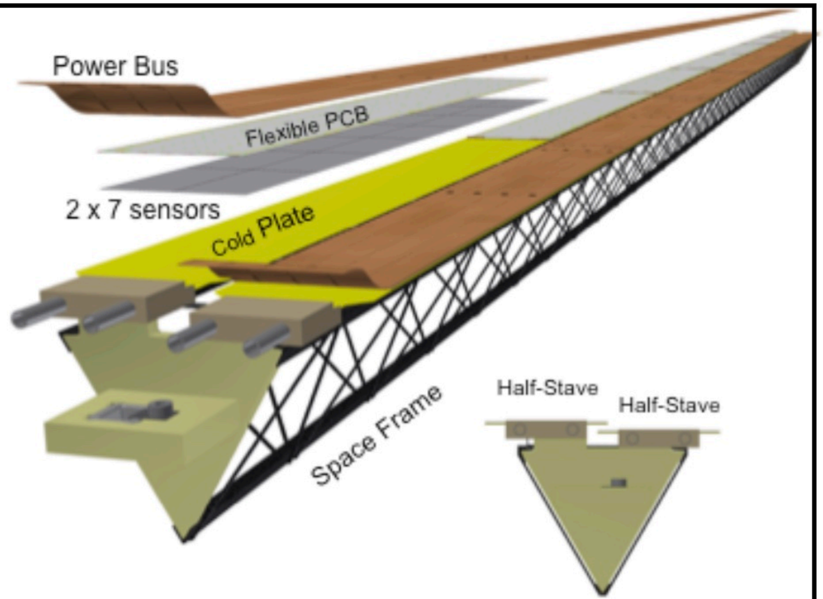


Outer Barrel

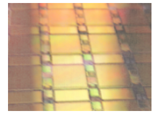
2 Middle Layers: 30+24 Staves
2×4 Modules / Stave
2 Outer Layers: 42+48 Staves
2×7 Modules / Stave

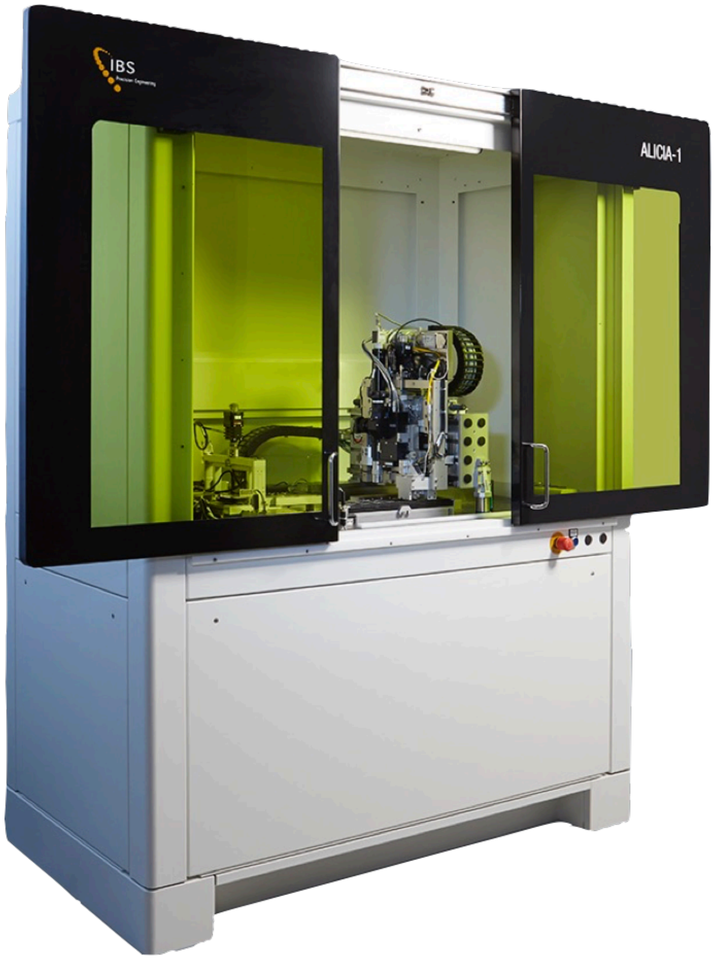
2×7 sensors / Module
(Middle and Outer Layers are equipped with the same Module Type)

2550 Modules to be produced
(including spares)



ALICE ITS Module Production



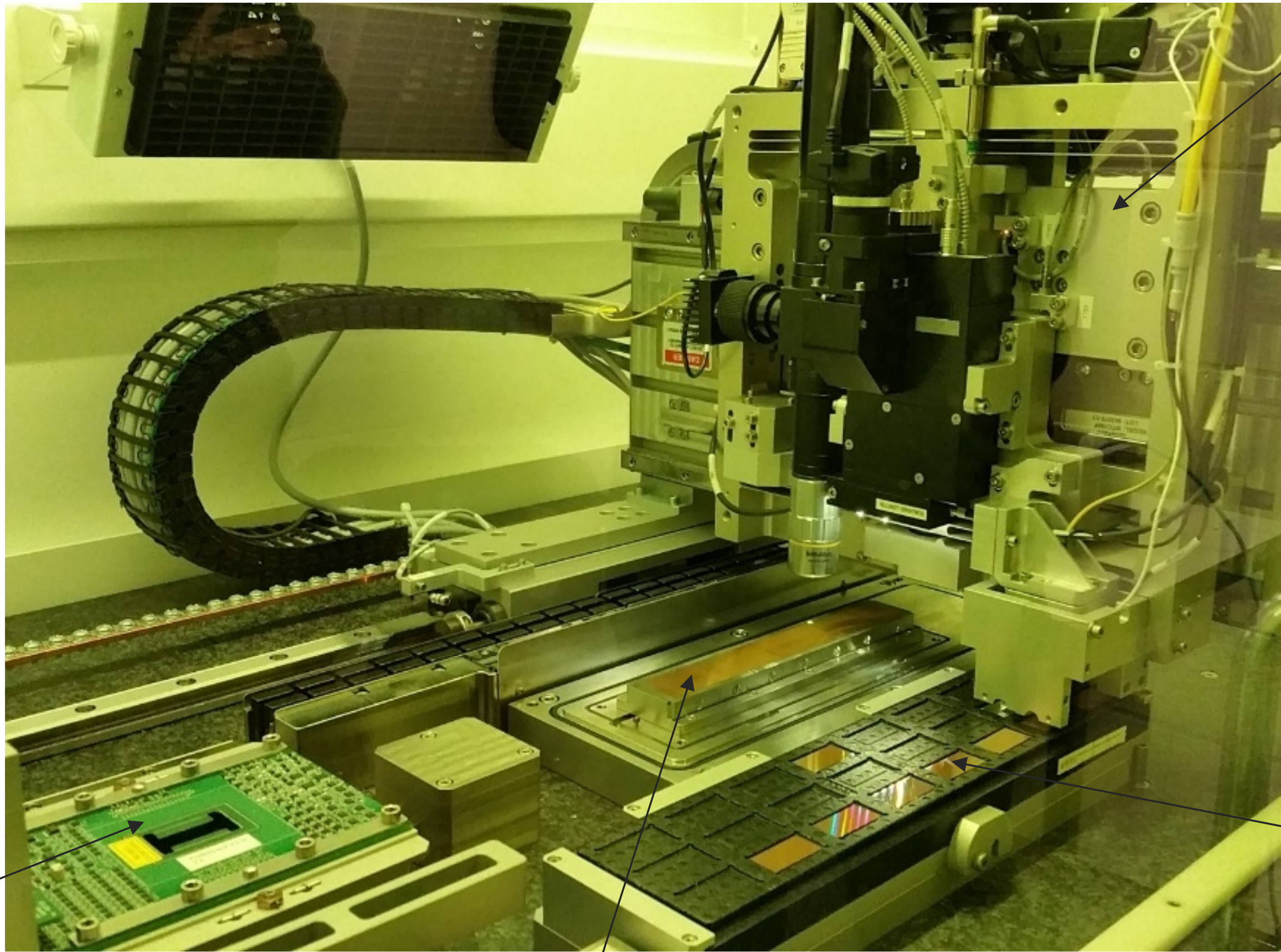


The modules are being assembled using a custom machine (ALICIA), which aligns the chips into the HIC positions (position accuracy +/- 5 μm) and provides the possibility to probe the chips and to do a fully automatic visual inspection.

The HICs will be produced in **5 construction centers:** CERN (DSF cleanroom), Bari (IT), Liverpool (UK), Pusan (South Korea), Wuhan (China).

IB and OB HIC Production

Automatic p&p arm with inspection camera

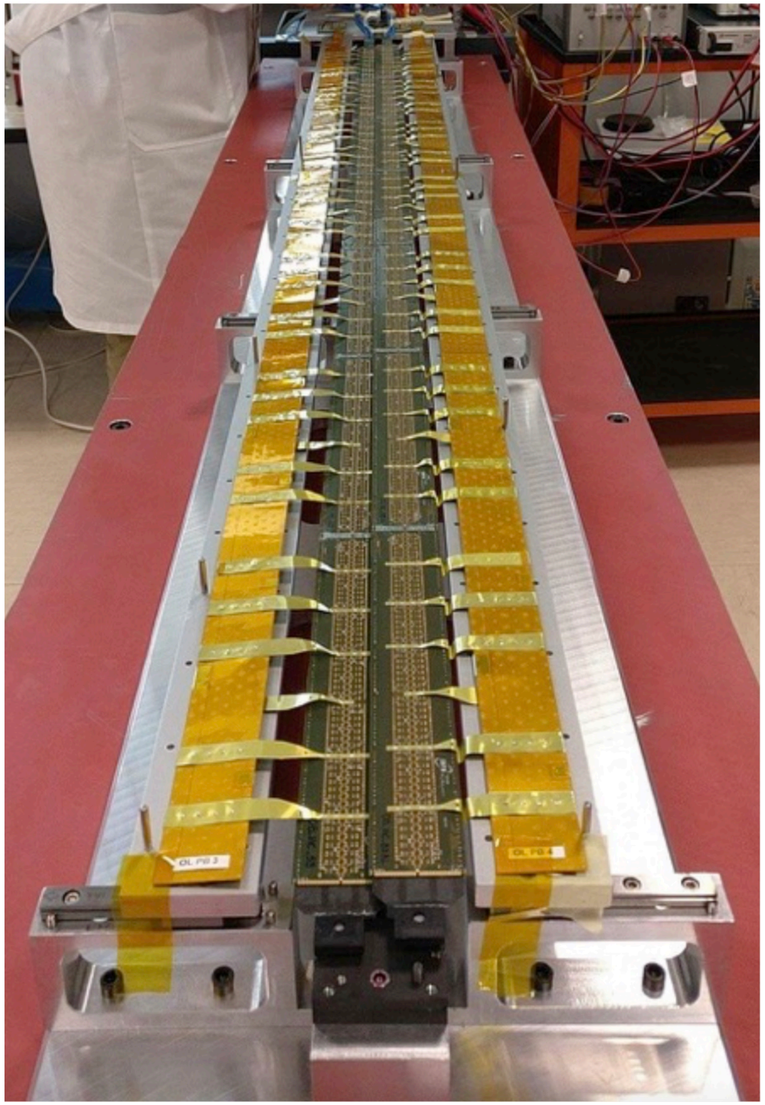


Probecard

Tray of chips

Alignment table for the chips

Outer Barrel Stave

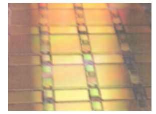


After gluing, wire bonding and testing the modules are mounted into staves.

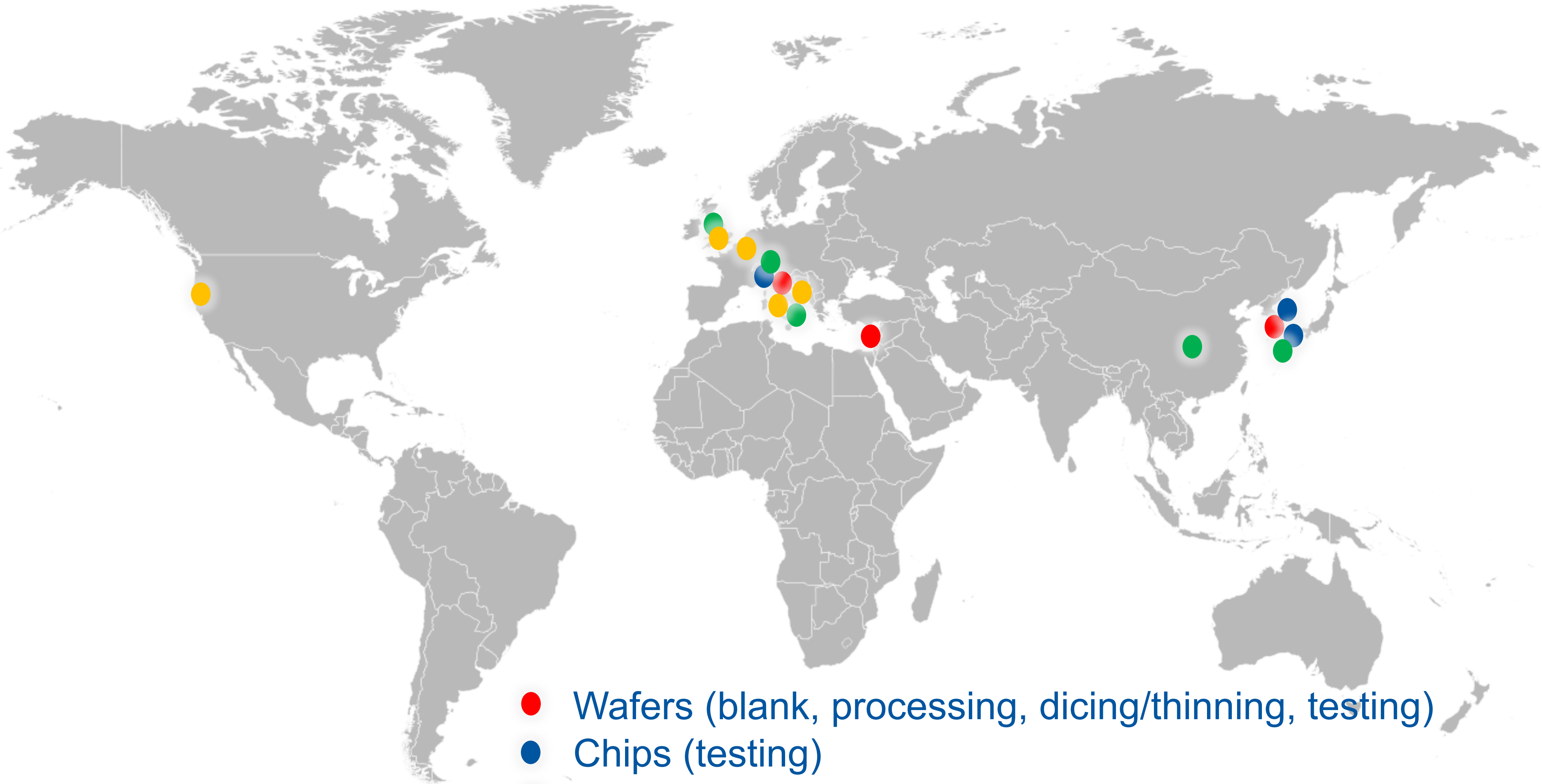
5 Stave assembly centers: Berkley (US), Daresbury (UK), Frascati (IT), NIKHEF (NL), Torino (IT)

Outer barrel stave:

- 2 x 7 modules
- Each module: 14 chips (100 um thick)
- ~ 100M channels/stave



Logistics…



- Wafers (blank, processing, dicing/thinning, testing)
- Chips (testing)
- Module assembly
- Stave assembly

Challenges for the Future

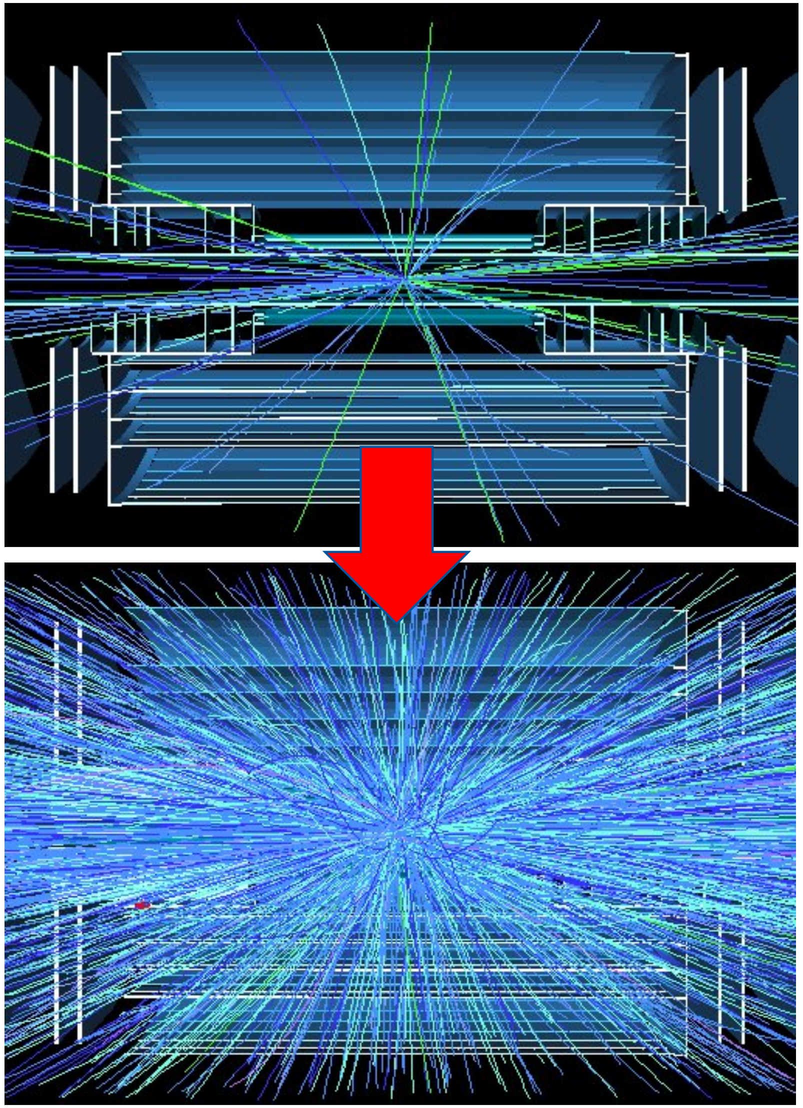
Increased luminosity requires

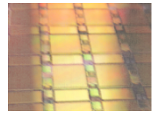
- Higher hit-rate capability
- Higher segmentation
- Higher radiation hardness
- Lighter detectors

Radiation hardness improvement compared to now

- Phase-2 approx. factor 10-30

Can MAPS be ready for this environment?





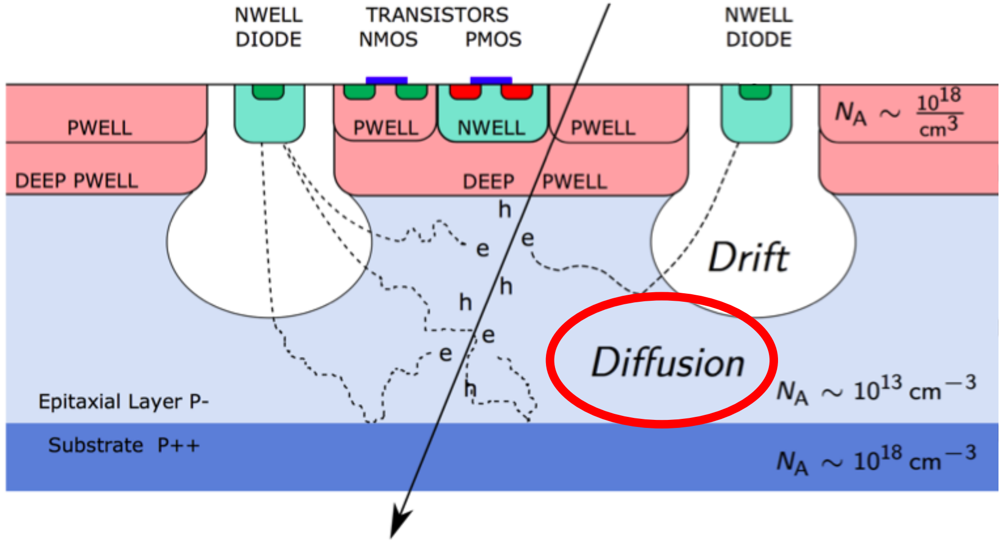
MAPS in Future Experiments

Present MAPS offer a number of very interesting advantages, but the diffusion is a limiting factor.

In a (very) high radiation environment (10^{15}-10^{16} n_{eq}/cm^2):

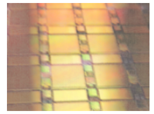
- The ionization charge is trapped/recombined in the non-depleted part → no more signal.
- Diffusion makes signal collection slower than typical requirements for pp-colliders.

Readout architectures are low power, but not designed for high rates like p-p at LHC.

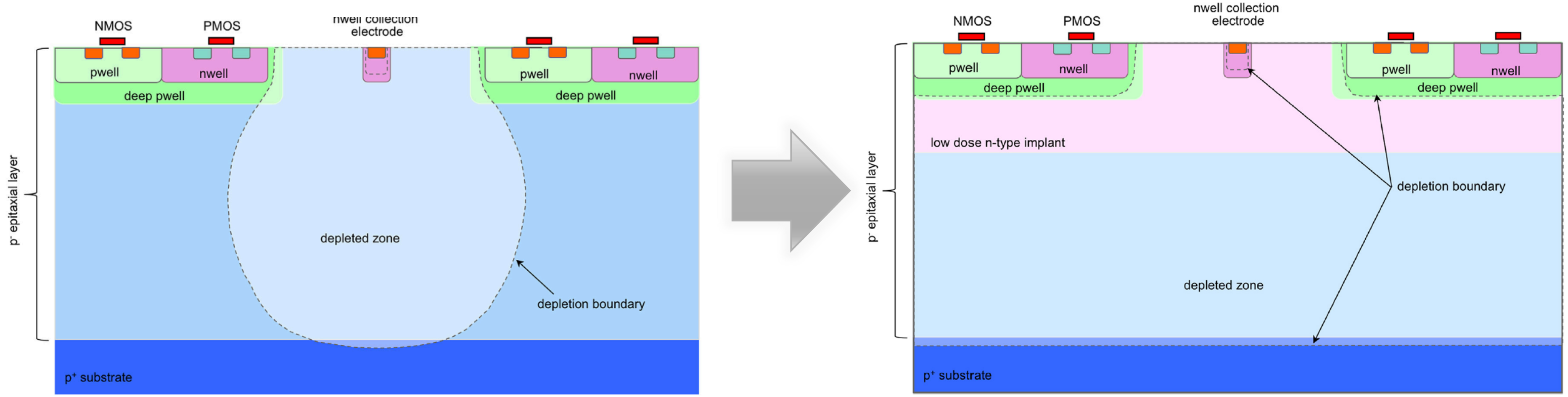


→ within the ALICE ITS upgrade studies were carried out to make the CMOS chips more radiation hard!

TJ 180 nm modified process



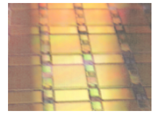
- Novel modified process developed in collaboration of CERN with TJ foundry in context of ALICE ITS.
- Combined with a small collection diode.

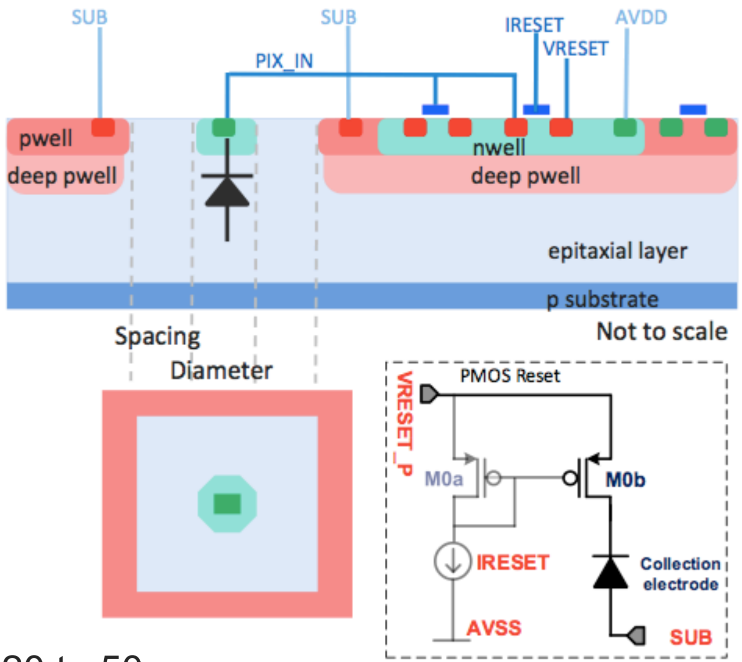


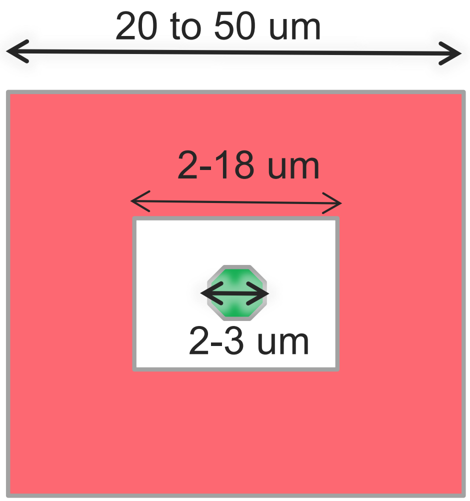
- Adding **a planar n-type layer** significantly improves depletion under deep PWELL
- Increased depletion volume → **fast charge collection by drift**
- better time resolution reduced probability of charge trapping (**radiation hardness**)
- Possibility to fully deplete sensing volume with no significant circuit or layout changes

W. Snoeys et al., NIM A871 (2017) 90 – 96.

TowerJazz 180nm Investigator







- **Pixel dimensions for the following measurements:**
- 20x20 to 50x50um² pixel size
- **3 um diameter electrodes** 25um EPI layer

Designed as part of the ALPIDE development for the ALICE ITS upgrade

Emphasis on small fill factor and small capacitance enables low analog power designs (and material reduction in consequence)

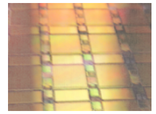
C. Gao et al., NIM A (2016) 831
http://www.sciencedirect.com/science/article/pii/S0168900216300985

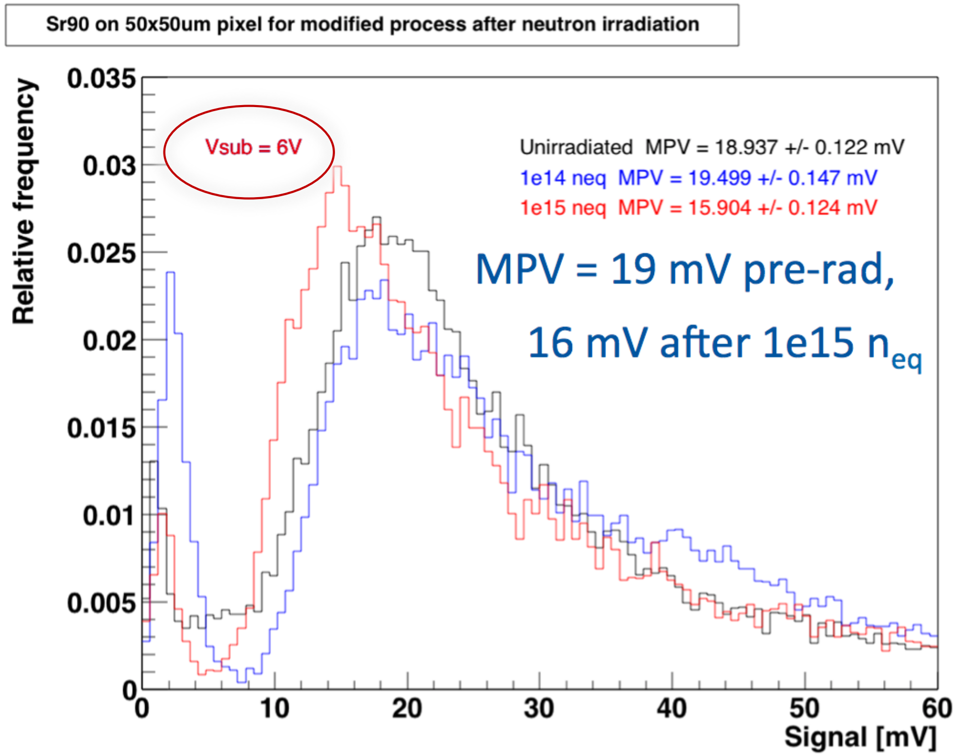
J. Van Hoorne, proceedings of NSS2016
http://2016.nss-mic.org/nss.php

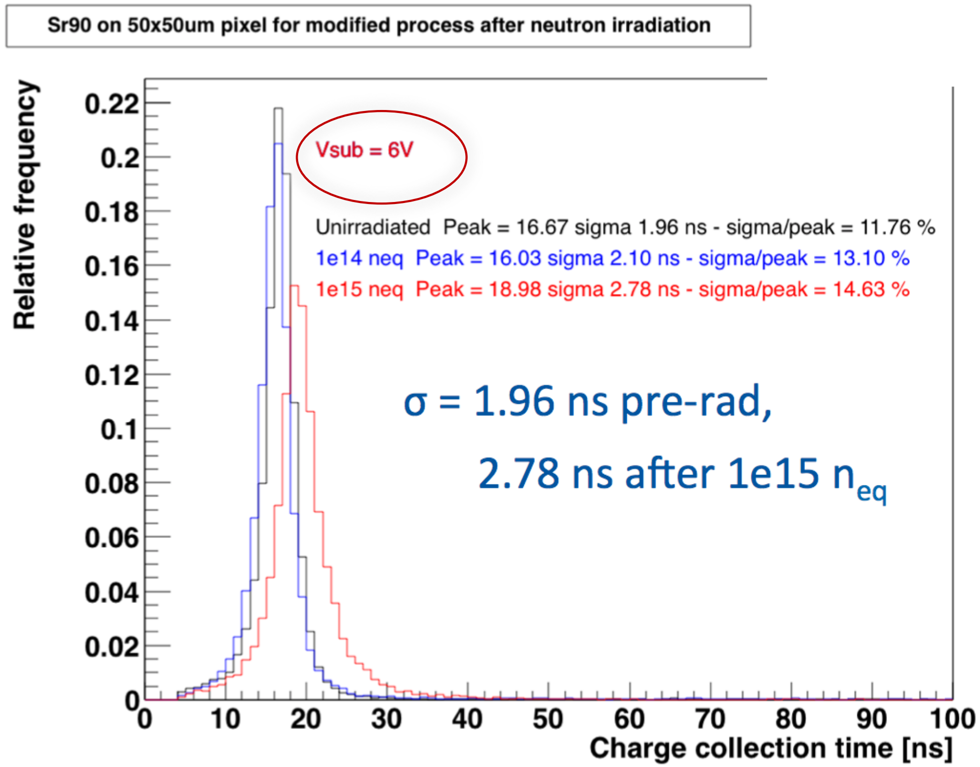
Produced in TowerJazz 180nm on 25-30um thick epi layer in the modified process

Design: C. Gao, P. Yang, C. Marin Tobon, J. Rousset, T. Kugathasan and W. Snoeys

After 10^{15} n_{eq}/cm^2 and 1Mrad TID

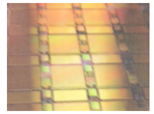






Very little signal loss after 10^{15}, also very encouraging results on detection efficiency.
Signal well separated from noise.
Measurements on samples irradiated to 10^{16} n_{eq}/cm^2 ongoing.

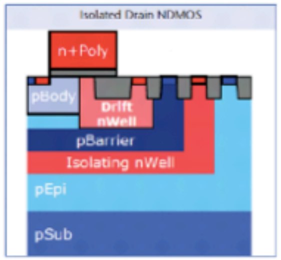
MAPS for the Future



Strong interest in the community! Many different types are under study, with the aim to achieve radiation hardness through depletion, high rate capability, low power, …..

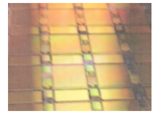
Enabling technologies are now available, which were not there some years ago ,e.g.:

"High" Voltage add-ons	Special processing add-ons (from automotive and power management applications) **increase the voltage handling capability** and create a depletion layer in a well's pn-junction of o(10-15 µm).
"High" Resistive Wafers	8" hi/mid **resistivity** silicon wafers accepted/qualified by the foundry. Create depletion layer due the high resistivity.
Technology features (130-180 nm)	Radiation hard processes with **multiple nested wells.** Foundry must accept some process/DRC changes in order to optimize the design for HEP.
Backside Processing	Wafer thinning from backside and backside implant to fabricate a **backside contact** after CMOS processing.

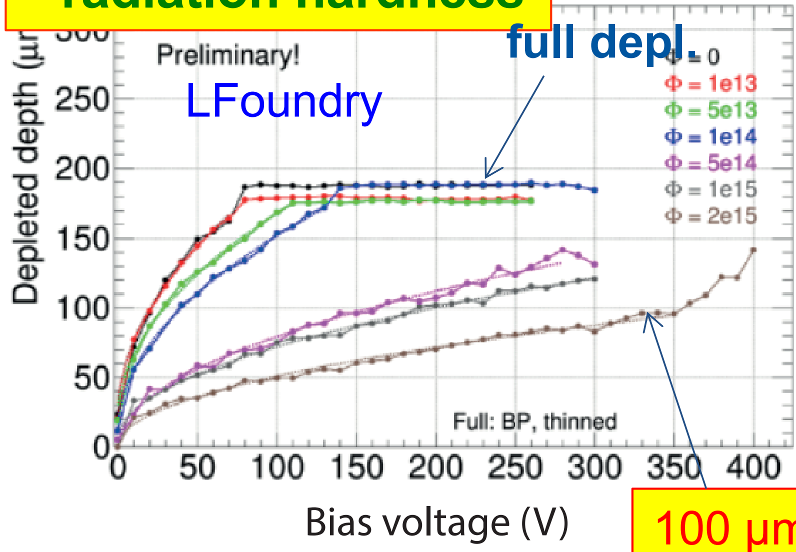


from: www.xfab.com

Many encouraging results…



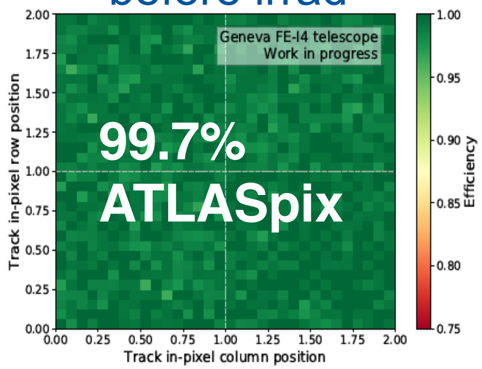
- **radiation hardness**

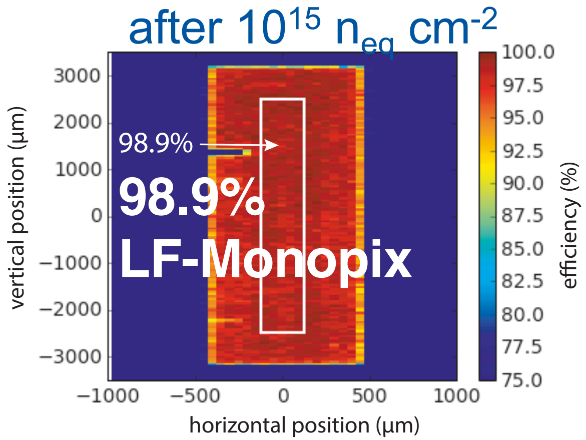


I. Mandić et al., JINST 12 (2017) no.02, P02021

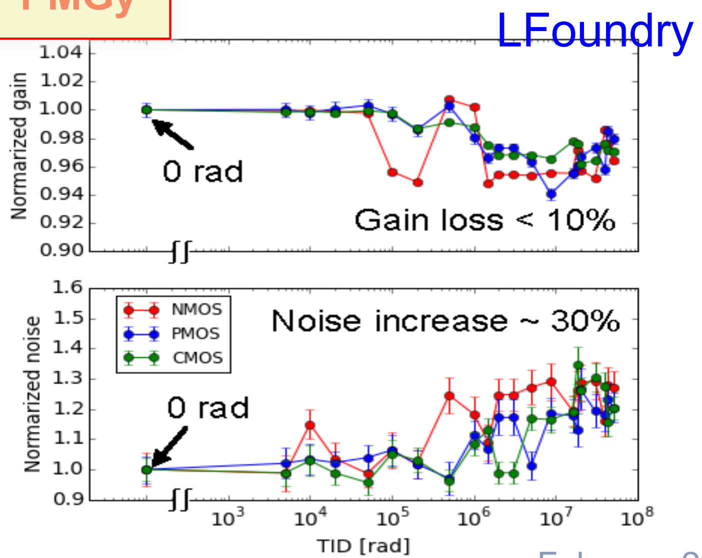
- **efficiency**

N. Wermes, HSTD11, Okinawa, 2017

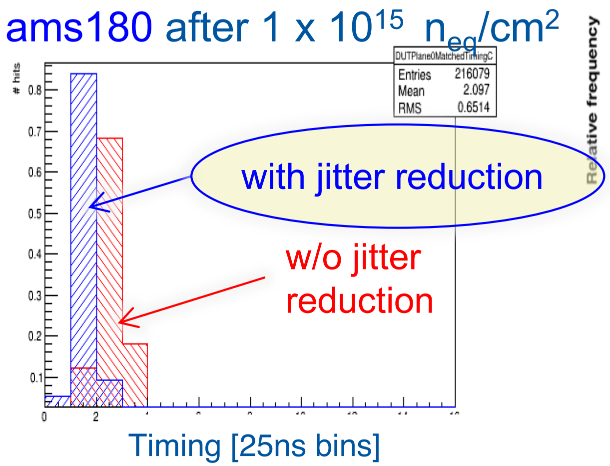


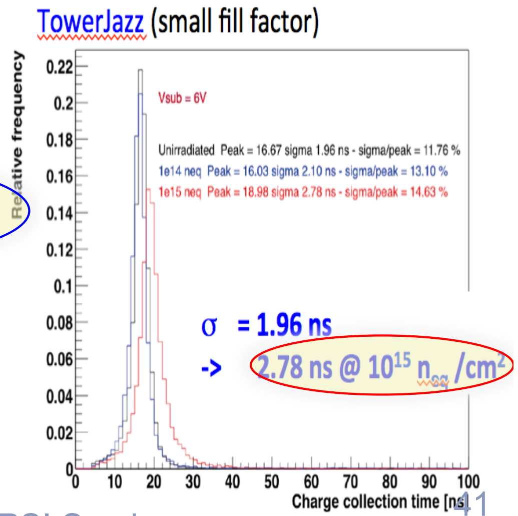


TID 1 MGy



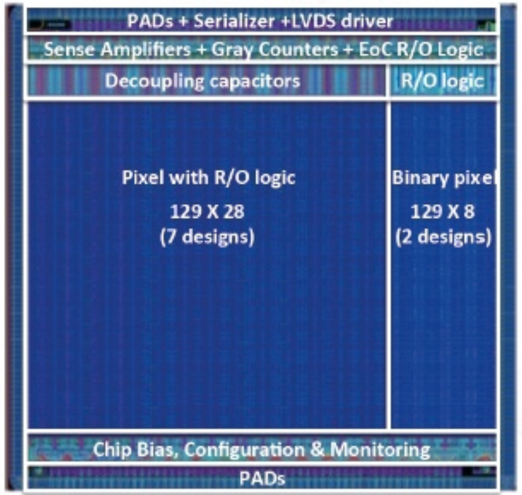
- **timing**

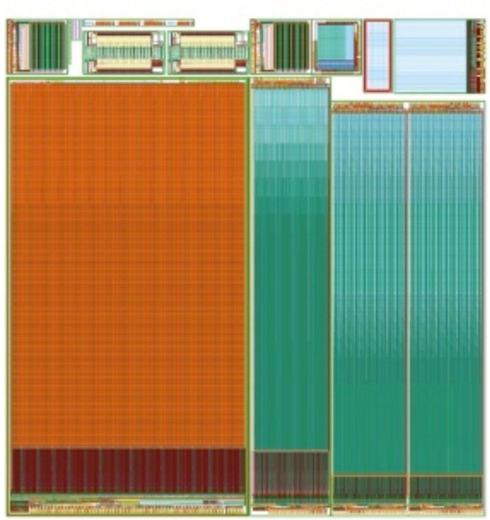


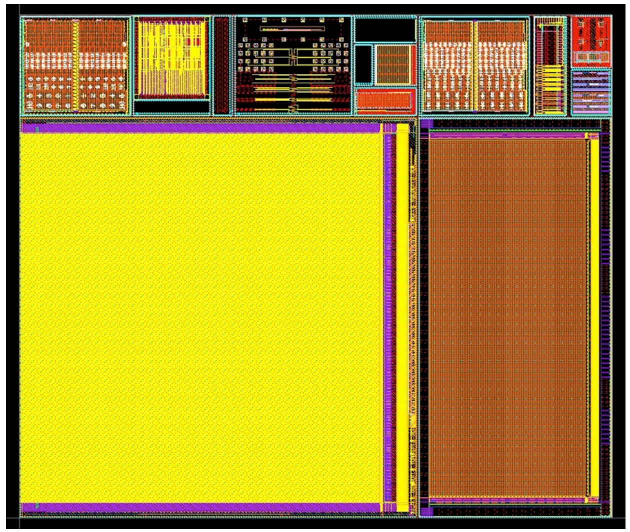


Moving to Larger Size Chips

Following the encouraging results obtained from test chips, larger size chips ($O(cm^2)$) have been designed and processed



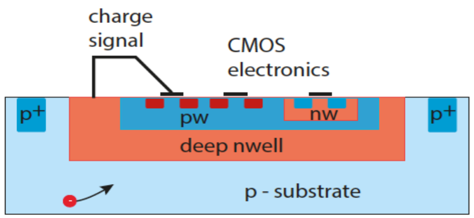




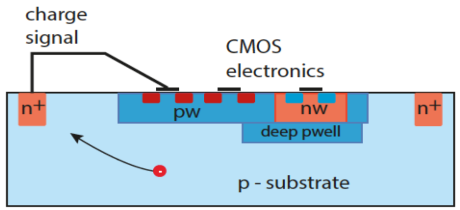
LFoundry 150 nm
substrate ρ > 2 kΩcm

ams 180 nm
substrate ρ ~ 0.08 - 1 kΩcm

TowerJazz 180 nm epitaxial (25 μm)
substrate ρ > kΩ cm



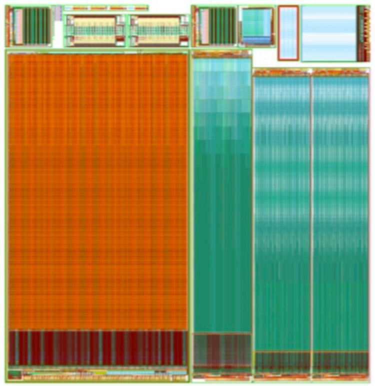
(a) Large fill-factor



(b) Small fill-factor

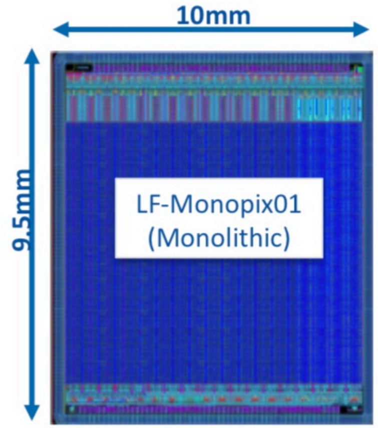
Chip name	Technology	CE Size*	Pixel size [μm²]	R/O architecture	Staust
aH18	AMS 180nm	Large	56 × 56	Asynchronous	Measurements
Malta	TowerJazz 180nm	Small	36 × 36	Asynchronous	Submitted Back after Xmas
TJ Monopix		Small	36 × 40	Synchronous	
LF Monopix	LFoundry 150 nm	Large	50 × 250	Synchronous	Measurements
Coolpix		Large	50 × 250	Synchronous	
LF2		Large	50 × 50	Synchronous	

* CE Size = Collection Electrode Size



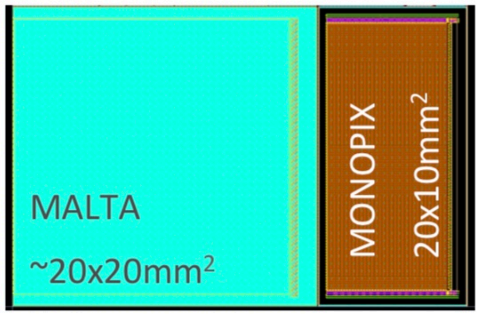
ATLAS Pix & MuPix

AMS 180 nm



MONOPIX, LF2 & COOLPIX

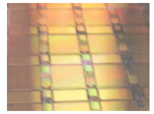
Lfoundry 150 nm



MONOPIX & MALTA

TowerJazz 180 nm

W. Snoeys, HSTD11, Okinawa, 2017



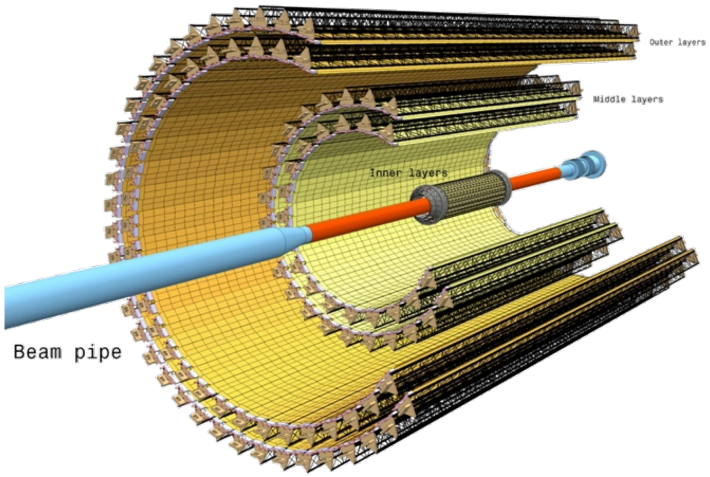
…really interesting times, indeed!

- The development of monolithic active pixel sensors have made significant progress in the last years.
- The STAR HFT pixel upgrade and the ALICE ITS upgrade are entirely based on MAPS.
- A lot of work is being done to make MAPS an attractive option for high rate and high radiation environments.
- We can expect some exciting results from new chips in the next months and will look out for new module assembly and interconnection ideas!

Spares

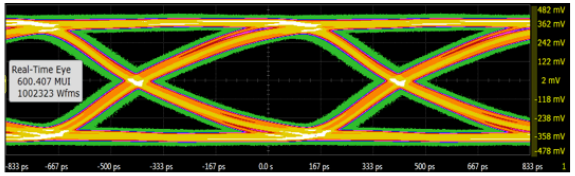
Readout

Detector



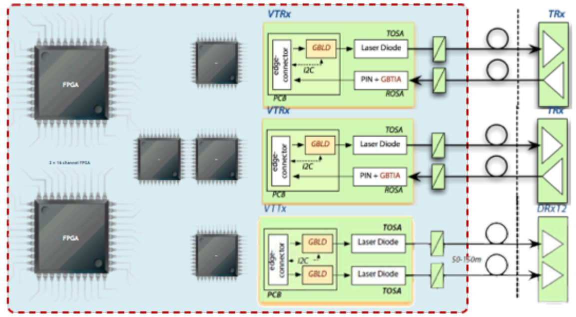
- Readout logic fully integrated into ALPIDE
- ALPIDE can directly drive 8 m cables using integrated high speed transmitters (up to1.2 Gb/s)
- No further electronics on detector

8 m cable



- 1.2 Gb/s (data IB)
- 400 Mb/s (data OB)
- 80 Mb/s (ctrl IB/OB)
- clock
- power

Readout Units



- Total: 192 Readout Units
- Distribute trigger and control signals
- Interface data links to ALICE DAQ
- Control power supply of chips
- Radiation level low enough to use (selected!) off-the-shelf electronics + soft-error mitigation techniques