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Research and development of silicon detectors for Future e^+e^- linear colliders

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Abstract

An overview of the recent R&D of silicon detectors in future e^+e^- Linear Colliders (FLC) is given. A particular emphasis on silicon devices for vertexing at the FLC is reviewed.

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Keywords: Silicon sensors; Future e^+e^- Linear Collider

1. Introduction

Future positron and electron linear colliders (FLC) will operate at energies from 500 GeV up to 1 TeV with a polarized electron beam and an upgrade option for positron beam polarization. The time scale for the FLC is that it operates concurrently with the Large Hadron Collider (LHC) at CERN. The accelerators and detectors for the FLC are being designed and developed at DESY (TESLA: TeV Energy Superconducting Linear Accelerator), Japan (GLC: Global Linear Collider) and US (Next Linear Collider) [1]. Two accelerator-technology options are being considered. The warm machine in the GLC/NLC and cold machine in the TESLA have room temperature and superconducting accelerating structures, respectively. A comparison of the beam structures in the two accelerator structures is given in Table 1.

The central main tracker options drive much of the detector configurations in the FLC. The Time Projection Chamber (TPC) and the silicon-tracking detectors are being designed as the central main tracker of the large detector (LD) and the small detector (SD) options, respectively, at the FLC. The innermost vertexing detector at the FLC will be very important for flavour-tagging performance. To achieve successful physics at the FLC, a pixelated vertexing detector is mandatory, with the smallest possible pixel sizes to provide good two-track separation and excellent pattern recognition. Physics simulation studies showed that the vertex

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Table 1
Comparison of the accelerator beam structures in the warm and cold machines

	Warm (GLC/NLC)	Cold (TESLA)
Bunch/train	192	2820
Train length	269 ns	950 μs
Bunch spacing (ns)	1.4	337
Train/s (Hz)	150/120	5
Gap/train (ms)	6.6	199

detector needs to have a thickness of 0.1–0.2% X_0 or less per layer for minimal multiple scattering, point resolution below 5 μm and an impact parameter resolution of $5\,\mu m \oplus 10\,\mu m/(p\sin^{3/2}\theta)$, where p is the momentum in GeV/c of the charged particle and θ is the angle of incidence of the charged particle with respect to the sensor surface.

The FLC environment requires silicon sensors which are substantially thinner and more precise than the LHC and thus motivates new directions for R&D on silicon sensors. This review will focus on the R&D of silicon devices for vertexing at the FLC and there is a brief discussion about ongoing R&D projects of the silicon detectors for tracking.

2. Vertex detector architectures

2.1. Charge coupled device (CCD)

The concept of the CCD is that the electrons released by a traversing particle are collected in a lightly doped thin layer and the technology of it is well established. The collected charge is manipulated by surface electrodes from buried channels to move along the columns toward the readout registers. The performance of CCDs at a positron and electron collider experiment was proven at the SLAC Large Detector (SLD) vertex detector [2] in the SLAC Linear Collider (SLC). The SLD vertex detector had 307 M pixels and its resolution is 3.7 μm for 20 μm square pixels. As baseline vertex-detector requirements for the FLC, a resolution of the order of 2 μm with $20 \times 20\,\mu m^2$ pixels is needed, which corresponds to about 1 G pixels on a full-scale detector.

Many R&D programs [3] have been carried for a CCD-based vertex detector suitable for the FLC operation environment. Since faster readout is needed for TESLA as shown in Table 1, a design of separate amplifier and readout for each column is considered. The concept of this design is that the charges from each column are moved toward readout circuits at the corner of the CCD. This is called a column parallel readout (CPCCD) and is illustrated in Fig. 1. A prototype of the CPCCD by E2V, CPC1, showed no degradation of noise performance. The CP readout ASIC by RAL, CPR1, was designed for 50 MHz clock speed with 250 parallel channels. A total noise of wire-bonded CPC1 and CPR1 is about $130e^-$ as shown in Fig. 2 and noise from the preamplifiers can be negligible (noise of CPC1 is about $100e^-$). The radiation tolerance of the CCD can be improved by sacrificial charge injection or faster readout before trapping. Fig. 3 shows that the CTI (Charge Transfer Inefficiency) at $5 \times 10^{11}\,e^-/cm^2$ electron irradiation is improved to the similar level of the ^{90}Sr result by fat charge injection in the CCD by a LED light [4]. The sacrificial charge fills up traps and improves CTI.

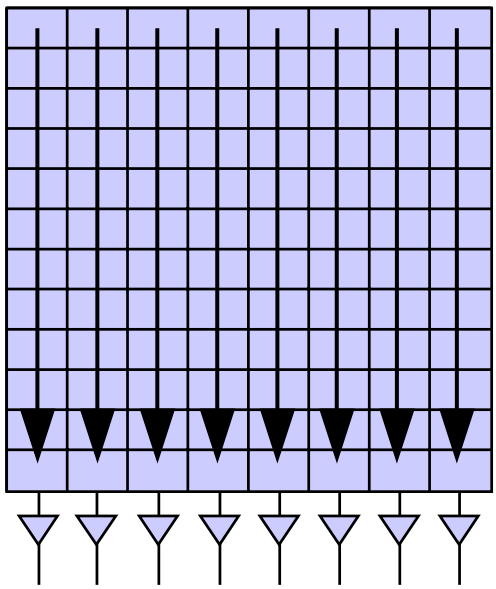

Fig. 1. The concept of a column parallel readout CCD (CPCCD) for faster readout.

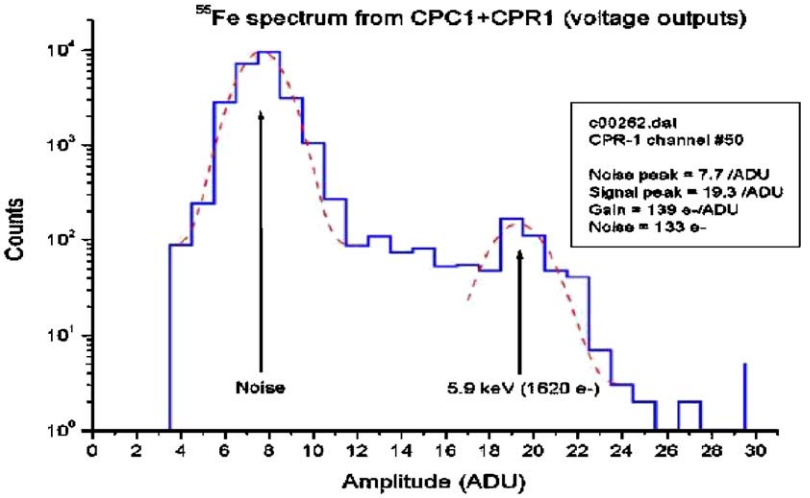

Fig. 2. Spectrum of 5.9 keV X-rays from a ^{55}Fe source for the CPCCD clocked at 50 MHz.

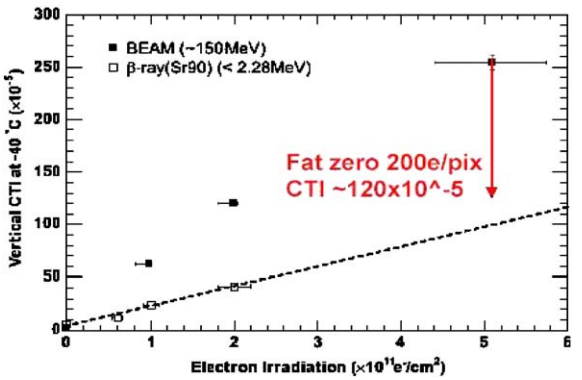

Fig. 3. The vertical charge transfer inefficiency (VCTI) is reduced by a factor of 2 by the sacrificial charge injection at the level of pair production electron background corresponding to 5 years of the FLC run.

2.2. Monolithic active pixel sensor (MAPS)

The MAPS is a novel silicon-detector technique which integrates all functions of a detector element and processing electronics on a standard CMOS wafer. The principle of the MAPS operation is illustrated in Fig. 4. The highly doped substrate creates a potential barrier and confines the charges. This increases the charge-collection efficiency. Because the signal charge is collected from the thin epitaxial layer, sensors have been thinned to 120 μm; this makes the MAPS very attractive as a vertex detector. Since no chip connections are needed, the same pixel size and precision determination of the position resolution as the CCD can be achieved. Much of the development has been concentrated on the MIMOSA chip [5].

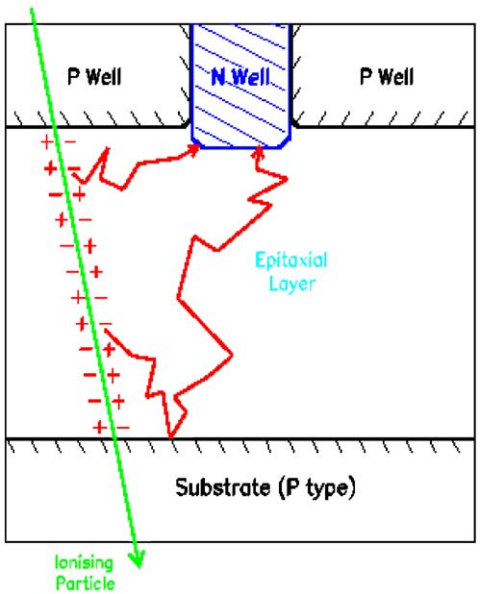

Fig. 4. The baseline of the MAPS operation. Since the charge is collected by diffusion from the epitaxial layer, the material budget of the detector is very attractive.

The MIMOSA prototypes with high granularity, minimal material budget and various options being investigated have been fabricated since 1999. The MIMOSA I chip achieved efficiencies of 99.5% with a 64×64 pixel array for a signal-to-noise cut of >5 and a resolution of 1.4 μm for $20 \times 20\,\mu m^2$ pixels. The MIMOSA II chip which has thinner epitaxial layer and higher speed showed a similar performance. A realistic scale MAPS is MIMOSA V, which was delivered in 2002, has 1 M pixels ($3.5\,cm^2 = 1.75 \times 1.75$, 17 μm pitch). A new approach based on the MAPS principle was considered in the following MIMOSA prototype, MIMOSA VI, to meet the requirements of the future linear collider detectors for the front-end electronics readout speed and data sparsification [6]. The MIMOSA VI, with a 4.2 μm epitaxial layer and device size $3.6 \times 0.84\,mm^2$ (pitch $28 \times 28\,\mu m^2$), is the first sensor with fully integrated signal processing. It has amplification and noise suppression on the pixel, a discriminator integrated on the chip periphery (1 per column) and CP readout (128 ch/line). Results from MIMOSA VI are shown in Fig. 5.

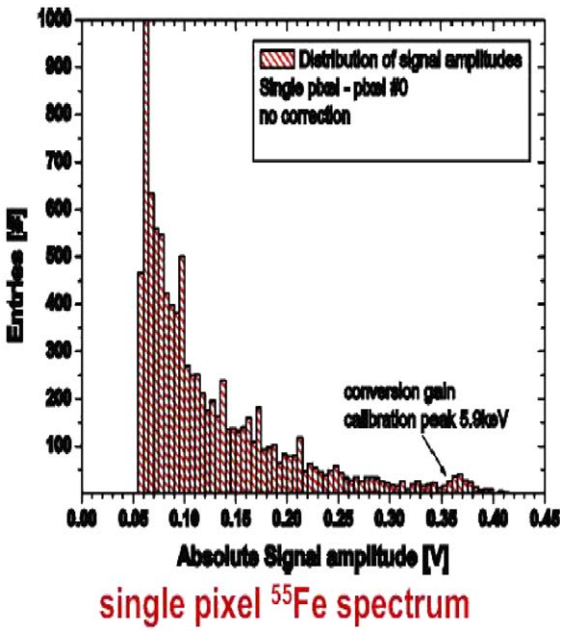

Fig. 5. Spectrum of single pixel clusters from 5.9 keV X-rays of a ^{55}Fe source for the MIMOSA VI.

An equivalent noise charge (ENC) of $20e^-$, a pixel dispersion of $120e^-$ and 6.5 nA/e^- of conversion gain are achieved. The next MIMOSA iteration with no epitaxial layer and with highly doped material to provide more flexibility in technology will be integrating pixel circuits with charge-sensitive elements similar to DEPFET (DEPleted Field Effect Transistor) but with all processing electronics integrated on the same circuit. Tests are in preparation and results are expected for the end of 2004. The MIMOSA I and II chips have been irradiated with neutron fluencies up to 10^{13} 1 MeV neutrons/cm^2 and the radiation performance showed that fluencies up to 10^{12} 1 MeV neutrons/$cm^2$are acceptable, considering FLC requirements which is about 10^9 n/cm^2/year. For ionizing irradiations, tests have been performed up to a few 100 kRad (the ionization radiation level due to the pair-produced electron background is expected to be of the order of 50 kRad/year) and there are performance losses. These could be due to parameters of the diode size and placements of the transistors. The exact sources of the charge losses are under investigation.

2.3. DEPleted Field Effect Transistor (DEPFET) sensor

The DEPFET structure has detector and amplification properties simultaneously. The sensor consists of the high-resistivity silicon substrate and fully depleted by sideward depletion [7] through an n^+ contact at the side of the sensor. The sensors were originally developed for X-ray applications but the TESLA vertex group [8] is pursuing FLC applications. Since the DEPFET has an excellent noise performance at room temperature and can achieve a good spatial resolution and a fast readout speed [9], the DEPFET is a promising candidate of future linear collider experiments.

Electrons from the traversing particles are collected in the internal gate and modify the transistor current to give the signal. The principle of the DEPFET detector-amplification structure is shown in Fig. 6. The first amplifying transistors are integrated directly into substrate and form the pixel structure. This allows a small input capaci-

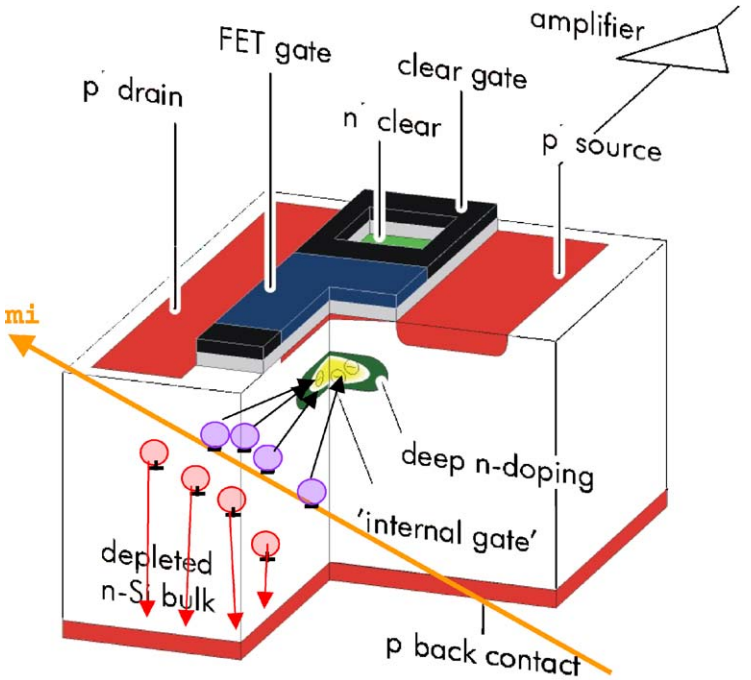

Fig. 6. Principle of the DEPFET structure which has detector and amplification properties simultaneously.

tance (~10 fF) and very low noise operation can be achieved at room temperature (10e$^-$). Since charge can also be collected in the turned-off mode, power consumption is very low. The possibility of thinning the sensor is being pursued. Thinning technology is that inner silicon oxide acts as a stop layer for the etchant, leaving the backside diode of the sensor wafer unaffected by the etching. The sensitive area is thinned to 50 μm and supported by a 300 μm thick frame [10]. To make the material budget less due to the support frame, a perforated frame (perforated frame: 0.05% of a radiation length, total: 0.11% X_0) is being developed. Fig. 7 shows a ^{55}Fe spectrum measured on a single DEPFET pixel at room temperature and excellent noise performance. For the operation mode, individual transistors or rows of transistors can be selected for readout while the other transistors are turned off. Those unpowered rows are still able to collect the signal charge. This makes fast random access to specific array regions and allows very low power consumption which will save material for the cooling structure.

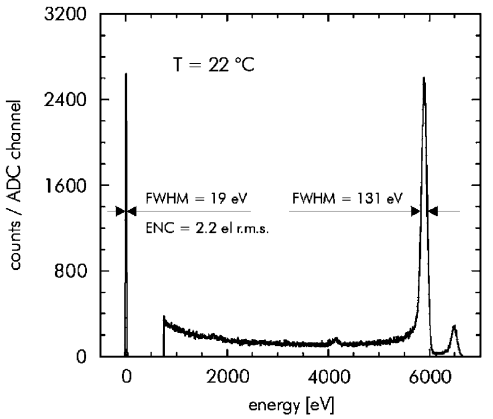

Fig. 7. ^{55}Fe source spectrum measured on a single DEPFET pixel at room temperature. The equivalent noise charge was fitted to be ENC = 2.2.

3. Silicon for tracking

One of the main purposes of the FLC is searching for the Higgs particle and studying its properties. For a Higgs tagging mode such as Z°H,

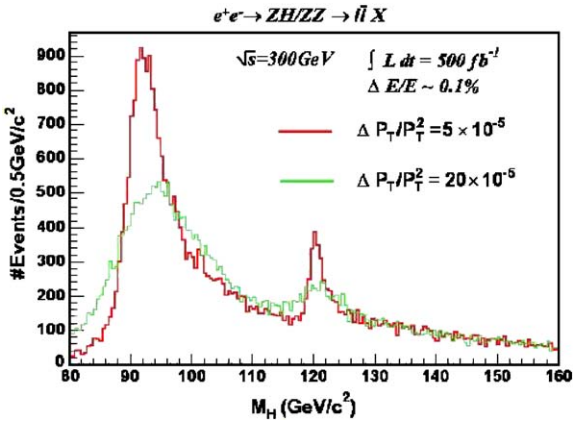

Fig. 8. Recoil mass distribution in $e^+e^- \to Z^\circ H$, $Z^\circ \to l^+l^-$ decay mode.

it is important to have good tracking resolution. It is clear that the tracking resolution ($\sigma(1/p_t)$) should be better than $5 \times 10^{-5}\,(\mathrm{GeV}/c)^{-1}$ from simulation studies as shown in Fig. 8. The silicon-tracking R&D activities [11] are applied to both detector configurations such as the SD and the LD: all-silicon tracking system or Si-envelop (Si tracking + TPC). The current ongoing tracking R&D includes the sensor design and fabrication of a single-sided silicon sensor with 100 μm pitch and a double-sided silicon sensor with 50 μm pitch on 380 μm thick of n-type high resistivity (5 KΩ cm) silicon wafer [12]. There are also R&D activities on prototype construction and front-end electronics for long ladders. Based on a simulation study for a 167 m ladder, ASIC design will incorporate 3 μs shaping-time and dual discriminator architecture. The design of the ASIC is now underway [13].

4. Summary

The CCD has well-proven performance at the SLD experiment and R&D programs such as improving slow readout speed, improving the radiation hardness, and room-temperature operation must continue for a suitable CCD-based detector for the FLC environment. Since 20 μm is enough thickness for detecting a charged particle, the reduction of material with unsupported silicon needs to be studied.

The MIMOSA prototypes studied since 1999 have shown consistently good performance with various options being investigated for different iterations. The performance showed that MIMOSA chips would easily withstand neutron fluencies of the FLC environment but performance tests should be done with whole system for more robust radiation hardness. Recently, using 0.35 μm CMOS, increasing functionality is being implemented at the periphery of the chip by the MAPS group.

A 64 × 64 matrix [14] of the DEPFET sensors showed the excellent low-noise performance at room temperature and low power consumption. R&D programs such as possibilities of thinning the sensor (20–30 μm) and readout chip, minimizing pixel size, and increasing readout speed and radiation tolerance are continuing for FLC vertexing applications.

The silicon tracking R&D activities including sensor design, fabrication, prototype construction and ASIC design for long ladders, are being carried on.

Intensive R&D in several technologies will surely be justified (cost effective) in terms of FLC physics reach. A premature choice of technology could seriously degrade the physics potential. Preferred technologies are to be selected on the basis of full-size and fully operational prototype detectors around 2010. Good world-wide communication of R&D efforts is building a proto-collaboration (CALICE, LC-TPC, SiLC) for the FLC detectors. We should reach the design phase of the actual detector within a few years.

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