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Analog front ends for highly segmented detectors

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Abstract

The evolution of analog front end ASICs is being driven by the increasing interest in fine-grained detectors and by rapid reduction in transistor feature size. Existing and proposed 2D pad and pixel detectors are moving towards higher segmentation in order to increase position resolution and/or signal-to-noise ratio. As pixel density increases above 10^4 pixels/cm^2, the power dissipation of the front-end ASIC becomes a serious constraint. We discuss the power-constrained noise optimization of ASIC front ends in scaled CMOS technology.
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1. Introduction

When a 2D detector is subdivided into finer and finer segments, not only does space-point resolution improve, but the signal-to-noise ratio also usually increases. Because of the lower capacitance, lower leakage current, and lower rate per pixel (hence longer shaping times) there will be less electronic noise. For most particle-tracking and photon counting applications the charge remains localized in a single pixel so there will not be a proportionate decrease in signal. Also, some detectors benefit from the so-called small-pixel effect, which effectively screens out charge induction from the undesirable hole or ion motion in the detector.

Since detector electrodes are most often produced photolithographically, the cost of a highly segmented detector depends on its area but is roughly independent of the number of pixels. By taking advantage of the low incremental cost of ASIC production one can control the cost of the front end electronic components—their power dissipation and interconnections become the major challenges.

2. Representative applications

2.1. Particle physics

High-density array detectors (pad/pixel) are in use or proposed at many accelerator experiments. The highest pixel densities presently under development are found in silicon hybrid pixel vertex detectors for use at the LHC [1]. For future linear colliders, three types of vertex detector are being explored. The monolithic active pixel sensor (MAPS) [2,3] has charge sensing diodes fabricated

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on standard CMOS wafers. Thinned CCDs with multi-column readout [4] and DEPFET arrays [5] are also being considered. Highly segmented detectors are also found in tracking pad chambers [6], Cherenkov imaging detectors, transition radiation detectors, and time projection chambers [7,8]. In each of these detectors, achieving low noise in the front end is important for efficient functioning of the detector. For instance, silicon tracking detectors must detect the small signal form a minimum ionizing particle, which may be further degraded by radiation-induced trapping and charge sharing, from noise. In gas proportional chambers low noise allows operation at low gain for longer lifetime, and may allow accurate position interpolation.

2.2. X-ray spectroscopy

Applications range from X-ray fluorescence studies at synchrotron sources [9] to instruments for nuclear medical imaging [10,11]. Position information is frequently not needed, but pixilated detectors allow good energy resolution at high rates over a large area detector.

2.3. Crystallography

Macromolecular crystallography at dedicated synchrotron beamlines demands large-area detectors with good position resolution. Such detectors can also be used as radiographic imagers. Recent developments are concentrating on pixilated solid-state detectors with bump-bonded CMOS readout circuitry [12–14]. Energy resolution is not critical, but low noise is needed to detect low-energy X-ray photons with good efficiency. Photon-counting circuitry is usually incorporated within each pixel.

2.4. Optical imaging

Scientific imaging in the visible wavelength range has traditionally been the domain of CCD sensors. Such devices avoid the need for per-pixel charge amplification by shifting charge across the array into a single readout amplifier. However, since the amplifier bandwidth limits the readout rate there is a tradeoff between readout speed and noise. Hybrid pixel devices, with light-sensitive silicon sensors bump-bonded to CMOS readout ASICs, are now being investigated for applications requiring high readout speed with low noise [15]. Similar hybrid sensors using low-bandgap semiconductors are used for infrared imaging.

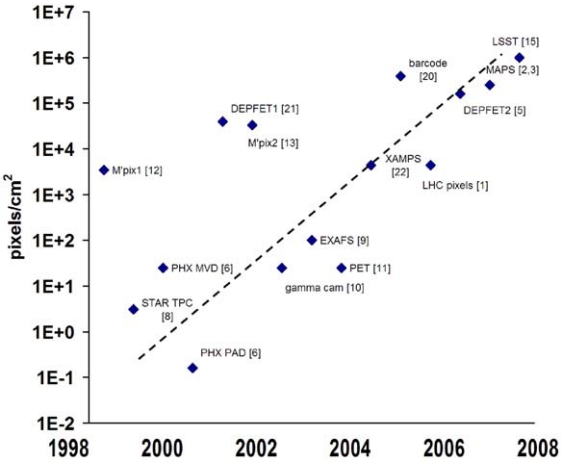

Fig. 1. Pixel density for existing and proposed area-array detectors. See also Refs. [1–3,5,6,8–13,15,20–22].

2.5. Pixel density trends

Fig. 1 shows the trend in pixel density compiled from a literature search of present and future array-based radiation detectors. From this figure, one can see a trend of exponential growth in pixel density with a doubling time of about 5 months. At the same time, projected total pixel count is also moving into the gigapixel regime for some projects.

3. Noise and power in CMOS front ends

It is likely that front-end electronics power dissipation will limit the achievable pixel density of proposed fine-grain detectors. To realize the low noise possibilities of pixel detectors with low-capacitance electrodes, the electronics must be located in close proximity to the detector. Detector temperature usually has to be controlled and kept at or below room temperature to prevent undesirable leakage currents or thermally induced gain

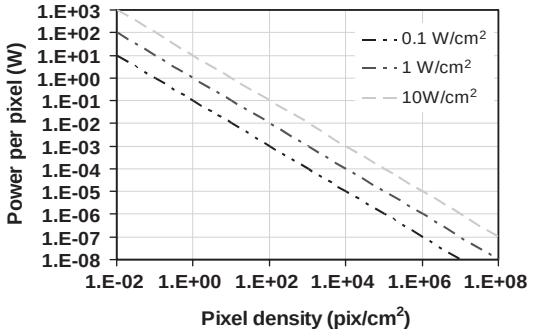

Fig. 2. Power dissipation per channel vs. pixel density. Dashed lines correspond to maximum heat removal capability of natural convection, forced air, and forced liquid cooling.

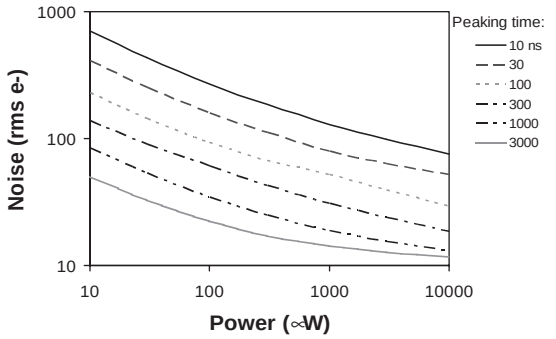

Fig. 3. Noise vs. power dissipation in the input NMOS transistor of a 0.25 μm CMOS charge-sensitive amplifier (simulated). Detector capacitance is 1 PF.

inhomogeneity. Therefore, available cooling technology must be considered when high density pixel electronics is designed.

Fig. 2 shows the allowed power dissipation per pixel versus pixel density, for three overall power density levels. The lowest level, 0.1 W/cm^2, corresponds roughly to the limiting heat flux that can be removed by natural air convection with 10°C temperature rise [16]. At the highest level, 10 W/cm^2, forced liquid cooling is required to limit the temperature rise to less than 10°C. It can be seen that as pixel densities exceed 10^4 cm^2, the electronics power budget will have to be at the microwatt per channel level to avoid exotic cooling schemes.

3.1. Optimum capacitive matching at constant power

Earlier published analyzes of CMOS noise optimization [17] emphasize the relationship of noise to detector capacitance and to shaping time. Now that detector trends force a strong power constraint on the electronics, it is important to clarify the tradeoff between noise and power dissipation in CMOS front ends. In a well-designed amplifier the noise should be dominated by the input transistor. In MOSFETs there are two noise sources, thermal noise of the channel and $1/f$ noise from interfaces. By increasing the bias current in the input transistor the contribution of the thermal noise can be reduced. For a given bias current and shaping time there is an optimum ratio C_{gs}/C_{det} that minimizes noise. Hence the input transistor has to be custom designed not only to match the detector capacitance and shaping time, but also according to the power budget. Unfortunately there is no closed form expression for this optimum device size especially in the submicron regime, and full-blown SPICE simulation is cumbersome and not always reliable. However, a simplified model based on the EKV equations [18,19] can be effectively used for optimization studies. The results are shown in Fig. 3 for 0.25 μm NMOS and a detector capacitance of 1 pF. The MOSFET length is set to the minimum allowed by the technology and the width is optimized for every combination of peaking time and power. It can be seen that noise decreases at a rate less than $P^{-0.4}$. For high power and long peaking time the $1/f$ noise dominates, and further increase in power has little effect on noise.

3.2. Filter order

Although noise originates in the preamp, the shaper weighting function must be chosen correctly. For a given rate-handling capability, the shaped pulse must return to baseline within a small fraction of the average interarrival time (Fig. 4). By choosing the most symmetric shape that satisfies the baseline return requirement, we lower the series noise weighting function to get a substantial reduction in noise. Higher-order shapers have more symmetric pulse shapes; however, they require a larger number of amplifier stages.

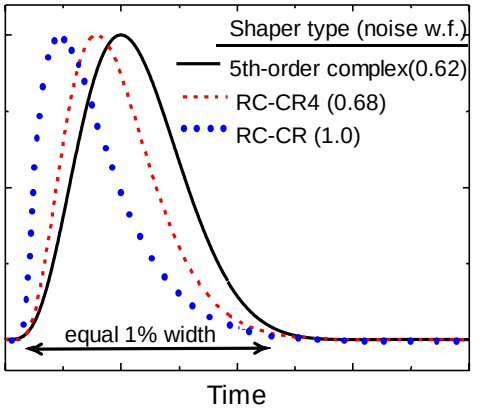

Fig. 4. Pulse shapes with equal return to baseline. Higher-order shapers have smaller series noise weighting function.

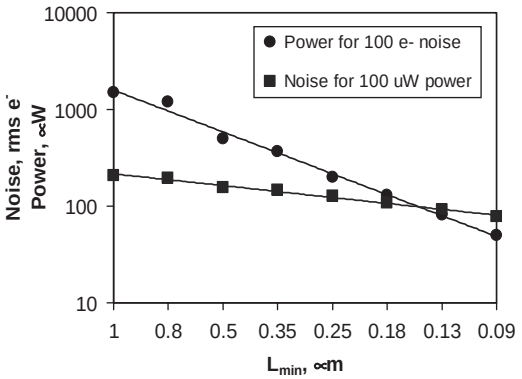

Fig. 5. Power and noise evolution with technology generation for CMOS charge-sensitive preamplifiers with NMOS front end. Detector capacitance = 1 PF, peaking time = 50 ns.

Increasing the shaper amplifier stages costs power, but may provide more noise improvement than by putting the equivalent number of milliwatts into the preamp.

3.3. Scaling effects

Using the same model discussed in Section 3.1, we can estimate the effects of CMOS scaling on noise performance. Fig. 5 shows the expected evolution of noise and power for CMOS charge-sensitive preamplifiers with 1 pF detector capacitance operating at 50 ns peaking time. It can be seen that noise is expected to decrease about 12% per generation at constant power, while power dissipation can be reduced 35% per generation while retaining the same noise performance. The assumptions used in these simulations were: classical scaling of transistor dimensions and doping levels; minimum gate length used in input NMOS transistor; and no increase in white thermal noise γ factor or $1/f$ noise coefficient K_F. Effects of gate tunneling current, expected to become significant below the 0.13 μm generation, were not included.

4. Interconnect issues

Mating the front end electronics to the detector electrodes introduces problems in selecting appropriate packaging/interconnect technology. The limits of conventional semiconductor packaging are shown in Fig. 6. Surface mount (quad flat pack, ball grid array), pin-grid array, and chip-on-board technologies are shown. For a given number of leads (pins, balls, or wirebonds) each type of package occupies a certain area. The ratio (number of leads divided by package area) is shown as a function of number of leads. For present-day surface mount technologies, there is an upper limit of about 100 interconnects per cm^2. Chip-on-board technology can increase the interconnect density by a small amount. For detectors with high pixel densities, new approaches to interconnecting the front end to the detector will

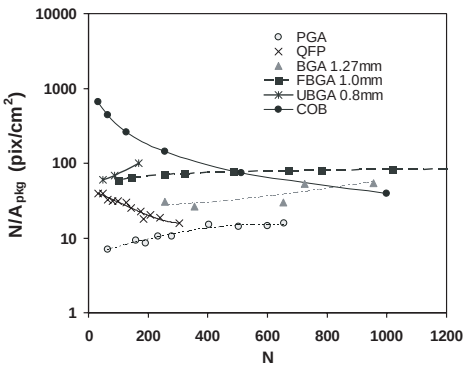

Fig. 6. Interconnect density of conventional integrated circuit packaging technologies.

need to be investigated. The hybrid approach (using solder balls to attach the detector directly to the readout ASIC) has been demonstrated with reasonable yield at the 10^4 pixels/cm^2 over areas of about 10 cm^2 [1] and above 10^5 pixels/cm^2 over 1 cm^2 [23].

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