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CCD-based vertex detectors

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Abstract

Over the past 20 years, CCD-based vertex detectors have been used to construct some of the most precise 'tracking microscopes' in particle physics. They were initially used by the ACCMOR collaboration for fixed target experiments in CERN, where they enabled the lifetimes of some of the shortest-lived charm particles to be measured precisely. The migration to collider experiments was accomplished in the SLD experiment, where the original 120 Mpixel detector was later upgraded to one with 307 Mpixels. This detector was used in a range of physics studies which exceeded the capability of the LEP detectors, including the most precise limit to date on the B_s mixing parameter. This success, and the high background hit densities that will inevitably be encountered at the future TeV-scale linear collider, have established the need for a silicon pixel-based vertex detector at this machine. The technical options have now been broadened to include a wide range of possible silicon imaging technologies as well as CCDs (monolithic and hybrid silicon pixel devices, DEPFET-based and SOI-based devices). However, there is a good chance that CCD-based detectors, or an architecture derived from CCDs, will still prove to be superior for this application. Groups in Europe, Asia and the USA are working semi-independently on various aspects of this development, with the goal of evaluating prototype detector elements within the next 5 years. If the CCD option is selected for one of the LC detector systems, it is hoped that these groups will join forces to construct the new detector. If the design goals can be achieved, this vertex detector will provide a tool not only for b and c tagging, but also for the measurement of 'vertex charge', allowing discrimination between b and $\bar{b}$ jets, and between c and $\bar{c}$ jets. Given the complex topological nature of much of the potential new physics in the TeV regime (multiple hadronic jets), such a tool could provide the key to unravel novel processes which may be unintelligible at the LHC.

Keywords: Pixel detectors; CCDs; Flavour ID; Linear colliders; Charm quark; Bottom quark

1. Introduction

CCD-based vertex detectors have been used for 20 years for the reconstruction of charm and bottom hadrons as well as tau leptons in fixed target and collider experiments. They have demonstrated the power of silicon pixel devices as tools for heavy flavour physics. Their particular attributes are small pixels, hence excellent spatial and 2-track resolution which permits them to be located close to the interaction point (IP), plus

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unsurpassed material budget (0.6% X_0 per layer in the SLD detector, with each layer providing unambiguous space point determination for each track). To date, CCDs are the only pixel devices to have been used successfully as vertex detectors for heavy flavour physics. Most past and present vertex detectors use silicon microstrips, but this nearly dominant position is about to change, as a variety of silicon pixel devices (CCDs, hybrid active pixel devices (HAPS), monolithic active pixels devices (MAPS), DEPFET arrays etc) are being developed for future experiments [1]. Indeed, we heard in this conference that every future experiment is now planning to use or considering using pixel devices for their next vertex detector. This is due to a combination of factors, such as their extreme rate capability, extreme radiation tolerance, as well as their fundamental attribute of precise and unambiguous space point determination. It is not possible to optimise all these features in the same detector, but it appears that the appropriate choice of pixel technology will provide the preferred vertex detector for a range of conditions: high luminosity hadron colliders, e^+e^- colliders (both B factories and the future TeV-scale linear collider or LC), heavy ion colliders (both RHIC and the LHC) and fixed target experiments.

The use of CCDs for vertex detectors was reviewed 6 years ago [2]. The interested reader is referred to that paper for a description of the early work. In this paper, we avoid covering the old ground, and provide an update to the earlier report. In recent years, the work has been primarily carried out by the GLC vertex collaboration [3], the US Linear Collider vertex collaboration [4] and the LCFI collaboration [5], in all cases directed towards the future LC.

2. Historical background

CCD-based vertex detectors have their roots in the discovery of the charm quark in 1974. After a challenging and only partly successful attempt by the ACCMOR collaboration at CERN to study the hadroproduction of charm particles using a single electron trigger, the emphasis shifted to observing their decays with silicon vertex detectors. The CERN-Munich group pioneered microstrip detectors, while the Rutherford Lab group explored CCDs, which had been invented a few years earlier at Bell Labs [6]. The possibility of using CCDs for particle tracking was explored theoretically in 1981 [7], and their capability for tracking minimum ionising particles with full efficiency and few micron precision was established experimentally in a CERN test beam in 1983 [8]. They were then used for some of the most precise charm lifetime measurements, and physics of charm hadroproduction, by the ACCMOR collaboration [9]. A combination of two CCDs placed 1 and 2 cm beyond the target, followed by 6 planes of microstrip detectors and a multiparticle spectrometer, provided one of the most powerful instruments ever built for the detection and lifetime measurement of charm particles.

Making the giant leap from fixed target experiments to the collider environment was carried out at SLD, for which R&D started in 1984. A first-generation detector of 120 Mpixels [10], installed in 1990, did some very good physics, and this was replaced by a 307 Mpixel upgrade detector [11], which continued till the end of running at SLD, being responsible (among other things) for setting what is still the most sensitive limit on the B_s^0 mixing parameter.

Over the past decade, the three collaborations mentioned above have been engaged in developing a much higher performance vertex detector for the future LC. Each has been exploring different ideas, but it is hoped that they will eventually join forces to produce a vertex detector for one of the experimental facilities (of which there will probably be a total of two) at the future machine. The preferred architecture for the LC vertex detector will depend on which accelerator technology is chosen (room temperature or superconducting RF cavities, the so-called warm and cold options).

From the detector point of view, the most essential difference between the accelerator technologies is the bunch structure of the colliding beams. At the warm machine, a bunch train consists of 190 bunches at 1.4 ns intervals, with a train frequency of 120 Hz. Detector backgrounds are sufficiently low that one can integrate the

signals through the train, reading out between trains. At the cold machine, a bunch train consists of 2820 bunches at 337 ns intervals, with a train frequency of only 5 Hz. Backgrounds integrated through the train would be excessive. For the vertex detector inner layer, it is necessary to divide the train into about 20 time slices, i.e., to read out the detector at approximately 50 μs intervals throughout the train of duration 1 ms.

In neither the warm nor the cold machine option is it guaranteed that CCDs will provide the optimal technology. There is unanimity within the LC community that silicon pixel devices will be used for vertex detectors at this machine, but beyond this there is healthy competition between different architectures (notably CCDs, MAPS, DEPFETs and an SOI-based design), any of which might prove superior. The various R&D groups are planning to develop full-scale prototypes so that choices can be made on the basis of performance achieved in test beams about 5 years from now, assuming that the LC adheres to its aggressive schedule of starting to do physics by 2015. In the meantime, it is not excluded that someone may come up with a revolutionary new idea, better than silicon pixels. In the case of SLC, the preferred vertex detector technology in 1982 was considered to be a rapid cycling bubble chamber! [12] Every technology sooner or later becomes obsolete, and over a 10 year period things can change a great deal. Imaginative young physicists are encouraged to take nothing for granted.

3. Current status of R&D programmes

A CCD in its most basic form consists of an array of pixels of dimensions typically 20 μm square, with the storage of signal charges being defined in one dimension by channel stops, and in the orthogonal dimension by voltages on polysilicon gates which overlay the imaging area. By manipulating these voltages, signal charges are moved physically towards the output node or nodes, where they are transferred onto the gates of voltage-sensing transistors for readout. There are numerous variations on this basic design, some of which have transformed this seemingly sluggish architecture into one which is matched to the requirements of particle physics experiments, and also to high speed photography, where the current record for a 100-frame burst camera is 10^6 frames per second. See Ref. [2] and references therein for a description of CCD operating principles, with particular emphasis on their use in vertex detectors.

The current R&D activities in this field can be divided into four categories. Firstly, physics simulations to define the appropriate technical goals for the TeV-scale linear collider. Secondly, the reduction of the layer thickness well below the figure of $0.6\%X_0$ achieved at SLD, probably to less than $0.1\%X_0$. (By layer thickness, we mean the total material budget, i.e., the thickness of the detector plus support structure, in each of the concentric barrel layers.) Thirdly, to understand the background radiation conditions and to develop a device architecture having sufficient radiation resistance. Fourthly, to design a detector which is compatible with the time structure of the collider. In this respect, the challenges presented by the warm and cold machines are quite different. In this section, we discuss the current status of the work in these four areas.

3.1. Physics studies, leading to overall detector layout

Before SLD, it was customary to think of the role of vertex detectors in collider experiments as primarily to permit B tagging, but the SLD experiment demonstrated that much more ambitious physics goals could be achieved. These lessons are particularly relevant to the TeV regime, where multi-jet events will be common, possibly involving production of Higgs bosons, supersymmetric and other heavy particles decaying to $q\bar{q}$ and more complex final states. A vertex detector matched to the physics goals of this environment will tag jets uniquely as light quark, c, $\bar{c}$, b and $\bar{b}$ separately, as well as identifying τ leptons. For example, the study of CP asymmetries in SUSY would require the efficient discrimination between b and $\bar{b}$ jets. The SLD experiment demonstrated that this can be achieved in cases of charged B hadrons by

measuring the vertex charge, and in cases of B_d^0 mesons by measuring the charge dipole [13].

The measurement of vertex charge is the most challenging technical requirement, since it depends on associating each track in a jet either with the primary vertex or with the $b/c/s$ decay chain, including the lowest momentum tracks for which the impact parameter resolution is dominated by multiple scattering in the beampipe and layer-1 of the vertex detector. While it is most important to carry out engineering studies to minimise the thickness of both, the most significant parameter in defining the achievable quality of the vertex charge measurement is the beampipe radius R_b. Here, ongoing dialogue with the accelerator physicists is essential. For example, there are trade-offs between R_b and L^*, the focal length of the final doublet, and it will be necessary to arrive at the correct balance between all parameters which influence the physics performance, such as flavour tagging, calorimetric hermeticity, particle flow information, and so on.

The 'default' vertex detector layout generally studied is sketched in Fig. 1. It consists of five concentric barrels, equally spaced in radius. The long barrels permit 3-hit coverage to $\cos\theta = 0.96$, which is probably as hermetic as will be feasible. Studies have been made of extending the polar angle coverage by means of forward disk detectors, but while these will be valuable in order to improve the tracking hermeticity, they are probably too far from the IP and behind too much material to be much use for flavour tagging. The five barrel layers permit standalone track reconstruction in the vertex detector, which is robust with respect to occasional missing hits due to detector inefficiency, and to high background hit density which will be encountered particularly on the inner layer. Standalone track reconstruction is important for two reasons. As found at SLD, independent track reconstruction in the vertex detector and in the main tracker permits each to be used to understand and correct deficiencies in the other. This is particularly important when commissioning these detectors. Secondly, such a layout is robust in terms of reconstructing low momentum tracks (which may not reach the outer tracker), handling γ conversions (absence of hits in the vertex detector inner layers being an important signature), reconstruction of hyperon and other short-lived strange particle decays, etc. A solenoid field of 4 T is sufficient to control the hit rate from the main background (low energy e^+e^- pairs produced by the beam–beam interaction at the

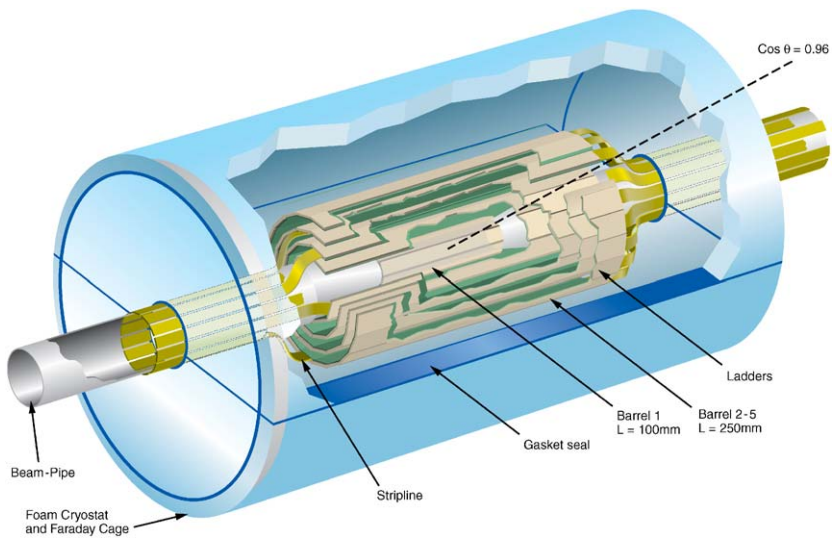

Fig. 1. Isometric view of the vertex detector. The beryllium shell supporting the ladders and stabilising the inner section of thin beampipe is not shown. The foam cryostat of outer radius approximately 12 cm permits operation of the gas-cooled detector at around 200 K or higher.

IP) for an inner layer radius of ~15 mm. It has been demonstrated that the 2-hit resolution of a CCD vertex detector with 20 μm square pixels is sufficient to ensure a low probability of hit merging even on the innermost layer, in the core of high energy hadronic jets.

The relationship between the detector parameters and the physics performance for this vertex detector layout has already been studied for *b* and charm tagging, based primarily on the topological vertexing program ZVTOP [14] developed for SLD, plus other information from the jet. The results [15] indicate that minimising the radius and thickness of the inner layer is the most important requirement in establishing the highest possible tagging purity for a given efficiency. Not surprisingly, this is most important for charm tagging, due to the shorter lifetimes and lower particle multiplicities in charm decays compared to bottom decays. The evaluation of vertex charge measurement now under way will extend the study to the most challenging physics requirements. As well as impact parameter resolution for low momentum tracks, there is another important reason to minimise the layer thickness. Photon conversions are particularly dangerous, given the goal of jet energy resolution by 'particle flow'. The probability of undesirable photon conversions is directly proportional to the layer thickness, unlike multiple scattering which scales only as the square root of the layer thickness.

3.2. Material budget

CCD tracking detectors use only the epitaxial silicon layer of thickness ~20 μm for signal generation, so the CCDs can in principle be thinned to the edge of this layer. Those used in SLD were thinned to about 150 μm, at which point the unsupported devices become significantly bowed due to internal stresses present in the processed surface of the wafer. In the 'unsupported silicon' option for ladder construction, it was proposed to largely eliminate this bowing and achieve mechanically stable ladders by spring tensioning from one end. Preliminary experimental studies were encouraging, but this approach is now considered to be perhaps overly ambitious, due to the tendency of the devices also to curl significantly across their width, a problem that is difficult to control by tensioning without adding material in the tracking volume.

For this reason, attention has now turned to other options, such as the 'semi-supported' structure, in which the thin silicon is attached to a mechanical substrate (beryllium, carbon fibre or some foam material such as silicon carbide). This substrate can also be thin, and stabilised along its length by tension, but can have sufficient stiffness to resist the tendency of the CCD to curl across its width. There are differential contraction issues to be considered in such assemblies, but these become less severe if the detector can be operated near room temperature, in contrast to the operating temperature of 180 K that was necessary at SLD. The GLC collaboration has been particularly active in exploring the possibility of operation near to room temperature, with encouraging results. As at SLD, it appears that the CCD-based detector can be designed to dissipate on average only some tens of watts in the fiducial volume, so gas cooling will suffice. Piped liquid or evaporative cooling should be avoided if at all possible, since this would impose an excessive contribution to the material budget.

Overall, there is good reason to expect that a design goal of 0.05–0.10% X_0 per layer may be achieved. As in any vertex detector, the material budget beyond the active volume will need to be higher than this. The ends of the CCDs will have readout chips bump-bonded to them, whose power dissipation could possibly necessitate tubes filled with liquid coolant. There will in addition be thin copper–kapton flex circuits carrying power in and digitised sparsified data out, routed along the surface of the beampipe, from each ladder end. For the DAQ system, it is envisaged that LVDS signals will be converted to optical data in the SR masking region where material is no longer so important, and transmitted out with only a single optic fibre being required at each end of the detector.

It is believed that the inner section of the beryllium beampipe of length 10 cm can have a wall thickness as low as 0.4 mm. This is more than enough to withstand the vacuum; the more

stringent requirement comes from stresses during the installation and removal of the beampipe/vertex detector assembly. But here one can take advantage of the fact that beyond the volume used for the very highest precision tracking, the vertex detector ladders are supported by a pair of beryllium half-shells which are clamped to one another and to the outer sections of beampipe. Using this support shell to help stabilise the beampipe permits a reduction in the strength required for the innermost section which is most critical for particle tracking. With a carefully planned installation strategy, it is believed that a wall thickness of 0.4 mm will suffice. A titanium liner is conventionally added to the beampipe to absorb fluorescence X-rays. A useful reduction in material budget where it matters most may be possible by relocating this liner on the surface of the vertex detector support shell. This assumes that the exceptional granularity of the 900 Mpixel vertex detector may make it tolerant of the background due to this flux of soft X-rays, but this question has still to be studied quantitatively.

The currently estimated material budget of the vertex detector is indicated in Fig. 2. For particles with 90° polar angle, the total material inside layer-5 may be kept below 0.5% X_0. This may increase or decrease in future, in the light of ongoing thin ladder R&D programme, together with guidance from the physics studies.

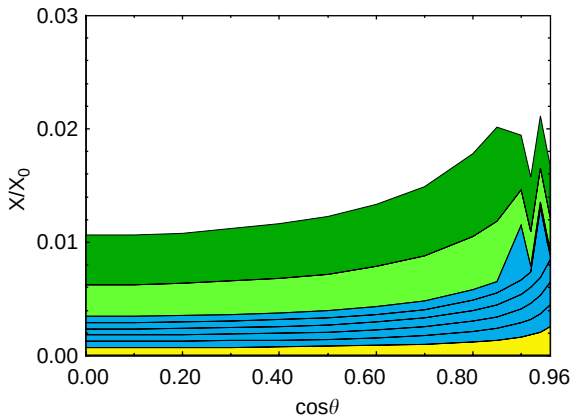

Fig. 2. Material budget as function of polar angle (the plot shows in turn from the bottom the beampipe, each of 5 layers, support shell and cryostat).

3.3. Radiation resistance

The most serious radiation effect in a CCD is bulk damage in the buried channel of the device, the volume in which the signal charge packets are collected and then transferred. In their long journey to the output node of the device (up to 6250 transfers in the outer CCDs of the default design) a charge transfer inefficiency (CTI) of 0.5×10^{-4} would result in a signal loss of up to 27%, which is about the worst one could tolerate before a significant hit inefficiency would be encountered.

The bulk damage at the LC will arise mainly from the e^+e^- pairs produced by the beam–beam interaction at the IP. Though they have typical energies of only ~20 MeV, it has been shown by the GLC group that these electrons will induce cluster damage as well as point defects [16], both of which degrade the CTE. The effects of neutron-induced damage clusters are more serious, but because of the low neutron flux at the interaction region (IR) of the LC (neutrons coming from the beamstrahlung dump and beam dump) they have less overall effect than the pair electrons. Furthermore, the US group has made an interesting discovery regarding neutron damage. They have observed that the trapping of signal charge shows an unexpected time dependence. By observing the effects of individual damage clusters in different pixels, they find that some of them trap signal charge rapidly, as would be expected from a simple calculation based on the known trapping time constant. However, other pixels experience much longer trapping times, up to many milliseconds [17]. A possible explanation could be that these particular damage clusters happen to lie slightly beyond the edge of the storage volume occupied by the signal charge, which can then only be captured when thermal fluctuations drive signal electrons one by one into the trapping volume. Further measurements and full simulations of these effects are now under way, to establish quantitatively whether such an explanation fits all the facts.

Between the GLC and US groups, there are valuable measurements of radiation-induced CTI in a variety of CCD structures. However, these do not translate directly into a lifetime estimate for

the LC vertex detector, because the CTI is a function of a number of negotiable parameters:

- storage volume (so 'notch' or 'supplementary channel' architecture can help) [18],
- clocking rate (faster clocking is beneficial, and is achievable with the column-parallel CCD (CPCCD)),
- operating temperature (lower temperature can dramatically reduce CTI),
- trap occupancy (so the high hit rate from the pair electron background is beneficial).

Preliminary calculations suggest that, as at SLD, it will be possible to design a CCD-based vertex detector with adequate radiation hardness for the LC environment. If the cold machine is selected and the novel architecture discussed in Section 3.4 is adopted, the maximum number of charge transfers would be reduced from 6250 to only 20. Thus a by-product of this approach would be that such devices will have orders of magnitude higher radiation resistance than will be required for the LC. This would open up potential applications in environments where radiation levels are far too hostile for the use of conventional CCDs.

3.4. Timing issues

If the warm machine is selected, conditions for DAQ will be similar to those at SLC. The background hit density integrated through the bunch train (190 bunches at 1.4 ns interval) will be sufficiently modest, even at the innermost layer of the vertex detector, to permit clean standalone track reconstruction in the vertex detector with a negligible level of ambiguous or spoiled (merged) hits. There will be a significant rate of low momentum tracks due to pair electrons, but these particles will also be detected in the forward tracking system, where most of them will be rejected by the fast timing information to be provided by those detectors (silicon hybrid pixels or microstrips). For the vertex detector, the only timing requirement is that it should be read out completely in the 8 ms between bunch trains. This can be accomplished easily with the CPCCD architecture (using a very relaxed 1 MHz clocking rate), or with a more conventional multi-port CCD, having its outputs wire bonded to the readout chip.

A CPCCD readout chip has already been implemented in prototype form by the LCFI collaboration, using a 0.25 μm CMOS process. It has separate channels on 20 μm pitch, each incorporating signal amplifier, correlated double sampling (CDS), 5-bit ADC and on-board memory. The final form of this chip will include data sparsification based on a pixel threshold followed by cluster threshold, as previously used for readout of the 307 Mpixel SLD detector [11]. Data from each readout chip at the ladder ends will be transferred via an LVDS cable to a local electro-optical converter, then out of the detector via a single optical fibre at each end.

If the cold machine is selected, the situation will be more challenging[1]. Background accumulated during the bunch train of 1 ms duration would be 20 times higher than for a bunch train at the warm machine. In order to solve this problem, it was suggested in 1998 to read out the detector repeatedly at 50 μs intervals throughout the train. While this strategy was adopted by the proponents of all silicon pixel technologies considered for the LC vertex detector (CCDs, MAPS, DEPFET, etc), it will in itself create major challenges. What makes this approach dubious is the experience at SLD of beam-induced electromagnetic interference (EMI). It is likely that this will always be worse for a vertex detector at a linear collider than at a circular machine, for several reasons. Firstly, the collimators and beam-position monitors near the final focus induce large wakefields which disrupt the beams. These are tolerable only because the beams pass through them once only—the cumulative effects of such disruptive components in storage rings would be intolerable. This instrumentation is obligatory at the IR of a linear collider in order to meet the challenge of maintaining luminosity with nanometre-sized beams. Secondly, the ceramic feedthroughs and

[1]On 20th August 2004, since writing this paper, ICFA announced that the cold technology has been selected. This means that the vertex detector groups have to deal with the more difficult of the two scenarios.

imperfect coax cables associated with these instruments, as well as apertures for vac pumps, etc, provide escape routes for the RF, as does the thin-walled inner section of the beampipe, which due to the finite skin depth is not perfectly opaque to RF. Thirdly, escaping RF radiation is particularly likely to cause problems for the vertex detector, where the tiny signal charges from about 20 μm active thickness of silicon must be sensed by a high bandwidth circuit with minimal input capacitance—such a circuit being particularly prone to EMI. Furthermore, the pixel-based vertex detector has about 10^9 channels, far more than any other detector in the system, so a tiny fraction of false signals could severely overload the DAQ system. In SLD, the vertex detector electronics was completely disrupted by beam-related pickup for some tens of microseconds after the bunch crossing, and was even then subject to a low level of EMI during the readout period. The former problem was solved by waiting for conditions to settle down, and the latter by using an extension of the correlated double sampling (CDS) technique, the so-called extended row filter [11].

For these reasons, it may be that multiple readout through the bunch train at the cold machine simply will not work. Tests will be carried out in a high energy electron beam at SLAC, and it is possible that the means will be found to suppress EMI to such a level compared to SLD that the problem will be solved. However, this seems unlikely, given the multitude of details on which beam-induced and other sources of EMI depend, and the likelihood that not all these details will be precisely the same in the real IR as in any test facility. Once the real detector is closed up and commissioning begins, it will be almost impossible to investigate such problems, because one cannot run beams with the detector open, as would be needed to operate equipment monitoring EMI conditions close to the IP.

These concerns have led to a variation of the CCD design concept that might be appropriate for the cold machine. We subsequently learned that this concept has already been developed, in the form of a high speed imaging device able to operate at 1 Mframe/s for 100 frames [19], where it is called the 'imaging system with in situ storage' (ISIS). The variant that we are considering for the vertex detector at the cold machine works as follows. The structure (Fig. 3) consists of an array of photogates arranged on a nearly square (slightly trapezoidal) array of dimension 20 μm. These are the charge collection nodes for the imaging pixels in the device. The CCD structure (n-type buried channel) is embedded in a deep p-well. This provides a reflective barrier so that collection of the signal charge by the photogates proceeds by diffusion of electrons generated within the epitaxial layer, as in a conventional CCD. Each photogate is adjacent to a 20-element linear CCD storage register plus conventional charge sensing output circuit. The layout is shown in a more realistic plan view in Fig. 4. Each of the large shaded rectangles at the end of the storage register contains an output circuit, as sketched on the right. Each source follower output of the charge sensing circuit is connected via a row select switch to a busline which runs the full length of the CCD, and is bump-bonded at the edge of the active area to a readout chip having signal inputs at the column pitch of 20 μm, just as in the CPCCD.

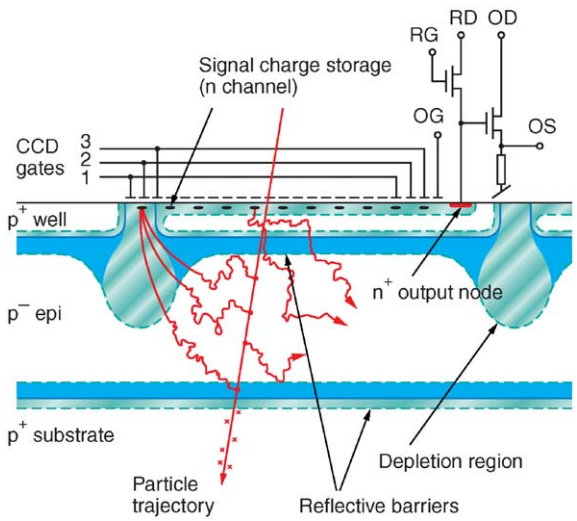

Fig. 3. Sketch of ISIS cross-section (not to scale). Signal charge is reflected from the p^-/p^+ edges above and below the epitaxial layer, so it diffuses within this layer till being collected in the depleted regions beneath the photogates. 10 storage pixels are shown: for the real detector there would be 20.

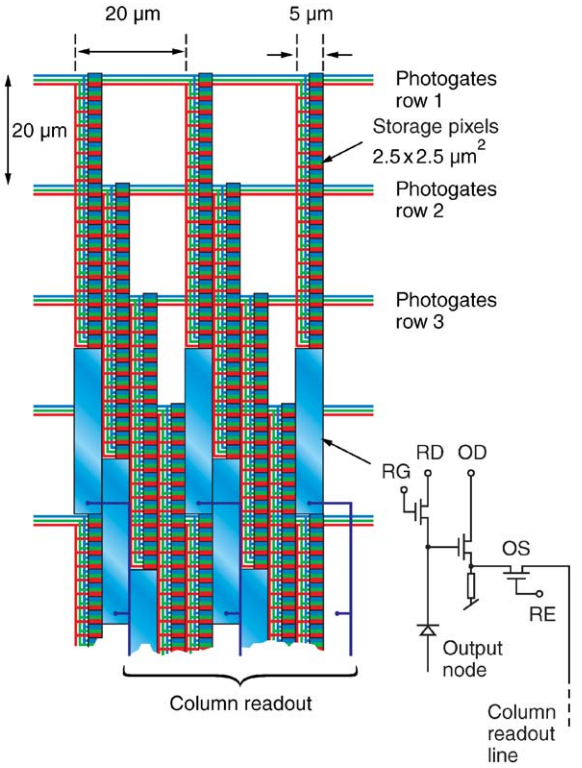

Fig. 4. Top LH corner of ISIS. Photogates are arranged on a regular trapezoidal matrix of elements with 20 μm pitch located at the upper end of each storage register. The tracks to the left of the storage registers represent schematically the buslines which distribute the external potentials to the 3-phase CCD gates. The column readout lines extend over the full length of the device, up to 12.5 cm for the largest devices. During readout, the source follower circuits are connected one row at a time by the Row Enable transistors (RE) to the column readout lines.

During the bunch train, signals accumulated under the photogate are shifted every 50 μs into the adjacent storage register. By the end of the train, the time-sliced signals are stored as charge in the buried channel of the CCD. This method of signal storage is extremely robust, for two reasons. Firstly, to disturb the stored charges, it would be necessary to create ~1 V fluctuations in gate potentials, whereas the signals when converted to voltage amount to typically ~1 mV. Secondly, the CCD gate capacitances are typically some nanofarad, in contrast to the tiny node capacitances of some tens of femifarad. It follows that CCD charge storage provides a factor $\sim 10^6$ greater immunity to EMI than would be achieved by conversion to voltage during the train. This enhanced immunity is achieved by comparison with any of the architectures considered for the LC vertex detector, not only the CCD option. After the end of the bunch train, once the beam-induced RF has died away, the detector is read out. Edge logic, running along the side of the active area, is used to enable one row at a time. Data from all the imaging pixels in that row (20 stored signals/pixel) are read via the output lines, one line per imaging pixel, and sensed by the input circuits on the readout chip. The charge signals which have been accumulated on the CCD nodes for this row are then dumped via the reset drains, while the register clocking is switched to the next row to be read. Reading at a relaxed rate of 1 μs per storage pixel requires a readout time for the largest CCD of $6250 \times 20\,\mu s = 125\,ms$, comfortably within the inter-train period of 200 ms.

It is not necessary to curl up the storage register within the 20 μm square pixel area; it suffices to fit the entire circuit within any rectangular region of area 400 μm^2. This could be achieved with the arrangement sketched in Fig. 4, in which the region allocated to each pixel amounts to $5 \times 80\,\mu m^2$. Discussions with manufacturers of CCDs and CMOS pixel arrays suggest that such a device architecture may be within the capability of currently available technology. However, the desired size of imaging pixels of 20 μm square is challenging. It is not yet clear whether this goal is achievable, nor whether the best hope is by adapting a CCD or CMOS process. A 16×16 element test device with larger pixels, to provide proof of principle for a particle detector, will be manufactured by the end of this year. Should the cold machine be selected, this will be followed by an intensive R&D programme. Given that the timescale for LC physics will be around 2015, one can afford to continue R&D for the vertex detector till about 2010. By that time, an ISIS-type detector with 20 μm pixels will very probably be within the capability of some manufacturers of scientific imaging devices. If the warm machine is selected, the problems are reduced and the next

step will be large CPCCDs with which to assemble full scale prototype ladders.

4. Conclusions

CCD-based vertex detectors have become established over the past 20 years as powerful tools for heavy flavour physics, and for studying high energy processes in which the identification of the leading heavy flavour quarks in jets is important. Although the number of experiments in which they have been used is small, CCDs have delivered the highest performance of any vertex detector architecture. World-wide R&D programmes are currently making excellent progress in the continued evolution of this technology towards a vertex detector at the TeV-scale linear collider.

If the warm machine is selected, the vertex detector requirements will be satisfied by a relatively straightforward extrapolation from the SLD design. Whether to use a CPCCD with every column bump-bonded to the readout chip, or a more conventional multi-port CCD with say 16 outputs wire-bonded, and whether to operate near room temperature or considerably colder, are details which will be decided by the world-wide R&D programme. On the basis of work already completed, one can be confident of a highly competitive vertex detector, which will be well matched to the physics requirements.

For the cold machine, we and all the current technology options face a dilemma, whether or not to hope that multiple readout through the bunch train will be feasible. It may be that studies of EMI in test beams will provide reassurance, but this should not be assumed. For this reason, if the cold option is chosen, we intend to pursue an aggressive R&D programme to establish the ISIS architecture for particle tracking. Since this combines features of both CCD and CMOS imagers, there is not a natural match to the current capabilities of CCD manufacturers. However, we are by no means alone in needing such advanced designs, and several companies are currently developing the necessary capability. Whether essential to overcome EMI or not, the ISIS approach may be preferred due to its other distinct advantages: much reduced power dissipation, greatly enhanced radiation resistance and enhanced spatial precision due to the relaxed readout speed.

The TeV-scale LC may pay enormous physics dividends, such as the discovery of SUSY particles, and precise measurement of their properties. To exploit this potential, a vertex detector (and also an electromagnetic calorimeter) of unprecedented performance will be needed. Through the efforts of the GLC, US and LCFI collaborations, we are well on the way to a vertex detector design that will satisfy these requirements. Once full-scale prototype ladders have been constructed, their tracking efficiency, spatial resolution, etc will be measured in test beams. These results, together with knowledge of the material thickness, readout speed and power dissipation, will be used by the LC experiment collaboration(s) to decide which technology or technologies to include in their overall detector systems. Based on past experience, one can expect ongoing advances in silicon imaging devices, driven partly by very different application areas, to lead to yet more powerful vertex detectors in the future. For this and other reasons, convenient access to the vertex detector, as well as to other equipment at small radius in the heart of the overall detector, will be mandatory. The design concept developed by the SLD collaboration for access to their small-radius equipment looks most attractive. With the endcap detector systems fully opened, the central tracker is transferred to a support rail so that it can be rolled along the beam axis by its full length, thereby exposing the inner tracking system, the vertex detector and other IR instrumentation. By establishing this as a design constraint from the beginning, it will be possible to avoid the problems encountered in some detector systems in which the small-radius detectors were virtually inaccessible without a major shutdown.

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