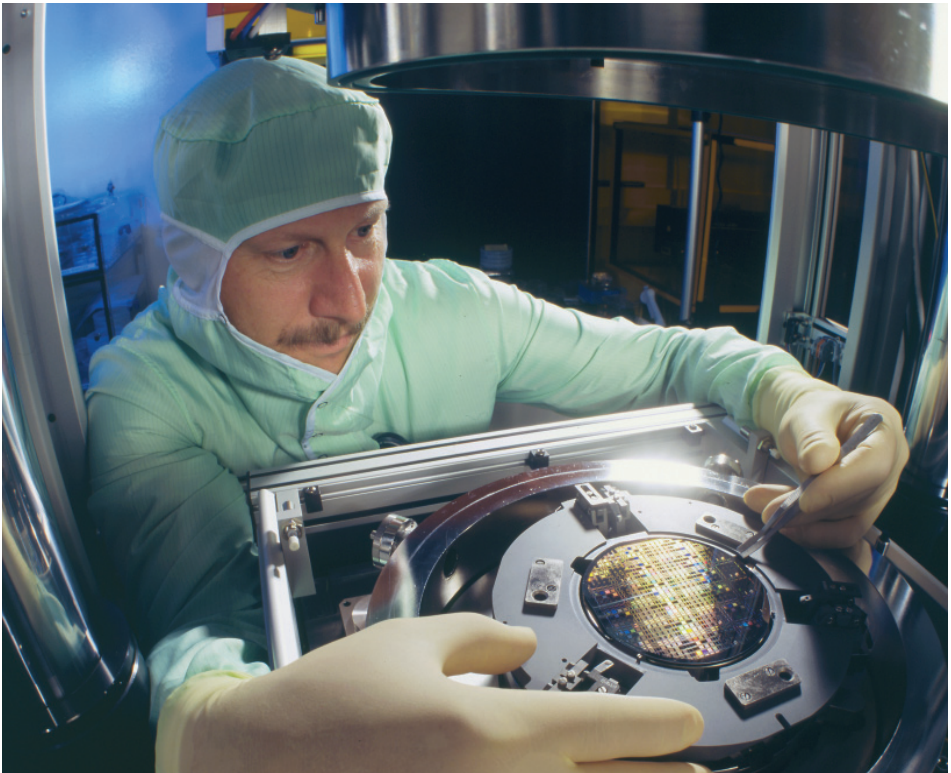


NaPa

Emerging Nanopatterning Methods



Library of Processes

Nanopatterning and Applications

First Edition with results of the NaPa-project, March 2008

Editor: H. Schiff

Publisher: J. Ahopelto, NaPa Consortium

NaPa – Library of Processes

Nanopatterning and Applications

First edition with results of the NaPa-project, March 2008

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NaPa - Library of Processes

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Disclaimer

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This library intends to be of help for a researcher, engineer or technician experienced in basic chemical and lithographic processes. It is intended for a person who is familiar with basic cleanroom and chemical process knowledge. The processes described in this library do not have the same level of maturity. Some of the recipes cannot be used without significant own further development. Therefore, the user should make a distinction between processes which are ready to use or which are still in development.

The “NaPa” Project

From 2004 to 2008, the EU Integrated Project “Emerging Nanopatterning Methods” (NaPa) brought together 35 leading academic and industrial European institutions with a vast amount of know-how in nanofabrication. In total, the partners contributed 4’500 person months to the project. The NaPa consortium integrated the new patterning methods, **Nanoimprint Lithography**, **Soft Lithography & Self-assembly** and **MEMS-based Nanopatterning**, into one project, both anticipating and responding to the increasing need for technologies, standards and metrology required to harness the new application-relevant properties of engineered structures with nm-scale features. The NaPa consortium complemented the deep UV technology by providing low-cost scalable processes and tools to cover the needs of nanopatterning from CMOS back-end processes through photonics to biotechnology. It showed the ability to integrate different materials and functionalities. In addition to the further development of process technology, including processes, tools, and materials, a range of applications is an intrinsic part of NaPa. This goes far beyond the development of a next generation nanolithography for chip manufacturing. While at the beginning of the project many processes were still at an embryonic stage, towards the end of the project many processes have gone through a phase of consolidation. An example for this is that during the last years many applications have emerged. The research in the three overarching themes was supported by developments in the subprojects **Materials**, **Tools** and **Simulation**. Complementing R&D, the consortium designed exciting nanoscience and nanoengineering courses to advance the training of the next generation of scientists and engineers and to create a positive attitude towards science among young people. Dissemination activities towards the lay public and sectors underrepresented in nanotechnology formed an integral part in NaPa. Thus, NaPa offered a unique opportunity to unleash the potentials of nanotechnology in Europe. Europe is very well positioned to play a major role in nanomanufacturing but there is strong competition from other parts of the globe. The NaPa project has made this positioning possible, as one of the 40 most successful projects of the European Commission 6th framework program. One of the main outputs of NaPa is the **NaPa Library of Processes**, which includes processes for scalable and cost-efficient manufacturing of e.g. polymer-based optical elements, organic LEDs and lab-on-a-chip systems among others. The NaPa library currently consists of 27 processes, which is a small fraction of the process developed during the project. The uptake of the NaPa project results will strongly affect the manufacturability in nanotechnology.

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PART I : INTRODUCTION – A COOKBOOK FOR NANOPATTERNING

1. Summary

This library is not an *introduction to nanopatterning*, with long introductions into the fundamentals of different processes and explanations about the limitations of processes. Nor is it presenting the state-of-the-art, i.e. the newest developments and shippings around the world. It is also not complete; therefore, many nanopatterning methods are missing. This is subject of publications, reviews and books. What is it then?

This is a *cookbook*, and a cookbook should be simple. It also requires a certain amount of familiarity with the subject. As in cookbooks, it will rather be a collection of processes, recipes, references, which can be selected without reading the entire book. It is the result of the European Integrated Project *NaPa*, which during a 4 years period gathered scientists and engineers to develop a range of nanopatterning method, with the aim that they become enabling techniques for a range of institutes.

In this library of processes (LoP) the need of applied scientists and process engineers in research and industry for reliable patterning processes is addressed. It is an introduction into basic nanopatterning processes from a practical point of view, and complements the reviews and publications already published in books and journals in a unique way only possible by a collective approach. This is done for the parallel patterning methods developed in the *NaPa* project, with a focus on thermal nanoimprint lithography (NIL), but it also takes up the input from the two other main processes for parallel processing from the *NaPa* project, soft lithography (SL) and stencil lithography (STEN). The aim is to enable researchers and engineers to choose from different processes depending on the specific challenges of a new application. Three different approaches are provided, ordered in two parts. In the first section of this *Part I* we try to satisfy the beginners' needs for practical advice, with easy-to-go recipes in a cookbook fashion. A second section gives more information about general processing issues, by presenting standard lithographic processes with emphasis on single layer pattern transfer. In addition, tables and schemes are provided. *Part II* - an appendix - is a collection of more elaborate processes, which - depending on equipment and application - can vary to a large extend. This collection of recipes is intended for the experienced user, and has to be complemented by the technological literature in publications and patents. The library is far from being complete and perfect, and does not have the ambition to cover every aspect of the processes used. It could serve as the basis for a living document, which - depending on its way of dissemination - can be an integral part of the nanofabrication community.

2. To Whom this Library is Addressed

Alternative nanopatterning methods are needed both by research institutes and by industry. This library is aimed on these different users, with the idea in mind that the *comparison of processes*, rather than the *description of single processes*, helps to step into the manufacturing. The library, however, is not meant to be a buyers' guide for building up a new nanoimprint laboratory or production site. Real comparisons of processes can only be made by benchmarking with defined rules and boundary conditions. In the last 4 years several rounds of benchmarking were performed on NIL within *NaPa*. The main result can be described as the following: good results can be achieved with almost any kind of equipment currently on the market, and different applications may profit from the advantages of different equipment. The resulting machine is often a compromise. Restrictions of flexibility, alignment, speed, technological limitations can be overcome by further developing both, equipment and processes. The user will profit from the competition between manufactures. However, the inability of machine builders to compare tools in an objective way makes it difficult for the customer to do this and demands a high level of knowledge about the state of the art.

3. Towards a Library of Processes for Alternative Lithography

3.1 Generalities

The vast number of publications, which describe complex processes and are often only valid for one application, overwhelms the user. Furthermore, in these publications, basic concepts are missing, which enable the beginner to become acquainted with the process in an easy-to-go manner. In this library, the need of process engineers in research and industry for reliable pattern processes is addressed.

The NaPa project was a unique platform for a collective approach to develop alternative processes for lithography. It has advantages over the bilateral exchange of scientists and the dissemination during conferences, because:

- It united partners with different equipment to work on related issues – with a practical point of focus (e.g. an application or process issue), and gives more room for exchange.
- It created a platform for exchange of researchers and collaborations, which is flexible and adaptable during the project time. Researchers opened their labs to visitors from other labs. They jointly used equipment, and exchanged tools, and samples.

All this is of benefit for the community, which currently grows steadily. While the number of research groups building up NIL processes is continuously increasing, nanoimprint is now moving into industry. All these people normally do not have a platform for comparison, or exchange.

3.2 How this Library is Structured

The reader often wants to get a simple ready-to-use process with a wide process window, or has an application that defines which process can be used. Most of the applications are based on simple pattern transfer: there the resist (one layer of polymer) is structured by an alternative patterning method and post-processing is similar to standard e-beam lithography. In this case, we have to note only the specific differences between conventional techniques and the NIL, i.e. steps or precautions that are necessary, have to introduce a new process step. E.g. for lift-off, undercuts have to be created, since the sidewalls in NIL are at best vertical. For more complex applications, e.g. when multilevel stamps are used, alignment is needed or pattern transfer is done via repeated reversal imprint, it is advisable to revise the entire traditional process route, which is a challenge to the thinking of a process engineer specialized and familiar with planar technology. While in the first case generalities are needed, in the latter case there is an abundance of processes, which cannot be written down in a process library. It is by definition incomplete, and often – depending on specific equipment and materials – not easily transferable without a deep understanding of process characteristics and knowledge about the fabrication tools used.

A library of processes will enable people to get quickly into processes:

- In the first section, we try to satisfy the beginners' needs for practical advice, with a short presentation and comparison of processes and easy-to-go recipes in a cookbook fashion, for the processes nanoimprint, soft lithography and stencil lithography. It is a mixture of concepts and some initial process parameters for a quick start.
- A second section gives more information about general processing issues in nanoimprint lithography, by presenting standard lithographic processes with emphasis on single layer pattern transfer. In addition, tables and schemes are provided. Simple (basic) recipes are presented, which are modified depending on the application.
- The third section, structured as an appendix to the introductory sections, is a collection of more elaborate processes, which – depending on equipment and application – can vary to a large extent. This collection of recipes is intended for the experienced user, and has to be complemented by the technological literature in publications and patents. The library is far from being complete and perfect, and does not have the ambition to cover every aspect of the processes used. It is a loose collection of processes rather than a book.

3.3 Mode of Dissemination

This library is printed as a booklet in a limited number by the Napa consortium and distributed by NaPa partners. It is not sold in bookshops or via internet. Information about how to get copies of this library will be placed on the NaPa web site [1] or elsewhere. The library's status is that of the end of the NaPa project (Feb. 2008). This has practical reasons, because the NaPa consortium will not meet any more as a whole as it did frequently during the active time of the NaPa project. Whether it becomes a "living document" in a future framework, with recipes added in a regular way, or made available for download, is an open question and largely depends on the feedback, but also the financial and logistic possibilities of a future editor, along with legal issues such as copy-right.

The library is not published as a textbook with theory and overviews, about the state of the art of nanopatterning, as it was done before the start of NaPa in [2], with contributions from several NaPa authors, for several reasons: First, time was too short at the end of the NaPa project to go through all the editing process for a book of this size and content. The lifetime of its recipes will be short and within a few years, many of them will be improved or obsolete. Second, the library is mainly the result of a collection of recipes from different researchers, and therefore not of same style and depth. Most recipes are not checked by independent sources, i.e. there is a chance that recipes do not work out if copied.

It can serve as the basis for lectures and courses on nanopatterning. The NaPa project organized a series of Summer Schools in Toulouse each year in July called PANAMA. The concept of this training was a "hands-on" approach of nanotechnologies focused on nanopatterning. PANAMA stands for "Patterning at the NANoscale – Methods and Applications". The concept of summer schools dedicated to nanopatterning and applications has been selected as the main tool for training actively young scientists in the domains relevant to NaPa project. The format was a small school (24 students), combining one week of magisterial courses on Nanopatterning, Applications in Industry and Ethical and Societal Issues and one week of practical training on Emerging Nanopatterning Methods. The school was organized by C. Vieu (LAAS-CNRS) together with his team. The lectures and practical training involved researchers from almost all NaPa partners, with a range of basic and specific questions on nanopatterning – with a focus on those processes within the NaPa subprojects. It is therefore a complement to the library of processes. It is planned that the PANAMA Summer Schools will continue in a different framework after the end of NaPa.

- [1] NaPa Integrated Project [online]. URL: <http://www.NAPAIP.org>.
- [2] C. Sotomayor Torres: *Alternative Lithography – Unleashing the Potential of Nanotechnology*, book series on Nanostructure Science and Technology, book series on Nanostructure Science and Technology in Kluwer Academic/Plenum Publishers, Springer, editor D.J. Lockwood. Hardbound, ISBN 0-306-47858-7, Nov. 2003, 425 pp. (2003).

3.4 Addresses for Feedback

This library is compiled from a range of inputs from different partners. The current version is a direct result from activities of the Napa project. The introduction and overview about nanoimprint lithography stems from lectures and articles written by H. Schiff (see Section 5.10), who is the library manager for this edition. Suggestions about new input and a possible update of the library should be addressed to J. Ahopelto, VTT and H. Schiff, Paul Scherrer Institut. Please do not contact the editor for copies of this library.

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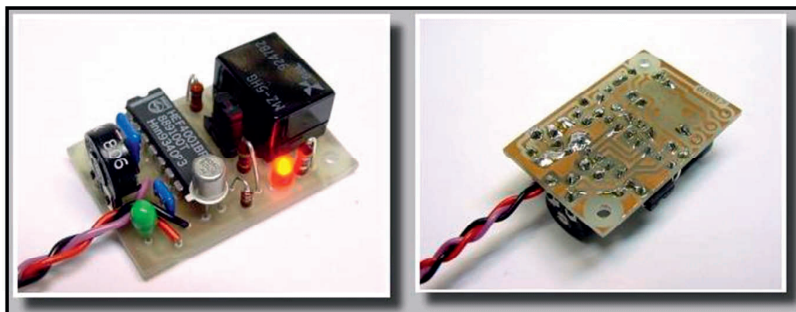
4. Cookbook for Alternative Nanopatterning

4.1 Generalities

Either a cookbook contains easy-to-go recipes with thumb rules for the beginner, or more elaborate recipes for the professional. The latter will be able to develop basic recipes into an own set of recipes. In the world of nanopatterning, this means that a basic recipe is something that always works out, with a great tolerance range, while the success of a more elaborate recipe is dependent on the experience and the ability to adapt these experiences to a new situation with many (new) parameters. In this section, we try to do satisfy the beginners' needs for practical advice, however, without going into technological details. More elaborate recipes for the experienced engineer are collected at the end of this report, without any claim on completeness. This cookbook is the part of the library, which may be used as an easy introduction for a beginner, with the aim, to enable him to get a fast hands-on experience with nanopatterning.

Printed circuit boards are a good example of how lithography was used for the patterning of metal wires on an insulating plastic substrate. The assembly of a variety of electronic elements was much facilitated by this board, which served both as a mechanical support, and for the wiring between them. For simple circuits made from discrete elements, a single layer of metal lanes was often sufficient (see Fig. 4.1). The mounting was done by drilling holes into the board and soldering the discrete elements to the wires of the backside of the board. These wires were defined by an optical mask, and produced by photolithography and etching as pattern transfer (see Fig. 4.2).

Printed Boards for Electronic Circuits



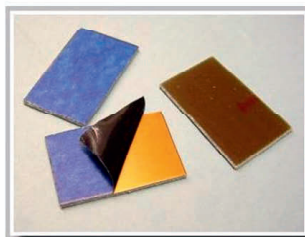
Printed board with mounted electronic elements

Backside with wires to connect electronic elements

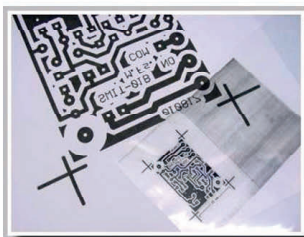
Figure 4.1: Photographs of a printed board after mounting of the electronic elements (front and back side).

The methods of printed circuit board fabrication were much refined in photolithography (see Fig. 4.2) and scaled down by many orders of magnitude. The mask fabrication, first by gluing patches of opaque tape on a transparent carrier, was then fabricated by plotters and photographic printers, and finally glass masks were fabricated by focused laser or electron beam lithography of resist with a thin opaque chromium layer as blocking layer for UV light. Mask aligners for 100 to 200 mm glass mask and silicon substrates are now precision tools with sub- μm alignment and leveling. The pattern transfer processes have been equally developed, and apart from etching processes, electroplating and lift-off methods are now widely used. An overview is given in Fig. 4.3

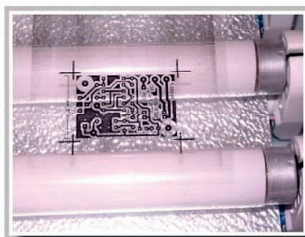
Printed Boards for Electronic Circuits - Lithography



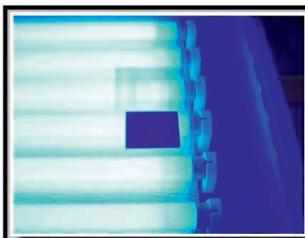
Base material



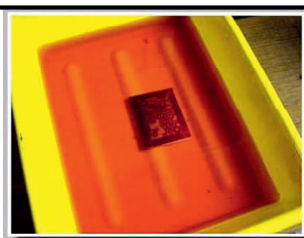
+ Mask foil



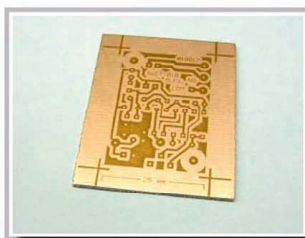
+ Exposure setup



⇒ Expose (UV-light)



⇒ Develop

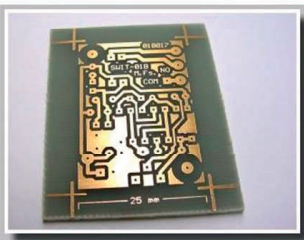


Developed Resist

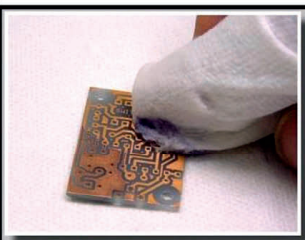
Printed Boards for Electronic Circuits – Pattern Transfer



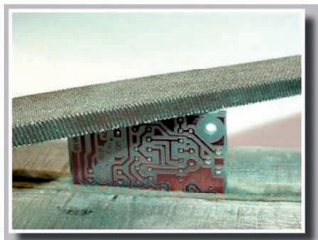
Copper etching



Conductor lines free



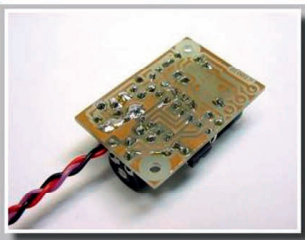
Remove protective coating



Drilling



Mounting

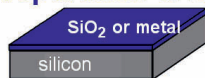


Soldering

Figure 4.2: Photographs of printed board fabrication sequence: lithography and pattern transfer (source unknown).

Lithography : Exposure and Pattern Transfer

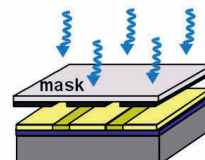
Preparation and exposure



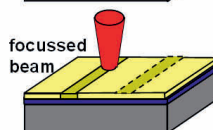
**oxidation
or deposition
of seed layer**



**photoresist
coating**



**exposure
with mask
(parallel)**



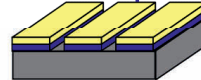
**exposure
with scanning
beam
(sequential)**

Development and pattern transfer

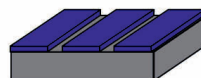


**positive
resist:
exposed areas
removed**

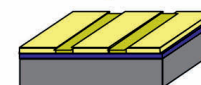
a) subtractive process (etching)



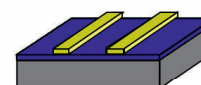
**SiO₂
removed
unexposed
photoresist
removed**



b) additive process (plating, lift-off)



electroplating



**unexposed
photoresist
removed**

Figure 4.3: Example of standard photon and electron based lithography and pattern transfer.

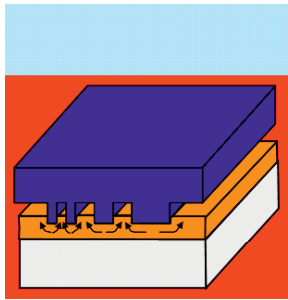
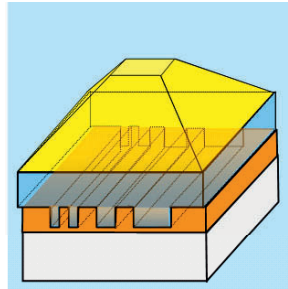
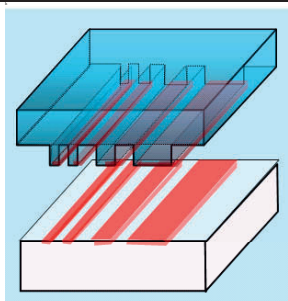
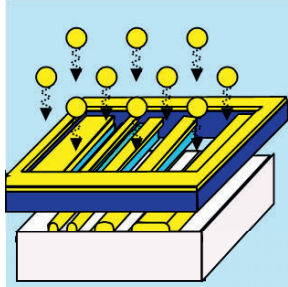
These schemes of lithography and pattern transfer are similar in the alternative patterning methods presented here, with some restrictions and variations.

4.2 Which Process to Choose

Everybody having access to advanced photolithography (PL) and electron beam lithography (EBL) enjoys the benefit of these techniques. He or she will not easily switch to a different process, which is less mature than the standard lithographies. The change is often necessary if either mass fabrication aspects have to be met, or – more and more often – standard lithographies come to their limits, in terms of throughput, resolution, accessibility and reproducibility. In many cases, the decision for a different lithographic process is based on the needs of a specific pattern transfer process. The lithographic process is only complete when the resist pattern is transferred into another material. This process, in which the resist is transformed into a patterned masking layer, allows the substrate to be attacked by plasma, etching solvents, electroplating, deposition of materials and other substrate altering processes. E.g. in NIL, a unique advantage of molding instead of exposure is that complex stamp profiles, such as staircases, V-grooves, pyramids, both convex and concave, can be replicated. They can be used for the generation of 3D structures as for T-gate transistors or contact holes or serve for the step-wise etching of underlying layers with variation of the opening width. As long as undercuts and 3D patterning is not necessary, in most cases this pattern transfer is therefore similar to EBL.

The general (very simple) rule is the following: If a resist has to be structured with a three-dimensional sub-500 nm pattern, then nanoimprint should be employed, because it is nearest to the common lithography. If chemical patterning is needed, then soft lithography, based microcontact printing is of advantage, it is also low cost, and suitable for fabrication in a chemical lab without expensive cleanroom facilities. In addition, if patterning has to be done over topography, a soft stamp or stencil method is predestined for use – stencil is very adapted to pattern different kinds of materials, too. However, there are many intersections where different techniques may be used with similar results. A first comparison can be seen in Tab. 4.1.

Table 4.1. Comparison of different alternative patterning methods.

Patterning Process	Patterning Scheme	Process	Specific advantages	Industrial Activity
Thermal Nanoimprint Lithography (NIL, T-NIL) – Hot Embossing Lithography (HEL)		<p>Stamp: hard, opaque (silicon wafers)</p> <p>Process: Thermoplastic molding at elevated temperature (100-200°C), demolding at low temperature (20-100°C)</p> <p>Tools: Hot presses (1-100 kN)</p>	<p>Similar to standard lithography (generating a thickness contrast of a resist)</p> <p>Maximum resolution: 2-5 nm</p> <p>Variety of thermoplastic materials</p> <p>Standard materials for stamps and substrates</p>	Very large research community, industry with increasing activity
UV-Nanoimprint Lithography (UV-NIL) a) Hard Stamp (Step and Flash) Lithography (SL) b) Soft Lithography (SL)		<p>Stamp: a) transparent (quartz) b) elastomer with hard backplate</p> <p>Process: Molding of liquid resin and hardening by UV-exposure</p> <p>Tools: a) step and repeat tool with UV-lamp b) modified mask aligner</p>	<p>Similar to standard lithography (thickness contrast of a resist, UV-exposure of negative resist)</p> <p>Maximum resolution: 2-5 nm</p> <p>Fast, no heating involved</p>	Fairly large research community with increasing activity, industry
Soft Lithography (SL) – Microcontact Printing (μCP)		<p>Stamp: Elastomer, often backed by a hard plate</p> <p>Process: Transfer of an ink from the stamp surface (and from the bulk)</p> <p>Tools: chemical lab, modified mask aligner</p>	<p>Surface patterning of functional molecules possible (chemical contrast)</p> <p>Maximum resolution: 50 nm</p> <p>Easy stamp fabrication and printing</p> <p>Unexpensive</p>	Beginning, first professional tools available
Stencil Lithography (STEN)		<p>Template: hard, thin MEMS membrane (Si_3N_4)</p> <p>Process: Thermal evaporation in vacuum</p> <p>Tools: Physical vapor deposition combined with modified mask aligner</p>	<p>Patterning over topography possible (topological contrast)</p> <p>Maximum resolution: 50 nm</p>	Beginning, first professional tools available

In the next section, we are presenting the different methods in more detail. For a better comparison, we start by standard optical lithography, before giving an introduction on imprint and stencil lithography.

Photolithography (through Semitransparent Mask)

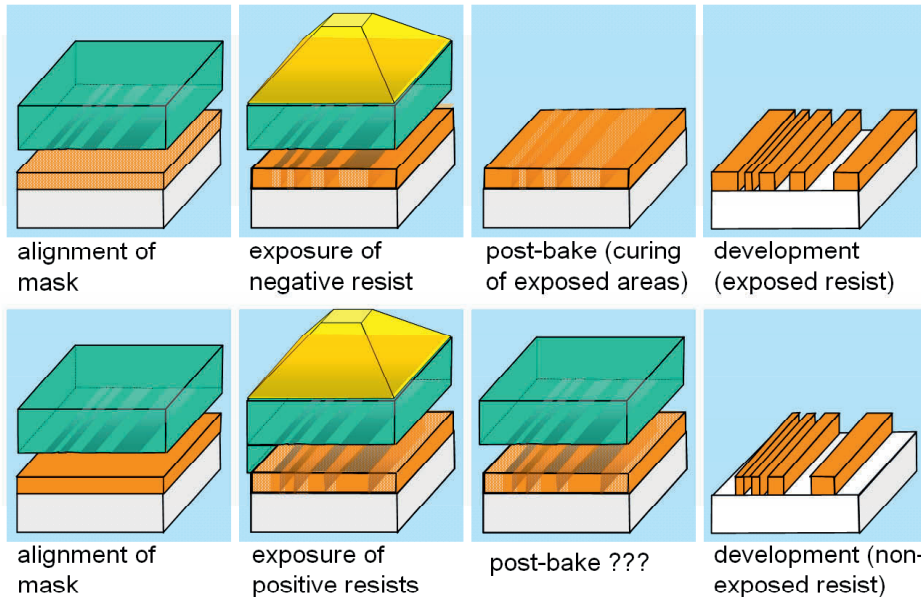


Figure 4.4: Process sequence for photolithography for top: negative resist and bottom: positive resist

Short description

Photolithography is a standard method for resist patterning. It uses a semitransparent mask and exposes the resist locally. Depending on the type of resist (positive or negative tone), the exposed areas become soluble or are crosslinked. This contrast in solubility makes it possible to selectively remove one part of the resist. Both contact of mask to resist and proximity patterning is possible.

Main application

- Standard lithography method for many applications (in the microrange).

Advantages

- No residual layer.
- No mechanical contact during proximity patterning.
- Undercuts can be created for better lift-off

Disadvantages

- Semi-transparent mask needed.
- Yellow room needed

References:

- [1] M.J. Madou: *Fundamentals of Microfabrication*. Second edition, CRC-Press. ISBN: 0849308267, March 2002, 723 pp., (2002) 239-278.
- [2] T.A. Brunner, *Why optical lithography will live forever*, J. Vac. Sci. Technol. B **21**(6) (2003) 2632-2637.

4.3 Nanoimprint Lithography (NIL) – for Beginners

What is Nanoimprint Lithography ? – Short description

In Nanoimprint Lithography (NIL), the thermal version is also called Hot Embossing Lithography (HEL), a hard stamp with a surface relief is used to deform a softened polymer layer. The generated thickness contrast can be used as a mask for pattern transfer to the substrate.

Nanoimprint Lithography in daily life? – Examples

- Molding of waffles with a hot structured iron.
- Printing a seal into wax.

When do you use Nanoimprint Lithography ? – Main applications

- Resist based processes (replacement of e-beam lithography), 3D patterning of surfaces
- Mix- and match applications with resist based (optical) lithography

Advantages

- The resist can be prepared as a solid layer on silicon and glass substrates by spincoating before imprint.
- A crosslinkable resist is more stable in subsequent processes
- A photosensitive resist can be exposed by optical lithography after imprint (add microstructures)

Restrictions

- The main bottleneck is to provide suitable stamps, which normally are fabricated via electron beam lithography and etching. It is highly advisable to make stamp copies via NIL and use them instead of the original, which reduces the risk of damaging the original due to handling errors.
- Nickel stamps (by electroplating) are often not suitable because of the thermal expansion mismatch between stamp and substrate

How do you start Nanoimprint Lithography ? – Main tools, materials, processes

- Basic cleanroom facilities and processes (mask aligner, silicon cleaning, plasma processes for ashing, residual layer etching) are of advantage. Laminar flow is necessary to avoid contamination by dust.
- Antiadhesive coating setup (basically once the stamp is coated, this coating can last for a long time, but occasional re-coating might be of advantage)
- Hot press (pressure and heat which a parallel force, or a press on a pressurized membrane) with sufficient plate size, pressure, and the possibility to heat and cool these platens
- Optical microscope (stereo / high resolution) for quality control
- Beginners often break stamps because silicon is susceptible to notching due to contamination, scratches (due to handling errors) and bad alignment of stamp and substrate
- Use same size of stamp and substrate (e.g. 20x20mm² or entire wafers), or smaller stamps

Beginners' "kit" for Nanoimprint Lithography

- Manual hydraulic press with up to 1 tons force and heating platens. Temperature range up to 200 °C. Cost: > 1000 €. Simpler (for demonstration) is a metal clamp which is heated in an oven. However, efficient cooling (e.g. with nitrogen gas is beneficial) is needed.
- Resist (PMMA, molecular weight 75k, or mr-I 8030E). Thickness 300 nm. Cost: 50 € to 2000 € / lit.
- Stamp with antiadhesive coating, regular pattern (grating) with largest features around 10 μm, depth around 200 nm, protrusion coverage around 50%.
- Antiadhesive coating. Cost of perfluorinated silane 100€ / 10 ml (for > 50 coatings)
- Rubber (PDMS), 1 mm thick, from the workshop
- Tweezers and doctors blade for demolding.

Thermal-NIL (Hot Embossing)

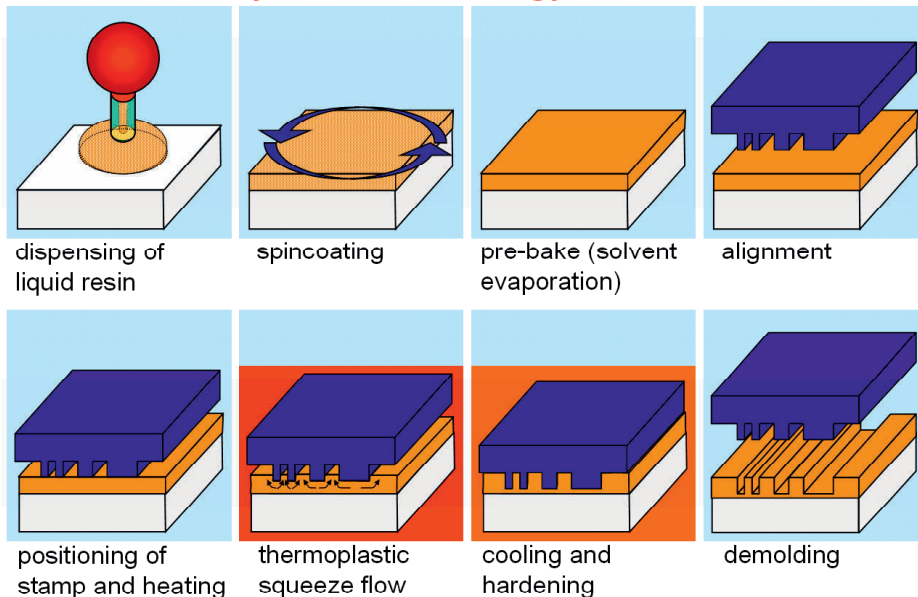


Figure 4.5: Process sequence for thermal nanoimprint lithography.

Nanoimprint : Process description

In a parallel press setup, the imprint is quite simple; apply heat and pressure in a controlled way

Stamp and materials

- Stack of stamp and substrate + compliance layer on top is assembled on press stamper
- Use stamp silicon with smooth vertical sidewalls, smaller or equal size than silicon substrate
- Antiadhesive coating needed

Process parameters

- Imprint in purely viscous state 50 – 70°C above the glass transition T_g . Demolding 20°C below T_g .
- Pressure between 10 – 100 bar, applied after imprint temperature is reached, maintained cooling
- Imprint time 1 min (without heating/cooling) up to 30 min, depending on structures and temperature; e.g. a stamp covered with a grating of dense micropillars will imprint in less than 1 min (without cooling)
- Evacuation before imprint is beneficial but not prerequisite (air is compressed and dissolves)
- Manual demolding using a doctor's blade – easier when substrates have a small wedge at the corner

Restrictions – and how to deal with them

- Avoid any kind of notch effect; furthermore reduce bending, shearing and local high pressures

References:

- [1] H. Schiff and A. Kristensen, *Nanoimprint lithography*: Chapter (Part A/8) in “*Handbook of nanotechnology*”. Volume editor B. Bhushan, second edition, rev. and extended, Springer Verlag, Berlin, Germany, Hardcover. ISBN: 978-3-540-29855-7, November 2006, XLIV, 1916 pp., 1593 illus, with CD-ROM, 239-278 (2007).
- [2] C. Sotomayor Torres: *Alternative Lithography – Unleashing the Potential of Nanotechnology*, book series on Nanostructure Science and Technology, book series on Nanostructure Science and Technology in Kluwer Academic/Plenum Publishers, Springer, editor D.J. Lockwood. Hardbound, ISBN 0-306-47858-7, November 2003, 425 pp. (2003).

4.4 Soft Lithography (SL) – for Beginners

What is Soft Lithography ? – Short description

In Soft Lithography (SL) a patterned soft elastomer stamp is the key element. Instead of generating a surface profile in a resist by mechanical hard contact through rigid inorganic materials, the pattern is transferred to the substrate by soft, conformal contact using flexible organic molecules and materials.

Soft Lithography in daily life? – Examples

- Printing of ink by rubber stamp.
- Fingerprints

When do you use Soft Lithography ? – Main applications

- Microcontact Printing (μ -CP)
- Soft UV-NIL

Advantages

- Low-cost (precursor SYLGARD 184, 1 bottle 100 €).
- No cleanroom facilities necessary.
- Low pressure, the flexible stamp accommodates planar and non-planar surfaces by conformal contact.
- Large areas, the flexible stamp can make contact with and pattern large areas.

Restrictions

- Balanced stamp hardness is necessary (too soft: shallow structures difficult because of local bowing; too hard: conformal contact difficult)
- Stamp swelling by many organic solvents

How do you start Soft Lithography ? – Main tools, materials, processes

- Basic chemical lab (thiols, buffer solutions, vacuum, etch chemistry)
- Template (master) with antiadhesive coating
- Oven for curing
- (Fluorescence) Microscope
- Metal deposition capabilities
- UV-Light source (for Soft UV-NIL)

Beginners' "kit" for Soft Lithography

Stamp fabrication:

- Mix precursor SYLGARD 184 elastomer base with curing agent 10:1 and degas.
- Pour on master in Petri dish.
- Cure at 60°C in oven.
- Cut and peel from master.

Pattern Transfer:

For μ -CP:

- Ink stamp with alkanethiol from solution or PDMS ink pad.
- Place gently on gold-coated surface.
- Detach.
- Wet etch.

For Soft UV-NIL:

- Spin-coat liquid resin onto substrate.
- Place stamp under moderate pressure and cure by UV-light exposure.
- Detach.
- Use residual layer etch and substrate etching techniques to transfer pattern into substrate.

Soft Lithography – Microcontact Printing

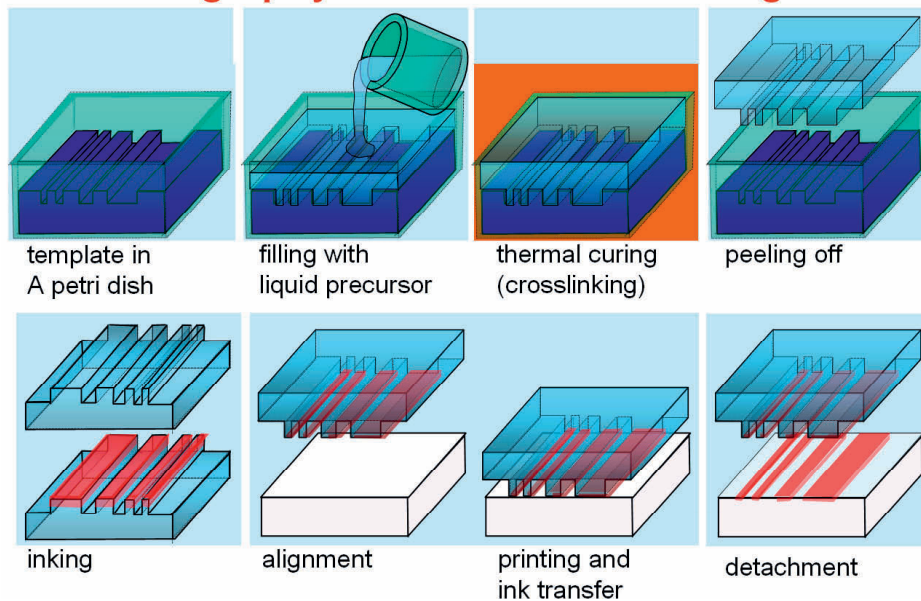


Figure 4.6: Process sequence for soft lithography – stamp manufacturing and microcontact printing.

Soft lithography / Microcontact Printing : Process description

For Microcontact Printing, one Soft Lithography technique, the soft elastomer stamp is fabricated by molding from a patterned template (master). Next, the stamp protrusions transfer the ink-like resist to the substrate by soft conformal contact.

Main application

- Printing of chemical patterns, alkanethiol SAMs on gold, biomolecules.

Advantages

- Applicable for a wide variety of inks.
- Possibilities for multiplexing.

Restrictions

- Pattern geometries: printing of very shallow structures is difficult (local bowing = sagging).
- Ink diffusion might limit resolution and sharpness of pattern.

References:

- [1] Y.N. Xia, G.M. Whitesides, *Soft lithography*, *Angew. Chem.-Int. Ed.* **37**, 551-575 (1998).
- [2] E. Menard and J.A. Rogers, *Stamping techniques for micro- and nanofabrication*: Chapter (Part A/9) in “*Handbook of nanotechnology*”, Volume editor B. Bhushan, second edition, rev. and extended, Springer Verlag, Berlin, Germany, Hardcover. ISBN: 978-3-540-29855-7, November 2006, XLIV, 1916 pp., 1593 illus, with CD-ROM, 279-297 (2007).
- [3] B. Michel, A. Bernard, A. Bietsch, E. Delamar, M. Geissler, D. Juncker, H. Kind, J.-P. Renault, H. Rothuizen, H. Schmid, P. Schmidt-Winkel, R. Stutz, and H. Wolf: *Printing meets lithography: soft approaches to high-resolution*, *IBM J. Res. Dev.* **45**(5) (2001) 697-719.
- [4] H. Schmid, B. Michel, *Siloxane polymers for high-resolution, high-accuracy soft lithography*, *Macromolecules* **33**, 3042-3049 (2000).

Soft Lithography – UV-Nanoimprint

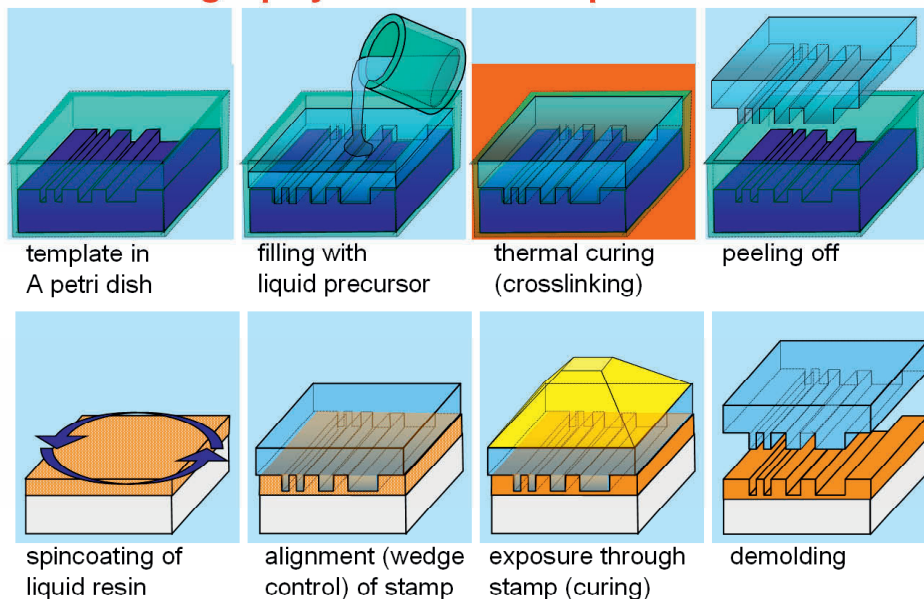


Figure 4.7: Process sequence for soft lithography – stamp manufacturing and UV-NIL.

Soft lithography / UV-Nanoimprint : Process description

Also for UV-NIL, another Soft Lithography technique, the soft elastomer stamp is fabricated by molding from a patterned template (master). Next, the soft stamp is used to generate a surface topography (resist thickness contrast) via molding of a liquid pre-polymer which is hardened by UV-exposure.

Main application

- Resist patterning
- 3D patterning

Advantages

- Low viscosity resist makes molding fast.
- Multilevel 3D geometries are accessible.
- Alignment through stamp is possible.
- Only low temperature and pressure required.
- Patterning of large areas possible.

Restrictions

- Liquid resist has to be applied before imprint by dispensing or spin-coating.
- Transparent stamps (elastomer and quartz backplane) are needed.
- Easy demolding requires controlled adhesion between stamp and resist

References:

- [1] Y. Xia, G. M. Whitesides: *Soft lithography*, *Angew. Chem. Int.* **37** (1998) 550-575.
- [2] U. Plachetka, M. Bender, A. Fuchs, B. Vratzov, T. Glinsner, F. Lindner, H. Kurz: *Wafer scale patterning by soft UV-Nanoimprint Lithography*, *Microelectron. Eng.* **73–74**, (2004) 167–171.
- [3] U. Plachetka, M. Bender, A. Fuchs, T. Wahlbrink, T. Glinsner, H. Kurz, *Comparison of multilayer stamp concepts in UV-NIL*, *Microelectron. Eng.* **83** (2006) 944-947

4.5 Stencil Lithography (STEN) – for Beginners

What is Stencil Lithography ? – Short description

Stencil lithography uses a pellicle instead of a stamp, and has much resemblance with optical proximity lithography, but uses particles instead of photons. Material is evaporated through the openings of the membrane in a shadow type way. In contrast to lift-off in optical lithography, the shadow mask is made for multiple use and either placed in a distance to the surface to be patterned or pressed against this surface. After evaporation the stencil has to be cleaned from material deposited on the stencil structures.

Stencil Lithography in daily life? – Examples

- Patterning sugar (icing / powdered sugar) by means of a pellicle onto a cake.
- Airbrush through mask (on cars or walls)

When do you use Stencil Lithography ? – Main applications

- Mix- and match applications by patterning on already patterned substrates.
- Dots

Advantages

- Coating on substrates which do not allow a resist process
- Patterning of a vast range of materials, which can be evaporated.
- Patterning over topography.

Restrictions

- Mask distortion due to material deposition and by heat.
- Possible clogging of openings.
- Design restrictions due to stability of mask (membrane openings).

How do you start Stencil Lithography ? – Main tools, materials, processes

- Basic cleanroom facilities and processes (mask aligner, silicon cleaning, plasma processes for ashing, residual layer etching) are of advantage. Laminar flow is necessary to avoid contamination by dust.
- Antiadhesive coating setup (basically once the stamp is coated, this coating can last for a long time, but occasional re-coating might be of advantage)
- Evaporation machine
- Optical microscope (stereo / high resolution) for quality control

Beginners' "kit" for Stencil Lithography

- Place stencil on substrate and clamp it
- Install it at the top of the evaporation chamber opposite to the evaporation source.
- Evaporate metal (no rotation)
- Detach stencil from substrate
- Clean stencil

Stencil Lithography (with Membrane Type Pellicle)

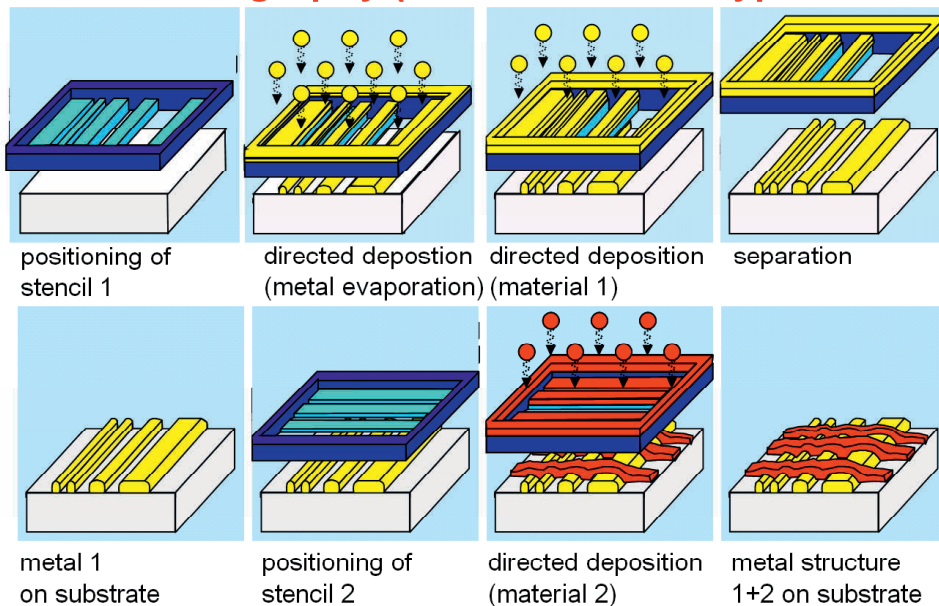


Figure 4.8: Process sequence for stencil lithography for two process steps (e.g. for metallization over non-flat surfaces).

Stencil Lithography : Process description

The stencil is placed in constant distance to the substrate. While evaporation takes place, the material builds up both at the substrate and the membrane.

Main application

- Mix- and match applications with optical lithography.
- Materials which are difficult to handle in dry and wet etching

Advantages

- Patterning over topography.
- Multiple layers

Restrictions

- UHV process
- Topology of stamps (closed openings needed).
- Cleaning of stencil after evaporation needed.
- Distorsion and cloggings during evaporation have to be minimized.

References:

- [1] J. Brugger, and G. Kim: *Nanofabrication by shadow deposition through nanostencils*: Chapter (7) in "Nanolithography and patterning techniques in microelectronics". Editor D.G. Bucknall, Woodhead Publishing, Cambridge, England, CRS-Press, hardback. ISBN: 1 85573 931 3, September 2005, 424 pp. (2005) 218-237.

5. Nanoimprint Lithography

5.1 Generalities - Overview

The main focus of NaPa was on Thermal Nanoimprint Lithography (NIL or T-NIL, often also called Hot Embossing Lithography). The process is low-cost and easy to employ because it uses non-transparent stamps, and can be used with standard hot presses without any kind of alignment. However, because of the relatively high viscosity of the resists, a high pressure has to be used, and the final thickness of the resist is much dependent on structure sizes and densities (fill factor). Therefore NIL can be quite simple if a regular pattern of nano- or microstructures is imprinted, but can become more complex if structure sizes and density varies over the surface of a stamp. A good example is shown in Figure 5.1.

Large Area Simulation of Imprints

In thermal imprint, your resist can look like

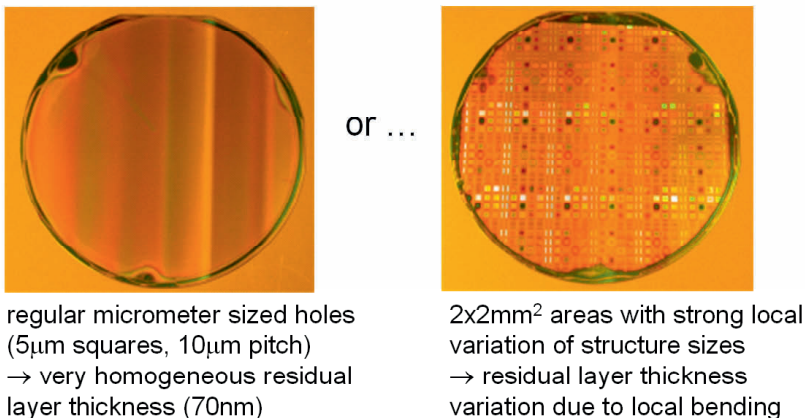
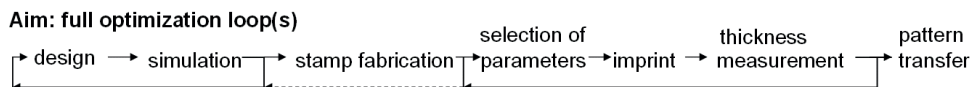


Figure 5.1: Photographs of typical resist patterns after imprint (see also Fig. 5.5).

Both results can be used for further processing, but while in the first case the pattern transfer is easy due to the homogeneous thickness of the residual layer of the resist, the second case the process window has to fit into the tolerances given by the variation of residual layer thickness (shown by the different colors of the resist). The optimum case would be, if a process is optimized according to the following sequence:



This process chain includes **two optimization loops**: The first loop includes a **simulation** step after the design, which means that the imprint of areas of a few mm up to the entire wafer area should be simulated and critical spots for molding and pattern transfer identified and avoided by adapting the design. Then structures can be optimized before expensive stamp manufacturing begins. The second loop characterizes the **optimization of an imprint process** with a given stamp **by experiment** and variation of process parameters. The whole process, however, is only complete if the complete process sequence, i.e. the process including the pattern transfer, and consequently all processes needed for the final application are considered. Simulation tools for large areas are currently been developed, see:

V. Sirotkin, A. Svintsov, S. Zaitsev, and H. Schiff, *Coarse-grain simulation of viscous flow and stamp deformation in nanoimprint*, J. of Vac. Sci. Technol. B **25** (6), 2379-2383 (2007)

For the less experienced user, the imprint of a large area micrograting is the best way to begin, with maximum stamp protrusion widths of a few $100\mu\text{m}$. The only restriction is that for large area stamps, the demolding forces increase and the demolding will become more difficult.

5.2 Hard Stamps

Stamp Fabrication

Any kind of surface relief can be replicated by hot embossing, as long as the thermomechanical properties can be varied between molding and demolding. For thermal NIL, it is of advantage to use silicon wafers rather than electroplated molds (because of the thermal expansion mismatch between stamp and substrate). Apart from standard silicon micromachining techniques, a process for the coating of antisticking layers is needed.

Master Fabrication using e-Beam Lithography and RIE

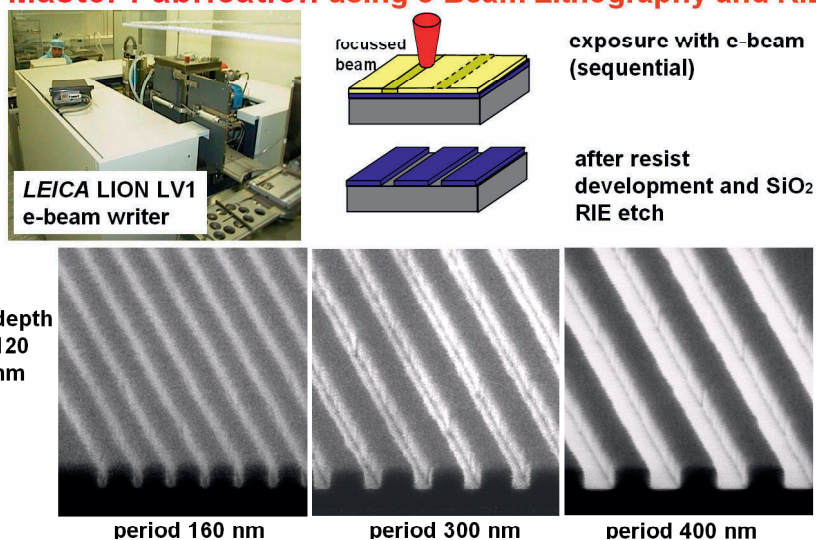


Figure 5.2: Exposure and pattern transfer for stamp fabrication by electron beam lithography.

Short description

Silicon as a stamp material for thermal nanoimprint is widely used.

Main application

- All kinds of thermal NIL processes where the substrate is silicon
- Moderate number of imprints due to limited mechanical strength (in contrast to SiC and Si₃N₄)

Advantages

- Standard material in semiconductor industry with high surface quality, availability, suitable for standard cleanroom processing such as RIE, KOH etching, anodic bonding in quartz and Pyrex.
- Possibility to coat antiadhesive layer with silane chemistry.
- Thermal expansion coefficient matched to substrate.

Disadvantages

- Non-transparent and not very resistant to damages due to notches.
- Cannot be easily clamped or fixed by screws (avoid strain due to thermal expansion mismatch)

Table 5.1. Comparison of different materials for stamps.

material	Young's modulus (GPa)	Poisson's ratio	thermal expansion (10^{-6} K^{-1})	Knoop micro-hardness (kg mm^{-2})	thermal conductivity ($\text{Wm}^{-1} \text{ K}^{-1}$)	specific heat $\text{J} \cdot \text{kg}^{-1} \cdot \text{K}^{-1}$
silicon	131	0.28	2.6	1150	170	705
SiO ₂ fused silica(bulk)	73	0.17	0.6	500	1-6	700
quartz (fused)	70-75	0.17	0.6	>600 (8 GPa)	1.4	670
silicon nitride (Si ₃ N ₄)	170-290	0.27	3	1450	15	710
diamond	1050	0.104	1.5	8000-8500	630	502
Nickel	200	0.31	13.4	700-1000	90	444
TiN	600	0.25	9.4	2000	19	600

5.3 Surface treatment

Since silicon is not hydrophobic, we need a kind of ultrathin Teflon-like coating. The common material for that is Heptadecafluoro-1,1,2,2-tetrahydrooctyl-trichlorosilane (F13-TFS), a silane with a reactive end group and a long hydrophobic tail group (see Fig. 5.3). The anti-adhesion treatment of the surface can be done in liquid or in gas phase. In the first case, difficulties are reported for stamps with structures of very high resolution and aspect ratio, due to the incomplete wetting of recessed surface areas. However, wet phase treatment is usually simpler and adequate for stamps with structures down to hundreds of nanometers.

Processes for coating

- 1) Chemical Vapor Deposition (CVD) using evaporation of fluorinated silanes by heating or in vacuum, as described by ref. [1] and [2]
- 2) Optool: wet coating of using Optool DXF a fluorinated silane in a fluorinated solvent, <http://www.daikin.com/chm/>, [3]
- 3) CVD tools fro NanoNex Ultra-100 Integrated tool for mold cleaning and surface release treatment for Nanoimprint Lithography, <http://www.nanonex.com/>
- 4) Molecular Vapor Deposition (MVD) from Applied MicroStructures, Inc., 1020 Rincon Circle, San Jose, California 95131-1325, <http://www.appliedmst.com/>

5.3.1 Treatment in liquid phase

The silane containing solution has to be prepared possibly in inert atmosphere, such as argon or nitrogen, in order to avoid water contamination. The solvent typically used is toluene, but other solvents, with lower water solubility such as heptane or dodecane have been used successfully to maintain the solution with a water content sufficiently low to avoid bulk polymerization. A typical process could be done in the following conditions:

- 1) Solution of perfluoroalkyltrichlorosilanes (for example (F13-TFS)) 0.1-1 mM in toluene or (heptane, octane, dodecane), prepared in inert atmosphere.
- 2) Immersion of the samples for 1 h at room temperature.
- 3) Rinsing in toluene.

5.3.2 Treatment in vapour phase

The most reliable surface treatment is obtained by chemical vapour deposition (CVD), by applying a moderate vacuum of some mbar in an atmosphere containing perfluoroalkyltrichlorosilanes molecules. One of the most prominent advantages of the vapour deposition method is that it is not affected by the wetting ability of a surface, so that it is suitable for stamps with extremely small nanostructures.

A possible surface treatment by chemical vapour deposition (CVD) is the following

- 1) Injection of perfluoroalkyltrichlorosilanes (for example F13-TFS) into a previously evacuated process chamber (with a 1-10mbar residual pressure of inert gas) at room temperature. The amount of molecules is in the range of 10 μL per liter of the chamber volume.
- 2) Optional: inject a small amount of water ($\sim 2 \mu\text{L}$ of the chamber volume).
- 3) Leave the samples under this atmosphere for between 10 min and 1 hour (depending on setup).
- 4) Rinse with toluene

Fluorinated organosilane as molecular anti-adhesive layer

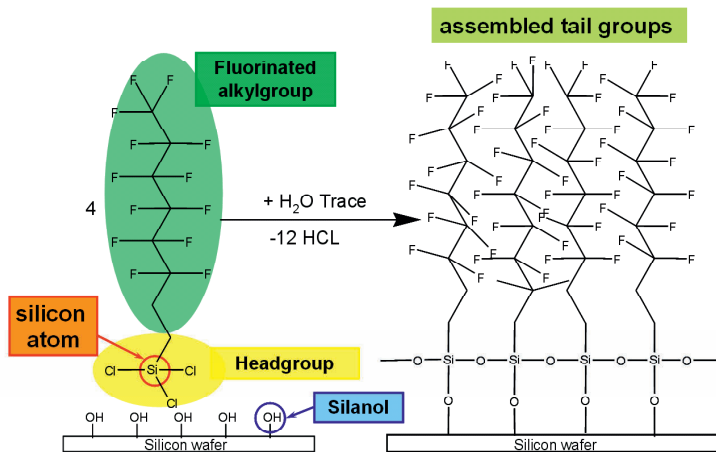


Figure 5.2: Silane binding on silicon dioxide.

Short description

Wet coating, CVD coating. Silane chemistry. Cleaning and activation either by so-called Pyranha etch, or by O₂-plasma (RIE) or ozone-UV cleaning. The qualities are different but oxygen plasma seems to be best.

Main application

- Critical processes with high aspect ratio
- Isothermal processes are possible (no cooling needed before demolding)

Advantages

- The crosslinked resist can be demolded more easily, and the resist is more stable in subsequent processes.
- The resist can be used in a mix- and match process (exposure by optical lithography)

Disadvantages

- The molding and curing step have to be temporarily separated.
- resist cannot be dissolved easily, e.g. if resist is sticking to the stamp.

References:

- [1] H. Schift, S. Saxer, S. Park, C. Padeste, U. Pielies and J. Gobrecht, *Controlled co-evaporation of silanes for nanoimprint stamps*, *Nanotechnology* **16** (2005) S171-S175.
- [2] M. Beck, M. Graczyk, I. Maximov, E.-L. Sarwe, T.G.I. Ling, M. Keil, L. Montelius, *Improving stamps for 10 nm level wafer scale nanoimprint lithography*, *Microelectron. Eng.* **61-62** (2002) 441-448.
- [3] J. Tallal, M. Gordon, K. Berton, A.L. Charley, D. Peyrade, *AFM characterization of anti-sticking layers used in nanoimprint*, *Microelectron. Eng.* **83** (2006) 851-854

5.4 Resists, Substrates and Tools

Resists for thermal NIL can be easily prepared by dissolving thermoplastic polymer, e.g. PMMA or PS (powder, pellets) in appropriate solvents. Meanwhile a range of commercial NIL resists is available with enhanced rheological and process properties specifically developed for NIL.

Table 5.3. Resist materials for thermal nanoimprint

Resist	Solvent	Glass transition temp. T_g and molecular weight M_w	Viscosity @ temp., Young's modulus	Comments
poly(methyl methacrylate) (PMMA)	anisole, ethyl acetate, ethyl lactate	100 °C, 25 – 120k	$10^5 - 10^7$ Pa·s @ 170 °C; 380-540 MPa	the "classic" NIL resist
poly(styrene) (PS)	toluene	100 °C, 50k		integrated optics
poly(carbonate) (PC)	cyclohexanone, 1,1,2,2-tetrachloroethane	145 °C, 34k	2350 MPa	integrated optics, $n=1.6$ high etch resistance
cyclic olefine co-polymer (COC)	toluene	60 – 180 °C	$2 \cdot 10^4$ Pa·s @ 170 °C 2600 MPa	highly transparent polymer, chemically resistant, low water absorption, lab-on-chip and optical applications
mr-NIL 6000	safe solvent	40 °C (before imprinting)	$0.2 \cdot 10^4$ Pa·s @ 100 °C	low T_g NIL resist for combined thermal and UV-based NIL (STU™ process of Obducat), mix-and-match, multi-level patterning, polymer stamps, reverse UV NIL [1], [3]
mr-I 7000E	safe solvent	60 °C	$3 \cdot 10^4$ Pa·s @ 120 °C	low T_g NIL polymer with very good flow ability and high plasma etch resistance
mr-I 8000E	safe solvent	115 °C	$10 \cdot 10^4$ Pa·s @ 175 °C	NIL polymer with very good flow ability, good thermal stability and high plasma etch resistance
mr-I 9000	safe solvent	65 °C (before imprinting)		thermally curable NIL resist
mr-I 9000E	safe solvent	35 °C (before imprinting)		low T_g thermally curable NIL resist allowing almost isothermal imprint process with high plasma etch resistance [2]
Hybrane	toluene	0 – 10 °C		room temperature imprint, SF ₆ RIE etch resistant
NEB22		80 °C, 3k		negative EBL resist, high etch resistance in fluoro- and chloro-based plasmas
mr-I T85	safe solvent	80 °C	$300 \cdot 10^4$ Pa·s @ 140 °C	thermoplastic NIL polymer for micro optical and bio applications with high chemical stability and excellent UV and optical transparency

References:

- [1] C. Schuster, M. Kubenz, F. Reuther, M. Fink, G. Gruetzner, Proc. SPIE **6517** (2007), 65172B.
- [2] F. Reuther, M. Kubenz, C. Schuster, M. Fink, M. Vogler, G. Gruetzner, J. Grimm, A. Kaepfel, Proc SPIE **5751** (2005), 976-985.
- [3] N. Kehagias, V. Reboud, G. Chansin, M. Zelsmann, C. Jeppesen, C. Schuster, M. Kubenz, F. Reuther, G. Gruetzner, C. M. Sotomayor Torres, Nanotechnology **18** (2007), 17, 175303.

5.5 Hot Embossing Machines

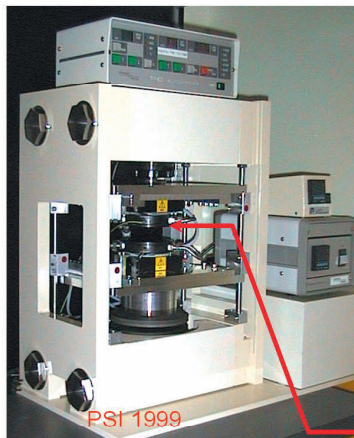
A press for hot embossing should be able to apply pressures over 10 bar and should have a temperature range between 60 and 200°C. The size of the stamp should be selected according to the pressure achievable.

Heating by electrical resistance heating is most suitable, and can also be integrated into a compact setup. Homogeneity is ensured by using large metal plates on top. However, this also enhances the thermal mass (slow heating and cooling). Cooling can be done by blowing nitrogen gas or air through holes in the holder. Cooling by air convection is extremely slow. Additional water cooling below an insulating sheet may be helpful to keep the heat away from the alignment and pressing unit. Because the wafers do not need to be attached to the stampers of the press, the only need is to use hard plates with flat surfaces. Be aware that the whole setup can bend during the high pressures involved, and if pressure is not equally distributed, even 5mm thick metal plates can bend. This means that silicon wafers can even cut into soft metals. Large wafers are therefore more likely to print homogeneously than small pieces of chips, as long as a compliance layer (e.g. a 1 mm thick layer of silicon – PDMS) is used for the homogenization of thickness variations (both due to tolerances of wafers and local pressure inhomogeneities during imprint).

Pressing mechanism:

It is advisable that the pressure is not built-up in an instant, but softly during a few seconds. The PDMS will also ensure that there is a gentle pressure build-up. NIL presses are easier to build than presses for high aspect ratio microstructures, because an equal distribution of the pressure can be ensured by the compliance layer, and does not need a totally stiff setup where a precise lateral alignment and a precise vertical movement is needed, involving an attachment of the stamp (and substrate). The stack can be removed from the press after embossing, and the demolding is done manually outside the press, using a doctors blade. Therefore after the imprint process, the pressure can be released instantly.

Hot Embossing Equipment (in PSI)



embossing press from Specac

hydraulic press for nanolithography machine parameters:

- press : hydraulic (oil)
- lateral resolution : < 50 μm
- stamp : 15 x 15 mm², up to 100 mm
wafers, substrate silicon
spincoated PMMA (thermoplast)
- samples : up to 100 mm wafers
- temperature : up to 280 °C
- applied force : up to 40 kN
- conditions : ambient,
laminar flow (clean room)
- heating : electrical
- cooling : water / air
- control : automatic

process area for sample and mold insert

Figure 5.4: A simple (oil) hydraulic imprint machine.

Pressure Equilibration – Cushion / Compliance Layer

A thick (1 mm) sheet of standard silicone, called PDMS (Polydimethylsilane), is sufficient to equilibrate any kind of unevenness, e.g. caused by substrate undulations or even dust particles. The stamp can bend around these particles and leaves some “halo”, where the imprint is not complete. PDMS can be taken from any kind of workshop. When made hot, it tends to glue, which is an advantage to keep the substrate or stamp fixed, but if not wished, a polyimide layer can be used as an intermediate layer for separation. The cushion layer can be placed at the backside of the stamp (or the substrate), see Fig. 5.5. Normal PDMS will expand when pressed (e.g. some cm over the borders of a 100 mm wafer). The initial size should be slightly bigger than the stamp.

Compliance Layer on Top – Induced Stamp Bending

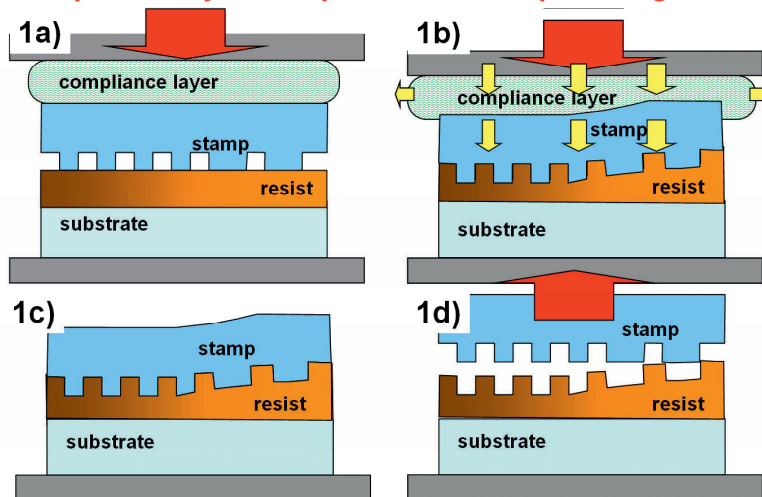
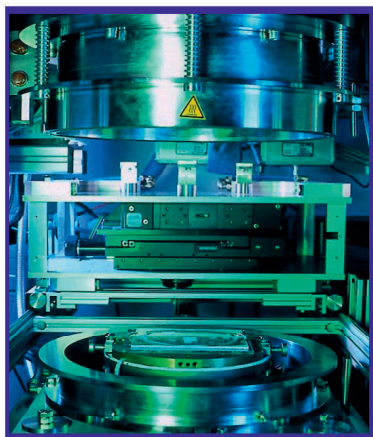


Figure 5.5: Principle of a cushion / compliance layer for pressure equilibration at the backside of the stamp. The bending of the stamp due to the variation of structure density in the stamp is exaggerated.

HEX03 Nanoimprint Machine from Jenoptik



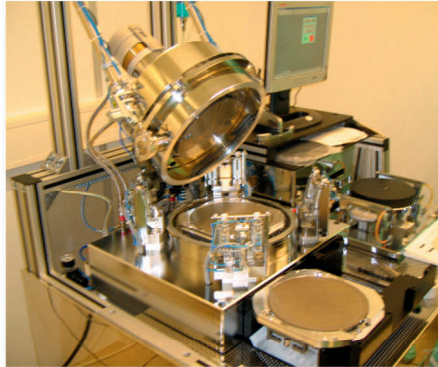
front side with opened embossing chamber and inserted microscope

Main Features

- molding of thermoplastic polymers with resolutions of below 10nm
- pressing force up to 200kN (operation force/position controlled)
- embossing temperature up to 320°C (heating electrical, cooling with oil)
- embossing under **vacuum**
- automatic mold release
- optical alignment with 3 μm overlay accuracy for double sided / aligned embossing

Figure 5.6: Integrated optical microscope in a hot embossing machine (Jenoptik HEX03).

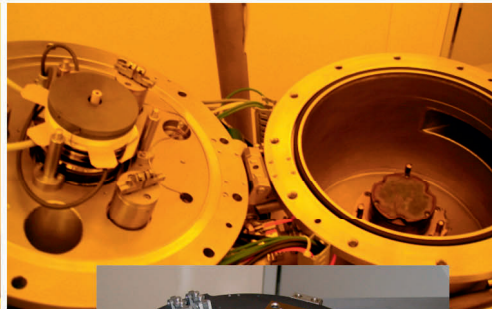
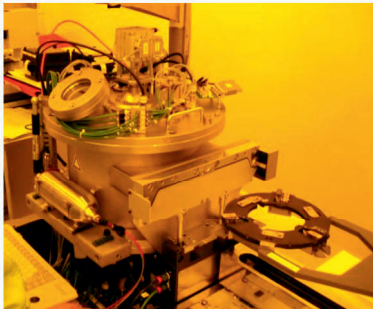
Nanoimprint Machines from EVG 620



- 8" imprint bonder in LETI / Gr noble
- imprint under vacuum
 - alignment separately in mask aligner
- (+) good accessibility, usable for anodic bonding
- (-) low pressure, speed (no water cooling)

Figure 5.7: Nanoimprint machine from EV Group based on an anodic bonder. Alignment is possible by using an appropriate mask aligner.

Nanoimprint Machines from S SS Microtec



- The S SS imprinter is based on the bonder
- using alignment fixture stacks of wafer / substrate can be transferred to the bonder
 - pre-alignment of the stamp to the substrate is possible in the S SS mask aligner (MA6) with +/- 1 m accuracy.
 - slow cooling (normally substrate is introduced into the hot machine)

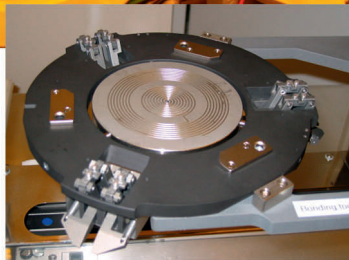


Figure 5.8: Nanoimprint machine from S ss based on an anodic bonder. Alignment is possible by using an appropriate mask aligner.

JENOPTIK HEX03 Adapter Mount with SÜSS Alignment Fixture



An adaptor for the SÜSS alignment fixture for the bonder can be integrated in the HEX.

- pre-alignment of the stamp to the substrate is possible in the SÜSS mask aligner (MA6).
- fast embossing possible (constant T)



Figure 5.9: Jenoptik HEX03 nanoimprint machine with and integrated adapter for a Süss alignment fixture for an anodic bonder. Alignment is possible by using the appropriate mask aligner.

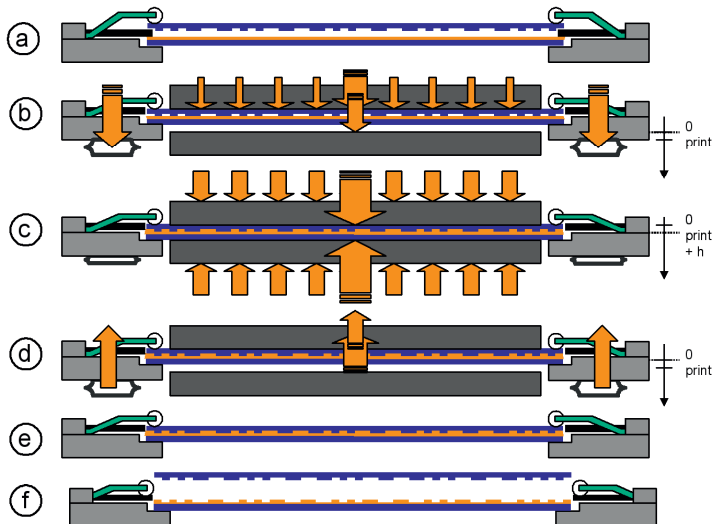
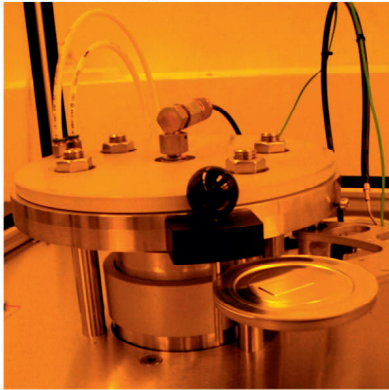
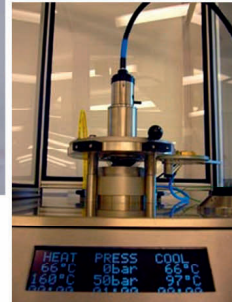


Figure 5.10: Schematic of a fast imprint with an alignment fixture: a) alignment and clamping of stamp (top) and substrate (bottom), b) contact of upper plate and down-movement, c) begin of molding upon contact to lower plate, d) pressure release and lift-up, e) cooling, f) manual demolding outside the press. For fast processing, the press plates are kept at constant (molding) temperature.

Nanoimprint Machines from OBDUCAT



- From 2.5" to 6" imprint
- imprint under vacuum, up to 250°C, 70 bar
 - alignment possible
- (+) simple setup, fast embossing, versatile tool for NIL
- (-) membrane tends to glue (small stamp on large substrate); not well adapted for micro-embossing



Thermal imprint: soft press technology, uniformity of pressure by using a membrane with air pressure over the entire imprint area

UV-cured imprint: simultaneous application of thermal and UV imprint

Figure 5.11: Nanoimprint machine from Obducat using a pressurized membrane on one side instead of a hard stamper (call soft imprint – not to be confused with soft lithography). By using a transparent membrane, thermal imprint can be combined with UV-curing.

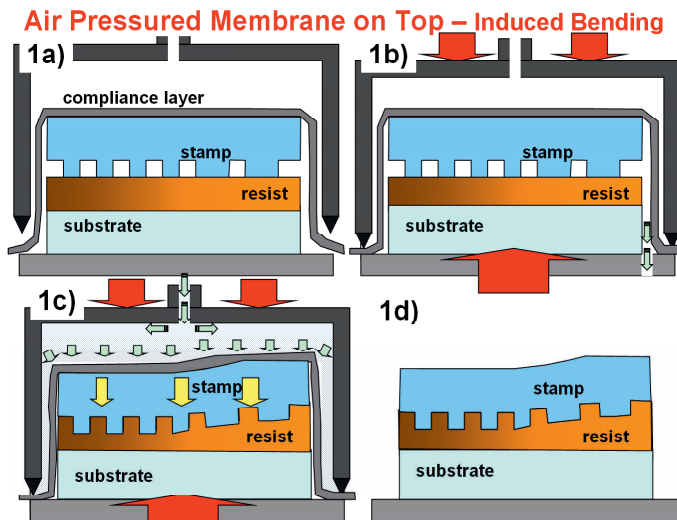


Figure 5.12: Principle of soft imprint approach by using a pressurized membrane.

5.6 Processes – Part 1 : Thermal Nanoimprint with Simple Pattern Transfer

Thermal Imprint Process

NIL was first reported as thermoplastic molding, and is therefore often referred to as hot embossing lithography (HEL). The unique advantage of a thermoplastic material is that the viscosity can be changed to a large extent by simply varying the temperature. The first stage of the NIL process is the molding of a thin thermoplastic film using a hard master. During a process cycle the resist material is made viscous by heating, and shaped by applying pressure (see Figure 5.13). Here the thermoplastic film is compressed between the stamp and substrate and the viscous polymer is forced to flow into the cavities of the mold, conforming exactly to the surface relief of the stamp. When the cavities of the stamps are filled, the polymer is cooled down, while the pressure is maintained. Thus the molten structure is frozen. After relieving the pressure, the stamp can be retrieved (demolded) without damage, and reused for the next molding cycle. The demolding step is often done by peeling (see Figure 5.14) and only by using stamps and substrates attached to the press stampers, or by using small stamps of a few mm size, parallel demolding can be anticipated. In a second step, the thickness profile of the polymer film can now be used as a resist for pattern transfer. For this, the residual layer remaining in the thin areas of the resist has to be removed, which is done by homogeneously thinning down the resist in an (ideally) anisotropic etching process. In this way, process windows are opened to the substrate and the polymer can be used as a masking layer for further processing steps (see Figure 5.15).

Thermal-NIL (Hot Embossing)

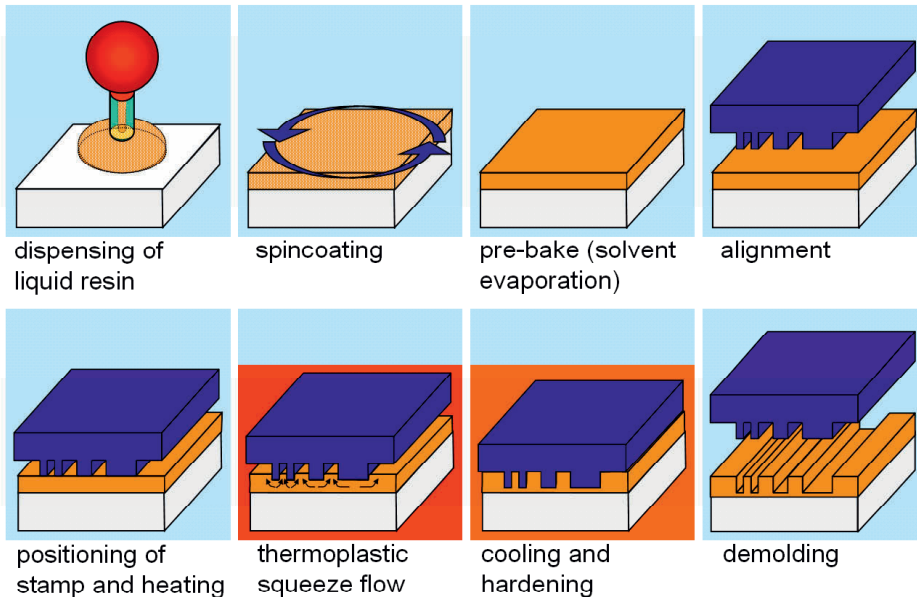


Figure 5.13: Process sequence for thermal nanoimprint (spincoating, imprint and demolding).

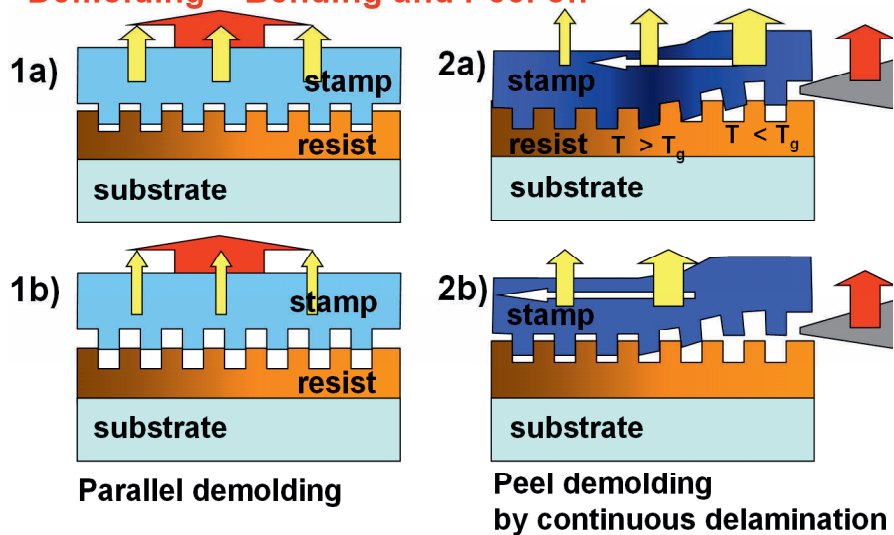
Demolding – Bending and Peel off

Figure 5.14: Principle for parallel and wedge induced demolding.

Residual Layer Etch (Substrate Window opening)

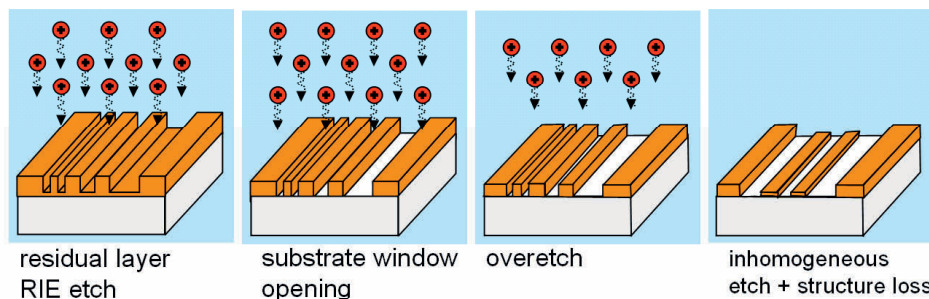


Figure 5.15: Process sequence for residual layer etching.

Short description

The residual layer is a result of the limited ability to mechanically squeeze material out of gap. In order to open windows to the substrate, the layer has to be removed, which is normally done by homogeneously thinning the resist by RIE.

Advantages

- By opening the substrate window, the substrate is chemically “activated”.

Disadvantages

- Possible dependence on structure size and depth results in inhomogeneous layer thickness.
- The exposure of the substrate to the RIE may result in damage, e.g. for biological coatings.
- Isotropic etching of structures may result in structure loss

Alternative solutions

- A hard mask below the resist may enhance the selectivity of the patterned structure with respect to the underlying substrate.
- Imprint at very high pressures was reported to result in a zero-residual layer
- A combination of imprint and exposure through a semitransparent stamp makes it possible to dissolve the residual layer in a developer after exposure of the elevated structures.

References:

- [1] M. Li, L. Chen, W. Zhang, S.Y. Chou, *Pattern transfer fidelity of nanoimprint lithography on six-inch wafers*, *Nanotechnol.* **14** (2003) 33–36
- [2] H. Schiff, S. Park, J. Gobrecht, *Nano-imprint - molding resists for lithography*, *J. Photopolym. Sci. Technol. (Japan)* **16** (3) (2003) 435–438.
- [3] H. Schiff, S. Park, C.-G. Choi, C.-S. Kee, S.-P. Han, K.-B. Yoon, J. Gobrecht, *Fabrication process for polymer photonic crystals using nanoimprint lithography*, *Nanotechnol.* **16** (2005) S261–S265.

Window Opening + Substrate Etching

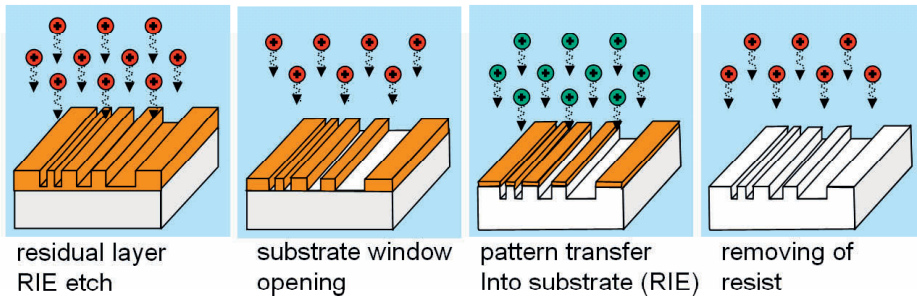


Figure 5.16: Process sequence for residual layer and substrate etching.

Short description

Etching of the substrate can be done as in normal resist processes. There is no major difference to optical or electron beam lithography

Advantages with respect to other pattern transfer processes

- Etching is the process of choice in industry because the pattern transfer is more precise than in additive processes.

Disadvantages

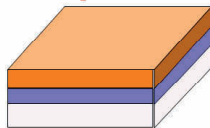
- Suitable etching gases have to be found for RIE with high selectivity.

References:

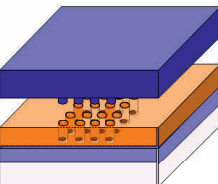
- [1] L.J. Heyderman, B. Ketterer, D. Bächle, F. Glaus, B. Haas, H. Schiff, K. Vogelsang, J. Gobrecht, L. Tiefenauer, O. Dubochet, P. Surlled and T. Hessler, *High volume fabrication of customised nanopore membrane chips*, *Microelectronic Eng.* **67-68** (2003) 208-213.

Fabrication of Sieves

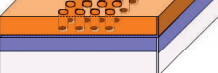
compression molding



spincoating of
thermoplast on
hard substrate

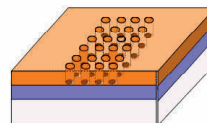


stamp
with nanorelief

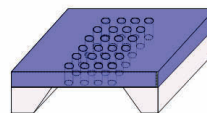


hot embossing
and demolding

pattern transfer

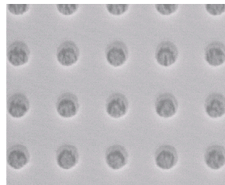
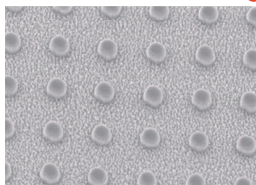


resist window
opening (RIE)
RIE into Si_3N_4



opening of
 Si_3N_4 membrane:
by wet etching

stamp



pores in Si_3N_4
period $1 \mu\text{m}$

Figure 5.17: Example for etching as a pattern transfer process after NIL.

Lift-off

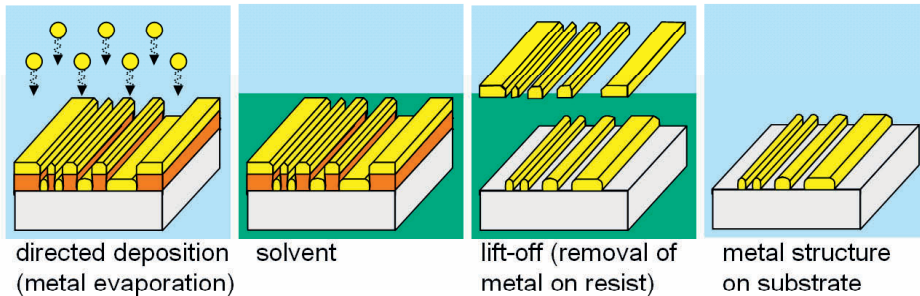


Figure 5.18: Example for lift-off as a pattern transfer process after NIL.

Short description

Lift-off is the adding of material by evaporation, and partial release of the material by dissolving the underlying resist. Lift-off works best if the resist has undercuts, which can be adjusted in optical or electron beam lithography, but not in NIL.

Advantages with respect to other pattern transfer processes

- Lift-off can be applied for a range of materials.

Disadvantages

- Directed evaporation avoiding sidewall coverage is crucial. Dependent on structure sizes.

References:

- [1] H. Schiff, R.W. Jaszewski, C. David and J. Gobrecht, *Nanostructuring of polymers and fabrication of interdigitated electrodes by hot embossing lithography*, *Microelectron. Eng.* **46** (1999) 121-124.

Fabrication of Interdigitated Electrode Arrays

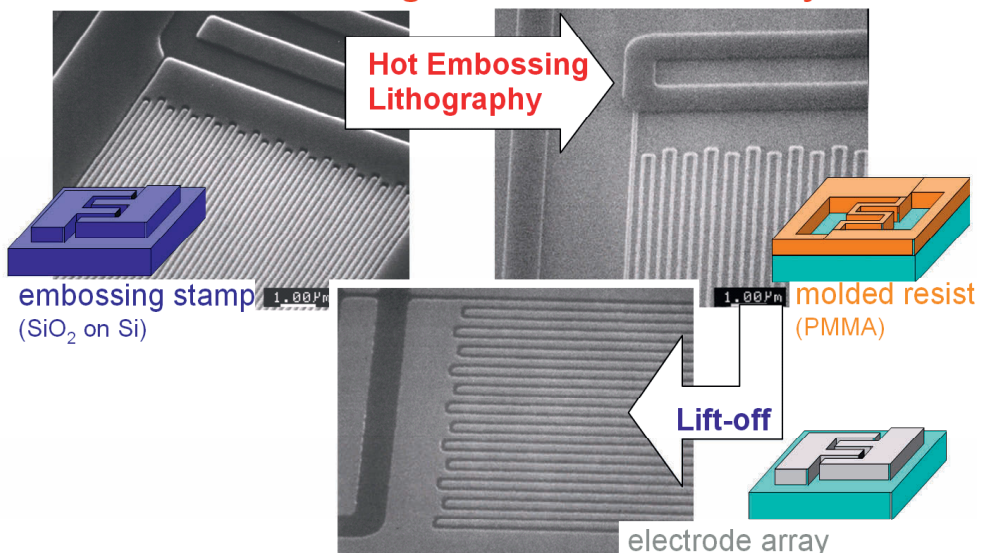


Figure 5.19: Example for lift-off as a pattern transfer process after NIL.

Electroplating

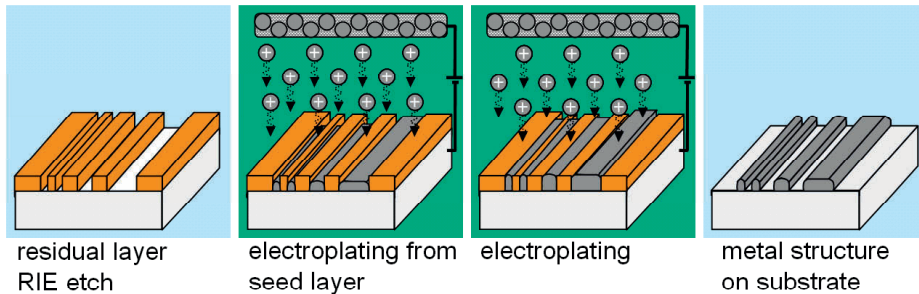


Figure 5.20: Example for electroplating as a pattern transfer process after NIL (with a conducting substrate).

Short description

Electroplating is a deposition by growing material from a solution. Lift-off works best if the resist has undercuts, which can be adjusted in optical or electron beam lithography, but not in NIL.

Advantages with respect to other pattern transfer processes

- Electroplating fills structures well from the bottom. Overplating is possible.

Disadvantages

- The range of materials is limited.
- A plating base (seed layer) has to be deposited before plating and often has to be removed selectively after plating.

References:

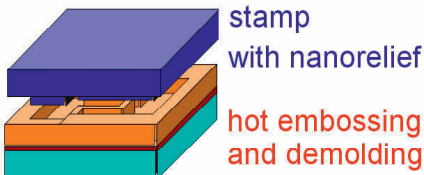
- [1] L.J. Heyderman, H. Schiff, C. David, B. Ketterer, M. Auf der Maur and J. Gobrecht, *Nanofabrication using hot embossing lithography and electroforming*, *Microelectron. Eng.* **57-58** (2001) 375-380.

Fabrication of Electrodes using Electroplating

compression molding

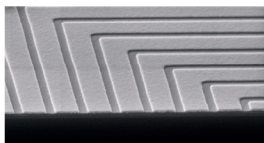


spincoating of thermoplast on hard substrate

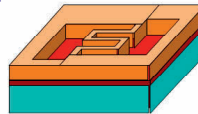


stamp with nanorelief
hot embossing and demolding

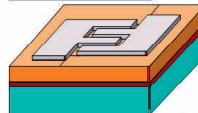
metal lanes
(period 1 μm)
PMMA: 50 nm
Nickel: 45 nm



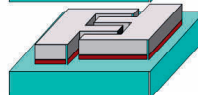
pattern transfer



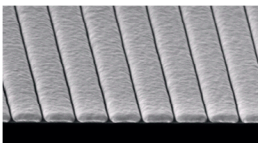
seed layer
window opening



electroforming



removing of resist and seed layer



500% overplated PMMA: 45 nm
Nickel: 270 nm

Figure 5.21: Example for electroplating as a pattern transfer process after NIL.

5.7 Processes – Part 2 : Process Variants for Resist Patterning

NIL is a parallel patterning method in which a surface pattern of a stamp is replicated into a material coated on a hard substrate by mechanical contact and 3D material displacement, to be used in fields until now reserved to electron beam lithography (EBL) and photolithography (PL). This definition fits very well for thermal NIL and UV-NIL, and can be extended to resists which can be both molded by heat and pressure and cured. It can also include all variants processes of reversal imprint, as long as a pre-patterned film is transferred and bonded to another substrate. However, often the term nanoimprint is often used when a pattern with nano-dimensions is molded in a functional material, without any further pattern transfer. Then the process is rather taking advantage of the toolbox of NIL than being a NIL process. The table 5.3 below gives an overview about the basic differences between thermal NIL and UV-NIL, but – as can be seen in the following and in Part II of this library – does not cover all possible variants of NIL processes.

Table 5.3. Comparison of hot embossing (NIL) and UV-imprint (UV-NIL), with typical parameters of current processes.

type of NIL / properties	NIL hot embossing	UV-NIL UV-imprint
basic process sequence (see Figure 6)	<ol style="list-style-type: none"> 1) spin-coat thermoplastic film 2) place stamp on film 3) heat until viscous 4) emboss at high pressure 5) cool until solid 6) demold stamp 	<ol style="list-style-type: none"> 1) dispense liquid resin 2) parallel alignment of stamp with defined gap 3) imprint at low pressure 4) expose with UV-light through stamp and crosslink 5) demold stamp
pressure p	20-100 bar	0-5 bar
temperature T_{mold}	100-200°C	20°C (ambient)
temperature T_{demold}	20-80°C	20°C (ambient)
Resist	solid, thermoplastic $T_g \approx 60-100^\circ\text{C}$	liquid, UV-curable
viscosity η	$10^3-10^7 \text{ Pa}\cdot\text{s}$	$10^{-3}-10^{-1} \text{ Pa}\cdot\text{s}$
stamp material	Si, SiO ₂ opaque	glass, SiO ₂ Transparent
stamp area	full wafer, > 200 mm diameter	25x25 cm ² , limited by control of gap
stamp contact	facilitated by bending	planarization layer
embossing time	from sec to minutes	< 1 min (per exposure)
Advantage	low-cost, large area equipment and stamps	low viscosity, low pressure, alignment through stamp
Challenge	process time, thermal expansion due to thermal cycle	step and repeat needed for large areas
development needed	alignment, residual layer homogeneity	material variety
Hybrid approaches	thermoset resists: embossing and curing before demolding	thermoplastic resists: hot molding and UV-curing before demolding
Advantage	low temperature variation cycle: demolding at high temperature possible	solid resist: full wafer single imprint possible

Thermal-NIL + Thermal Curing (before Demolding)

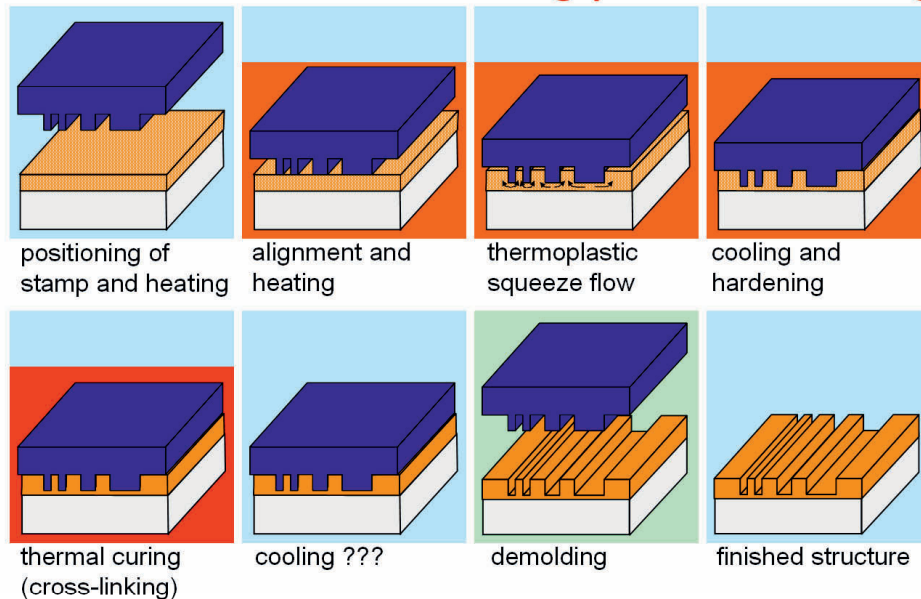


Figure 5.22: Process sequence for thermal NIL with a curable resist.

Short description

Thermal curing imprint uses a thermoset resist instead of a purely thermoplastic resist, which can be crosslinked after imprint. This is normally done before demolding, while the stamp is still within the molded resist. Maintaining the pressure during curing can compensate for shrinkage.

Main application

- Critical processes with high aspect ratio
- Isothermal processes are possible (no cooling needed before demolding)

Advantages

- The crosslinked resist can be demolded more easily, and the resist is more stable in subsequent processes.
- The resist can be used in a mix- and match process (exposure by optical lithography)

Disadvantages

- The molding and curing step have to be temporarily separated.
- resist cannot be dissolved easily, e.g. if resist is sticking to the stamp.

References:

- [1] H. Schulz, D. Lyebdyev, H.-C. Scheer, K. Pfeiffer, G. Bleidiessel, G. Grütznert, J. Ahopelto, *Master replication into thermosetting polymers for nanoimprinting*, J. Vac. Sci. Technol. B **18**(6) (2000) 3582-3585.
- [2] K. Pfeiffer, F. Reuther, M. Fink, G. Gruetzner, P. Carlberg, I. Maximov, L. Montelius, J. Seekamp, S. Zankovych, C.M. Sotomayor-Torres H. Schulz, H.-C. Scheer, *A comparison of thermally and photochemically cross-linked polymers for nanoimprinting*, Microelectron. Eng. **67-68** (2003) 266-273.

Thermal NIL + UV-Curing (after Demolding)

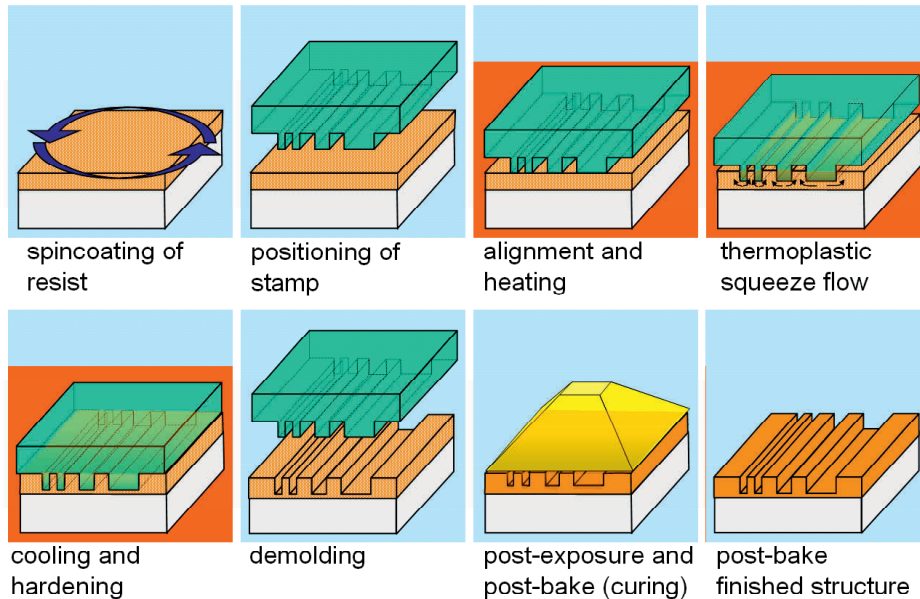


Figure 5.23: Process sequence for sequential thermal NIL into a low T_g thermoplastic material and subsequent curing.

Short description

Thermal imprint of a UV-curable material uses a thermoplastic resist instead of a liquid resin, which can be crosslinked after imprint and demolding. This can be done through exposure through the stamp (or substrate).

Main application

- Mix- and match applications.
- Isothermal processing

Advantages

- The resist can be prepared as a solid layer by spincoating before imprint. The crosslinked resist is more stable in subsequent processes.
- The resist can be used in a mix- and match process (exposure by optical lithography)

Disadvantages

- Transparent stamps or substrates needed.
- Material can be too soft for demolding before crosslinking (low T_g). Crosslinked resist cannot be dissolved easily, e.g. if resist is sticking to the stamp.

References:

- [1] F. Reuther, K. Pfeiffer, M. Fink, G. Gruetzner, H. Schulz, H.-C. Scheer, F. Gaboriau, C. Cardinaud, *Mix and match of nanoimprint and UV lithography*, Proc. SPIE **4343** (2001) 802-809.
- [2] K. Pfeiffer, M. Fink, G. Gruetzner, G. Bleidiessel, H. Schulz, H.-C. Scheer, *Multistep profiles by mix and match of nanoimprint and UV-lithography*, Microelectron. Eng. **57-58** (2001) 381-387.

UV-NIL + Residual Layer Etch + Substrate Etching

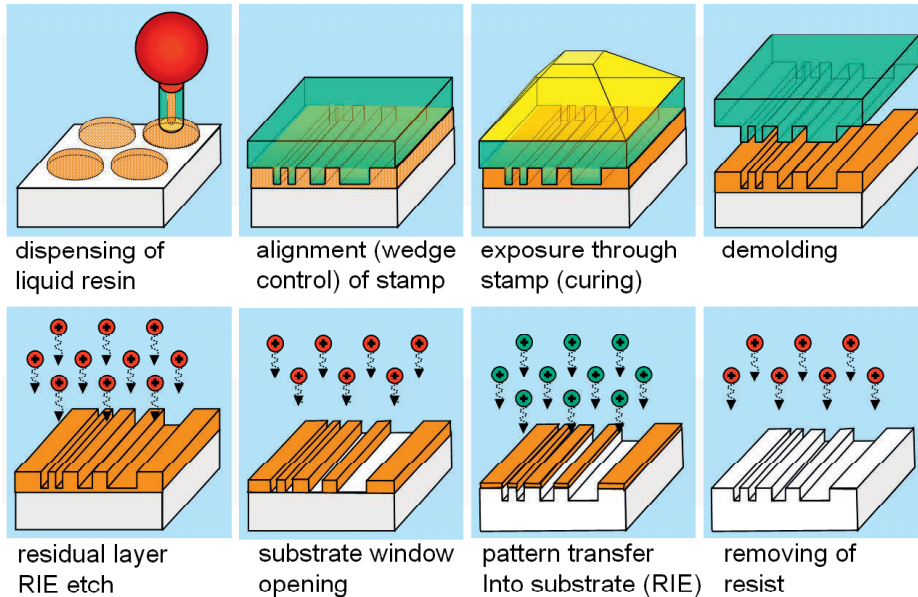


Figure 5.24: Process sequence for UV-NIL, residual layer etch and substrate etching.

Short description

With the integration of light sources into imprint machines, UV-NIL was developed for curable resists. The basic difference between UV-NIL and NIL is that a resin, which is liquid at room temperature, is shaped by a moderate pressure, which is then crosslinked and hardened by curing.

Main application

- Step & Flash Imprint Lithography (SFIL) process.

Advantages

- Low viscosity resist makes molding fast.
- Alignment through mask possible
- Room temperature process.

Disadvantages

- Liquid resist has to be applied before imprint by dispensing. Transparent stamps needed (quartz).
- Equilibration (wedge control) before exposure, low pressure does not squeeze stamp around dust particles

References:

- [1] M.D. Stewart, S.C. Johnson, S.V. Sreenivasan, D.J. Resnick, C.G. Willson, *Nanofabrication with step and flash imprint lithography*, J. Microlith. Microfab. Microsyst. **4**(1) (2005) 011002.
- [2] D.J. Resnick, W.J. Dauksher, D. Mancini, K. J. Nordquist, T.C. Bailey, S. Johnson, N. Stacey, J.G. Ekerdt, C.G. Willson, S. V. Sreenivasan, N. Schumaker, *Imprint lithography: lab curiosity or the real NGL?*, Proc. SPIE **5037** (2003) 12-23.
- [3] D.J. Resnick, S.V. Sreenivasan, C.G. Willson, *Step & flash imprint lithography*, Materials Today **8** (2005) 34-42.

Thermal + UV-NIL (before Demolding)

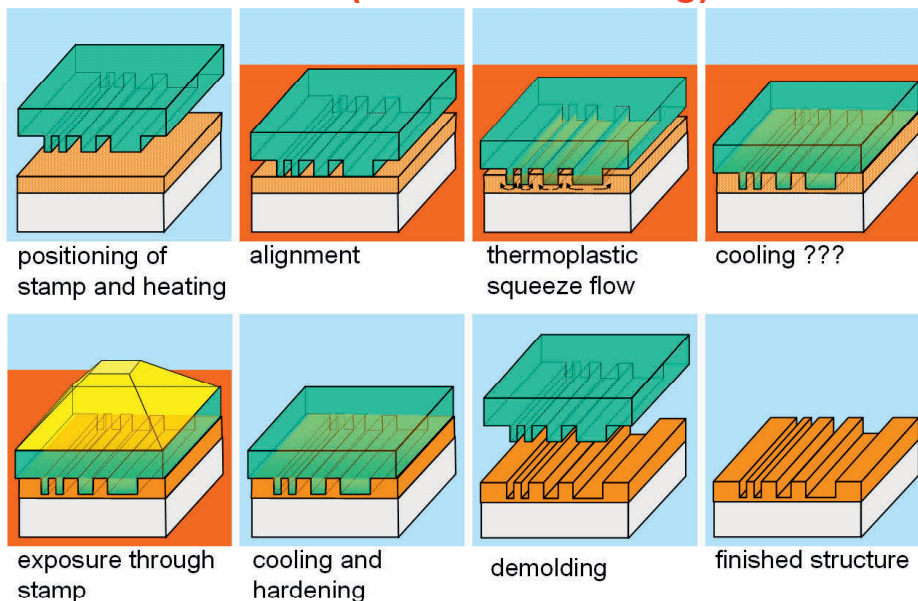


Figure 5.25: Process sequence for combined thermal and UV-NIL.

Short description

Thermal imprint of a UV-curable material uses a thermoplastic resist instead of a liquid resin, which can be crosslinked after imprint (but before demolding). This can be done through exposure through the stamp (or substrate).

Main application

- Mix- and match applications.
- Isothermal processing

Advantages

- The resist can be prepared as a solid layer by spincoating before imprint. The crosslinked resist is more stable during demolding and in subsequent processes.
- The resist can be used in a mix- and match process (exposure by optical lithography)

Disadvantages

- Transparent stamps or substrates needed.
- Crosslinked resist cannot be dissolved easily, e.g. if resist is sticking to the stamp.

References:

- [1] M. Beck, B. Heidari, *Nanoimprint lithography for high volume HDI manufacturing*, OnBoard Technology Sept. 2006, 52-55, URL: <http://www.Onboard-Technology.com/>, accessed July 11, 2007.

NIL + Photolithography (with Semitransparent Stamp)

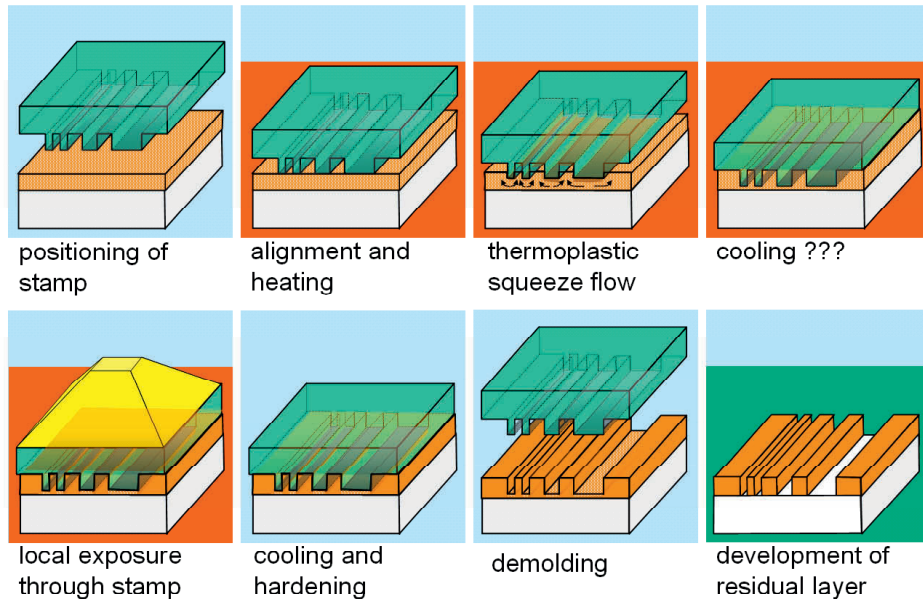


Figure 5.26: Process sequence for combined thermal and photolithography with a semi-transparent stamp.

Short description

Thermal imprint of a UV-curable material through a semitransparent stamp uses a thermoplastic resist instead of a liquid resin, which is a negative photoresist that can be crosslinked after imprint (but before demolding). This can be done through exposure through the stamp. If the elevated areas are nontransparent, then the thinned regions of the resist (residual layer) stay soluble and can be selectively removed in a developer.

Main application

- Processes where the reduction of process steps is of advantage.
- Isothermal processing

Advantages

- The resist can be prepared as a solid layer by spincoating before imprint. The crosslinked resist is more stable in subsequent processes.
- The resist can be used in a mix- and match process (exposure by optical lithography)

Disadvantages

- Semi-transparent stamps or substrates needed. Possible problems with diffraction.
- Works only for very thin residual layer thickness.

References:

- [1] X. Cheng, L.J. Guo, *A combined-nanoimprint-and-photolithography patterning technique*, *Microelectron. Eng.* **71** (2004) 277–282.
- [2] X. Cheng, L.J. Guo, *One-step lithography for various size patterns with a hybrid mask-mold*, *Microelectron. Eng.* **71** (2004) 288–293.
- [3] M.B. Christiansen, M.Schøler, A. Kristensen, *Combined nano-imprint and photolithography (CNP) of integrated polymer optics*, *Proc. SPIE* **6462** (2007) 64620.

Reversal Imprint (Hot Embossing)

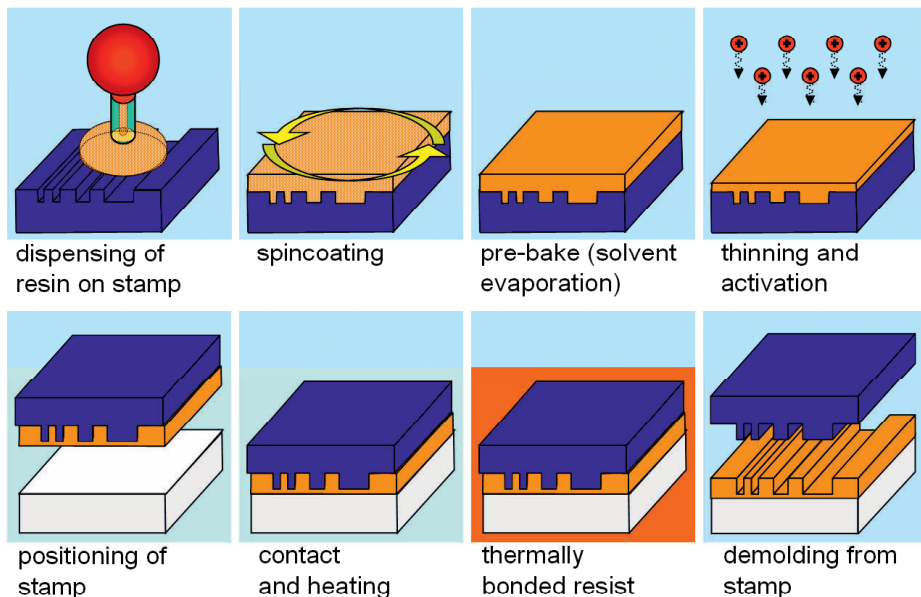


Figure 5.27: Process sequence for reversal imprint by thermal bonding of a resist layer from a stamp to a separate substrate.

Short description

Reversal imprint makes it possible to structure a resist before transfer to another substrate. The transfer is done via thermal bonding of the resist and demolding is done after bonding.

Main application

- Applications where a larger degrees of freedom is needed.
- 3D structures (embedded channels) possible

Advantages

- Patterning of substrates is possible which do not support solvents.
- Reduction of residual layer thickness possible

Disadvantages

- Spincoating on stamp with antiadhesive coating not easy.
- Possible dependence of transfer on local structure size and aspect ratio.

References:

- [1] T. Borzenko, M. Tormen, G. Schmidt, L.W. Molenkamp, *Polymer bonding process for nanolithography*, Appl. Phys. Lett. **79**(14) (2001) 2246-2248.
- [2] X.D. Huang, L.-R. Bao, X. Cheng, L.J. Guo, S.W. Pang, A.F. Yee, *Reversal imprinting by transferring polymer from mold to substrate*, J. Vac. Sci. Technol. B **20**(6), (2002) 2872-2876.
- [3] T. Yoshikawa, T. Konishi, M. Nakajima, H. Kikuta, H. Kawata, Y. Hirai, *Fabrication of 1/4 wave plate by nanocasting lithography*, J. Vac. Sci. Technol. B **23**(6) (2005) 2939-2943.
- [4] K. Sogo, M. Nakajima, H. Kawata, Y. Hirai, Yoshihiko, *Reproduction of fine structures by nanocasting lithography*, Microelectron. Eng. **84**(5-8) (2007) 909-911.

5.8 Step and Repeat Nanoimprint Lithography

Step and Stamp Imprint Lithography (SSIL) is complementary to full wafer single imprint (FWSI), because it allows to pattern entire wafers by repeated imprint of a small stamp with a lateral movement after each imprint. New setups such as the NPS300 from Suss Microtec are equipped with heating stages, and can imprint thermoplastic resists, which makes the process comparable to thermoplastic molding of full wafer stamps. Small stamps allow to employ small forces, which results in pressures similar to full wafer single imprint. By using a low density of sub-micron sized protrusions on a stamp, an extremely small residual layer thickness can be achieved, due to the high local pressure of the protrusions and the ease of the polymer to flow laterally. Then standard RIE processes, with pure oxygen at low pressure, as common in many laboratories, can be used for the etching of the residual layer with good control of CDs. In this report this is demonstrated along with the pattern transfer using standard fluorine plasma chemistry.

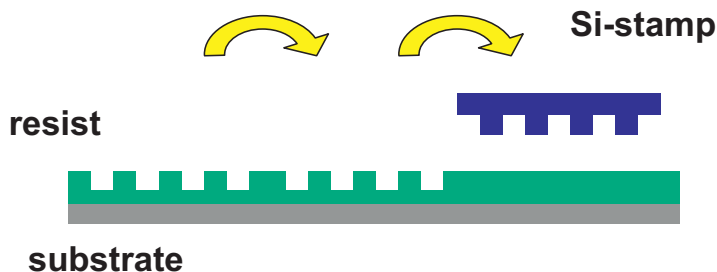


Figure 5.28: Process sequence for step and repeat imprint.

Process description : Step and Stamp Nanoimprint Lithography

Sequential imprint method, in which stamp heating and cooling are repeated in each pressure applying cycle.

Stamp and materials

Small stamp (size few millimeters). Stamp is attached to SiC-support by glue or vacuum chuck. Antiadhesive coating recommended

Process parameters

- Imprinting at 50-70 °C stamp temperature (in viscous state) and substrate temperature 0-10 °C above T_g .
- Pressure is applied until stamp and substrate are cooled 10-20 °C below T_g .
- Stamp to substrate levelling (collimation) needed before imprints. Possibility to align stamp to substrate using automatic or manual alignment
- Imprint time: From few seconds to several minutes depending on stamp size, feature density and lateral dimensions (collimation and alignment increase cycle time by 10-20 s.)

Restrictions

Wafer backside must free of particles. Wafer bending leads failure during collimation.

References:

- [1] T. Haatainen, J. Ahopelto, G. Grueztner, M. Fink, K. Pfeiffer, *Step & stamp imprint lithography using a commercial flip chip bonder*, Proc. SPIE **3997** (2000) 874 – 880.
- [2] T. Haatainen, J. Ahopelto, *Pattern Transfer using Step&Stamp Imprint Lithography*, Physica Scripta **67** (4) (2003) 357 – 360.

5.9 References

An introduction into nanoimprint for engineers and scientists:

- [1] H. Schiff and A. Kristensen, *Nanoimprint lithography*. Chapter (Part A/8) in “*Handbook of nanotechnology*”, Volume editor B. Bhushan, second edition, rev. and extended, 2007, Springer Verlag, Berlin, Germany, Hardcover. ISBN: 978-3-540-29855-7, November 2006, XLIV, 1916 pp., 1593 illus, with CD-ROM, 239-278 (2007).

A third edition with revised chapters is planned for publication in 2009.

A good overview about the state of the art in nanoimprint and critical issues:

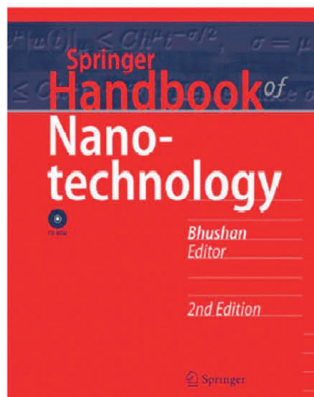
- [2] L.J. Guo, *Recent progress in nanoimprint technology and its applications*, J. Phys. D: Appl. Phys. 37 (11)(2004) R123-R141.
- [3] L.J. Guo, *Nanoimprint Lithography: Methods and Material Requirements*, Adv. Mater. 19 (2007) 495–513.
- [4] H. Schiff, *Nanoimprint lithography: An old story in modern times? A review*, J. Vac. Sci. Technol. B 26(2) 458-480 (2008).

Recent review article with emphasis on nanorheology and material deformation:

- [5] G. L.W. Cross, *The production of nanostructures by mechanical forming*, J. Phys. D: Appl. Phys. 39(20) (2006) R363–R386.

An overview about nanoimprint, with emphasis on developments in Japan (most chapters in Japanese):

- [6] Book “*Science and new technology in nanoimprint*”. Volume editor Y. Hirai. Frontier Publishing Co., Ltd., Japan, ISBN4-902410-09-5, June 2006, 281 pp., English 74-89, Japanese translation (extract) 90-93 (2006).



2nd Edition

Contents: Forewords by Neal Lane and James R. Heath
 Part A: Nanostructures, Micro- Nanofabrication, and Materials
 Part B: MEMS/NEMS and BioMEMS/BioNEMS
 Part C: Scanning Probe Microscopy
 Part D: Nanobiology and Nanomechanics
 Part E: Molecularely Thick Films for Lubrication
 Part F: Industrial Applications
 Part G: Micro- Nanoscale Reliability
 Part H: Technological Convergence and Governing Nanotechnology
 About the Authors - Subject Index
 2006, 2nd ed., Approx. 1800 p., 1349 illus., in color. With CD-ROM. Hardcover
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 For PC and Mac for the complete system requirements see: springer.com

Doi 7 November 2006

Nanoimprint lithography is an emerging nanopatterning method, combining nanometer-scale resolution and high throughput. In a top-down approach, a rigid stamp with a surface relief is pressed into a thin film of soft material on a hard substrate. The film is hardened before the stamp is retrieved, and the surface relief is copied into the thin film. A pattern with nano- to micrometer scale features can be replicated in a parallel process, and the stamp may be reused many times. This makes nanoimprint lithography a promising technique for volume manufacturing of nanostructured components. At present, structures with feature sizes down to 5 nm have been realized, and the resolution is limited by the ability to manufacture the stamp relief. For historical reasons, the term nanoimprint lithography (NIL) refers to a hot embossing process, where a thin film of thermoplastic material is softened by heating it, and the embossed film is hardened again when it is cooled down. In ultraviolet (UV)-NIL, a photo-polymerizable resin is used together with a UV-transparent stamp. The resin is liquid at room temperature, allowing easy embossing of the stamp, before the resin is hardened by UV exposure. In this chapter we will give an overview of nanoimprint lithography, with emphasis on NIL. Material aspects of stamps and resists are discussed. Thin-film rheology plays a central role of the understanding of the nanoimprint process, since the resist is patterned by mechanical deformation. We discuss specific applications where imprint methods have significant advantages over other structuring methods. We conclude by

Take a piece of wax between your fingers and imprint the fingerprints from both sides into it. The pressure is sufficiently high to replicate the soft surface pattern of our skin into the wax by mechanical deformation. The process is facilitated by the heat resulting from our blood circulation, which softens the wax in order to make it deform until it conforms to the three-dimensional (3D)

8. Nanoimprint Lithography

Nanoimprint

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discussing the areas where further development in this field is required.

Partials

pattern of our skin. Surely the fidelity of the original pattern is distorted during molding, but even an incomplete molding allows the identification of the person according to the purely two-dimensional (2D) code of its fingerprint. The pattern resolution of below 1 mm is similar to that of the first records fabricated over 100 years ago in celluloid. In 1887 *Emile Berliner* applied for a patent

Figure 5.29: Nanoimprint Lithography in Chapter A/8 of the Springer Handbook on Nanotechnology.

PART II : APPENDIX - PROCESS LIBRARY

1. Summary

This appendix contains rules for the process library, and was used by NaPa partners to prepare their processes. It is planned that these processes are either used as a growing collection of a living appendix, or used as a collection of processes which can be separately stored, e.g. as PDFs in a web page.

2. Rules for this Library

2.1 Rules

The library of processes shows and documents typical processes that can be used by customers. It gives insight into main results, but also critical steps and solutions. This is not only to lower the threshold for using a NIL or other nanopatterning process, but also to give a hint which of the processes are reliable and which process needs careful optimization. The emphasis should be on processes that are reliable (with a large process window)

The process description should be simple and compact. The aim is the chronological description of the main processes needed for the fabrication of the device, with emphasis on the issues related to the nanopatterning steps. In case that the process has been published, the main references should be added.

2.2 Structure of Processes

Every process in this library is structured in three parts: a header, a process flow and references/additional remarks. The title of the process will be as name for the process in a web-based library.

- a) The **header** should be in the format proposed here and should contain information that makes it possible to identify the process and where the process was done. The information should help to make a glossary or contents page for all processes. It would be very suitable if the device could be illustrated with one simple micrograph, which makes it possible to identify the structure and process in an easy way.
- b) The format for the **process flow** is more relaxed. The process flow should describe the process in chronological order, aiming to give relevant information about the parameters used and the critical issues.
- c) The **references** should indicate where more information can be found about this or similar processes. It could also contain more micrographs and information about the application in a concise and compact form. It should show which steps you consider as standard and at which steps further development is needed. Any further **remark**, e.g. on alternative processes, should be added at the end of the process.

2.3 New Entries

For entries into the LoP, please follow these rules

Generate front page which makes it possible to get a quick overview of the process

- a) **classify** the process (here only NIL, Soft Lithography, Stencil)
- b) **name** the process and add a **picture** (as an identifier)
- c) give major references
- d) give a **minimum information** about WHO is responsible for each step and who is the **main contact**

Stick to the format as much as possible, particularly keep all information in ONE single front page

2.4 Templates

Using the the templates is a prerequisite for any new entry. The library manager will shorten information, which does not fit to the page outline, or will move abundant information to the end of the process run sheet (remarks).

PAGE 1 : identify process / application / partner
Put essential information on this ONE page in a standardized way

BEGINNING OF PAGE 1

A.X TITLE Device (A: process category, X number, only one line!).

DESCRIPTION Fabrication of ... Short description of process (max. two lines!).

MAIN PROCESS CATEGORY Process: nanoimprint lithography, soft lithography, microcontact printing, stencil lithography **one category only**

<p>Essential: <i>Insert a micrograph or figure here which serves as an eye-catcher (rather than describing the process)</i></p>	<p>Figure: <i>Description of the micrograph (not the whole process)</i> <i>This figure should be an identifier and eyecatcher</i></p>	<p>Process: <i>processes used and tasks of partners</i> ...</p> <p>Application: ...</p>
----------------------------------------------------------------------------------------------------------------------------------------	--------------------------------------------------------------------------------------------------------------------------------------------------------	------------------------------------------------------------------------------------------------------------------------------------------------------

Keywords: thermal nanoimprint, ... – one line only

1. HEADER : identify the laboratory, the active person and the process

Project leader: LEAD PARTNER / INSTITUTE Address: postal (only town and country) Web-Address: web-page of institute	Process: partner – process Responsible: person / group E-mail: if wished
------------------------------------------------------------------------------------------------------------------------------------------------	-----------------------------------------------------------------------------------------------------

Partner: ADDITIONAL PARTNER / INSTITUTE Address: Web-Address:	Process: Responsible: E-mail:
------------------------------------------------------------------------------------------	----------------------------------------------------------

Process description: A process is described ...

Purpose: The aim of this process is ...

Major challenges: ...

Application and state-of-the-art: Research process, used for ...

Level of maturity:

Area:

Industrial relevance: for which products

References:

- [1] A.
- [2] B. ...

Contact information (only one partner):

Additional information, e.g. full address of responsible researcher or supervisor

Institute

Street

ZIP Code and Town – Country

Phone : Only if wished

This name below is standardized and should be unique : future new processes will be saved as PDF or DOC , this name will be given by the library manager

DOCUMENT NAME LoP2007_NIL000_process name (max 30 characters). PDF

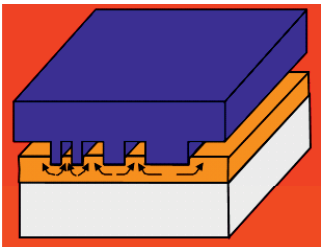
PAGE 2 and following : process description

Put PROCESS STEPS into chronological order, do not forget figures and remarks

BEGINNING OF PAGE 2

TITLE Device ... (not necessarily "fabrication of...", but short identifier, only one line!).

MAIN PROCESS CATEGORY Process: nanoimprint lithography, soft lithography, microcontact printing, stencil lithography **one category only**

	Process (general headline + figure)	Technical Parameters (specific)	Remarks (general - text)
Number	What was done in chronological order (major steps and schematic figures)	How it was done, relevant process parameters (machines, materials used, size, temperature, ...)	Critical issues and alternatives
1.0	Process 1: Preparation		
1.1	wafer selection and preparation	standard Si substrate Si substrate, 4", <100>, d=465 μm, one side polished	
1.2	substrate preparation	oxidation RCA clean (Caros Acid)	
	End of Process 1		
2.0	Process 2: Lithography		
2.1	resist coating	spincoating of PMMA	
2.2	Nanoimprint Lithography 	imprint with HEX03 (PSI) temperature.(heat).....180°C pressure.....20 kN heating time (80-180°C).. cooling time (180-80°C).. hold time (180°C)..... overall time.....20 min temperature.(demold)....80°C residual polymer thickness in grooves 20-30 nm	•
2.3		demolding	
2.4	process control	SEM	•
	End of Process 2		
3.0	Process 3: Pattern Transfer		
3.1	Residual Layer (Breakthrough) Etching	O2 RIE:	•
3.2	process control		•
	End of Process 3		
	End of Process		

General remarks:

any other relevant information

other resources (web-pages), micrographs and specific tools and processes, or information which could not be placed on page 1

END OF PROCESS DESCRIPTION

3. Nanoimprint Lithography

Contributions to this section of the library are from

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Dr. Vincent Reboud / Dr. Nikolaos Kehagias / Prof. Dr. Clivia Sotomayor-Torres

AMO GmbH, Aachen, Germany

Dr. Ulrich Plachetka

CNM - Barcelona/Spain

Irene Fernandez-Cuesta / Prof. Dr. Francesc Pérez-Murano

CRF Fiat - Orbassano/Italy

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LPN-CNRS - Marcoussis/France

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LTM-CNRS - Grenoble/France

Dr. Cécile Gourgon

MIC/DTU - Lyngby/Denmark

Prof. Dr. Anders Kristensen

PSI/LMN - Villigen/Switzerland

Dr. Helmut Schift

INFN TASC - Trieste/Italy

Dr. Massimo Tormen

Tekniker - Eibar/Spain

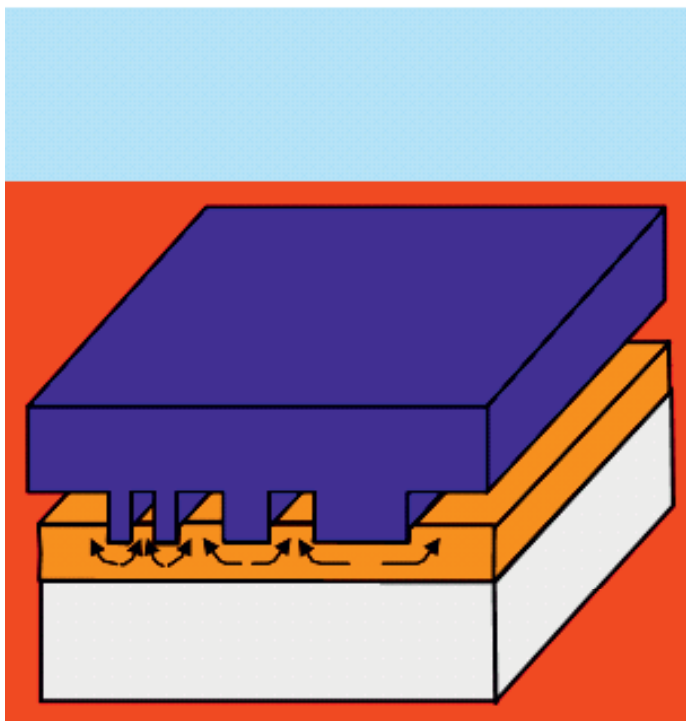
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Lund University - Lund/Sweden

Dr. Ivan Maximov / Prof. Dr. Lars Montelius



3.1 Stamps for Nanoimprint Lithography

Standard fabrication process for stamps and antiadhesive surface coating for Nanoimprint lithography

Process: nanoimprint lithography

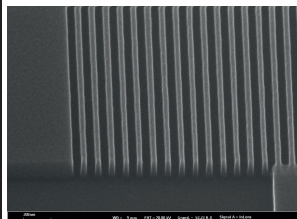


Figure:
SEM micrograph of a Grating with 100 nm period etched in Si using dry etching process (ICP) and PMMA resist as an etch mask.

Process:
Electron beam lithography on positive or negative resists and plasma etching

Application:
NIL stamps for optical, photonic, electronic or micro/nano-fluidics.

Keywords: thermal nanoimprint, electron beam lithography, plasma etching, surface coating

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Process: Thermal Nanoimprint
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Partner: Paul Scherrer Institut (PSI)
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Process: Thermal Nanoimprint
Responsible: Helmut Schiff
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Process description: A general purpose process is described for fabrication of stamp and surface functionalization for reducing adhesion forces towards polymers after the imprinting step.

Purpose: The aim of this process is to produce large arrays of microstructures (e.g. lenses) with a high control of geometrical parameters of the elements.

Major challenges: Accurate pattern definition by Electron Beam Lithography, control of sidewall profile and roughness in the reactive ion etching process, durability of surface treatment process.

Application and state-of-the-art: Standard process

References (mainly on antiadhesive coatings):

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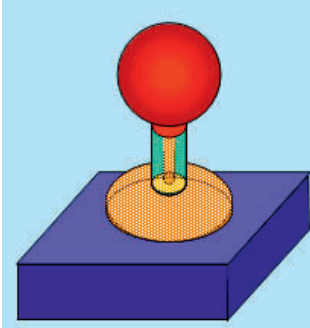
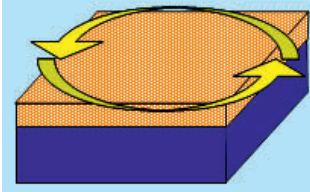
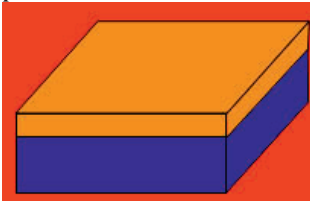
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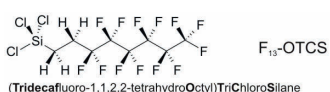
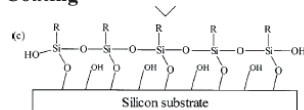
LoP2007_NIL001_Stamps for NIL. PDF

Stamps for Nanoimprint Lithography

Process: nanoimprint lithography

	Process	Technical Parameters	Remarks
	What	how it should work	critical issues
1.0	Process 1: Wafer preparation	Silicon wafer format	
1.1	wafer selection and preparation	standard Si substrate Si substrate, 4", <100>, thickness d=400-600 μm one side polished	
1.2	substrate preparation 	pretreatment no pretreatment needed (if wafer is clean and hydrophilic)	
	End of Process 1		
2.0	Process 2: Resist coating	for electron lithography	
2.1	dispensing of resist 	resist no priming Allresist PMMA 4 % in ethyl-lactate (safer solvent) (EL) (600k), process lab (clean room)	<i>Ethyl lactate is a safer solvent (in contrast to chlorobenzene (CB)) and results in similar thickness. Only for very high concentrations of PMMA (e.g. 9%) CB is a better solvent.</i>
2.2	coating resist (homogeneous layer) 	spincoating of PMMA speed: 3000rpm, acceleration: 3000rpm/sec, time: 45 s -> ~200 nm thickness	<i>PMMA is known for its high resolution as a positive resist, but has a limited sensitivity for electron exposure and etch resistance. An alternative positive resist with better etch resistance is ZEP520A. For stamps with low density of protruding structures, a solution is to use negative resists, such as NEB22, HSQ, SU8.</i>
2.3	post bake 	solvent evaporation bake 1 min @ 170°C (hot plate)	<i>Alternative: convection oven at 180°C, for 30 min</i>
	End of Process 2		
3.0	Process 3: Lithography	Electron beam lithography	
3.1	Design and file generation	Functional structures if the stamp consists of large arrays of pillars, then either: crossed gratings can be ex-	<i>The exposure strategy often depends on the preference for positive or negative resists and the pattern transfer</i>

		<p>posed in a positive resist and transferred to the substrate by RIE single dots can be exposed in a negative resist and transferred by RIE crossed gratings can be exposed in a positive resist, a metal dot pattern created by lift-off and this hard mask transferred to the substrate by RIE</p>	<p><i>process to be used. Often it is also dependent on the ability to reduce exposure time. For different resists datasheets are available with the range of exposure and development parameters.</i></p>
3.2	<p>Pattern definition</p>	<p>serial exposure with focused beam PMMA expose exposed to a 30 kV electron beam dose: 200 $\mu\text{C}/\text{cm}^2$</p>	<p><i>For different resists datasheets are available with the range of exposure and development parameters.</i></p>
3.3	<p>Resist development</p>	<p>wet development in MIBK:IPA(1:3) ...60 sec and rinsed in IPA 30 sec</p>	
End of Process 3			
4.0	Process 4: Pattern transfer		dry etching of silicon
4.1	<p>Substrate patterning</p>	<p>Dry etching of silicon A typical process uses combination of gases (e.g. C_4F_8 45sccm / O_2 3 sccm / SF_6 30sccm). The etching parameters are usually strongly dependent on the tool. In an ICP system RF Power 450 W (ICP RF source), 30 W (Platen RF source), 5.5 mTorr using PMMA as an etch mask.</p>	<p><i>Reactive Ion Etching (RIE) or Inductively Coupled Plasma (ICP) tools are highly anisotropic etching processes and can generate deep structures with vertical sidewalls or sidewalls with defined (positive) slope. Control of Critical Dimensions (CD) is needed, undercuts and roughness have to be avoided, because this results in enhanced demolding forces and damage of structures in NIL</i></p>
4.2	<p>Resist removal (stripping)</p>	<p>RIE resist ashing A low bias oxygen plasma for few seconds allows to remove the resist without damage of the patterned silicon surface. For positive resist an alternative solution is to dissolve the resist in a convenient solvent.</p>	
4.3	process control	<p>optical and electron microscopy non-destructively</p>	<p><i>destructive (cleaving, metal coating) in SEM profilometry</i></p>

	End of Process 4		
5.0	Process 5: Anti-adhesive coating	surface treatment by chemical vapor deposition	
5.1	Preparation of stamp surface	cleaning and activation Typically, RIE treatment with O ₂ plasma removes organic contaminants and activates the surface (generation of free reactive silanol bonds for silane binding) for about 60 min. Alternatively, UV-ozone treatment can be used.	<i>Alternatively to dry treatment of the surface, the cleaning and activation of the surface can be done in a fresh solution of H₂O₂:H₂SO₄ (1:4). Attention: danger of explosion! Dip the silicon stamp for 5-10 min.</i>
5.2	Solution preparation  (Tridecafluoro-1,1,2,2-tetrahydroOctyl)TriChloroSilane	Diluted silane Prepare a solution 1-10 mM of perfluorotrichlorosilane molecules in toluene. The preparation of the solution and the surface treatment is to be performed in an atmosphere with low content of humidity. A convenient solution is to operate in glovebox.	<i>Alternatively, chemical vapor deposition methods have been developed which allow to generate the silane monolayer from the gas phase. The coating should be done within about 1 hour after surface activation</i>
5.3	Coating  Silicon substrate	Dip of the stamp The stamp is inserted in the silane solution for 1-2 hours, where the silane reacts with the silanol groups of the surface, but also with neighboring molecules (crosslinking).	<i>In order to avoid the formation of a bulky deposit of molecules instead of a monolayer, washing of the stamp in acetone has to be performed in dry atmosphere.</i>
5.4	Process control	Optical microscope, AFM The quality of the antisticking layer can be done by contact angle (CA) measurement, for perfluorotrichlorosilane a CA 115° can be reached	<i>Profile control not any more with SEM (exposure and damage of anti-adhesive layer); a high CA can also be a result of roughness due to deposits; these deposits are removed after a few imprints</i>
	End of Process 5		
	End of Total Process		

General remarks:

This is only one of many processes to fabricate stamps in a silicon substrate by e-beam lithography. Basically every cleanroom provides processes using different resists for electron beam or other lithographies. Apart from PMMA directly coated on Si, hard (metal, e.g. Cr) masks are beneficial for etch ratio enhancement. They can be applied at the bottom of the resist and etched, or evaporated onto the patterned resist and locally removed by lift-off. Furthermore negative resists are commonly used.

In case of substrate etching, care has to be taken that undercuts and high sidewall roughness are avoided. Sloped sidewalls are beneficial but no prerequisite for moderate aspect ratio structures. A further issue is that residual polymer or other contaminants deposited during the etching on the structure sidewalls should be fully removed before applying the antiadhesive coating. In most cases this can be effectively done in wet (oxidizing) etching or ashing in oxygen plasma, which is also the step to activate surface (creating silanol groups) for silane binding.

3.2 Suspended Polymer Membranes

Fabrication of suspended polymer membranes on LOR resist

Process: nanoimprint lithography

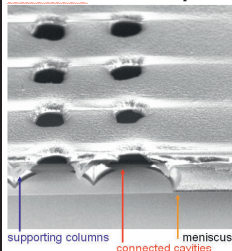


Figure:

SEM micrograph of a pore array in 1 μm thick polystyrene supported by 2 μm high pillars with 3 μm hole diameter and 5 μm period (cleaved sample)

Process:

Thermal nanoimprint of a thermoplastic polymer on top of a sacrificial polymer. Pattern transfer using RIE and underetch.

Application:

Microfluidic devices (alternative to sieves based on pillar array)

Keywords: thermal nanoimprint, double resist, sacrificial layer, perforated membrane

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Process: Thermal Nanoimprint

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Process description: A process for polymeric sieve structures is presented. It is based on a two-layer resist (LOR) with a sacrificial layer below a thermoplastic resist. Because the two polymer layers have different sensitivities to solvents, the LOR can be selectively dissolved through the pores.

Purpose: The aim of this process is not the fabrication of a specific device, but to demonstrate a process sequence which the specific requirements on NIL processing.

Major challenges: While the thermoplastic molding step is standard therefore standard resists such as PMMA, PS or COC, as well as the common MRT resists can be interchanged, the LOR dissolution is dependent on structure sizes, resist thickness and process conditions.

Application and state-of-the-art: Research process, used for DNA separation

References:

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- [2] H. Schiff, S. Bellini, U. Pieves and J. Gobrecht, *Sustained polymer membranes fabricated by nanoimprint lithography*, *J. Microlith., Microfab., Microsyst.* **5**(1), 011010 (Jan–Mar 2006).


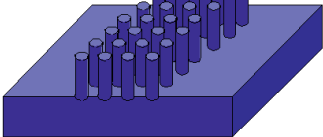
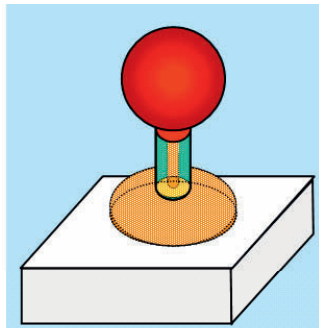
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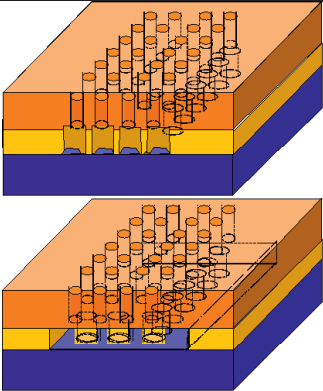
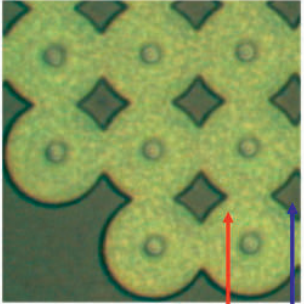
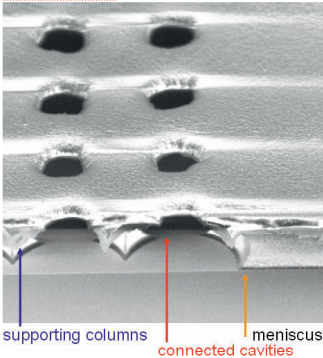
LoP2007_NIL002_suspended polymer membranes. PDF

Suspended Polymer Membranes

Process: nanoimprint lithography

	Process	Technical Parameters	Remarks
	What	How it should work	Critical issues
1.0	Process 1: Wafer preparation		
1.1	wafer selection and preparation	standard Si substrate Si substrate, 4", <100>, thickness d=465 μm one side polished	
1.2	substrate preparation 	no pretreatment	
	End of Process 1		
2.0	Process 2: Stamp preparation		
2.1	layout 	Functional structures the stamp consist of large arrays of pillars (about 1mm ² area) with a 10 mm pitch between arrays, all over the wafer. Arrays consist of orthogonal patterns with pillar diameters from 1.5 to 6 μm and periods of 5 to 15 μm (800 nm deep). The (p : a) combinations were (5:1.5), (5:3), (10:2), (10:4), (15:4) and (15:6) μm.	<i>microstructures are very good for the set-up of the process, because the process control can be done using optical microscopy</i>
2.2	antiadhesive coating	silane CVD evaporation standard process	<i>silane coating from gas phase is beneficial for side-wall coating</i>
	End of Process 2		
3.0	Process 3: Lithography		
3.1	coating of layer 1 (sacrificial layer) 	double-spincoating of LOR no priming LOR 10B from Microchem™ 3000rpm, 60 s -> ~1000nm bake 3 min @ 190°C (hot plate) 3000rpm, 60 s -> ~1000nm bake 3 min @ 190°C (hot plate) total thickness: 2000 nm	<i>long prebake of 3 min at 190°C on a hot plate was chosen in order to achieve a high T_g and a low etching rate almost independent from further heat treatment</i>
3.2	coating of layer 2 (functional NIL layer)	spincoating of PS no priming of LOR Polystyrene 125kg/kmol, Polyscience GmbH, dissolved in dissolved in toluene 3000rpm, 60 s -> ~1000nm bake 1 min @ 170°C (hot plate)	<i>PS was chosen because of its excellent optical and physiological properties.</i>

<p>3.3</p>	<p>Nanoimprint Lithography</p>	<p>Jenoptik HEX03 (PSI) no vacuum stack preassembled before heating and pressing (order from top to bottom): PI (polyimide) 50µm, PDMS (standard) 1mm, PI 50µm stamp (loose or clamped) substrate with resist, PI 50µm temperature.(heat).....180°C pressure.....20 bar heating time (80-180°C).. cooling time (180-80°C).. hold time (180°C).....30min overall time.....40 min temperature.(release)....70°C residual polymer thickness in grooves 150 nm</p>	<p><i>the PI (polyimide) reduces the adhesion of the PDMS to the silicon</i> <i>the loosely assembled stack is first fixed with contact force(for better heat transfer), then heated to $T_{process}$ then equilibrated, and pressure applied</i> <i>cooling while pressure is kept constant</i> <i>The thickness of the resist h_{top} (1000nm) was chosen in order to have a sufficient lateral flow of material with the 800 nm high structures.</i> <i>Similar values and process parameter were used for PS, PMMA and COC</i></p>
<p>3.4</p>		<p>demolding pressure release at about 70°C demolding manually by applying a razor blade between stamp and substrate and inducing a wedge</p>	<p><i>demolding of dense array of pillars more difficult</i> <i>reduction of thermal expansion by molding at low / demolding at high temperatures</i></p>
<p>3.5</p>	<p>process control</p>	<p>optical microscopy non-destructively</p>	<p><i>destructive (cleaving, metal coating) in SEM profilometry</i></p>
<p>End of Process 3</p>			
<p>4.0 Process 4: Pattern Transfer</p>			
<p>4.1</p>	<p>Residual Layer (Breakthrough) Etching</p>	<p>RIE Oxford Plasmalab 100: thinning of resist PMMA etch with no cooling O₂.....20 sccm gas pressure 20 mtorr power 20 W temperature 300 K etching rates PS 30 nm/min, LOR 10B 48 nm/min</p>	<p><i>residual layer can either be measured by profilometry (near the relevant structures)</i> <i>PS etching rate in oxygen plasma is significantly lower relative to LOR, which means that once the windows are opened, the etching continues at a higher speed in the LOR</i></p>
<p>4.2</p>	<p>process control</p>	<p>Profilometer /Microscope</p>	
<p>4.3</p>	<p>Sacrificial layer etching</p>	<p>LOR wet etching Microposit MF319 (from Microchem™) dilution of MF319/water of 3:2 (60%) underetching rates of LOR range from 2.5 nm/sec for</p>	<p><i>The developer penetrates the pores and dissolves the LOR isotropically.</i> <i>In order to reduce the process time, the dilution was changed to 5:1 (85%). In this</i></p>

		<p>smaller to 5 nm/sec for larger periods For the (10:2) μm combination a time t_{min} of about 13 min for half the distance etch was observed. Stopping the process was possible by extensive rinsing in de-ionized water. After drying in nitrogen, the water is completely removed from the cavities.</p>	<p>case the underetching rates were enhanced and range from 22 nm/sec to 36 nm/sec. Although for combinations of smaller periods and pore diameters the underetching rate slows down, no limitation for the application of this technique for smaller diameters of below $1\mu\text{m}$ could be seen.</p>
<p>4.4</p>	<p>process control</p>  <p>b) connected cavities with supporting columns</p>	<p>optical microscope 100 x</p> <p>Connected cavities with supporting columns (PS $1\mu\text{m}$ / LOR $1\mu\text{m}$, view size $30 \times 30\mu\text{m}^2$). The area between the pores and the sidewalls of the undercuts (bright) defines the membrane, and contrasts well the border and columns (dark) in diamond shape</p>	<p>online, without breaking substrate pores and undercuts with $<0.4\mu\text{m}$ can be resolved, not suitable for nanopores ($<200\text{nm}$)</p>
<p>4.5</p>	<p>process control</p>  <p>supporting columns connected cavities meniscus</p>	<p>SEM</p> <p>Micrograph of a pore array in $1\mu\text{m}$ thick polystyrene supported by $2\mu\text{m}$ high pillars with $3\mu\text{m}$ hole diameter and $5\mu\text{m}$ period (cleaved sample)</p>	
	<p>End of Process 4</p>		
	<p>End of Total Process</p>		

General remarks:

3.3 Polymer Multilayeres by Reverse UV-NIL

Fabrication of multi-layered woodpile-like structures by reverse UV-NIL

Process: nanoimprint lithography

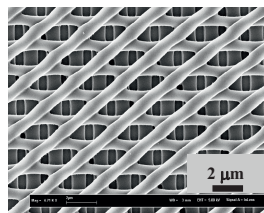


Figure:

SEM images of a three-layer woodpile-like structure fabricated by the reverse contact imprinting technique.

Process:

A lift-off resist and a UV cross-linkable polymer are spin-coated successively onto a patterned UV mask-mold. These thin polymer films are then transferred from the mold to the substrate by contact at a suitable temperature and pressure. The whole assembly is then exposed to UV light. After separation of the mold and the substrate, the unexposed polymer areas are dissolved in a developer solution leaving behind the negative features of the original stamp.

Application:

Microfluidic devices, Photonic crystals

Keywords: reverse nanoimprint lithography, three-dimensional nanofabrication

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Process description: A lift-off resist and a UV cross-linkable polymer are spin-coated successively onto a patterned UV mask-mold. These thin polymer films are then transferred from the mold to the substrate by contact at a suitable temperature and pressure. The whole assembly is then exposed to UV light. After separation of the mold and the substrate, the unexposed polymer areas are dissolved in a developer solution leaving behind the negative features of the original stamp.

Purpose: This process delivers a resist pattern transfer without a residual layer thereby rendering unnecessary the etching steps typically needed in the imprint lithography techniques for three-dimensional patterning. Three-dimensional woodpile-like structures were successfully fabricated with this new technique.

Major challenges: At a too high temperature and pressure, the polymer layer will flow in the underlying structure. The UV exposure dose must be controlled to avoid the formation of a residual layer. The UV light diffracted by the metallic protrusion of the stamp may be back-scattered from the imprinted substrate. The control of the exposure dose can be done by selecting the light intensity and the exposure time.

References:

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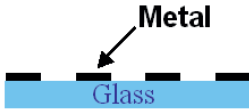

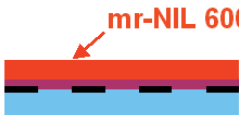
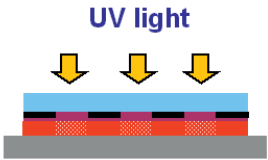
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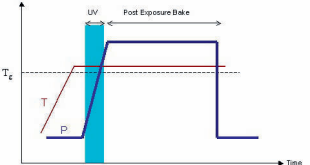

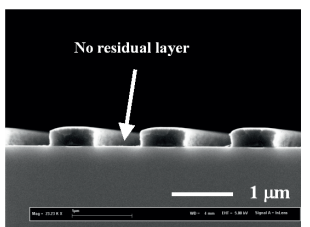
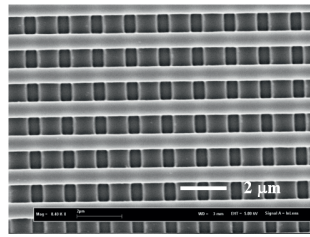
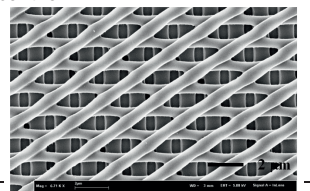
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LoP2007_NIL003_RUVNIL woodpile. PDF

Polymer Multilayers by Reverse UV-NIL

Process: nanoimprint lithography

	Process	Technical Parameters	Remarks
	What	How it should work	Critical issues
1.0	Process 1: Wafer preparation		
1.1	wafer selection and preparation	Standard Si substrate Si substrate, <100>, thickness $d=500\ \mu\text{m}$ one side polished Standard glass or Pyrex substrate	
1.2	substrate preparation 	no pre-treatment for the first layer	
	End of Process 1		
2.0	Process 2: Stamp preparation	Standard glass or Pyrex substrate with metal protrusion	
2.1	layout 	Functional structures the stamp consist of gratings (about $5\ \text{mm}^2$ area) with a pitch variation from $200\ \text{nm}$ to $10\ \mu\text{m}$ between lines, all over the wafer.	
2.2	Spin coat sacrificial polymer layer 	A thin film of lift-off resist (LOR 1A from Micro Chem) is spin coated at $1000\ \text{rpm}$ for $1\ \text{min}$ on the stamp and baked at $150\ ^\circ\text{C}$ for $5\ \text{min}$. This sacrificial polymer layer is used as an adherence promoter, a planarization layer and to protect the stamp from contamination by the photo-curing resist.	<i>No antiadhesive coating needed</i>
2.3	Spin coat UV crosslinkable polymer 	A film of a UV crosslinkable polymer (mr-NIL 6000 from micro resist technology) is spin coated at $3000\ \text{rpm}$ on the LOR layer and soft-baked at $120\ ^\circ\text{C}$ for $5\ \text{min}$ to evaporate the residual solvent	
	End of Process 2		
3.0	Process 3: Lithography		
3.1	Reverse imprint  Heat, pressure, UV light exposure apply	The polymer bilayer is reverse imprinted onto a Si substrate. Stamp and substrate are then heated to a temperature above the T_g of mr-NIL 6000 and exposed to UV radiation. Optimized imprint parameters on a non-flat substrate are: temperature of $90\ ^\circ\text{C}$, UV exposure time of $3\ \text{s}$, pressure of $40\ \text{bars}$ and PEB time of $30\ \text{s}$.	The UV exposure dose must be controlled to avoid the formation of a residual layer. The UV light diffracted by the metallic protrusion of the stamp may be back-scattered from the imprinted substrate. The control of the exposure dose can be done by selecting the light intensity and the exposure time. In our experiments the dose was con-

	 <p>Schematic of RUVNIL process showing the time at which point of UV light exposure occurs and the time of post exposure baking.</p>	<p>Nanoimprint has been performed with a 2.5" Obducat embosser.</p>	<p>trolled by the time duration of UV light exposure. As shown in Figure below the UV light must be applied just before the pressure is applied in order to avoid a polymer flow in the underlying first imprinted layers. The trade-off of the imprint process has been performed.</p>
<p>43.2</p>	<p>Separation and development.</p> 	<p>Demolding Demolding in a developer bath. Unexposed polymer areas as well as the LOR layer are removed with acetone and/or remover 1165 (Shipley) leaving behind the negative features of the original stamp. No residual layer in final structure.</p>	<p><i>The oxygen plasma-etching step, usually necessary in standard NIL is avoided.</i></p>
<p>End of Process 3</p>			
<p>4.0 Process 4: Pattern Transfer</p>			
<p>4.1</p>	<p>First layer transfer</p> 	<p>Test of the technique on a flat Si substrate. The imprint temperature was carried at 90 °C with 40 bars of pressure applied for 30sec. UV light exposure was applied for 3 sec prior applying the pressure.</p>	<p><i>Due to the difference of surface energies between the stamp surface and the Si substrate, the polymers are successfully transferred onto the Si substrate.</i></p>
<p>4.3</p>	<p>Second layer transfer</p> 	<p>Imprint parameters on a non-flat substrate are: temperature of 90 °C, UV exposure time of 3 s, pressure of 40 bars and PEB time of 30 s.</p>	<p><i>Surface patterned about 4 mm²</i></p>
<p>4.4</p>	<p>Third layer transfer and process control</p> 	<p>Imprint parameters on a non-flat substrate are: temperature of 90 °C, UV exposure time of 3 s, pressure of 40 bars and PEB time of 30 s.</p>	<p><i>Surface patterned less of 0.5 mm²</i></p>

4.5	Process control	Optical microscopy <i>non-destructively</i> SEM <i>destructive (cleaving, metal coating)</i>	
	End of Process 4		
	End of Total Process		

General remarks:

Other references:

- [3] N. Kehagias, G. Chansin, V. Reboud, M. Zelsmann, C. Schuster, M. Kubenz, F. Reuther, G. Gruetzner, C. M. Sotomayor Torres, Embedded nano channels fabricated by non-selective reverse contact UV nanoimprint lithography technique, Microelectronic Engineering, accepted.

3.4 Combined Nanoimprint and Photolithography

Fabrication of optical SU-8 integrated optics by Combined Nanoimprint and Photolithography (CNP)

Process: Combined Nanoimprint and Photolithography (CNP)

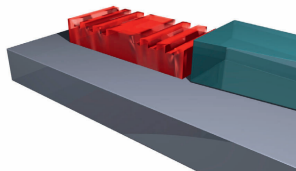


Figure:

Schematic illustration of a polymer DFB laser made of Rhodamine 6G laser dye doped SU-8, integrated with an undoped SU-8 waveguide

Process:

Combined nanoimprint and photolithography using a hybrid stamp/UV mask

Application:

Definition of arbitrary structures containing nm to mm sized features, and made from an imprintable and UV definable material

Keywords: combined nanoimprint and photolithography, CNP, polymer optics, integrated optics

Project leader: MIC - DTU

Address: DTU building 345E, 2800 Lyngby, Denmark

Web-Address: www.mic.dtu.dk/ak

Process: CNP

Responsible: Anders Kristensen

E-mail: ak@mic.dtu.dk

Process description: A process is described for waferscale definition of nm to mm sized optical structures by combining nanoimprint lithography with UV lithography. A hybrid stamp/UVmask is used and additional structures are added in a standard UV lithographic process. Both active (lasers) and passive (waveguides) optics are defined.

Purpose: Definition of rhodamine 6G laser dye doped SU-8 first order DFB lasers integrated with optical waveguides

Major challenges: Stamp/mask fabrication. The fact that the stamp is made of quartz complicated E-beam lithography somewhat, but once the stamp is done, the process is quite straight forward.

Application and state-of-the-art: Research process, used for definition of polymer lasers and integrated waveguides.

References:

- [1] M. B. Christiansen, M. Schøler, and A. Kristensen, "Integration of active and passive polymer optics", *Optics Express* 15(7) pp. 3931-3939 (2007)

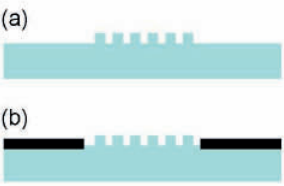

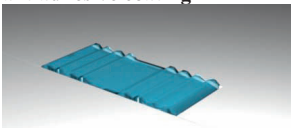


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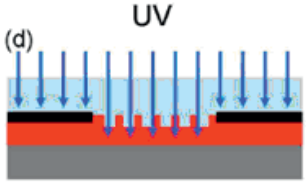

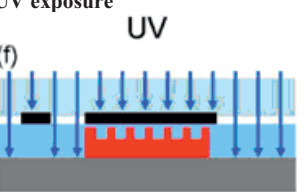
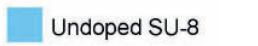

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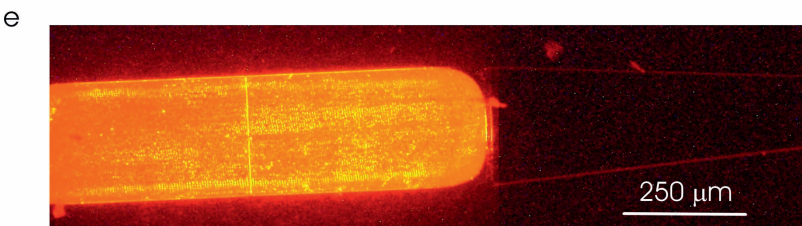
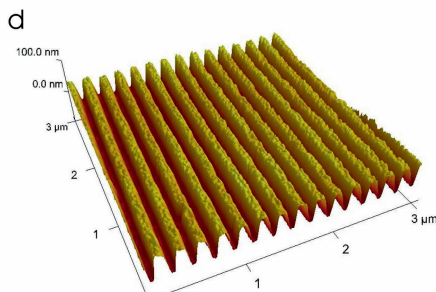
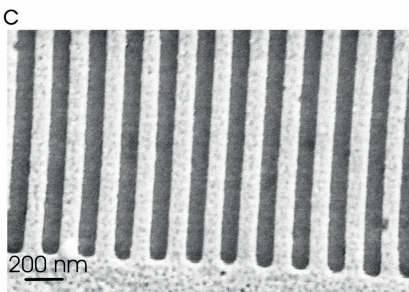
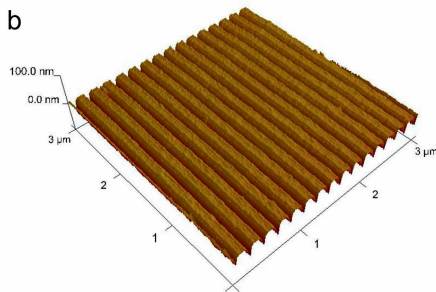
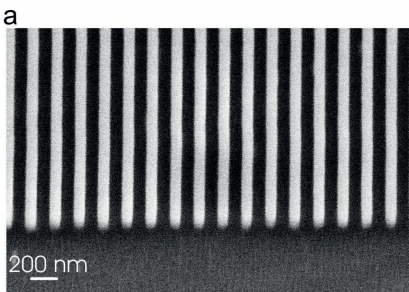
LoP2007_NIL004_CNP Combined NIL and PL process.PDF

Combined Nanoimprint and Photolithography

Process: nanoimprint lithography

	Process	Technical Parameters	Remarks
	What	how it should work	critical issues
1.0	Process 1: Wafer preparation		
1.1	wafer selection and preparation	Si substrate, 10 cm,	
1.2	substrate preparation	oxidation thermal oxide, approximately 3 μm	
	End of Process 1		
2.0	Process 1: Stamp preparation		
2.1	layout 	Functional structures the stamp is made of fused silica, with an integrated Cr shadow mask. In the mask windows, which are 1 mm by 250 microns, 100 nm tall glass lines with a width of approx. 100 nm and a period of approx. 200 nm are protruding.	
2.2	antiadhesive coating  <i>Stamp layout</i>	FDTS coating Standard recipe in MVD 100 molecular vapour deposition tool from Applied Microstructures Inc.	<i>Rather slow deposition is chosen to allow good side-wall coverage</i>
	End of Process 2		
3.0	Process 3: Combined nanoimprint and UV lithography (CNP)		
3.1	coating of layer 1	spincoating of Rh6G doped SU-8 no priming SU-8 2002 from MicroChem thinned to 20% with 3.2 μmol Rh6G dye per g solid. Spun at 7000 RPM, 3000 RPM/s, 60s. Pre-baked @ 90°C for 1 min	
3.2	thermal imprint 	EVG 520HE imprinter stack preassembled before heating and pressing (order from top to bottom): Al foil graphite (standard) 0.5 mm, stamp substrate with resist, graphite Al foil temperature.(heat).....100°C pressure.....(10 kN) hold time (100°C).....10 min overall time.....45 min temperature.(release)....40°C residual polymer thickness in	

		grooves 150 nm on purpose. We just want a surface corrugation	
3.3	UV exposure 	Karl Suss aligner 9 mW/mm ² 30 s x 11 with 15 s breaks PEB: 90°C, 2 min	
3.4	Demolding	Separation using scalpel	
3.5	Development 	PGMEA 30s IPA rinse N ₂ or spin dry	
3.6	process control	SEM and AFM	
	End of Process 3		
4.0	Process 4: Waveguide definition		
4.1	Spin coat	spincoating of undoped SU-8 no priming SU-8 2005 from MicroChem Ramp to 500 RPM at 100 RPM/s. Ramp to 3000 RPM at 300 RPM/s, spin for 30 s Pre-baked @ 90°C for 1 min	
4.2	UV exposure 	Cr Mask used. Aligned to laser layer Karl Suss aligner 9 mJ/mm ² Hard contact 20 s PEB: 90°C, 2 min	
4.3	development 	PGMEA 3 min IPA rinse N ₂ or spin dry	
4.4	process control	Optical microscope, AFM and SEM, see figure below:	



SEM and AFM of hybrid stamp/UV mask (a-b) and imprinted structures (c-d). (e) is an optical microscope image of an operating SU-8/rhodamine 6G laser integrated with an SU-8 waveguide, where the pump light is filtered away.

End of Process 4		
End of Total Process		

3.5 Double Side Patterned OLED

Fabrication of OLED device with double side patterned substrate

Process: nanoimprint lithography



Figure:

Organic light emitting device with both side nanopatterned surfaces with squared shape (resolution 1 μm and height 300 nm).

Process:

OLED device fabrication on double side UV nanoimprinted substrate.

Application:

Lighting systems and displays.

Keywords: OLED, UV nanoimprint

Project leader: Centro Ricerche Fiat

Address: Strada Torino 50, 10043, Orbassano (TO)

Web-Address: www.crf.it

Process: OLED fabrication

Responsible: Vito Lambertini

E-mail: vitoguido.Lambertini@crf.it

Process description: A process is described to fabricate a light emitting devices based on organic materials deposited by spin coating onto a double side nanopatterned substrate. The process described for the double side patterning is UV nanoimprinting.

Purpose: The aim of this process is demonstrate the increasing of efficiency more than 50% introducing low cost nanostructured surfaces enhancing the light extraction.

Major challenges: Anti-sticking treatments and deposition of ITO on plastic materials.

Application and state-of-the-art: the structuring of OLED device has been proposed in several work mainly based on microstructuring. Only in the last 2 years the introduction of sub-wavelength patterns has been proposed.

References:

- [1] Improvement of the external extraction efficiency of OLED by using a pyramid array, Stanley Electric Co., Ltd. (Japan)
- [2] Nanohole OLEDs embedded in the 2D periodic SiO₂ nanohole array. Yoon-Chang Kim R&D Center, Samsung SDI Co. Ltd., Young Rag Do Dep. of Chemistry, Kookmin Un., Seoul, 2005 Optical Society of America.

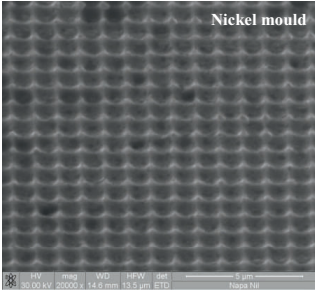
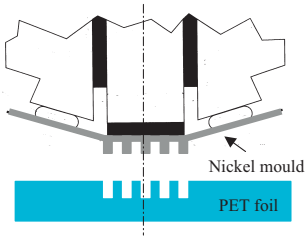
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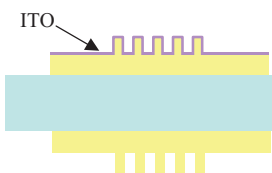
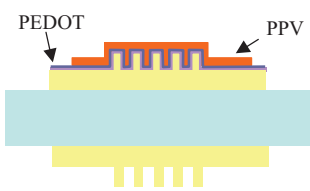
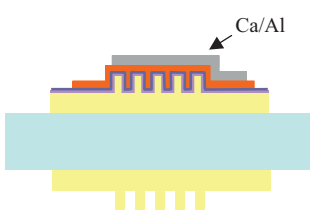
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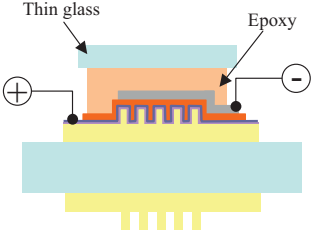
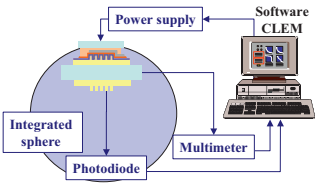
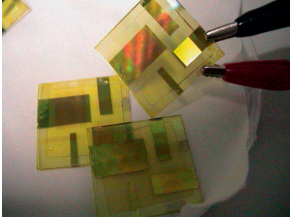
Double Side Patterned OLED

Process: nanoimprint lithography

	Process	Technical Parameters	Remarks
	What	how it should work	critical issues
1.0	Process 1: Substrate preparation		
1.1	wafer selection and preparation	transparent substrate Glass substrate 35x45 mm Thickness 1 mm	
1.2	substrate preparation	Cleaning washing in Micro90 solution diluted (2%); ultrasonic baths cycles (5 min) in water and ethanol	
1.3	adhesive coating	treatment spin coating of MICROPOSIT or AP300 followed by 80°C for 2 min.	
	End of Process 1		
2.0	Process 2: Flexible stamp preparation		
2.1	Layout 	Functional structures the stamp consist of: nickel mould squared pattern height 300 nm period 1 µm wafer selection 100 µm sheet PET	
2.2	stamp preparation 	Hot embossing JRP recombiner machine: Nickel shim thickness 50 µm; Shim dimensions 30x40 mm; Heating time 0.5 s Cooling time 10 s DC current 80 A Pressure 1.4 tons	

<p>2.3</p>	<p>Process control</p>	<p>SEM</p>	
<p>2.4</p>	<p>antiadhesive coating</p>	<p>silane saturation chamber 1 min</p>	
<p>End of Process 2</p>			
<p>3.0 Process 3: Double UV imprinting</p>			
<p>3.1</p>	<p>UV resin casting</p>	<p>UV polymers: UV acrylates (bisphenol-A-diglycidyl-ether-diacrylates BGEDA, bi-functional acrylates EBECRYL 210, 270, 600); organic modified alkoxy silanes (ORMOCLAD).</p>	<p><i>No bubbles formation during flexible stamp positioning.</i></p>
<p>3.2</p>	<p>UV curing</p>	<p>EVG620 mask aligner stack pre-assembled before UV exposition outside the machine. Exposition time 10 s.</p>	
<p>3.3</p>	<p>Demolding</p>	<p>Manual demolding HEX03 (PSI) demolding manually by peeling the flexible stamps.</p>	
<p>3.4</p>	<p>Replica</p>	<p>Repeat processes form 2.1 to 2.3 to get the second side patterned.</p>	<p><i>The process can be done in a single UV exposition using a stack composed by 2 flexible stamps.</i></p>

	End of Process 3		
4.0	Process 4: OLED fabrication		
4.1	Anode deposition 	DC/RF sputtering system Target: Indium-tine oxide 10-90 (Lesker) 2 inches Vacuum 5×10^{-3} mbarr Current 300 mA	<i>Rotating sample holder to increase homogeneity; Alternating on/off of plasma to avoid overheating of the polymer layer.</i>
4.1	Process control	Profilometer Thickness 250 nm UV/Vis spectra Transmittance 75% Multimeter Resistance 100 W/	
4.2	Active layers deposition 	Spin coating Karl Suss RC8 spin coater Double layer: PEDOT/PSS suspension (Bayer) no vacuum 2500 rpm 5000 rpm/s 20-40 nm PPVs (yellow/orange from Merck) no vacuum 2000-2500 rpm 5000 rpm/s 75-90 nm	
4.3	Cathode deposition 	Thermal vacuum evaporation AUTO306 coater Double layer: Ca Vacuum 9×10^{-6} mbarr 20-40 nm Al (capping layer) Vacuum 9×10^{-6} mbarr 20-40 nm	
3.4	Packaging	Epoxy resin casting The liquid epoxy resin (UV or thermal) is placed directly onto the cathode and a thin glass (microscope glass) is used to close the device. The curing is made: Thermal Tamb	<i>The contact of the device with oxygen degrades the device quickly; the oxygen exposition time has to be reduced as much as possible. The ideal condition is to use a</i>

		<p>2 hours UV (spot light) : 60 mW/cm² 10 s</p>	<p><i>glove box.</i></p>
<p>4.5</p>	<p>Measurement</p>  	<p>Electro-optical analysis I/V curves Efficiency curves (Lm/W) Software CLEM (CRF): power supply HP3432A multimeter HP34401 photodiode/integrated sphere IL1700</p> <p>Characterization devices: four square shapes with different area (4, 16, 36,100 mm²)</p>	
	<p>End of Process 4</p>		
	<p>End of Total Process</p>		

General remarks:

The architectures of devices with double side nanoimprinted glass substrates showed an increasing of external efficiency in OLED technology is in the range of 65-70%.

3.6 High Resolution Linear Encoder

Fabrication of a high resolution linear encoder

Process: Nanoimprint Lithography

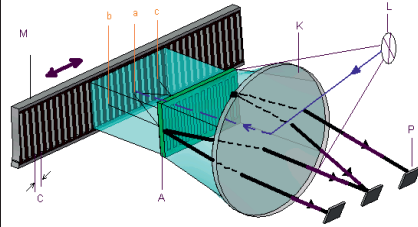


Figure:

Principle of an optical decoder

Process:

Pattern transfer on glass (read head) by lift-off with a double layer NIL process. Pattern transfer on silicon.

Application:

High resolution optical encoders fabricated by a process compatible with a high throughput.

Keywords: thermal nanoimprint, metrology, optical encoders

Project leader: FUNDACIÓN TEKNIKER

Address: Avda. Otaola, 20. 20600 Eibar. Spain

Web-Address: www.tekniker.es

Process: Double layer NIL

Responsible: Santos Merino

E-mail: smerino@tekniker.es

Process description: NIL on large areas (20x20 mm) patterned with gratings of 500 nm periods (300 nm lines and 200 nm spaces). Silicon and glass wafers used. Residual layer etching and lift-off with chromium on glass and pattern transfer on silicon. A bilayer NIL was used for successful lift-off.

Purpose: To manufacture linear encoders with a pitch below 500 nm. A phase scale and a read head were fabricated by pattern transfer on silicon and glass, respectively. The process developed points out that this technology may be suitable for mass produced encoders with a very high resolution and/or accuracy in the nanoscale range.

Major challenges: Fabrication by double layer NIL of a large grating (20 mm of length) on glass getting a successful lift-off on the whole of the area.

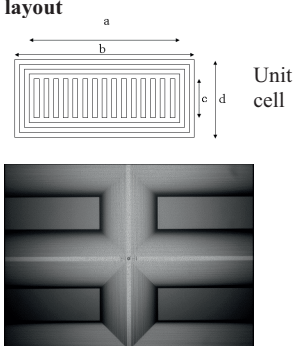
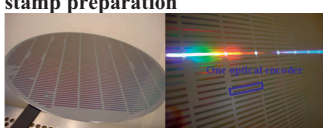
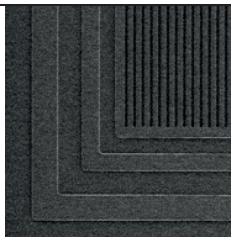
Application and state-of-the-art: All modern high-precision tools that require ultimate accuracy over distances larger than a fraction of a millimeter. The main drawback of encoders today is that commercially available encoder plates are limited in accuracy to worse than 100 nm. The work developed and shown here, is focused on the manufacturing of a linear optical encoder by NIL [2] -scale and read head- on the nanoscale range.

References:

- [1] F.C. Demarest, Meas. Sci. Technol. **9** (1998) 1024.
- [2] S. Merino, A. Retolaza, I. Lizuain. Microelec. Engineering **83** (2006) 897

High Resolution Linear Encoder

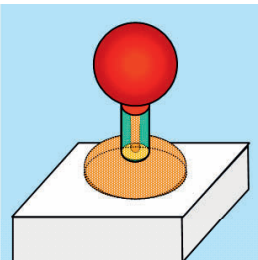
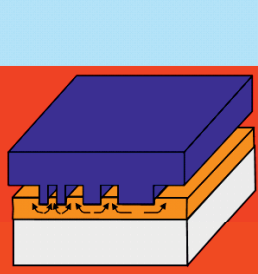
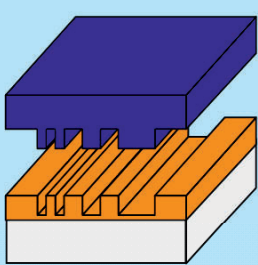
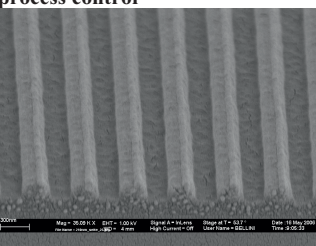
Process: nanoimprint lithography

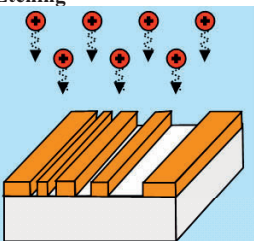
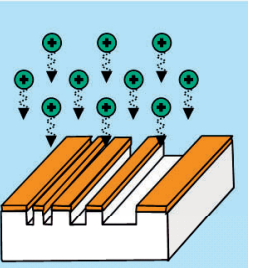
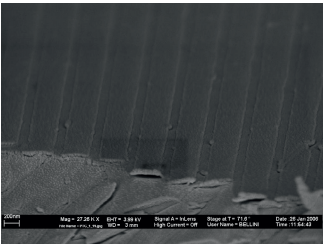

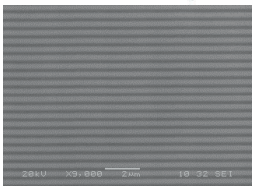
	Process	Technical Parameters	Remarks
	What	how it should work	critical issues
1.0	Process 1: Wafer preparation		
1.1	wafer selection and preparation Silicon	standard Si substrate Si substrate, 4", <100>, d=500 μm one side polished	
1.2	Wafer selection and preparation. Glass	Pyrex™, 4" substrate D=500 μm . $R_a \sim 1 \text{ nm}$	
1.3	substrate preparation	oxidation RCA clean. Two steps: NH_4OH , H_2O_2 , H_2O HCl , H_2O_2 , H_2O	
	End of Process 1		
2.0	Process 2: Stamp preparation		
2.1	layout  Unit cell repeated through the stamp)	Functional structures the stamp consist of unit cells repeated many times through the total surface. Unit cell: linear optical encoder, $a=20\text{mm}$, $b=21.7 \text{ mm}$, $c=1 \text{ mm}$, $d=3.5 \text{ mm}$. Pitch=500 nm (300 nm lines and 200 nm spaces). Rectangles were chosen to surround the lines and protect them from large residual layer variations.	
2.2	stamp preparation 	wafer selection The design was drawn on a 7" mask size and the patterns were transferred on 8" silicon wafers with DUV optical lithography ($\lambda=248 \text{ nm}$). Resist: UV5 positive resist from Rohm and Haas Company. Stamp depth=200 nm (Cl_2 , HBr/O_2) *Stamps were cut into 21x20 mm pieces.	 *15 μm top view SEM picture at the encoder corner stamp *The ratio (duty) between silicon surfaces and trenches is estimated to be around 320-180 nm

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LoP2007_NIL006_optical encoder. PDF

<p>3.1</p>	<p>coating of layer 1 (sacrificial layer)</p> 	<p>Spin-coating of mr-I7030 no priming 210 nm coated at 5500 rpm. Bake: 3 min at 140°C *Substrates were coated into 25x25 mm pieces.</p>	<p>This resist was used for glass and silicon wafers.</p>
<p>3.2</p>	<p>coating of layer 2 (NIL layer)</p>	<p>Spin-coating of LOL1000 from Shipley. Thickness: 60 nm coated at 5500 rpm.</p>	<p>This double layer was used only on glass and this resist was coated before coating the substrate with mr-I7030 resist.</p>
<p>3.3</p>	<p>Nanoimprint Lithography</p> 	<p>HEX03 (PSI) no vacuum stack preassembled before heating and pressing (order from top to bottom): PDMS (standard) 1mm Stamp (no clamped) substrate with resist, PDMS (standard) 1 mm temperature.(imprinting):140°C pressure.....(70 bar) temperature.(demold):50°C residual polymer thickness in grooves: 130 nm of mr-I7030 on silicon and glass and 60 nm more of LOL resist on glass.</p>	
<p>3.4</p>		<p>demolding Manual demolding.</p>	
<p>3.5</p>	<p>process control</p>  <p>Sample after imprinting on silicon</p>	<p>SEM</p>	<p>Residual layer around 130 nm measured.</p>
<p>End of Process 3</p>			
<p>4.0 Process 4: Pattern Transfer</p>			

<p>4.1</p>	<p>Residual Layer (Breakthrough) Etching</p> 	<p>O2 RIE: O₂:50 sccm gas pressure: 50 mtorr RF power: 50 W Etch rate ~ 2 nm/s</p>	<p>Identical process carried out on silicon and glass.</p>
<p>4.2</p>	<p>process control & substrate etching (Pattern transfer on silicon).</p> 	<p>SF₆/C₄F₈ silicon etching</p> <p>*Gases introduced at the same time by ICP-etching.</p> <p>RF power= 20W ICP power= 220W P=15 mtorr SF₆ flow=20 sccm C₄F₈ flow=30 sccm Depth etched=180 nm</p>	
<p>4.3</p>	<p>Lift-off on glass</p> 	<p>*After residual layer etching, the glass sample was dipped into a solution of developer MF319 from Shipley diluted 1:1 in de-ionised water for 30 seconds and rinsed plentiful water.</p> <p>*The sample was shortly treated with a low-temperature glow-discharge with oxygen before coating it.</p> <p>*50 nm of chromium coated on the substrate by sputtering.</p> <p>*Final lift-off by dipping the sample into an NMP ultrasonic bath at 50°C for 1 h.</p>	
<p>4.4</p>	<p>Process control (SILICON)</p>	<p>SEM, AFM</p>   <p>AFM topography and SEM picture after silicon etching.</p>	
<p>4.5</p>	<p>process control (GLASS)</p>	<p>SEM, AFM</p>	

		<p>AFM topography and SEM picture after lift-off with chromium.</p>	
<p>4.6</p>	<p>Measurement on silicon</p>	<p>AFM *The mean R_a values of 4.2 nm were obtained from over 50 measurements taken on different points of the encoder length. *Using these parameters and measurements, the loss of CD was reduced up to a duty of 350 to 150 nm (320 to 180 nm on silicon stamp).</p>	<p>The same measurements on the stamps gave mean R_a values of 2.2 nm.</p>
<p>4.7</p>	<p>Measurement on glass</p>	<p>AFM *Using these parameters and measurements, the loss of CD was reduced up to a duty of 340 to 160 nm (320 to 180 nm on silicon stamp).</p>	
<p>End of Process 4</p>			
	<p>Substrates of 25x25 mm with seven encoders each one on glass and silicon.</p>	<p>Glass scale was tested successfully by scratch tape tests to check the adherence of chromium on glass.</p>	
<p>End of Total Process</p>			

General remarks:

*The developing of LOL resist is critical and with a great dependence of temperature. The soft-bake temperature and bake-time of LOL lead to a high variation in the dissolution rate and, therefore, the soft-bake conditions should be strongly controlled to ensure a repetitive process. This is key parameter to ensure a right lift-off process.

*A sample cleaning in vacuum before metal deposition is critical to ensure a good adhesion of metal. In this case, it is even more relevant due to the tight conditions of developing with MF319 previously carried out, which can lead to keep resist debris on the glass surface.

Application and state-of-the-art: All modern high-precision tools that require ultimate accuracy over distances larger than a fraction of a millimetre, such as chip lithography and metrology equipment, coordinate measuring machines or diamond turning machines, depend on a displacement measuring interferometer for measuring motion of the stage that supports the sample or work piece. Commercial interferometers typically have sub-nm resolution [1] but the practical precision and accuracy that can be achieved are usually far worse. The primary errors plaguing interferometers include environmental disturbances such as temperature, pressure and humidity fluctuations, atmospheric turbulence, position-dependent geometric errors and several optical and electronic non-linearities [2], errors that are difficult to eliminate due to the nature of interferometers. Optical encoders have been used for decades as displacement measuring devices. Optical encoder scales are rigidly attached to a metrology frame and consist of grating or grid plates, and a read head, with the same period, which senses displacement relative to the grating scale (figure 1). Highest resolution, as a small fraction of the grating period, is achieved with a variety of diffraction based schemes [3, 4]. The main advantages of optical encoders are the short and constant beam path lengths between gratings and sensors, reducing the effects of the atmosphere by orders of magnitude compared to laser interferometers. However, the main drawback of encoders today is that commercially available encoder plates are limited in accuracy to worse than 100 nm. Since the encoder can only be as accurate as the grating scale, advance in this area crucially depends on the availability of encoder plates with sub-nanometer accuracy over macroscopic distances.

Diverse techniques have been used to manufacture high accuracy optical encoders. Logically, the suitability of each technique is defined by the grating pitch. Thus, for pitches above 2 μm , UV-Lithography represents a reliable and high throughput manufacturing process and has been jointly used with physical vapour deposition technology to manufacture amplitude and phase scales for decades. However, when pitches below 1 μm are needed, the manufacturing process is not as clearly defined and very different techniques have been used. They can be mechanically ruled with a diamond tip, which is a very slow, expensive, and difficult to control process, especially for large gratings with fine periods, or the grating pattern can be defined lithographically, typically by interference lithography or electron beam lithography. Interference lithography is fast, but prone to hyperbolic distortions when expanded spherical beams are used [5], while electron beam lithography patterns suffer from stitching errors and take considerable time to write. The latest approach to define pattern gratings uses a patterning method [6] called scanning beam interference lithography (SBIL), which combines the capabilities of laser interferometry with narrow, collimated beams, resulting in a low distortion image grating. However, sophisticated environmental controls to mitigate the effects of disturbances such as acoustics, vibration, air turbulence and variations of temperature, pressure and humidity must be strictly controlled.

The work developed and shown here, is focused on the manufacturing of a linear optical encoder by NIL [7] - scale and read head- on the nanoscale range. A read head and a phase scale are fabricated on glass and silicon respectively. The first one is supposed to work in a transmission mode while the phase scale works by reflection. If the process is tightly controlled, it constitutes an alternative manufacturing process, compatible with high-throughput and with less constraints than the processes based on conventional lithography.

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- [1] FC. Demarest, *Meas. Sci. Technol.* **9** (1998) 1024.
- [2] N. Bobrof, *Meas. Sci. Technol.* **4** (1993) 907
- [3] Y. Jourlin, Y. Jay, O. Perriaux. *Prec. Eng.* **26** (2002) 1
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- [5] J. Ferrera, M.L. Schattenburg, H. Smith. *J. Vac. Sci. Technol. B.* **14**, (1996) 4009.
- [6] R.K. Heilmann, C.G. Chen, P.T. Konkola, M.L. Schattenburg. *Nanotechnology* **15** (2004) S504.
- [7] S. Merino, A. Retolaza, I. Lizuain. *Microelec. Engineering* **83** (2006) 897

3.7 Optical Grating by Step&Stamp NIL

Fabrication of periodical optical structures by Step&Stamp NIL

Process: Nanoimprint lithography

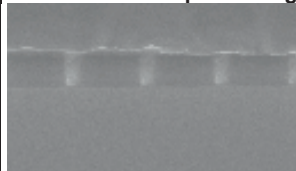


Figure:

Imprinted 180nm grating in 300 nm thick mr-I 7030 resist.

Process: Thermal SSIL to pattern thermoplastic polymer using Nano imprinting Stepper.

Application:

Optical grating

Keywords: thermal nanoimprint, Step&Stamp, SSIL

Project leader: VTT Technical Research Centre of Finland

Address: FI-02044 VTT, Finland

Web-Address: <http://www.vtt.fi>

Process: Step&stamp NIL

Responsible: Tomi Haatainen

E-mail:

Partner: S.E.T. SAS (Smart Equipment Technology)

Address: 74490 Saint Jeoire, France

Web-Address: <http://www.set-sas.fr>

Process: NPS300 Step&stamp Tool

Responsible: Gilbert Lecarpentier

E-mail: glecarpentier@set-sas.fr

Process description: This document contains a description of a general thermal imprint process for fabrication of periodical structures using sequential imprinting to pattern large areas. the parameters are valid for small stamps ($< 5 \times 5 \text{ mm}^2$) and submicron scale features.

Purpose: The aim of this process is transfer periodical structures of stamp into thermoplastic polymer which can be used as an etch mask, lift-off or a mold for fabrication of metal templates by electroplating.

Major challenges: Uniformity of residual layer on the large substrates due to waviness and wedging of the stamp in the single imprints.

Application and state-of-the-art: Anti-reflection gratings etc.

References:

- [1] T. Haatainen, J. Ahopelto, G. Grueztner, M. Fink, K. Pfeiffer, Step & stamp imprint lithography using a commercial flip chip bonder, Emerging Lithographic Technologies IV, Proceedings of SPIE, Vol. 3997. SPIE-The International Society for Optical Engineering (2000), 874 – 880.
- [2] T. Haatainen; J. Ahopelto, Pattern Transfer using Step&Stamp Imprint Lithography, Physica Scripta. Vol. 67 (2003) No: 4, 357 – 360.

Contact information:

VTT Technical Research Centre of Finland

Tietotie 3

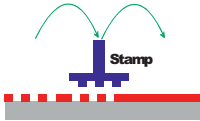
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FI-02044 VTT, Finland

LoP2007_NIL007_Step and Stamp NIL for optical gratings. PDF

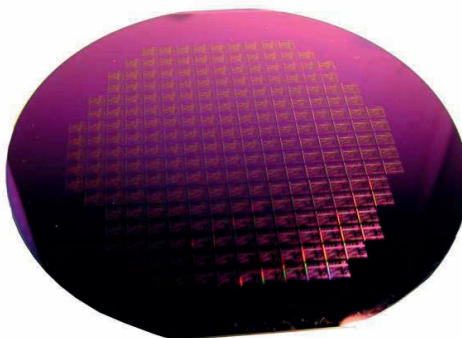
Optical Grating by Step&Stamp NIL

Process: nanoimprint lithography

	Process	Technical Parameters	Remarks
	What	how it should work	critical issues
1.0	Process 1: Wafer preparation		
1.1	wafer selection and preparation	standard Si substrate Si substrate, 4", <100>, d=525 μm one side polished	<i>Substrates up to 200 mm can be patterned by SSIL using NPS300</i>
1.2	substrate preparation	oxidation RCA clean (Caros Acid)	
	End of Process 1		
2.0	Process 1: Stamp preparation		
2.1	layout	Functional structures the stamp consist of grating structure (linewidth <1μm)	
2.2	stamp preparation	Stamp attachment Stamp is glued to SiC-plate with silicone adhesive	<i>Thermally conductive adhesive must be used to ensure the stamp heating</i>
2.3	antiadhesive coating	silane CVD evaporation clean or silane vapour	<i>CVD evaporation preferred if available</i>
	End of Process 2		
3.0	Process 3: Lithography		
3.1	coating of layer 1 (NIL layer)	spincoating no priming mr-I 7000 (microresist) mr-I 7010 (100nm) mr-I 7030 (300nm) @3000 rpm bake 3 min at 140 °C (hotplate)	
3.3	Nanoimprint Lithography 	SET NPS300 temperature.(stamp).....140°C temperature (chuck).....70°C pressure.....(>10MPa) heating time (60-140°C)..10s cooling time (140-60°C)..60s hold time (140°C).....2min overall time.....20 min temperature.(demold)....60-65°C residual polymer thickness in grooves 10-20 nm	<i>SET is a former branch of the SÜSS company in Annecy, France</i>
3.4	process control	AFM, SEM	<i>Imprint depth measured by AFM</i>
	End of Process 3		
3.0	Process 3: Pattern Transfer		
3.1	Residual Layer (Breakthrough) Etching	O2 RIE: O ₂40 sccm gas pressure 125 mtorr power 150 W time 5 sec	<i>Plasmalab 80Plus RIE</i>

		temperature 300 K	
3.2	process control	AFM	<i>Before substrate etching residual removal confirmed by AFM</i>
3.3	substrate etching 	CF4+Ar RIE CF4.....20 sccm Ar.....5 sccm gas pressure.....20 mTorr power.....100 W time..... temperature.....300K	<i>Plasmalab 80Plus RIE Selectivity Si:Resist(1:1.6) Etch rate (Si)=40 nm/min</i>
3.4	process control	optical microscope 100 x	
3.5	process control	Ellipsometer	<i>Resist thickness check</i>
3.6	measurement	AFM,SEM	
3.6	measurement	SEM LION video prints No.	
	End of Process 3		
	End of Total Process		

General remarks:



Figures: NPS Step and Stamp machine for thermal and UV NIL used for these experiments (until 2007 SET was part of SÜSS Microtec), installed at VTT (left side), and example (right side) of a 237 consecutive thermal imprints into a 300 nm thick mr-1 7030 film on a 100mm Silicon wafer. Stamp size 4x4mm², micrometer features with sizes of down to 2 μm and height of ~ 200nm. Stamp Temperature:140 °C, substrate temperature 70 °C, cycle time ~ 3 minutes (without collimation and arm movements).

3.8 Photonic Crystals for Enhanced Light Extraction

Fabrication of nanoimprinted photonic crystals for light extraction enhancement via surface plasmons

Process: nanoimprint lithography

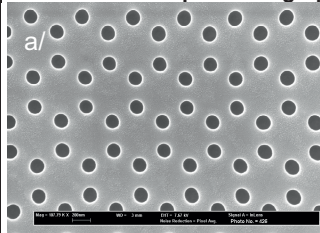


Figure: a/ Scanning electron micrograph of a nanoimprinted two-dimensional PhC with a 380 nm lattice constant honeycomb array of holes (holes depth 350 nm), b/ cross-section schematic of the studied system.

Process: A thermal NIL process is used to replicate the 2D periodic Si stamp in a dye-doped polymer. The dye-doped polymer is composed of rhodamine 6G directly dissolved in a printable polymer. The metallic substrates used have 50 nm thick layers of gold, aluminium and silver deposited by thermal evaporation on quartz substrates.

Application:

Light extraction applications (LEDs, OLEDs)

Keywords: thermal nanoimprint, photonic crystal, surface plasmon, light extraction

Project leader: Tyndall National Institute
Address: Lee Maltings, Prospect Row, Cork, Ireland
Web-Address: <http://www.tyndall.ie>

Process: Thermal nanoimprint
Responsible: C.M. Sotomayor Torres
E-mail: clivia.sotomayor@tyndall.ie

Process description: A process is described for two-dimensional nanoimprinted polymer photonic crystal coupled to surface plasmons. A stamp with different lattice constant PhCs was fabricated in a silicon wafer by using electron-beam lithography and dry etching. A thermal NIL process is used to replicate these 2D periodic patterns in a dye-doped polymer.

Purpose: The aim of this process is to provide a method to enhance the photoluminescence of dye chromophores-loaded by coupling the emission to surface plasmons in nanoimprinted photonic crystals.

Major challenges: The major challenge in this process is to control clusters formation on the metallic film to allow the matching of the surface plasmon resonance wavelength with the emission wavelength of the dyes

Application and state-of-the-art: The combination of surface plasmons and nanoimprinted structures in an active layer can lead to a new class of cost effective and high efficiency OLEDs. Furthermore, the metallic surface could be used as an electrical contact.

References:

- [1] V. Reboud, N. Kehagias, M. Zelsmann, M. Fink, F. Reuther, G. Gruetzner and C. M. Sotomayor Torres, *Photoluminescence enhancement in nanoimprinted photonic crystals and coupled surface plasmons*, Optics Express, 15, 12, 7190, 2007.

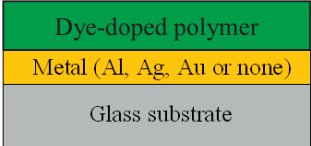
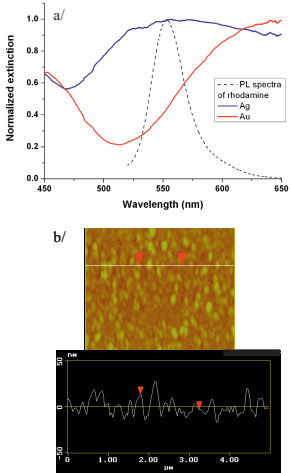
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LoP2007_NIL008_photonic crystals. PDF

Photonic Crystals for Enhanced Light Extraction

Process: nanoimprint lithography

	Process	Technical Parameters	Remarks
	What	how it should work	critical issues
1.0	Process 1: Wafer preparation		
1.1	wafer selection and preparation	Standard glass or Pyrex substrate	
1.2	substrate preparation 	no pre-treatment of the substrate Evaporation of metal films deposited using NFC 2000 Temescal 6 kW electron beam guns with a deposition rate of 10 Angstroms per second. A 400 nm thick layer of this modified polymer is spun on substrates.	
1.3	Process control 	Figure: a/ Normalized extinction spectra of the different used substrates, presenting the surface plasmon wavelength tunability. b/ right upper image: AFM images ($5 \times 5 \mu\text{m}^2$) of a 50 nm thick Ag evaporated on quartz substrate, (black inset: the depth profile along the white line). To determine the plasmon resonance frequencies of the different substrates, normalized extinction spectra were measured.	The second advantage in using silver islands films apart from the tunability of the SP resonance wavelength is that the non-negligible surface roughness scatters the SP modes to radiated light.
	End of Process 1		
2.0	Process 1: Stamp preparation		
2.1	layout	Functional structures The stamp consists of 10 arrays of pillars (350 nm height) on an area of $100 \times 100 \text{ mm}^2$ with a 100 mm pitch between arrays. The size of the Si is $2 \times 2 \text{ cm}^2$.	
2.2	stamp preparation	wafer selection The stamp was fabricated in a silicon wafer by using electron-beam lithography and dry etching (for details, see introduction of this process).	

2.3	<p>Anti-adhesive coating</p>	<p>The silicon stamp is treated with a self-assembled anti-adhesive monolayer (tridecafluoro-1, 1, 2, 2-tetrahydrooctyl trichlorosilane deposited in vapour phase).</p>	
<p>End of Process 2</p>			
3.0	<p>Process 3: Nanoimprint Lithography</p>		
3.1	<p>Process control : SEM top-view of the nanoimprinted photonic crystals</p>	<p>The stamp and the coated substrates are pressed together in a 2.5 inch <i>Obducat</i> nanoimprinter at 60 bar for 5 min at 90 °C. The pressure is sustained during the cooling phase until the temperature fell below 35 °C.</p>	
2.2	<p>Measurement: Optical characterization</p>	<p>Figure: a/ Photoluminescence spectra of a nanoimprinted unpatterned dyed-polymer film on a quartz substrate (black line), of a 2D photonic crystal with a 380 nm lattice constant (blue line), with a 500 nm lattice (green line) and with a 700 nm lattice (red line), b/ photoluminescence spectra of a flat surface imprinted on a quartz substrate (black line), of a 2D photonic crystal with a 700 nm lattice constant imprinted on a 50 nm Ag quartz substrate (blue line), of a 2D photonic crystal with a 700 nm lattice constant imprinted on a quartz substrate (red line), of a</p>	

		nanoimprinted unpatterned dye-doped polymer film on a 50 nm Ag quartz substrate (green line).	
	End of Process 3		
	End of Total Process		

General remarks:

Process description: A process is described for two-dimensional nanoimprinted polymer photonic crystal coupled to surface plasmons. A stamp with different lattice constant PhCs was fabricated in a silicon wafer by using electron-beam lithography and dry etching. The electron-beam exposure was carried out on a Jeol 6000 equipment with a dose of $130 \mu\text{C}/\text{cm}^2$ under a beam current of 100 pA on single layer of a ZEP 520 resist (positive tone resist from Zeon Corporation). Development is carried out during 30 sec in a solution of ZED N50 (Zeon Corporation). The silicon stamp is then etched to a depth of 350 nm by inductively coupled plasma etching and treated with a self-assembled anti-adhesive monolayer (tridecafluoro-1, 1, 2, 2-tetrahydrooctyl trichlorosilane deposited in vapour phase). A thermal NIL process is used to replicate these 2D periodic patterns in a dye-doped polymer. The dye-doped polymer is composed of rhodamine 6G (from Sigma Aldrich) directly dissolved with a concentration of $5 \times 10^{-4} \text{ mol/L}$ in a printable polymer (mr-NIL 6000 from micro resist technology), which is optically transparent in the visible range. A 400 nm thick layer of this modified polymer is spun on a quartz wafer and on metal-coated quartz wafers and baked at 60°C for 10 min before the NIL process. The stamp and the coated substrates are pressed together in a 2.5 inch *Obducat* nanoimprinter at 60 bar for 5 min at 90°C . The pressure is sustained during the cooling phase until the temperature fell below 35°C . The metal films were deposited using NFC 2000 Temescal 6 kW electron beam guns with a deposition rate of 10 Angstroms per second. The control of the deposition rate allows the tuning of the surface plasmon frequency of the film throughout the visible.

Purpose: The aim of this process is to provide a method to enhance the photoluminescence of dye chromophores-loaded by coupling the emission to surface plasmons in nanoimprinted photonic crystals. Two critical research issues in organic optoelectronics are to reduce the cost of organic LEDs and to improve their external efficiency. One approach to improve the extraction efficiency is to use two-dimensional (2D) photonic crystals (PhCs). A PhC structure enhances the light emitted from the active layer by slowing the propagation speed of the photons, thus increasing the coupling to the out-of-plane radiative modes. Another approach is to increase the spontaneous recombination rate of the emitters. This can be based on the energy transfer between light emitters and surface plasmons (SPs).

Major challenges: The major challenge in this process is to control clusters formation on the metallic film to allow the matching of the surface plasmon resonance wavelength with the emission wavelength of the dyes

Application and state-of-the-art: The two approaches mentioned above have been combined to enhance the light-emission efficiency of organic thin films. An active polymer film deposited on a metal surface is patterned by NIL and the SP energy is matched to that of the emitter in the PhC, reaching up to a x 27 enhancement. Our results indicate that nanoimprint lithography is a well suited process to fabricate these challenging photonic structures and that the combination of surface plasmons and nanoimprinted structures in an active layer can lead to a new class of cost effective and high efficiency OLEDs. Furthermore, the metallic surface could be used as an electrical contact.

3.9 Refractive Microlenses

Fabrication of microlenses and complex refractive surfaces

Process: nanoimprint lithography

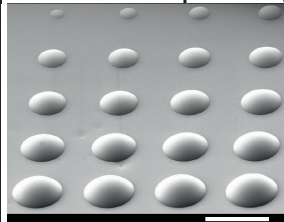


Figure:

Arrays of microlenses with two different radii of curvature hot embossed in PMMA (above) and arrays of microlenses with different apertures (same radii of curvature) by polymer casting and UV exposure of SU8 resist. The unit bars correspond to 10 μm .

Process:

Isotropic wet etching of glass with patterned chromium mask. Hot embossing or polymer casting.

Application:

Spherical or cylindrical microlens arrays with full control on radii of curvature and diameter

Keywords: Isotropic wet etching, glass template, hot embossing, polymer casting

Project leader: TASC Laboratory

Address: S.S.14km 163,5; 34012 Basovizza (Trieste, Italy)

Web-Address: www.tasc-infm.it

Process: Isotropic wet etching/ NIL

Responsible: Massimo Tormen

E-mail: tormen@tasc.infm.it

Process description: A process is described for the fabrication of polymeric arrays of microlenses or more complex systems of lenses (lenses on curved surfaces, arrays of lenses with multiple radii of curvature) by means of a process of wet etching of glass and hot embossing or polymer casting.

Purpose: The aim of this process is to produce large arrays of microlenses with a high control of geometrical parameters of the elements.

Major challenges: Accurate pattern definition in a chromium layer on glass with high etching resistance to concentrated hydrofluoric acid.

Application and state-of-the-art: Research process, light concentrators for CCD's elements or photovoltaic cells,

References:

- [1] Massimo Tormen, Alessandro Carpentiero, Enrico Ferrari, Dan Cojoc and Enzo Di Fabrizio, *Novel fabrication method for three-dimensional nanostructuring: an application to micro-optics*, Nanotechnology 18, 385301 (2007).
- [2] Massimo Tormen, Alessandro Carpentiero, Lisa Vaccari, Matteo Altissimo, Enrico Ferrari, Dan Cojoc, Enzo Di Fabrizio, *Fabrication of three-dimensional stamps for embossing techniques by lithographically controlled isotropic wet etching*, Journal of Vacuum Science and Technology B 23, 2920 (2005).



Contact information:

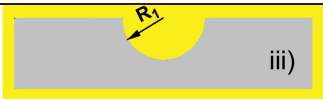
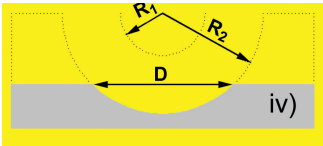
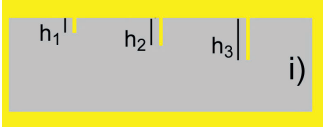

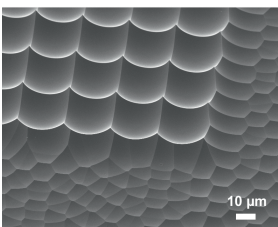
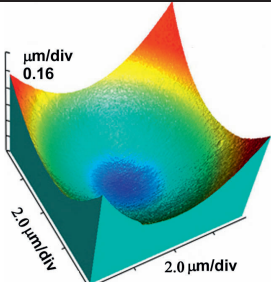
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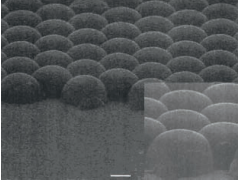
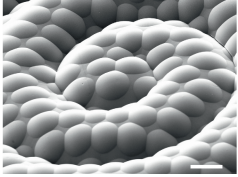
LoP2007_NIL009_Microlenses with spherical molds. PDF

Refractive Microlenses

Process: nanoimprint lithography

	Process	Technical Parameters	Remarks
	What	how it should work	critical issues
1.0a	Process 1: Stamp preparation First option (a)		
1.1a	Stamp substrate preparation	Sputter coating soda-lime glass with 100 nm chromium film.	Quality of the deposited chromium film, that should not have pin-holes
1.2a	Layout	Functional structures the pattern to be defined consists of dots or lines, corresponding to the centers of curvature of the spherical or cylindrical lenses in the plane of the glass surface.	
1.3a	Pattern definition by lithography	Standard electron beam or UV lithography can be used to define the pattern in a positive tone resist. For instance: Spin-coating 200 nm PMMA, expose exposed to a 30 kV electron beam 200 $\mu\text{C}/\text{cm}^2$ dose and develop developed in MIBK:IPA(1:3). Alternatively, UV lithography can be used for defining the center of curvature of microlenses larger than 5-10 μm	
1.4a	Chromium etching 	Open holes or trenches in the chromium layer by etching in aqueous solution of ammonium cerium (IV) nitrate (0.6 M) and acetic acid (1 M) for 1 min. The resist is stripped in solvents (e.g. acetone)	Loss of resolution due to wet etching of Chromium. The alternative is to use dry etching techniques
1.5a	Wet etching of glass 	Isotropic etching of quartz is performed in aqueous HF (48 wt.%) at room temperature, with an etching rate of $\sim 1\mu\text{m}/\text{min}$. The etching time is adjusted at each etching step in order to produce the required etching depth (=radius of curvature) in the glass substrate. For the etching of structures with fine details, more diluted HF solution (15 wt.%) is used to lower the etching rate to tens of nm/min.	Etching of holes through pin-holes in chromium lead to undesired spherical cavities .
1.6a	Chromium stripping	Stripping the chromium film by etching in aqueous solution of ammonium cerium (IV)	

		nitrate (0.6 M) and acetic acid (1 M) for 1 min.	
1.7a	Second step of wet etching of glass 	Simple geometrical constructions show that for an etching time t_2 after the stripping of the mask, the surface results in a spherical cap with a diameter $D = 2v\sqrt{t_1^2 + 2t_1t_2}$ and radius of curvature $R = v(t_1 + t_2)$, where v is the etching rate.	
1.0b	Process 1: Stamp preparation Second option (b)		
1.1b	Process 1: Stamp substrate preparation	Clean soda-lime glass surface is required as initial substrate.	
1.2b	Focused ion beam 	Hholes are milled at different depths in a quartz substrate by focused ion (Ga+) beam at 30 KeV. Centers of curvature can be located at different coordinates (x,y,z), below the glass surface.	
1.3b	Wet etching of glass 	Different diameter (same radius of curvature) are obtained as a function of the height of the milled holes.	
1.8a and 1.4b	Process control: SEM, AFM 		
2.0	Process 2: Coating for antiadhesion		
2.1	Coating with a hydrophobic monolayer of dodecyltrichlorosilane	The glass stamp is immersed for 10min in freshly prepared solution of $H_2O_2:H_2SO_4$ (1:4). Dodecyltrichlorosilane 1-5 mM in toluene is prepared in glovebox under nitrogen atmosphere. The stamp is dip for 1-2 hours in the solution. Rinse in toluene before taking into air atmosphere	Safety precaution: pour H_2SO_4 into a beaker with H_2O_2 , not vice-versa.
3.0	Process 3: Embossing or polymer casting		

<p>3.1</p>	<p>Different option for producing plastic microlenses.</p> <p>nanoimprinting hot embossing polymer casting</p>  <p>Nanoimprinting in PMMA</p>  <p>Hot embossing into Zeonex (see reference [1] and [2] for more details).</p>	<p>Glass templates fabricated according to the processes outlined above can be used to microstructure a large selection of materials with various processes such as nanoimprint, hot embossing or casting processes with different polymers.</p> <p>Nanoimprinting of relatively thick (>5 μm) polymethylmetacrylate (PMMA) films on silicon can be carried out at 210 °C at a pressure of 5 MPa.</p> <p>Hot embossing of pellets of the polyolefin ZEONEX (Zeon Chemicals) can done at 160-190 °C at a pressure of 2-10 MPa, to produce 50-100 μm thick polymer sheets with one or both patterned surfaces.</p> <p>PDMS precursor can be cast on the template and baked can</p> <p>Examples of optics produced with these methods are shown in figure on the left.</p>	<p>Possible trapping of air in the cavities, leading to defects in hot embossed microlenses.</p> <p>Vacuum is helpful in removing defects created by air inclusion.</p>
	<p>End of Process 3</p>		
	<p>End of Total Process</p>		

General remarks:

3.10 Fast Isothermal Imprint

Fast isothermal imprint for full wafers

Process: nanoimprint lithography

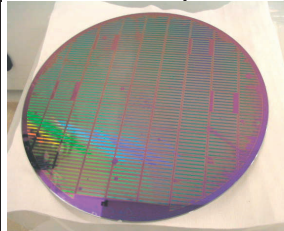


Figure:

Photograph of a 200 mm wafer imprinted using a 2 min process

Process:

A 200 mm wafer is imprinted uniformly in a 2 minutes process with features sizes down to 250 nm or 50 nm.

Application:

Large scale imprint applications

Keywords: thermal nanoimprint, throughput

Project leader: LTM

Address: 17 R. Martyrs, 38 054 Grenoble, France

Web-Address: <http://www.ltm-cnrs.fr/>

Process: Fast isothermal imprint

Responsible: Cécile Gourgon

E-mail: cecile.gourgon@cea.fr

Partner: CEA-LETI

Address: 17 R. Martyrs, F- 38 054 Grenoble

Web-Address:

Process: Fast isothermal imprint

Responsible: Stefan Landis

E-mail: Stefan.landis@cea.fr

Process description: The fast imprint process is based on a constant temperature of the equipment. The spin-coated wafer is introduced directly on the heated chuck, and its temperature uniformity is obtained very fast thanks to the equipment design. The resist is fluid enough to induce a very fast imprint as soon as the pressure is applied on the mold, and the demolding is performed outside of the machine. The mold/wafer stack is removed from the heated chuck at high temperature. The adhesion forces between the mold and the imprinted patterns guarantee a stability of the features when the pressure is stopped, until the external cooling. The demonstration is made in this library with 250 nm dense lines. It has also been proved that the same result can be obtained with 50 nm features, but the patterns are not covering the complete surface since a mold fully covered with such high resolution structures is still a challenge.

Purpose: The aim of this process is the increase of the NIL throughput on large surfaces. It was demonstrated that a process can be performed in 2 minutes. This value could be decreased by a up-grade of the equipment with a faster chamber pumping and a automatic loading.

Major challenges: The polymer film has to be heated as fast as possible with a good uniformity. This is a limitation for the fast imprint of very thick polymers. The mold cavities have to be filled very quickly and this is more difficult to achieve for very deep structures. But this fast process is really optimized for the production of nanostructures on large surfaces.

References:

- [1] C. Gourgon, N. Chaix, S. Landis, M. Zelsmann, J. Boussey, C. Perret, *The impact of the cycle time on the pattern filling and uniformity in thermal Nanoimprint lithography*, NanoImprint and Nanoprint Technology Conference, San Francisco, December 2006
- [2] C. Gourgon, N. Chaix, H. Schiff, M. Tormen, S. Landis, C.M. Sotomayor-Torres, A. Kristensen, R.H. Pedersen, M.B. Christiansen, I. Fernandez-Cuesta, D. Mendels, L. Montelius, T. Haatainen, *Benchmarking of 50 nm features in thermal Nanoimprint*, J. Vac. Sci. Technol. B 25(6)(2007) 2373-2378


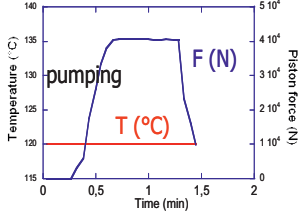
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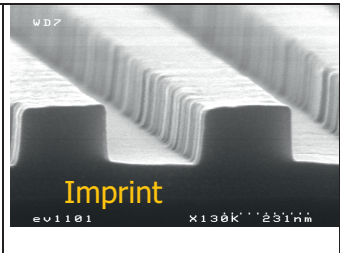
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LoP2007_NIL010_Fast isothermal imprint. PDF

Fast Isothermal Imprint

Process: nanoimprint lithography

	Process	Technical Parameters	Remarks
	What	how it should work	critical issues
1.0	Process 1: chamber and wafers preparation		
1.1	Pre-heating of the equipment	EVG®520HE Heating up to T_{imprint} 5 min waiting time to stabilize the temperature	
1.2	Mold/wafer assembly 	200 mm Si wafers Thin film of resist spin-coated on the Si substrate Mold coated with a standard anti-sticking layer Teflon sheet to improve the printing uniformity	<i>The resist thickness has to be in the range of few 10 nm to few 100 nm. A micrometer thick film could result in a limited temperature uniformity</i>
	End of Process 1		
2.0	Process 2: imprint process		
2.1	Pumping and temperature uniformization	Pressure down to 100 mbars in 30 seconds	<i>Limited by the pumping speed</i>
2.1	imprint 	Applied force: 40 kN During 1 minute In the case of NEB22 resist and mr-17000 polymers, the viscosity is low enough to induce to fast filling at a moderate temperature of 120°C	<i>The filling is uniform after less than 1 minute only if the mold depth is limited to ~200 nm and if the pattern size is in the few 100 nm range</i>
2.3	decrease of the force and chamber venting	T = T imprint	
	End of Process 2		
3.0	Process 3: demolding		
3.1	Unloading of the stack	The mold/wafer stack is put on a plate cold with water to fasten the cooling Waiting time: 2 minutes	
3.2	Demolding	Manual demolding with a razor blade	
3.3	process control	SEM 250 nm dense lines covering the 200 mm wafer	

			
	<p>End of Process 3</p>		
	<p>End of Total Process</p>		

General remarks:

3.11 Pattern Transfer Optimization

Pattern transfer optimization for full wafer NIL

Process: development of anisotropic transfer processes

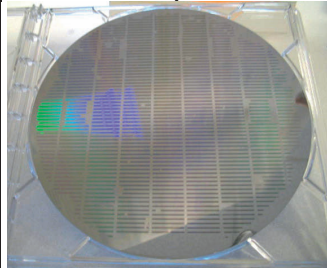


Figure:

Photograph of a 200 mm wafer imprinted and etched using an anisotropic process

Process:

Plasma etching processes are optimized to anisotropic pattern transfer, allowing the transfer of various densities of structures

Application:

Si devices with various patterns size and densities

Keywords: plasma etching, critical dimension, residual layer

Project leader: LTM

Address: 17 R. Martyrs, 38 054 Grenoble, France

Web-Address: <http://www.ltm-cnrs.fr/>

Process: anisotropic pattern transfer

Responsible: Cécile Gourgon

E-mail: cecile.gourgon@cea.fr

Process description: Large surfaces require a high imprint uniformity, which is easier to achieve with residual layers in the 50-100 nm range. A anisotropic plasma etching process is developed to remove this residual polymer film. The anisotropy allows a high quality transfer into patterns with various densities, with a good fidelity of the pattern size. This process uses a $O_2/Cl_2/Ar$ plasma chemistry in a ICP reactor.

Purpose: The aim of this process is the development of etching processes which allow a high quality transfer in patterns with different densities or sizes, and therefore with different residual layer thickness.

Major challenges: A challenge of this process is the reduction of the resist budget which limits the Si depth that can be achieved finally. Indeed a high difference of the residual thickness implies longer etching processes. The fidelity of all the patterns is guaranteed by the anisotropy, but the polymer is still vertically etched in the features whose residual layer is opened first. The resist mask for the following Si etching is therefore reduced.

References:

- [1] N. Chaix, C. Gourgon, C. Perret, S. Landis, T. Leveder, NIL processes on 200 mm Si wafer for optical applications : residual thickness etching anisotropy, J. Vac. Sci. Technol. B 25 (6) (2007) 2346-2351
- [2] N. Chaix, S. Landis, C. Gourgon, S. Merino, V.G. Lambertini, G. Durand, C. Perret, Nanoimprinting lithography on 200 mm wafers for optical applications, Microelectronic Engineering 84 (2007) 880-884


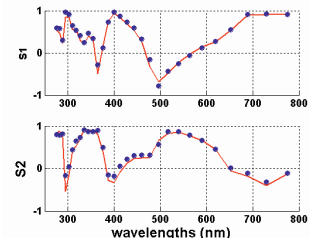
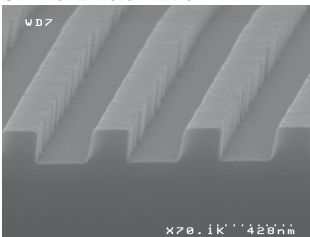
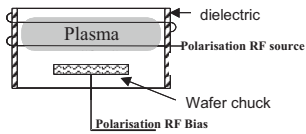
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LoP2007_NIL011_Pattern Transfer Optimization. PDF

Pattern Transfer Optimization

Process: nanoimprint lithography

	Process	Technical Parameters	Remarks
	What	how it should work	critical issues
1.0	Process 1: imprint		
1.1	Wafers preparation 	200 mm Si wafers Thin film of resist spin-coated on the Si substrate Mold coated with a standard anti-sticking layer Teflon sheet to improve the printing uniformity	
1.2	Imprint process	EVG® 520HE 40 kN, 120°C, 5 minutes	
	End of Process 1		
2.0	Process 2: residual thickness (hr) measurement		
2.1	Ellipsometry for scatterometry	Spectroscopic ellipsometer 300 – 800 nm Spot size 40 μm Mapping on the 8’’ surface	
2.2	Fit of the ellipsometry spectra 	Calculation time determined by the pattern geometries: few seconds for 200 nm dense lines, but few hours for 3D structures	<i>A high accuracy measurement of $n(\lambda)$ and $k(\lambda)$ has to be performed before.</i> <i>Limitation : homogeneous pattern gratings with standard geometries</i>
2.3	SEM characterization 	Top-down SEM for pattern quality and homogeneity control, or cross-section SEM Line width: 209 nm	<i>test wafer needed if cross-section measurement</i>
	End of Process 2		
3.0	Process 3: hr etching		
3.1	Loading of the imprinted wafer	Platform 5200 from applied Materials, DPS ICP reactor	
3.2	Etching process 	O₂/Cl₂/Ar plasma O ₂ : 30 sccm, Cl ₂ : 40sccm, Ar:30sccm Pressure 10 mTorr Source power: 500 W Bias power: 60 W for NEB22 resist	<i>The anisotropy is mostly dependent on the bias power. Some resists, which are less resistant, require lower bias, and this limits the anisotropy control.</i>
3.3	process control	SEM and scatterometry to measure the pattern size after	

	<p>CD after hr etching (nm)</p> <p>CD after imprint (nm)</p> <ul style="list-style-type: none"> 158 nm etching 109 nm etching 38 nm etching 	<p>the hr etching and compare it to the imprinted one</p> <p>Line width: 202 nm</p>	
<p>End of Process 3</p>			
<p>End of Total Process</p>			

General remarks:

3.12 Biodegradable Polymer Scaffold

Fabrication of a biodegradable micro- and nano-structured polymer scaffold for tissue engineering

Process: Nanoimprint, hot embossing



Figure:

Photograph of a 200 mm wafer imprinted and etched using an anisotropic process

Process:

Plasma etching processes are optimized to anisotropic pattern transfer, allowing the transfer of various densities of structures

Application:

Si devices with various patterns size and densities

Keywords: thermal nanoimprint, PDMS, rolling

Project leader: Glasgow University

Address: Glasgow University

Web-Address: www.gla.ac.uk/centres/cellengineering

Process: Nanoimprint Lithography

Responsible: M. Riehle

E-mail: m.riehle@bio.gla.ac.uk

Process description: Large surfaces require a high imprint uniformity, which is easier to achieve with residual layers in the 50-100 nm range. An anisotropic plasma etching process is developed to remove this residual polymer film. The anisotropy allows a high quality transfer into patterns with various densities, with a good fidelity of the pattern size. This process uses a $O_2/Cl_2/Ar$ plasma chemistry in a ICP reactor.

Purpose: The aim of this process is the development of etching processes which allow a high quality transfer in patterns with different densities or sizes, and therefore with different residual layer thickness.

Major challenges: A challenge of this process is the reduction of the resist budget which limits the Si depth that can be achieved finally. Indeed a high difference of the residual thickness implies longer etching processes. The fidelity of all the patterns is guaranteed by the anisotropy, but the polymer is still vertically etched in the features whose residual layer is opened first. The resist mask for the following Si etching is therefore reduced.

References:

- [1] N Gadegaard, S Thoms, D S Macintyre *et al.* *Microelectronic Engineering* 162 (2003) 67-68.
- [2] N. Gadegaard, E Martines, M.O.Riehle *et al.* *Microelectronic Engineering* 83 (2006) 1577-1581.
- [3] K. Seunarine, N. Gadegaard, M. Tormen *et al.* *Nanomed.* 1 (2006) 281-296.





Contact information:

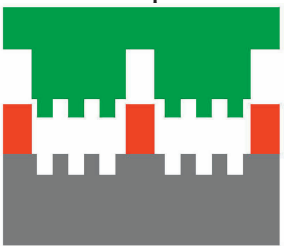


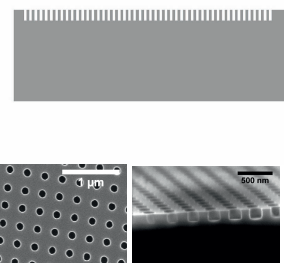
Dr. Mathis Riehle
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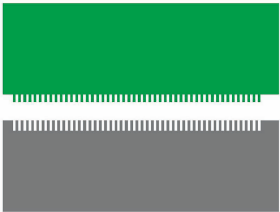

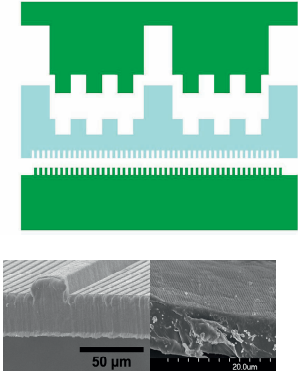
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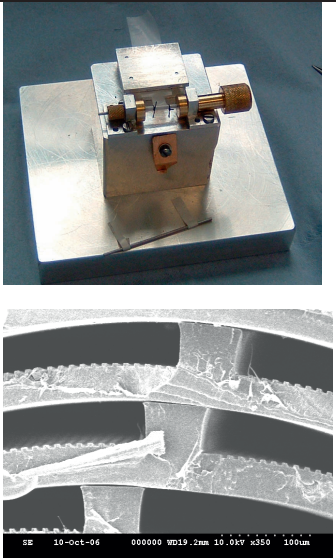
Biodegradable Polymer Scaffold

Process: nanoimprint lithography

	Process	Technical Parameters	Remarks										
	What	how it should work	critical issues										
1.0	Process 1: Micro master fabrication	Micrograting: 6 μm pitch, 6 μm deep											
1.1	Wafer selection	standard Si substrate Si substrate, 4", <100>, d=525 μm one side polished											
1.2	Resist coating 	spin coat resist Primer at 5 krpm for 5 s S1818 @ 4 krpm for 60 s Bake 10 minutes @ 90°C (hot plate)											
1.3	Photolithography 	Suss MA6 Expose (i-line) for 5 s Develop in 1:1 Microposit concentrate:RO water for 70 s Dry in N ₂ stream											
1.4	Dry etch - micro grooves 	<table border="1"> <tbody> <tr> <td>C₄F₈, SF₆</td> <td>50 sccm, 40 sccm</td> </tr> <tr> <td>Coil power</td> <td>600 W</td> </tr> <tr> <td>Platen power</td> <td>10 W</td> </tr> <tr> <td>Pressure</td> <td>10 mT</td> </tr> <tr> <td>Etch rate</td> <td>825 nm/min</td> </tr> </tbody> </table> <p>6 μm deep</p>	C₄F₈, SF₆	50 sccm, 40 sccm	Coil power	600 W	Platen power	10 W	Pressure	10 mT	Etch rate	825 nm/min	
C₄F₈, SF₆	50 sccm, 40 sccm												
Coil power	600 W												
Platen power	10 W												
Pressure	10 mT												
Etch rate	825 nm/min												
1.5	Spacers 	SU8 2050 @ 3 krpm (75 μm) 30 min at 95°C MA6, 20 seconds PEB 95°C for 7 minutes Develop in EC solvent for 7-10 minutes Rinse in IPA and dry in N ₂ stream	<i>Low thermal cycling to prevent SU-8 cracking</i>										
1.6	Anti-sticking layer	Ash in a O ₂ plasma (60W, 3 min) Immerse stamp in mixture of heptane with small drop of perfluoro silane (C ₈ H ₄ Cl ₃ F ₁₃ Si) from Gelest for 5-10 minutes.											

1.7	PDMS micro stamp 	Rinse in heptane and dry in N ₂ stream Cast 4:1 (pre-polymer:curing agent) Sylgard 184 to make inverse replica of stamp											
End of Process 1													
2.0 Process 2: Nano master fabrication													
2.1	Wafer selection	standard Si substrate Si substrate, 4", <100>, d=525 μm one side polished											
2.2	Resist coating 	spin coat resist 60% ZEP520A @ 4 krpm for 60 s Bake 60 minutes @ 180°C (oven)											
2.3	e-beam lithography 	50 kV accelerating voltage 80 nm beam spot size 300 nm beam step size 42 μC/cm ² exposure dose for an array of 10 ⁹ spots/cm ² Develop O-xylene 60 s Rinse in IPA and dry in N ₂ stream	<i>See[1]</i>										
2.4	Dry etch 	<table border="1" data-bbox="611 1183 862 1428"> <tr> <td>C₄F₈, SF₆</td> <td>120 sccm, 40 sccm</td> </tr> <tr> <td>Coil power</td> <td>18 W</td> </tr> <tr> <td>Platen power</td> <td>525 W</td> </tr> <tr> <td>Pressure</td> <td>10 mT</td> </tr> <tr> <td>Etch rate</td> <td>100 nm/minute</td> </tr> </table> 100 nm deep	C₄F₈, SF₆	120 sccm, 40 sccm	Coil power	18 W	Platen power	525 W	Pressure	10 mT	Etch rate	100 nm/minute	
C₄F₈, SF₆	120 sccm, 40 sccm												
Coil power	18 W												
Platen power	525 W												
Pressure	10 mT												
Etch rate	100 nm/minute												
2.5	Anti-sticking layer	Strip resist in Piranha etch (7:1) sulphuric acid:hydrogen peroxide Immerse stamp in mixture of heptane with small drop of perfluoro silane (C ₈ H ₄ Cl ₃ F ₁₃ Si) from Gelest for 5-10	<i>Piranha etch also oxidizes silicon prior to fluorination</i> <i>Warning – Piranha is a highly oxidizing</i>										

		minutes. Rinse in heptane and dry in N ₂ stream	<i>solution</i>
2.6	PDMS nano stamp 	Cast 4:1 (pre-polymer:curing agent) Sylgard 184 to make inverse replica of stamp	
End of Process 2			
3.0	Process 3: Polymer membrane fabrication and embossing		
3.1	Solvent casting 	Cast polymer mixture 1.25 g of PCL (Sigma, Poole, UK) dissolved completely in 25 ml of chloroform (Fisher scientific Inc., UK) left at room temperature for 2 hrs with frequent agitation 20 ml of PCL solution is deposited on a fluorinated 4" silicon wafer in a petridish. The solvent is evaporated overnight before the PCL film is demoulded. Average film thickness produced is between 60-80µm.	
3.2	Melt embossing 	PCL film cut, aligned and sandwiched between the PDMS micro and nano-stamps. Melt embossed (80°C) at a low pressure and allowed to cool.	
End of Process 3			
4.0	Process 4: Rolling		

<p>4.1</p>		<p>Custom built rolling jig Double side embossed film is trimmed into a manageable shape, the length of the film determines the subsequent number of layers that the scaffold will possess.</p> <p>The jig is a split pin configuration that clamps the edge of the film. The film is laid flat on a special 'runway' that is weighted by a special lid – this ensure that tension is exerted while the film is rolled providing a tight roll.</p> <p>The roll is secured either by surgical suture thread or by the use of a bio-compatible superglue, 2-Octyl Cyanoacrylate.</p> <p>After rolling and securing the pin clamps are loosened and removed.</p> <p>Excess film is trimmed and the scaffold is ready for use.</p>	
	<p>End of Process 4</p>		
	<p>End of Total Process</p>		

General remarks:

3.13 Fluidic Channels by Roll to Roll NIL

Fabrication for fluidics channels by using Roll to Roll NIL

Process: nanoimprint lithography, roll to roll printing, lithography

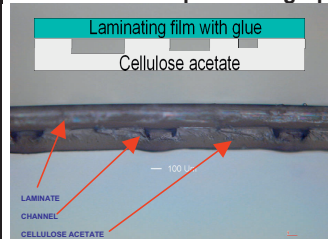


Figure:

Optical micrograph of a fluidics channels in 95 μm thick celluloseacetate sealed with ca. 90 μm thick laminate foil. Fluidisc channel is 50 μm high and 150 μm width.

Process:

Thermal roll to roll nanoimprint of a polymer film. Channels imprinted and sealed using custom made roll to roll device.

Application:

Microfluidic devices in high volume applications. Continuous processing.

Keywords: thermal nanoimprint, roll embossing, roll to roll NIL

Project leader: VTT Technical Research Centre of Finland

Address: FI-02044 VTT, Finland

Web-Address: <http://www.vtt.fi>

Process: Roll-to-roll NIL

Responsible: Tapio Mäkelä

E-mail: Tapio.Makela@vtt.fi

Process description: A process is based on continuous roll to roll manufacturing of fluidistic channels by using custom made manufacturing tool. Printing instrument consist two sequential units; thermal imprint and lamination. In continuous manufacturing process; fluidics channels were imprinted on cellulose acetate web and sealed with an laminate foil during the same printing cycle. In roll to roll NIL process a softening temperature of web is higher than in a laminate film.

Purpose: The aim of this process is to demonstrate a high volume continuous roll to roll nanoimprinting process. In this process we show possibility to manufacture fluidics channels with continuous process. A specific requirements of sequential process were shown.

Major challenges: In this novel process a many challenges can be listed: Manufacturing methods for imprint master (on a roll) and optimal parameters for pressure, temperature and time. Suitable plastic materials on web is needed, since in roll to roll manufacturing typical imprint time is 1 s or shorter. This process is developed by optimizing parameters suitable for cellulose acetate but PMMA, TOPAS, PS and other materials where softening or glass transition temperature are below 200 C are possible to use. Aspect ratio in roll to roll process can not exceed much above 1:1 in rectangular shapes.

Application and state-of-the-art: Research process

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- [1] T. Mäkelä, T. Haatainen, P. Majander and J. Ahopelto, MNE07 (2007).
- [2] T. Mäkelä, T. Haatainen, P. Majander and J. Ahopelto, Microelectr. Eng. 84 (2007) 877-879.
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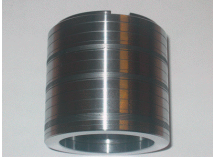
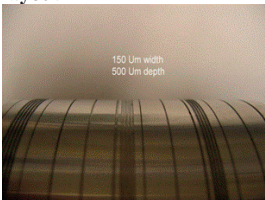

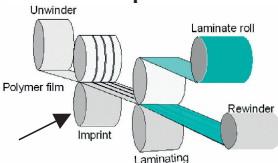
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LoP2007_NIL013_RtoR for fluidics channels. PDF

Fluidic Channels by Roll to Roll NIL

Process: nanoimprint lithography

	Process	Technical Parameters	Remarks
	What	how it should work	critical issues
1.0	Process 1: Master fabrication		
1.1	Metallic cylinder 	Metal roll and engraved channel structure on roll roll size 66 x 60 mm (diameter x width)	
1.2	Substrate preparation	Substrates <i>Plastic roll:</i> 50 mm width , 95 um cellulose acetate , no pre-treatment <i>Laminate roll:</i> 50 mm width , 90 um thick laminate with meltable glue	
	End of Process 1		
2.0	Process 2: Stamp preparation		
2.1	layout 	Functional structures Engraving of roll The stamp consist of 150 μm width and 500 μm depth grooves.	engraved grooves are relatively good but edges not clean
2.2	process control 	optical microscope 100 x	
	End of Process 2		
3.0	Process 2: Roll to roll nanom-printing		
3.1	Roll to roll imprint 	Thermal roll to roll imprint Pressure 8 MPa Temperature 105 C Speed 0.2 – 8 meter/minute 5 mm contact area between printing and backing rolls	Tg of cellulose acetate 120 C
3.2	Cooling/demolding	Cooling at room atmosphere (no blow) 30 cm distance between units	
3.3	process control	Optical microscope	

	End of Process 3		
4.0	Process 3: Cover		
4.1	<p>Laminated cover for fluidics</p>	<p>Thermal roll to roll laminating</p> <p>Pressure < 0.1 MPa Temperature 80 C Speed 0.2 – 8 meter/minute 1 mm contact area between printing and backing rolls</p>	
4.2	<p>process control</p>	<p>optical microscope cross section 100 x</p>	
4.3	<p>process control</p>	<p>Channel test tested with water (+ dye)</p>	
	End of Process 4		
	End of Total Process		

General remarks:

3.14 V-Grooves for Plasmon Confinement

Fabrication of V-groove waveguides for plasmon confinement by Nanoimprint Lithography

Process: nanoimprint lithography

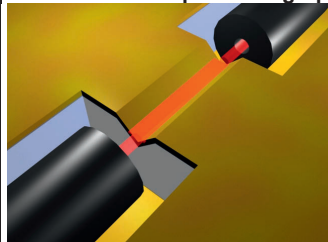


Figure:

Schematic illustration of the device: two deep channels (to place the optical fibers) are integrated with the v-groove (to confine the plasmon). The device is made in gold (200nm) onto a transparent and flexible substrate (Ormocomp®).

Process: The process is based on nanoimprint lithography, metallization, and casting of a UV curable hybrid polymer (Ormocomp), allowing to fabricate the same structures of the stamp in different materials.
Application: The v-grooves are used as subwavelength waveguides, where plasmons are confined and guided at the bottom. Further applications may be in the biosensing field.

Keywords: thermal nanoimprint, v-groove, plasmon confinement.

Project leader: MIC-DTU

Address: DTU building 345E, 2800 Lyngby, Denmark

Web-Address: www.mic.dtu.dk/ak

Process: Design and fabrication

Responsible: Anders Kristensen

E-mail: ak@mic.dtu.dk

Partner: CNM-Barcelona

Address: Campus de la UAB, 08193 Bellaterra, Spain

Web-Address: www.cnm.es

Process: Sample fabrication

Responsible: Irene Fernandez Cuesta

E-mail: irene.fernandez@cnm.es

Process description: A process is described for wafer scale fabrication of integrated devices, based on v-groove cavities for plasmon confinement. The process includes a double replication, thus, the final structures are equal to those fabricated in the initial stamp (silicon), but made in different materials. This goal is achieved by combining nanoimprint lithography, metallization and casting of a UV curable polymer onto the imprinted structures, and finally dissolving the imprinted polymer. The stamp is fabricated in two steps: photolithography and wet etching in KOH, and photolithography and Deep RIE.

Purpose: The aim of this process is to fabricate cavities with V shape and smooth sidewalls (in gold onto a transparent and flexible substrate), and simultaneously two deep channels, integrated with the groove, where optical fibers can fit, to facilitate light coupling in the groove and measure the output signal.

Major challenges: stamp fabrication: to achieve smooth and vertical sidewalls in the D-RIE step. Gold deposition is critical. Due to thermal expansion problems, the gold layer appears cracked sometimes.

Application and state-of-the-art: Research process, used for the fabrication of V-grooves, to study the confinement of plasmons in the bottom of the V-grooves.

References:

[1] S.I. Bozhevolnyi, et al. Nature, 2006. 440(7083): p. 508-511

[2] I.Fernandez-Cuesta, R. B. Nielsen, A. Boltasseva, et. Al., J. Vac. Sci. Technol. B 25(6), p. 2649 (2007).

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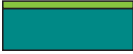








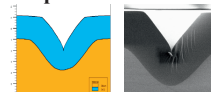
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

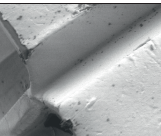
URL: www.mic.dtu.dk/ak

LoP2007_NIL014_V-Groove Waveguides. PDF

V-grooves for Plasmon Confinement

Process: nanoimprint lithography

	Process	Technical Parameters	Remarks
	What	how it should work	critical issues
1.0	Process 1: Stamp fabrication		
1.1	wafer selection	standard Si (100) substrate 4", d=500 μm double side polished	
1.2	substrate preparation 	Wet oxidation at 1100°C (oxide thickness ~200nm)	
1.3	Photolithography 1 	Spin coating of UV resist (1.5 μm of AZ5214B), UV exposure, and development.	
1.4	RIE 	RIE of 200 nm of SiO ₂ . Stripping of the photoresist (acetone)	
1.5	KOH to define de V 	Anisotropic wet etching in KOH (wt 30%), at 80°C, during 1h.	
1.6	Oxide removing 	HF 50%, 1 minute.	
1.7	Photolithography 2 	Spin coating of UV resist (1.5 μm of AZ5214B), UV exposure, and development.	
1.8	D-RIE to define the channels 	Deep RIE of silicon, to define the channels (300 μm deep).	<i>Vertical and smooth side-walls should be obtained, otherwise demolding would be difficult.</i>
1.9	Resist stripping 	Acetone and ultrasounds, to remove the resist.	
1.9 b	Process control 	SEM	
1.10	Optional: improvement of the sharpness of the V. 	Wet oxidation, 6h at 1150°C.	<i>For each size of the grooves, the oxidation time can be optimized (by simulations), to achieve the sharpest angle in the bottom.</i>

1.11	Optional: improvement of the thickness of the stamp	Anodic bonding of another silicon wafer to the bottom of the stamp.	<i>After etching 300um to create the deep channels, in a 500um thick wafer, it becomes very fragile.</i>
1.12	Antisticking coating	FDTS-layer (1H,1H,2H,2H-perfluorodecyltrichlorosilane) using a MVD system (Applied Microstructures Inc.)	
	End of Process 1		
2.0	Process 2: NIL		
2.1	Substrate preparation	PMMA sheet, 5mm thick. Dehydrated in an oven, at 90°C, 8hours.	
2.2	NIL 	Imprint with EVG: 180°C, 10min, at 20kN. Demolding at 80°C.	
3.0	Process 3: pattern replication inOrmocomp and gold		
3.1	Gold deposition 	Evaporation of 200 nm of gold onto the imprinted face of the PMMA.	<i>A silicon wafer has to be stuck to the backside of the PMMA sheet, to avoid thermal gradients and bubbles formation.</i>
3.2	Ormocomp deposition 	Casting of Ormocomp (r) onto the gold layer. The sample is left for 10min. UV curing: 4 cycles of 30seconds.	<i>The Ormocomp has to be cured in short cycles, otherwise, internal stress appears and bends the structures.</i>
3.3	Releasing of the structures 	The sample is rinsed in acetone some hours, and cleaned afterwards in an O2 plasma.	
3.3b	process control 	SEM 	
	End of Process 3		
	End of Total Process		

General remarks:

3.15 NEMS Device

UV nanoimprint lithography for making NEMS devices

Process: UV Nanoimprint lithography

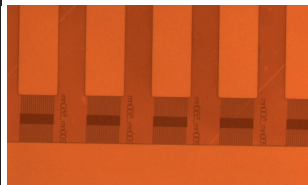


Figure:

Optical micrograph of UV nanoimprinted patterns on double layer resists with the features at both 200 nm and several millimeters.

Process:

UV nanoimprint of a UV cure resist on top of a soluble resist (LOR). Pattern transfer by using RIE and wet etching.

Application:

NEMS devices fabrication (alternative to any pattern transfer processes)

Keywords: UV nanoimprint

Project leader: Lund University

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Web-Address: www.nano.ftf.lth.se

Process: UV-NIL

Responsible: Ivan Maximov

E-mail: ivan.maximov@ftf.lth.se

Process description: A process is described for UV nanoimprint lithography. It is based on a double-layer resist system with a sacrificial layer (LOR) below a UV cured resist (UV-cur 06). Because the two polymer layers have different sensitivities to solvents, the LOR can be selectively dissolved through the UV cured resist.

Purpose: The aim of this process is not the fabrication of a specific device, but to demonstrate a processing method for pattern transfer, which is able to transfer the pattern with the features of both nanometers and millimeters on the whole wafer.

Major challenges: The UV nanoimprint lithography is making the monomers cross-linked, which can not be dissolved by the solvent. For pattern transfer, it will make it difficult for the lift-off process. Sacrificial layer (LOR) is used to solve this problem. The imprinted residue layer thickness of UV cured resist, the dry etching rate of UV cured resist and the wet etching rate of LOR are the crucial factors for this process.

Application and state-of-the-art: Research process for pattern transfer of the NEMS device fabrication, it could also be widely used for any pattern fabricating processes.

References:

- [1] Carlberg P, Graczyk M, Sarwe E L, Maximov I, Beck M and Montelius L, *Lift-off process for nanoimprint lithography* Microelectron. Eng. **67/68**, 203 (2003).
- [2] Luo G, Maximov I, Adolph D, Graczyk M, Carlberg P, Ghatnekar-Nilsson S, Hessman D, Zhu T, Liu Z.F., Xu H.Q and Montelius L, *Nanoimprint lithography for the fabrication of interdigitated cantilever arrays*, Nanotechnology, **17**, 1906–1910 (2006).

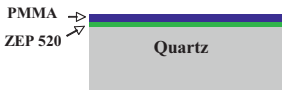
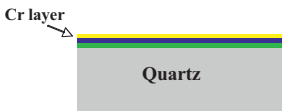
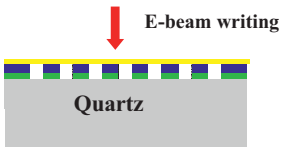
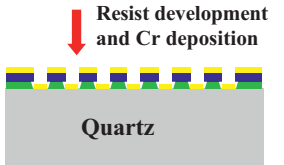
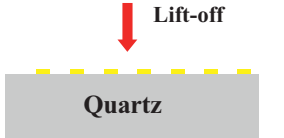
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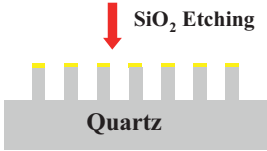
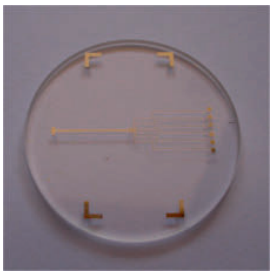

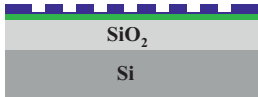
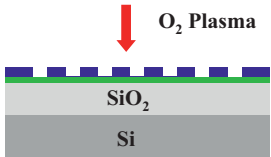
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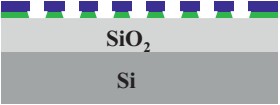
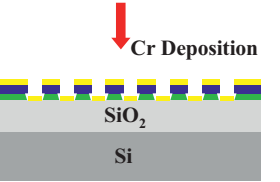
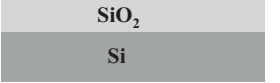
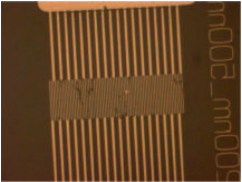
LoP2007_NIL015_NEMS Device. PDF

NEMS Device

Process: UV-nanoimprint lithography

	Process	Technical Parameters	Remarks
	What	How it should work	Critical issues
1.0a	Process 1: Wafer preparation		
1.1	Substrate preparation	Cleaning of quartz wafer prior to spin-coating of resist layers. Rinsing in acetone, IPA and water for 2 min with ultrasonic agitation. Nitrogen blow dry.	
	End of Process 1a		
1.0b	Process 1: Stamp preparation		
1.1	Spin-coating 	<ul style="list-style-type: none"> • Sping-coating of ZEP-520A7 resist at 9000 rpm for 60 s, baking at 160 °C at hot plate for 10 min. • Spin-coating of PMMA 950 K at 6000 rpm for 60 s, baking at 160 °C for 15 min. 	
1.2	Evaporation of Cr layer 	Evaporation of 10 nm thick Cr layer to dissipate charge in EBL exposure step.	
1.3	EBL exposure 	Exposure of the structure in EBL system (Raith 150) at 20 keV energy and exposure dose of 66 $\mu\text{C}/\text{cm}^2$.	
1.4	Development and Cr deposition 	<ul style="list-style-type: none"> • Removal of Cr layer in a Cr etching solution • Development of the PMMA layer in MIBK:IPA 1:3 solution for 60 s • Development of the ZEP 520A7 resist in o-xylene for 2 min • Evaporation of 30 nm Cr layer for lift-off 	
1.5	Lift-off process 	Lift-off process in Remover S-1165 at 80 °C for 10 min.	

<p>1.6</p>	<p>Reactive Ion Etching</p> 	<p>Reactive Ion Etching conditions:</p> <ol style="list-style-type: none"> 1. CHF₃ flow 65 sccm 2. P=35 mbar 3. RF-power is 75 W 4. Etching time 6 min 5. Etch rate 30-35 nm/min 	
<p>1.7</p>	<p>Stamp image (Cr is still present)</p> 	<ul style="list-style-type: none"> • Removal of Cr after RIE • Anti-sticking treatment using a vapor of CF₃(CF₂)₃(CH₂)₂SiCl₃ at 250 °C in N₂ glove box for 2 hours 	
<p>End of Process 1b</p>			
<p>2.0 Process 2: Lithography</p>			
<p>2.1</p>	<p>UV-Cur06 Spin-coating LOR</p> 	<ul style="list-style-type: none"> • Sping-coating of LOR 0.7A resist at 3000 rpm for 60 s, baking at 200 °C in oven for 30 min. • Spin-coating of UV-Cur06 resist (Micro Resist Technology GmbH) at 3000 rpm for 60 s, baking at 80 °C for 60 s at hot plate. 	<ul style="list-style-type: none"> • <i>Control of the resist thickness is important</i>
<p>2.2</p>	<p>UV-NIL</p> 	<p>UV-NIL process using Obducat 6" Nanoimprinter:</p> <ul style="list-style-type: none"> • Pressure 20 bar • Room temperature • Imprint time 3 min • Exposure time 10 s 	<ul style="list-style-type: none"> • <i>Cleanliness of the stamp and substrate is crucial</i>
<p>2.3</p>	<p>Oxygen plasma ashing</p> 	<ul style="list-style-type: none"> • Oxygen plasma ashing in PlasmaPreen system • P=5 mbar • Ashing time 20-30 s • Full power (600 W) 	<ul style="list-style-type: none"> • <i>Ashing time is important</i>

2.4	Wet etching 	<ul style="list-style-type: none"> Wet etching in MF319:H₂O (3:1) Etching time 3 min Rinsing in DI H₂O 	<ul style="list-style-type: none"> <i>Wet etching time is important to avoid too much underetching</i>
2.5		Deposition of 30 nm Cr by thermal evaporation	
2.6	Lift-off 	Lift-off process in Remover S-1165 at 80 °C for 10 min.	
2.7		Left: optical image of the NEMS pattern after UV-NIL and lift-off	
End of Process 2			
End of Total Process			

General remarks:

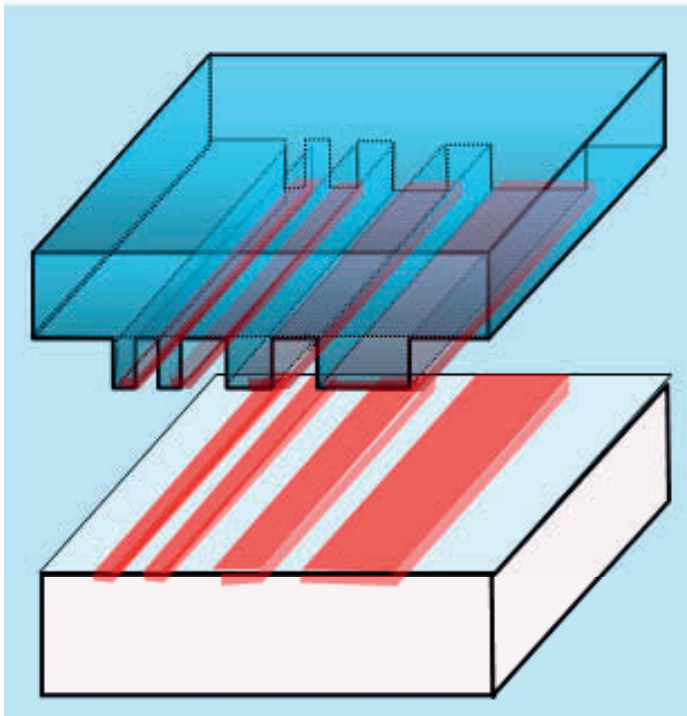
Subsequent transfer of the imprinted lift-off mask into the substrate can be performed using reactive ion etching.

4. Soft Lithography - Microcontact Lithography

Contributions to this section of the library are from

IBM ZRL - Zürich/Switzerland
Dr. Heiko Wolf

CNRS - LAAS, Toulouse, France
Prof. Dr. Christophe Vieu



4.1 Alkanthiol Printing

Microcontact Printing of Alkanethiols on Gold

Process: microcontact printing lithography



Figure:

Casting PDMS (silicone) precursor onto a structured template in a Petri dish.

Process:

Casting PDMS (silicone) precursor (elastomer base and curing agent) onto a structured template in a Petri dish. Curing (hardening) by heat (60°C, 12-24 h).

Application:

Microfluidic devices
Photonic crystals

Keywords: microcontact lithography, soft lithography, protein patterning, PDMS

Project leader: IBM Research Laboratory

Address: CH-8803 Rueschlikon / Switzerland

Web-Address: <http://www.zurich.ibm.com/>

Process: microcontact lithography

Responsible: Heiko Wolf

E-mail:

Process description: Microcontact printing (μ CP, mCP) of alkanethiols on gold

Purpose: A process is described for transferring a pattern from a silicon master via an elastomeric stamp onto a solid substrate.

Major advantages: In comparison to standard photolithography, microcontact printing is a low-cost, large-area, high-resolution patterning process.

References:

- [1] Libioulle, L.; Bietsch, A.; Schmid, H.; Michel, B.; Delamarche, E. *Langmuir* **1999**, *15*, 300-304.
- [2] Larsen, N. B.; Biebuyck, H.; Delamarche, E.; Michel, B. *Journal of the American Chemical Society* **1997**, *119*, 3017-3026.
- [3] Geissler, M.; Wolf, H.; Stutz, R.; Delamarche, E.; Grummt, U.-W.; Michel, B.; Bietsch, A. *Langmuir* **2003**, *19*, 6301-6311.





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LoP2007_mCP001_microcontact printing alkaethiols. PDF

Alkanethiol Printing

Process: microcontact printing lithography

	Process	Technical Parameters	Remarks
	What	how it should work	critical issues
1.	Stamp		
1.1	Master fabrication 	Fabricate patterned silicon master by photo- or E-beam lithography	<i>ideal with smooth bottom surfaces and smooth vertical sidewalls</i>
1.2	Master preparation	Coat master with fluorinated separation layer	hydro-phobic surface treatment to facilitate stamp separation
1.3	Mixing of PDMS	Mix precursor SYLGARD 184 elastomer base with curing agent 10:1	<i>good mixing required for catalytic reaction,</i>
1.4	Degasing	Degas mixture to avoid air bubbles in stamp	<i>premixed aliquots can be stored at -20 °C for 1-3 months</i>
1.5	Stamp curing 	Pour liquid prepolymer onto master inside of petri dish and cure at 60 °C for 12-24 hours.	
1.6	Stamp work-up	Cut and peel stamp off master. Rinse stamp three times with EtOH and dry under a flow of N ₂ for 30 s.	
2	Ink [1]		
2.1	Alkanethiols as ink	Chose an alkanethiol, e.g. dodecanethiol (DDT), hexadecanethiol (HDT) octadecanethiol (ODT) or eicosanethiol (ECT)	<i>higher molecular weight thiols decrease ink diffusion, but increase disorder of monolayer and tend to crystallize at the stamp surface</i>
2.2	Purification (optional)	Purify by chromatography using silica gel (20:1 hexane-ethyl acetate on Silica Gel 60, ~200 g per 0.5 mL of thiols), and degas by successive freeze-pump-thaw cycles at a pressure of <100 mTorr for 24 h.	<i>purification removes low-molecular-weight thiols</i>
2.3	Ink solution	Prepare diluted thiol solution in ethanol, e.g. 0.1 mM	<i>changing the concentration allows to control the amount of ink transferred to the stamp</i>
2.4	Storage	Store purified ink solution at 4 °C in the dark for up to one week.	
3	Substrate [1]		
3.1	Surface preparation	Evaporate ~1 nm Ti onto a Si/SiO ₂ wafer, e.g. with an e-beam evaporator at ~2x10 ⁻⁷ Torr and a rate of ~0.5 nm s ⁻¹ .	
3.2	Au deposition 	Immediately following, evaporate 15 nm gold (same evaporation parameters)	
4	Inking		
4a	Immersion inking [2] 	Inking by placing a drop of ink solution onto the stamp.	<i>only the average amount of ink transferred can be controlled.</i>
4a.1	Inking	Place two drops (~0.2 mL) of the freshly prepared (<1 h) ink solution on top of the stamp. After 30 s remove liquid quickly (<0.5 s) under a stream of N ₂ .	<i>make sure there's enough liquid to cover the surface.</i>

4a.2	Drying	Continue the flow of N ₂ for 30 s after evident disappearance of the bulk drop to evaporate residual EtOH, use within 15 s.	
4b	Contact inking [1] 	Inking with an ink pad selectively directs the ink where it is needed.	<i>quality of monolayer is less dependent on pattern geometry, diffusion is minimized.</i>
4b.1	Ink pad fabrication	Prepare small blocks (~2 cm ² and 4mm thick) of cured PDMS as ink pads.	
4b.2	Impregnation	Immerse the ink pad in the thiol-solution for at least 12 h.	
4b.3	Drying and storage	Withdraw from the solution, dry in a stream of N ₂ for 10 s and store in a small glass flask.	
4b.4	Inking	Place the patterned stamp on the ink pad without applying pressure for 40s.	<i>conformal contact allows transfer of thiols. Inking times control amount of thiols transferred.</i>
5	Printing		
5.1	Making Contact 	Place stamp onto gold substrate, monitor formation of conformal contact optically.	<i>conformal contact is made by the stamps own weight.</i>
5.2	Detaching	Remove the stamp after 10-20 s.	<i>the longer the printing time, the fewer the defects in the printed monolayer, but the higher the ink diffusion.</i>
6	Etching [3]		
6.1	Preparation of etch bath	Prepare a ferric nitrate etch bath (20 mM Fe(NO ₃) ₃ •9H ₂ O and 30 mM thiourea in DI water, adjusted to pH 2.0 using HCL)	<i>the concentration of the ferric and thiourea in solution determine the etch rate</i>
6.2	Etching 	The bath should be operated at 23-25 °C with moderate stirring and has an etch rate of ~ 10 nm min ⁻¹ .	<i>the granularity of the gold substrate limits the edge resolution to the size of the gold grains (15-30 nm).</i>

4.2 Protein Patterning

Fabrication of high resolution protein patterns

Process: microcontact printing lithography



Figure:

Casting PDMS (silicone) precursor onto a structured template in a Petri dish.

Process:

Casting PDMS (silicone) precursor (elastomer base and curing agent) onto a structured template in a Petri dish. Curing (hardening) by heat (60°C, 12-24 h).

Application:

Microfluidic devices
Photonic crystals

Keywords: microcontact lithography, soft lithography, protein patterning, PDMS

Project leader: IBM Research Laboratory

Address: CH-8803 Rueschlikon / Switzerland

Web-Address: <http://www.zurich.ibm.com/>

Process: microcontact lithography

Responsible: Heiko Wolf

E-mail:

Process description: Subtractive Printing of High Resolution Protein Nanopatterns

Purpose: The Ink-Subtract-Print strategy is described in which an inked elastomer is patterned by subtracting proteins from the surface using a nanotemplate followed by printing from the elastomer to a final substrate.

Major advantages: This technique is designed to produce high resolution patterns of single or multiple proteins with intrinsic alignment. Other advantages include: easy to use, high throughput pattern production, large area patterns, and no stamp collapse.

General:

References:

- [1] S. R. Coyer, A. J. García, E. Delamarche, *Angew. Chem. Int. Ed.* **2007**, *46*, 6837-6840 .
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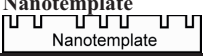
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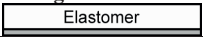
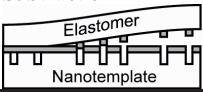
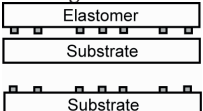
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LoP2007_mCP002_Protein Patterning. PDF

Protein Patterning

Process: microcontact printing lithography

	Process	Technical Parameters	Remarks
1.	 <p>Nanotemplate</p>		
1.1	Fabrication	Fabricate patterned silicon nanotemplate using a system capable of nanoscale features (E-beam lithography, nanoimprint, nanoparticle patterning)	<i>The nanotemplate material must be more hydrophilic than the elastomer material.</i>
2.	Elastomer		
2.1	Mixing of elastomer	Polydimethylsiloxane (PDMS) prepolymer prepared using SYLGARD® 184 (elastomer base to curing agent 10:1)	<i>Good mixing required for catalytic reaction. Premixed aliquots can be stored at -20 °C for 1-3 months</i>
2.2	Degasing	Degas mixture to remove air bubbles in stamp. This can be completed by leaving the poured dishes at room temperature for ~20 mins. or by placing the dishes in a vacuum.	
2.3	Elastomer curing	Pour liquid prepolymer onto flat polystyrene petri dish and cure at 60 °C for 24 hours	
2.4	Stamp work-up	Cut elastomer into desired stamp size. Mark the surface of the stamp that is not in contact with the petri dish. Peel stamp off petri dish. Ultrasound stamp in isopropanol/DI H ₂ O (20/80) solution for 5 mins. Rinse stamp in Millipore H ₂ O. Rinse stamp with EtOH. Dry under a flow of N ₂ for 30 s.	
3	Ink		
3.1	Protein as ink	Chose a protein, e.g. anti-IgG, streptavidin. Available protein labels include fluorophores and gold conjugates.	<i>Protein must meet the requirement of adsorbing to hydrophobic surfaces from solution.</i>
3.2	Ink solution	Prepare dilute protein solution in phosphate buffered saline (PBS). Desired concentration ranges from 0.05 to 0.5 mg/mL	<i>Concentration is an important factor for producing patterns with complete protein coverage and high edge definition. Optimal concentration varies depending on the protein.</i>
3.3	Storage	Use fresh protein solution when available. If necessary, store solution at 4 °C for up to one week.	
4	Substrate		
4.1	Substrate selection	For atomic force microscopy (AFM), silicon is used for its low surface roughness. For fluorescence, glass is used because it does not quench the fluorophore.	<i>The substrate must be more hydrophilic than the elastomer material.</i>
4.2	Cleaning	Place substrate in isopropanol/DI H ₂ O (20/80) solution. Ultrasound 5 mins. Rinse substrate in Millipore H ₂ O. Rinse stamp with EtOH. Dry under a flow of N ₂ for 30 s.	

4.3	Plasma treatment	Treat cleaned substrate with O ₂ plasma for 1 min.	<i>Plasma treatment increases the hydrophilicity of the surface.</i>
5	Inking 		
5.1	Immersion inking	Place ink solution on surface of stamp that was in contact with the petri dish. Coat the entire surface with a droplet of solution.	<i>For 5 × 5 mm² elastomer surface, use ~0.1 mL protein solution.</i>
5.2	Incubation	Incubate protein solution on stamp for 1 hour.	
6	Subtraction 		
6.1	Plasma treatment	Treat nanotemplate with O ₂ plasma for 1 min.	<i>Plasma treatment increases the hydrophilicity of the surface. Complete this step shortly before subtraction.</i>
6.2	Rinsing	Wash ink solution off of stamp using hand pipette. PBS 3 × 1mL. Millipore 1 × 1mL.	
6.3	Drying	Dry stamp in N ₂ flow for 15 s.	<i>Under or over drying the protein monolayer on the stamp will affect the printed pattern quality.</i>
6.4	Contact	Bring inked surface of stamp into contact with nanotemplate for 15 s.	<i>Light pressure can be applied to assure conformal contact between stamp and nanotemplate.</i>
6.5	Release	Release stamp from nanotemplate.	
7	Printing 		
7.1	Contact	Place stamp onto substrate for 30s.	<i>Light pressure can be applied to assure conformal contact between stamp and nanotemplate.</i>
7.2	Release	Release stamp from substrate.	
8	Repeat Ink-Subtract-Print		
8.1	Additional steps	Patterns of multiple proteins can be produced by repeating the ink-subtract-print steps. Also, the individual steps can be rearranged to produce a variety of protein patterns. The steps ink-subtract-ink-subtract-print using two different protein inks allows printing of multiple proteins at the same time with intrinsic alignment.	

General remarks:

4.3 Polar Ink Printing

Surface Modification of PDMS Stamps for Microcontact Printing of Polar Inks

Process: microcontact printing lithography

Figure:

Casting PDMS (silicone) precursor onto a structured template in a Petri dish.

Process:

Casting PDMS (silicone) precursor (elastomer base and curing agent) onto a structured template in a Petri dish. Curing (hardening) by heat (60°C, 12-24 h).

Application:

Microfluidic devices
Photonic crystals

Keywords: microcontact lithography, soft lithography, protein patterning, PDMS

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Process: microcontact lithography
Responsible: Jurriaan Husken
E-mail:

Process description: Plasma polymerization of allylamine; a process for surface modification.

Purpose: A process is described for surface modification of polydimethylsiloxane (PDMS) stamps and transferring a hydrophilic ink pattern from the modified stamp to various substrates with different chemistry of inks and substrates.

Major Advantages: In comparison to general oxygen plasma method to treat the stamp surface, plasma polymerization process is efficient, stable and substrate independent, high density of functional groups on the surface, versatile chemical structures, and suitable for further surface modification based on reactive amine groups.

References:

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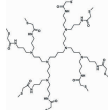
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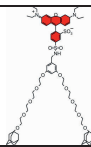

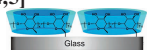



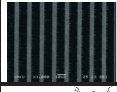
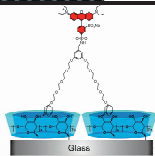
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LoP2007_mCP003_polar ink printing. PDF

Polar Ink Printing

Process: microcontact printing lithography

	Process	Technical Parameters	Remarks
	What	how it should work	critical issues
1.	Stamp		
1.1	Master fabrication 	Fabricate patterned silicon master by photo- or E-beam lithography.	<i>Ideal with smooth bottom surfaces and smooth vertical sidewalls.</i>
1.2	Master preparation	Coat master with fluorinated anti-sticking layer.	<i>Hydro-phobic surface treatment to facilitate stamp separation.</i>
1.3	Mixing of PDMS	Mix precursor SYLGARD 184 elastomer base with curing agent 10:1 by volume.	<i>Good mixing required for catalytic reaction.</i>
1.4	Degasing	Degas mixture to avoid air bubbles in stamp	<i>Premixed aliquots can be stored at -20 °C for 1-3 months.</i>
1.5	Stamp curing 	Pour liquid prepolymer onto master inside of petri dish and cure at 60 °C for 12-24 hours.	
1.6	Stamp work-up	Cut and peel off the stamp from master. Rinse stamp three times with EtOH and dry under a flow of N ₂ for 30 s.	
2.0	Plasma Deposition of Allylamine [1]		
2.1	Chamber cleaning	Plasma coating system (CCR, Rheinbreitbach, Germany). cleaning chamber with air plasma (30 min, 300 W). After plasma deposition chamber was brought to atmospheric pressure with argon.	<i>Cleaning removes all impurities in the chamber</i>
2.2	Plasma deposition	samples were positioned on the base plate at the same distance from the center of the reactor. Deposition of allylamine for 1 min at 300 W.	<i>Optimized conditions. No physical damage of the surface. Stable and high density of functional groups can be achieved.</i>
2.3	Stamps storage	Samples were transferred to storage container, sealed in an aluminum foil pouch under a nitrogen atmosphere at reduced (30 %) pressure and stored at -20 °C.	<i>This way modified surfaces are stable for longer periods (more than a year).</i>
3.0	Inks [1]		
3.1	G2-S Dendritic ink [2] 	A second generation of dendritic ink having 8 dialkyl sulfide end groups as positive ink on gold substrate yield positive gold patterns by positive microcontact printing (μCP).	<i>Low diffusion ink with polar end groups. This could be used to create positive patterns of Si master.</i>
3.2	Ink solution	Prepare diluted G2-S ethanol, e.g. $c = 2 \times 10^{-5}$ M.	<i>Optimized ink concentration.</i>
3.3	ODT ink [2]	Octadecanethiol ink in ethanol as backfilling ink for positive μCP. $c = 10^{-4}$ M	<i>Increasing the concentration causes to replace printed G2-S molecules and distorted patterns.</i>
3.4	Divalent Guest ink [3]	Divalent guest bearing two adamantyl units and labeled with lissamine rhodamine dye. Substrate: β-cyclodextrin terminated glass.	

			
3.5	Ink solution	Prepare diluted solution of divalent guest in water, e.g. 10 μM	<i>Low concentration is good enough to transfer monolayers from the stamp.</i>
4	Substrates [1]		
4.1	Gold substrates 	Evaporate ~ 2 nm Ti onto a Si/SiO ₂ wafer. Immediately following, evaporate 20 nm gold.	<i>Used gold substrates are commercially available by Ssens B.V., Hengelo, Netherlands.</i>
4.2	β-Cyclodextrin glass [4,5] 	β -cyclodextrin terminated glass substrates are fabricated in 3 steps starting from amine terminated glass.	<i>Please see ref. [4,5] for fabrication of β-cyclodextrin terminated substrates.</i>
5	Inking		
5.1	Immersion inking 	Inking by placing a drop of ink solution onto the stamp.	
5.2	Inking	Place two drops (~ 0.2 mL) of the freshly prepared (< 1 h) ink solution on top of the stamp. After 60 s remove liquid quickly (< 0.5 s) under a stream of N ₂ .	<i>Make sure there's enough liquid to cover the surface.</i>
5.3	Drying	Continue the flow of N ₂ for 30 s after evident disappearance of the bulk drop to evaporate residual EtOH or water, use within 15 s.	
6	Printing		
6.1	Making Contact 	Place stamp onto gold or glass substrate, monitor formation of conformal contact.	<i>Conformal contact is made by the stamps own weight. If needed apply slight pressure with tweezers.</i>
6.2	Detaching	Remove the stamp after 60 s.	<i>The longer the printing time, the fewer the defects in the printed monolayer.</i>
7	Case Studies^a		
7a	μCP of G2-S	G2-S dendrimer is printed on a gold surface with modified PDMS stamp. After printing, non-printed areas is backfilled with ODT for 10 s. Then the gold is etched away in etching bath.	<i>ODT backfilling time is optimized. If backfilling time is increased printed G2-S replaces by ODT.</i>
7a.1	Preparation of etch bath	Prepare an acidic solution of 10 mM Fe(NO ₃) ₃ , 15 mM thiourea and 1.2 % HCl. etch at 45 °C for 2.2 min.	<i>The concentration of the ferric and thiourea in solution determine the etch rate.</i>
7a.2	Etching & SEM image 	Use scanning electron microscopy (SEM) or optical microscopy to analyze gold patterns after gold etches.	 <i>Positive gold patterns are clearly visible in the SEM image.</i>
7b	μCP of Divalent Guest	Divalent guest labeled with lissamine rhodamine dye is printed on cyclodextrin terminated glass. Ink should bind on substrate via host-guest supramolecular interactions.	

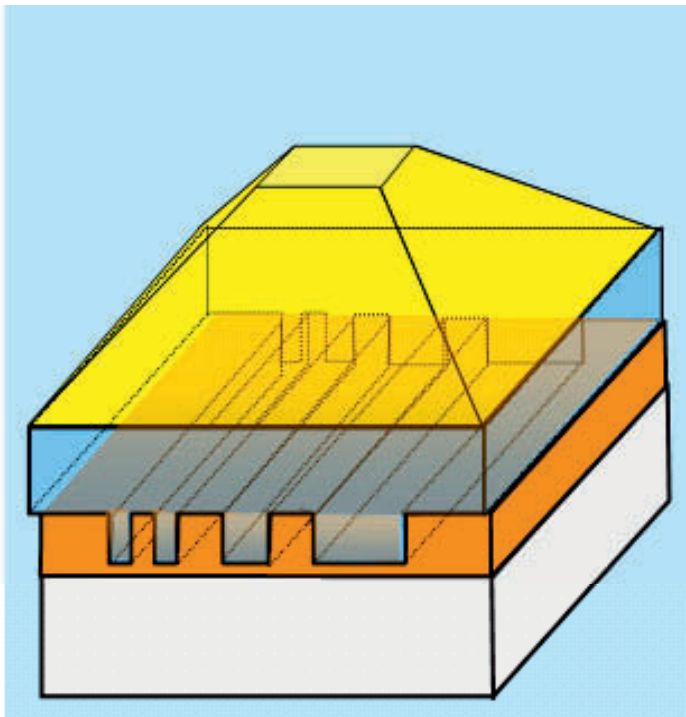
7b.1	Fluorescence Microscopy Analysis	Use fluorescence microscopy to analyze fluorescent patterns which obtains from binding guest molecules on glass via supramolecular interactions during printing.	<i>Fluorescent pattern clearly indicates supramolecular binding of ink.</i> 
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5. Soft Lithography – UV-Nanoimprint Lithography

Contributions to this section of the library are from

AMO GmbH, Aachen, Germany
Dr. Ulrich Plachetka

LPN-CNRS - Marcoussis /France
Prof. Dr. Yong Chen



5.1 Optical Resonators

Fabrication of Optical Resonators by Soft UV-NIL

Process: soft lithography

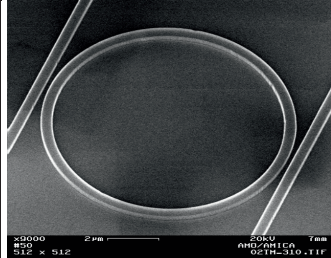


Figure:
SEM-image of an imprinted microring resonator.

Process: A polymeric imprint template is cast moulded from a master pattern and replicated by imprinting into a UV-curable resist. Afterwards the device is etched into the appropriate substrate.

Application:
Large scale patterning

Keywords: soft UV-NIL, PDMS stamps

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Process: Soft UV-NIL
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Process description: An imprint template is fabricated via cast moulding of from a pre-structured form and used during an imprint process. During the imprinting, first a thin layer of a low viscosity resist is spin coated onto the desired substrate followed by pressing the flexible imprint template into the liquid layer. Then the resist is polymerized by UV exposure, the template is removed and may be used for numerous other replications via Soft UV-NIL. Etching may be performed using standard RIE equipment

Purpose: This imprinting process can be used to pattern on large area scale with resolutions down to the 20nm regime. Due to the elastomeric properties of the imprint template patterning can also be performed on non-flat substrates, with very low imprint pressures and at room temperature. The major purpose for the development of this process is cost reduction.

Major challenges: The major challenge when using soft template materials is the adaptation of the young's modulus.

Application and state-of-the-art: Products and prototypes that rely on large area nano-patterning at high resolutions at cheap costs. In this library it is used to fabricate photonic structures in silicon waveguide technology.

References:

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[2] M. Bender, A. Fuchs, U. Plachetka and H. Kurz; *Status and Prospects of UV-Nanoimprint Technology*, *Microelectronic Engineering* 83 (2006) 827-830

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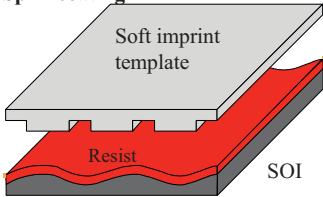
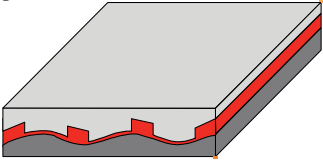
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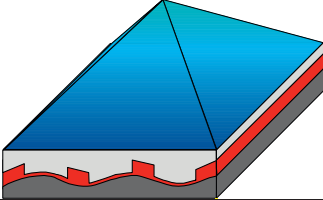
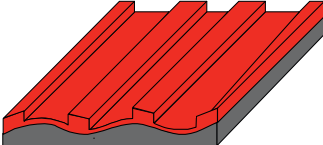
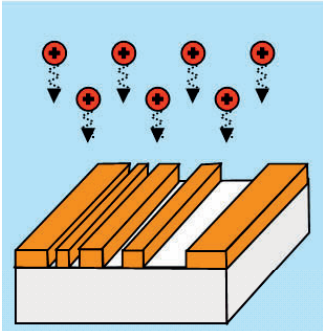
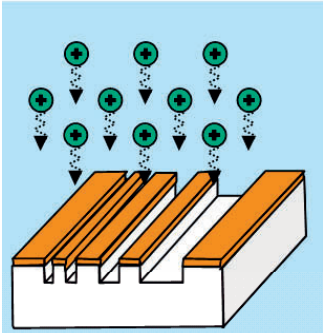
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LoP2007_SoftNIL001_Resonators by SoftNIL. PDF

Optical Resonators

Process: soft lithography

	Process	Technical Parameters	Remarks
	What	how it should work	critical issues
1.0a	Process 1: Master preparation		
1.1	Master fabrication:	Si substrate, 6", <100>, one side polished, standard ebeam, followed by RIE (other substrates may also be used, i.e. metals, resist, etc.)	
1.2	Deposition of anti-adhesion layer:	Whatever the chosen master material is, an antiadhesion layer needs to be deposited onto its surface by plasma deposition (i.e. in an etching chamber); CxFx-plasmas works (standard passivation settings for your tool)	
	End of Process 1		
1.0b	Process 2: Stamp preparation		
1.1	Elastomeric template material:	A 10:1 (base:curing agent) mixture of Sylgard 184 (Dow Corning) is prepared and degassed in a vacuum	
1.1	Cast moulding of imprint template:	The mixture is poured onto the master, degassed in a vacuum and afterwards cured on a hotplate (110°C@30min)	
1.2	Detachment	The template is then cut and detached from the silicon master.	
2.0	Process 3: Lithography		
2.1	Spin -coating 	spincoating of UV-curable resist onto an SOI-substrate (depending on the application other substrates may be used freely) imprint resist: AMONIL MMS4 (3000rpm@30sec)	
2.2	Soft imprinting with flexible template 	The flexible imprint template is pressed into the liquid resist at an imprint pressure of 50mbar; the template adjusts to the non-flat parts of a substrate The used tool may be a EV620 custom modified mask aligner	
2.3	UV-exposure	The AMONIL resist is cured directly through the flexible	

		<p>imprint template by UV-exposure in the EV620 imprint tool</p>	
<p>2.4</p>	<p>Detachment of template</p> 	<p>After completely curing the resist the imprint template is removed from the polymerized imprint resist; the moulded flexible imprint template can be used for other imprints</p>	
	<p>End of Process 2</p>		
<p>3.0</p>	<p>Process 3: Pattern Transfer</p>		
<p>3.1</p>	<p>Residual Layer (Breakthrough) Etching</p> 	<p>BCl₃ -RIE (The plasma is used to open the SOI substrate)</p>	
<p>3.2</p>	<p>Substrate Etching</p> 	<p>HBr-RIE (This plasma will stop perfectly on the BOX of an SOI-wafer)</p>	

General remarks:

5.2 Mix- and Match of Soft-NIL and OL

Soft UV nanoimprint and optical lithography based mix-and-match technique

Process: soft lithography, optical lithography

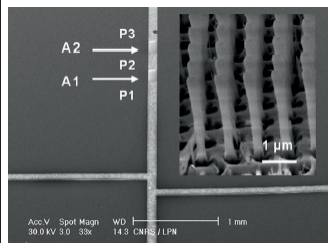


Figure:

Cross microfluidic channels with two integrated nanopillar arrays (A1 and A2) obtained using a mix-and-match approach based on i) soft UV nanoimprint lithography, ii) standard photolithography and iii) reactive ion etch techniques

Process:

Soft UV nanoimprint lithography

Application:

The mix and match approach can be applied for any type of micro and nanostructures patterning as well as their device integration. In the case of microfluidics, the nanopillar are used as sieving gels for DNA molecule separation

Keywords: soft UV nanoimprint lithography

Project leader: LPN

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Process: soft UV nanoimprint

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E-mail: yong.chen@lpn.cnrs.fr

Partner: ENS

Address: Ecole Normale Supérieure, F-75231 Paris

Web-Address: www.ens.fr

Process: soft UV nanoimprint

Responsible: Yong Chen

E-mail: yong.chen@ens.fr

Process description: Soft UV NIL is used to pattern only high density nanostructures. Then, after lift-off, the mould pattern is defined on the substrate with alignment markers. A standard photolithography is applied to define patterns with large size features, followed by the second lift-off. Afterwards, both micro and nanoscale features are etched into the substrate by reactive ion etch. Finally, the pattern structures are covered by a PDMS layer, forming a microfluidic device with integrated high density nanopillars arrays. Such a mix-and-match process is highly parallel which can be used for large scale manufacturing of many other types of nano-devices.

Purpose: To integrate high density nanostructures into micro-devices. A particular example is given for the fabrication of microfluidic chips for large size DNA molecule separation but other types of micro-devices can also be obtained in a similar way.

Major challenges: Integration of high density nanostructures into functioning microfluidic devices with parallel process

Application and state-of-the-art: The proposed process has been validated by demonstration of microfluidic device with integrated high density nano-pillars arrays for large size DNA molecule separation. The same device has already been fabricated by electron beam lithography based techniques but this is the first demonstration of highly parallel process for such microfluidic devices.

References:

- [1] J. Shi, A. P. Fang, L. Malaquin, A. Pépin, and D. Decanini, J. L. Viovy and Y. Chen, *Highly parallel mix-and-match fabrication of nanopillar arrays integrated in microfluidic channels for long DNA molecule separation*, Appl. Phys. Lett. **91**, 153114 (2007)



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LoP2007_SoftNIL002_NIL Mix&Match. PDF

Mix- and Match of Soft NIL and OL

Process: soft lithography

	Process	Technical Parameters	Remarks
1.0	Process 1: Master fabrication		
1.1	Pattern definition of by electron beam lithography	Standard EBL Silicon substrate PMMA resist	<i>Including only nanostructures and alignment markers</i>
1.2	Pattern transfer	40nm Nickel evaporation Lift off Reactive ion etch with SF ₆ gas	
1.3	Surface treatment	Evaporation of anti-sticking reagent In TMCS vapour during 1 min	
	End of Process 1		
2.0	Process 2: Soft stamp preparation		
2.1	Thin layer PDMS deposition	Spin coating Approximately 10µm thickness	
2.2	Soft PDMS layer deposition	Casting and curing 5-10mm thick and baked at 80°C for 30min	
2.3	PDMS stamp separation	Manual	
2.4	Surface treatment	Evaporation of anti-sticking reagent In TMCS vapour during 1 min	
	End of process 2		
3.0	Process 3: Photolithography mask		
	Mask design and fabrication	Standard photolithography	<i>Including all large size features and alignment markers</i>
4.0	Soft UV nanoimprint Soft UV NIL 		
4.1	Spin coating of layer 1 (sacrificial layer)	Spin-coating of PMMA 300 nm thickness	<i>A thin quartz plate can be used for facilitating optical imaging of DNA migration.</i>
4.2	Spin coating of layer 2 (UV-NIL layer)	Spin coating of AMONIL 100 nm thickness	
4.3	Soft UV Nanoimprint	Imprint at low pressure UV expose (1 min)	<i>Nanostructures alone can be easily replicated with large process latitude.</i>
4.4		De-moulding	
4.5	Residual Layer (Breakthrough) Etching	Reactive ion etch O ₂ plasma	
	End of Process 4		
5.0	Process 5: First lift-off Lift-off 	Nickle	

5.1	Lift-off	Ni thin film E-beam evaporation (40nm) Dissolution of AZ resist	
End of Process 5			
6.0	Process 6: Photolithography Photolithography		
			
6.1	Resist deposition	Spin coating AZ 5215E Resist pre-bake at 125°C for 1min	
6.2	UV exposure	UV exposure 1min with a standard aligner	<i>With alignment</i>
End of Process 6			
7.0	Process 7: Second lift-off Lift-off		
			
7.1	Lift-off	Ni thin film E-beam evaporation (40nm) Dissolution of AZ resist	
End of Process 7			
8.0	Process 8: Pattern transfer Reactive ion etch		
			
8.1	Etch of micro and nanostructure into the substrate	Reactive ion etch SF ₆ plasma	<i>Both micro and nanostructures are etched simultaneously.</i>
8.2	Nickel mask removal	Chemical etch HNO ₃ for 1min	
End of Process 8			
9.0	Process 9: Device assembling Bonding		
			
9.1	Preparation of PDMS cover slide	PDMS coating (1:10) Over a flat silicon wafer	<i>Other materials can also be used as cover layer</i>
9.2	Access hole drilling	Manuel	
9.3	Surface activation	Plasma treatment 1 min in a plasma cleaner for both PDMS and etched sample	
9.4	Device assembling	Thermal bonding In an oven of 70°C for 30min	
End of process 9			

General remarks:

Since only nanoscale features are replicated by nanoimprint lithography, the fabrication process latitude can be largely enhanced. In addition, both lift-off and reactive ion etch steps can be replaced by other pattern transfer techniques. Therefore, the above mix-and-match process is highly parallel and versatile not only for microfluidic device fabrication but also for manufacturing of other types of nano-devices at low cost and high throughput.

6. Stencil Lithography

Contributions to this section of the library are from

EPFL-IMM - Lausanne/Switzerland

Prof. Dr. Jürgen Brugger / Dr. Marc A. F. van den Boogaart

CRF Fiat - Orbassano/Italy

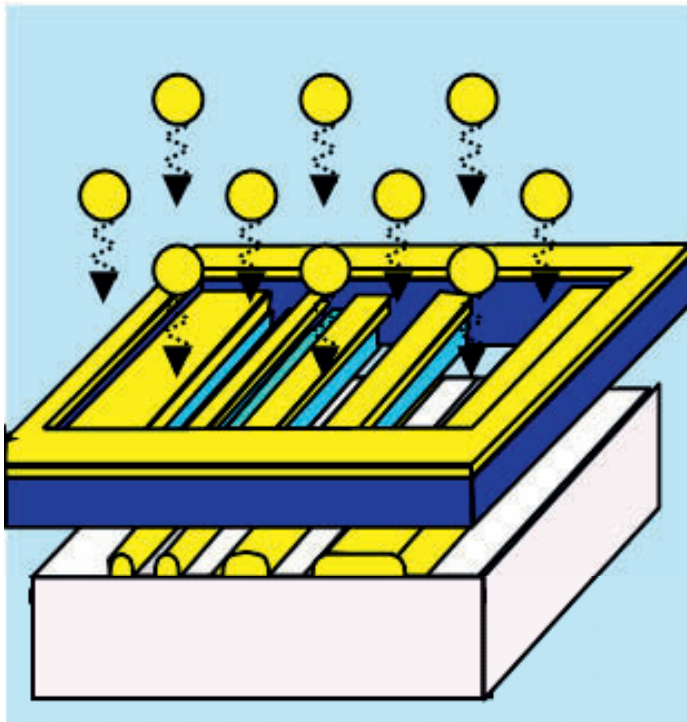
Dr. Vito Lambertini

CNM - Barcelona/Spain

Prof. Dr. Francesc Pérez-Murano / Julien Arcamone

MESA+ - Enschede/The Netherlands

Dr. Jurriaan Huskens / Dr. Veera B. Sadhu



6.1 Surface Structures

Fabrication of surface structures via Stencil Lithography

Process: Stencil Lithography (STEN)

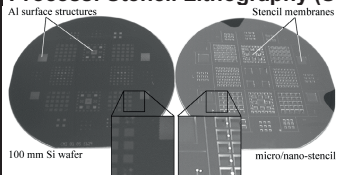


Figure:

A full wafer scale stencil and a substrate with the resulting surface patterns.

Process:

Placing the stencil onto a substrate and simply depositing the wanted material through the stencil apertures onto the substrate.

Application:

Life science, nano electronics, material science, flexible electronics, etc.

Keywords: Stencil Lithography, Shadow Mask, Stenciling, Stencil Deposition

Project leader: EPFL, Lausanne, Switzerland

Address: 1015 Lausanne, Switzerland

Web-Address: <http://lmis1.epfl.ch/>

Process: Stencil Lithography

Responsible: Marc van den Boogaart

E-mail: nanostencil@epfl.ch

Process description: Resistless patterning of micro and nano structures on any type of substrate.

Purpose: The standard stencil lithography process is described in which a large range of materials can be directly structured via the use of a stencil. The process is applicable to any type of substrate and any type of stencil (i.e. chip or full wafer sized, standard or stabilized stencils, etc.)

Major challenges: Pattern resolution is dependent on the geometrical conditions present during stencil lithography. Stencil lifetime is dependent on minimum resolution.

Major advantages: Stencil Lithography is a direct deposition technique where a controlled amount of material is deposited only where needed. No cyclic process steps are needed as seen in photolithography, which drastically increases its ease of use and lowers the risk of contamination associated with resist processing and material removal (i.e. etching).

Application and state-of-the-art: in-situ device fabrication (e.g. single electron transistors, organic electronics) compatible with large scale processing (e.g. CMOS).




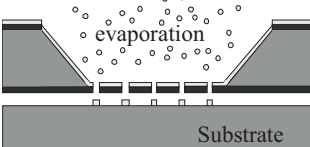

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- [1] van den Boogaart, M. A. F. (2006). Stencil Lithography: An ancient technique for advanced micro- and nanopatterning. Konstanz, Hartung-Gorre Verlag. ISBN:3-86628-110-2
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LoP2007_STEN001_Stencil Lithography. PDF

1.0a	Process 1: Wafer preparation		
1.1	wafer selection and preparation	Any substrate can be used	<i>Topographic features on substrate will influence the minimum pattern resolution.</i>
	End of Process 1a		
1.0b	Process 1: Stencil Fabrication		
1.1	Membrane material definition 	Deposition of Low Stressed SiN on Si wafer	
1.1	Aperture definition 	Pattern the membrane apertures into the SiN via lithography and etching. Then open large windows on the back side using lithography and etching. The windows on the backside will define the membrane size.	
1.2	Wafer through etching 	Etch all the way through the wafer to release the membrane form the bulk Si.	<i>SiN is an excellent etch mask for KOH etching.</i>
	End of process 1b		
2.0	Process 2: Stencil Lithography		
2.1	Place stencil on substrate	Place and fix the stencil with the membrane side on the substrate	
2.2a	Deposition of material 	Place the stencil/substrate into deposition equipment and deposit a controlled amount of material.	<i>Geometrical conditions will determine the minimum resolution of the deposited structures. In general a minimum gap between stencil and substrate is favorable</i>
2.2b	Etching of material	Stencil can be used as a mask to etch material (dry etch).	<i>Etch rate of SiN is too high to effectively use it directly as an etch mask. Deposited a thin Al layer as a hard mask layer on the stencil.</i>
2.2c	Ion implantation	Stencil can be used for directed ion implantation	<i>Check ion energy</i>
2.3	Remove stencil from substrate 	Remove the stencil from the substrate	
	End of process 2		

General remarks:

Examples:

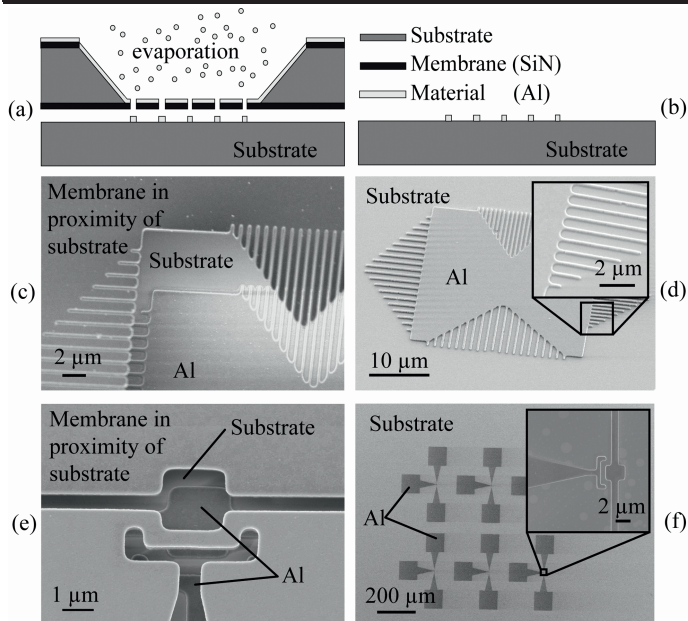


Figure 1: Deposition process using a stencil. (a): The stencil is placed in contact or in close proximity to the substrate and a material is evaporated from a distant source and deposited through the apertures in the membrane onto the substrate; (b): The stencil is removed from the substrate; (c) and (e): The SEM-images show a stencil mask with a gap to a substrate after evaporation. The membrane in Fig. 1c has a gap of approx. 5 μm, whereas a gap of approximately 1 μm is observed in Fig 1e; (d) and (f): The SEM-images show the corresponding Al pattern from Fig. 1c and 1e.

6.2 Alignment

Alignment process for Stencil Lithography

Process: Stencil Lithography (STEN)

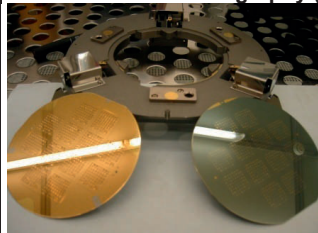


Figure:

A full wafer scale stencil and the a substrate with the resulting surface patterns after alignment and deposition.

Process:

Placing the stencil onto a substrate and simple deposited the wanted material through the stencil apertures onto the substrate.

Application:

Life science, nano electronics, material science, flexible electronics, etc.

Keywords: Stencil Lithography, Shadow Mask, Stenciling, Stencil Deposition

Project leader: EPFL, Lausanne, Switzerland

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Process: Stencil Lithography

Responsible: Marc van den Boogaart

E-mail: nanostencil@epfl.ch

Process description: Resistless patterning of micro and nano structures on and aligned to any type of substrate.

Purpose: A standard Alignment process for stencil lithography is described in which a full wafer (100mm) stencil is aligned to prefabricated structures on any type of substrate (100mm). The process can be applied to any bond alignment equipment.

Major challenges: A stencil membrane needs to be used as an alignment marker. If the stencil has already been used a couple of times the membrane might be stressed which will cause a loss of alignment resolution. The trick is to make a membrane that is not sensitive to deformation due to thin film stresses. After alignment the stencil/substrate need to stay in its aligned position which can be achieved by placing the whole alignment chuck into the deposition equipment.

Major advantages: Stencil Lithography is direct deposition technique where a controlled amount of material is deposited only where needed. No cyclic process steps are needed as seen in photolithography which drastically increased its ease of use and lowers the risk of contamination associated with resist processing and material removal (i.e. etching).

Application and state-of-the-art: in-situ device fabrication (e.g. single electron transistors, organic electronics) compatible with large scale processing (e.g. CMOS).

References:

- [1] van den Boogaart, M. A. F. (2006). Stencil Lithography: An ancient technique for advanced micro- and nanopatterning. Konstanz, Hartung-Gorre Verlag. ISBN:3-86628-110-2
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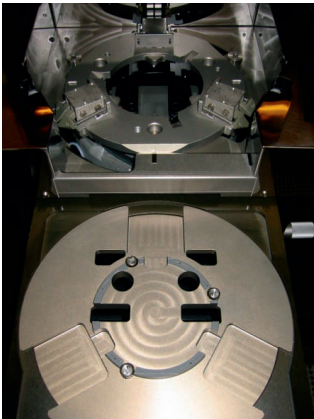
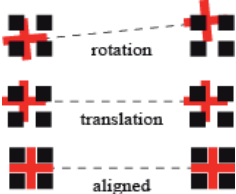
Contact information:

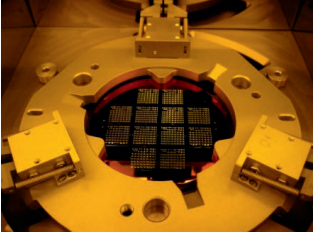
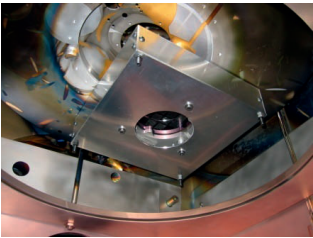
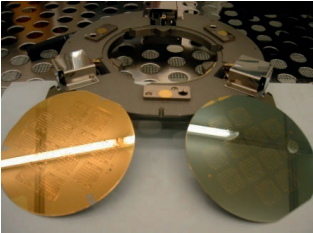
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LoP2007_STEN002_Stencil Alignment. PDF

Alignment

Process: stencil lithography

	Process	Technical Parameters	Remarks
	What	how it should work	critical issues
1.0a	Process 1: Wafer preparation		
1.1	wafer selection and preparation	<p>Any substrate can be used compatible with bond-aligner.</p> <p>A set of alignment markers need to be present on substrate to which the stencil will be aligned.</p>	<p><i>Topographic features on substrate will influence the minimum pattern resolution.</i></p> <p><i>Full wafer (100mm)</i></p>
	End of Process 1a		
1.0b	Process 1: Stencil Preparation		
1.1	Fabricate stencil 	Include a set of alignment markers in a membrane which will be used during alignment process	<i>Full wafer stencil (100mm)</i>
	End of process 1b		
2.0	Process 2: Alignment of Stencil to Substrate		
2.1	Place stencil on substrate  Image of Karl Süss MA/BA 6	<p>Place the stencil with the membranes facing down (facing substrate) and load into bond aligner. Stencil will be fixed to clamping chuck.</p> <p>Place the substrate with alignment features facing upwards.</p> <p>Use a magnification and alignment gap so not to damage the stencil membranes and have both markers in the same focal plane.</p>	<p><i>Depending on your bond aligner and if you're using a top side alignment (TSA) or back side alignment (BSA).</i></p> <p><i>With TSA, stencil first.</i></p> <p><i>With BSA, substrate first.</i></p> <p><i>Due to wafer curvature and warping use a alignment gap larger than 50 μm (wafer characteristic dependant)</i></p>
2.2	Alignment 	<p>Simply align the stencil to the substrate. Usually start by an angular correction then translation.</p> <p>Mechanically clamp the sub substrate to the stencil and verify the alignment.</p>	

<p>2.3</p>	<p>Remove clamping chuck from bond-aligner</p> 	<p>Gently remove clamping chuck from the bond aligner and place in a protective box.</p>	<p><i>The protective box is used to ensure that there is no deposition on the clamping chuck.</i></p> <p><i>The box houses the clamping chuck and has a single hole the size of a wafer to facilitate material transport.</i></p>
<p>2.4</p>	<p>Aligned Stencil Lithography</p> 	<p>Place the protective box with the aligned stencil/Substrate into an deposition equipment and deposited an controlled amount of material</p>	<p><i>For best pattern resolution and uniformity place the stencil/Substrate centered and as far away as possible from the source.</i></p>
	<p>Separate stencil from substrate</p> 	<p>Simply remove the substrate form the stencil.</p>	
<p>End of process 2</p>			

General remarks:

Examples:

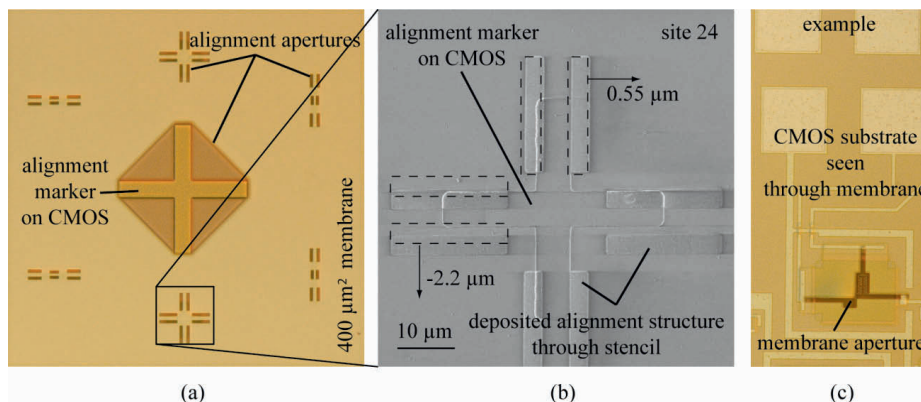


Figure 1: Alignment markers of stencil and CMOS substrate. (a): optical image of a membrane containing alignment apertures aligned to the corresponding marker on CMOS substrate, (b): SEM image of alignment feature after Stencil Lithography, image shows a miss-alignment of +0.55 and -2.2 μm, and (c): optical image showing an example of a membrane aligned to CMOS circuit.

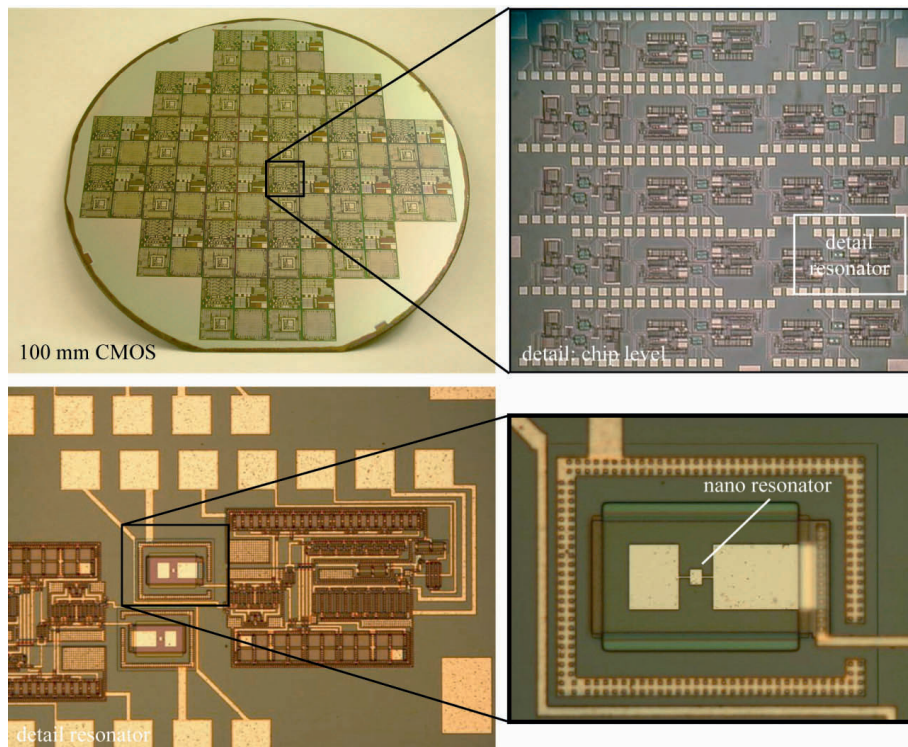


Figure 2: Optical images of an aligned nanostructure to a CMOS substrate.

6.3 Cleaning

Cleaning of stencils for Stencil Lithography

Process: Stencil Lithography (STEN)

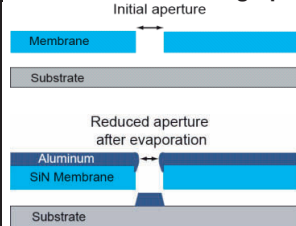


Figure:

Schematic illustration of a stencil being clogged during stencil Lithography

Process:

Cleaning the stencil after stencil lithography.

Application:

Life science, nano electronics, material science, flexible electronics, etc.

Keywords: Stencil Lithography, Shadow Mask, Stenciling, Stencil Deposition

Project leader: EPFL, Lausanne, Switzerland

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Process: Stencil Lithography

Responsible: Marc van den Boogaart

E-mail: nanostencil@epfl.ch

Process description: Cleaning of stencils after resistless patterning of micro and nano structures on and aligned to any type of substrate.

Purpose: A cleaning process is described to enable the reuse of stencils after they get clogged.

Major challenges: Clogging is caused during stencil lithography when the deposited material is not only deposited through the stencil apertures but also on and in the stencil apertures. Eventually this might lead to a complete closure of the stencil apertures. Clogging will also cause a loss of pattern resolution and is especially evident at the nano scale.

Major advantages: Stencil Lithography is direct deposition technique where a controlled amount of material is deposited only where needed. No cyclic process steps are needed as seen in photolithography which drastically increased its ease of use and lowers the risk of contamination associated with resist processing and material removal (i.e. etching).

Application and state-of-the-art: in-situ device fabrication (e.g. single electron transistors, organic electronics) compatible with large scale processing (e.g. CMOS).

References:

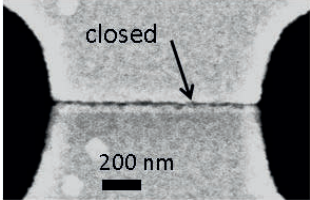
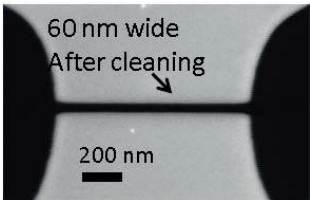
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- [2] O. Vázquez-Men, G. Villanuev, M.A.F. van den Boogaart, V. Savu and J. Brugger, Reusability of nanostencils for the patterning of Aluminum nanostructures by selective wet etching, Microelectronic Engineering Journal, (2007). **Accepted**

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LoP2007_STEN003_Stencil Cleaning. PDF

Cleaning

Process: stencil lithography			
	Process	Technical Parameters	Remarks
	What	how it should work	critical issues
1.0	Process 1: Stencil Clogging		
1.1	Stencil Clogging 	<p>During stencil lithography a controlled amount of material is deposited through but also on the membrane.</p> <p>The accumulated material will gradually clog the membrane apertures.</p>	<p><i>The speed at which a membrane aperture is clogged depends on the material which is deposited.</i></p> <p><i>For Al: membrane aperture size reduction is proportional to the deposited thickness with a factor of 1:1.</i></p> <p><i>For Ag: membrane aperture size reduction is proportional to the deposited thickness with a factor of 1:5.</i></p>
	End of Process 1		
2.0	Process 2: Stencil Cleaning		
2.1	Prepare etch solution	<p>Prepare etch solution for the material that is clogging the membrane aperture.</p> <p>Example: for Al an etch solution of CH₃COOH (100%), HNO₃ (70%) and H₃PO₄ (85%) in proportions 5:3:75 at 35°C can be used.</p>	<p><i>Verify that chosen etch solution does not attack the membrane itself, i.e. chose an etch solution with a high selectivity towards the membrane material.</i></p>
2.2	Clean Stencils 	<p>Place the clogged stencil into the etch solution and remove all the unwanted material.</p>	<p><i>Material inside a nano aperture require additional etch time because of the restricted access of the etch solution (e.g. air bubbles).</i></p>
	End of process 2		

General remarks:

Examples:

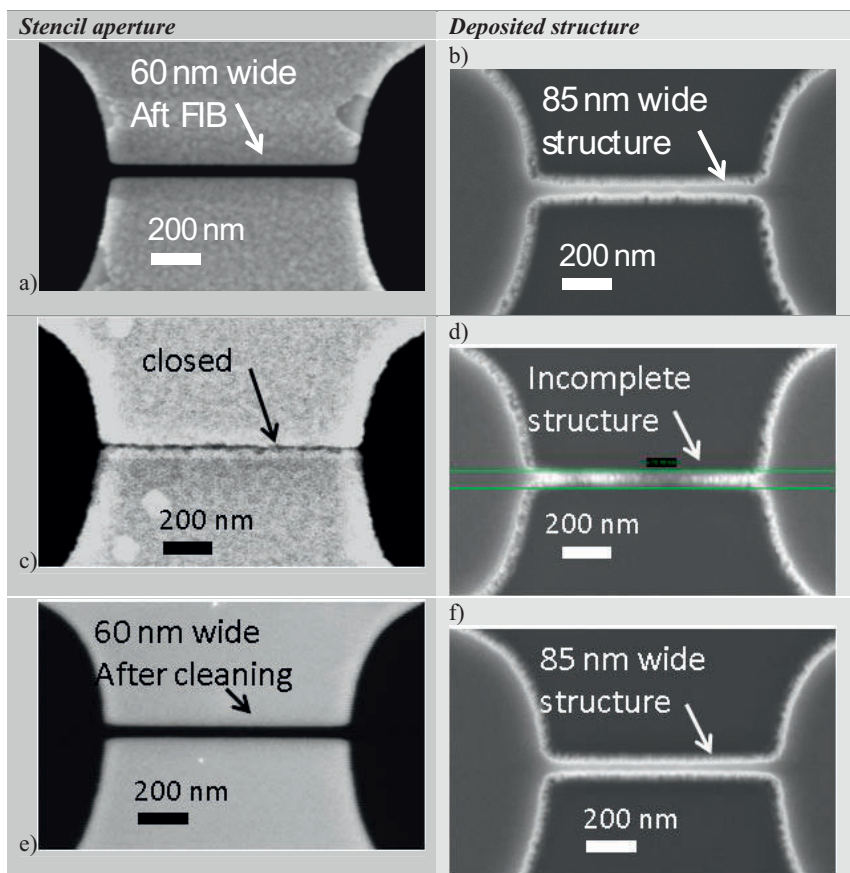


Figure 1: Stencil Lithography, clogging and Cleaning. A stencil aperture after FIB milling is shown in Fig 1a and the corresponding deposited structure is shown in Fig 1b. After three evaporations (75 nm Al) the stencil gets clogged and the aperture is almost closed as shown in Fig 1c. The deposited structure through the clogged stencil is incomplete (Fig 1d). Then the stencil is cleaned using the “stencil cleaning” procedure. Fig 1e shows the stencil aperture after this process. As it is observed, the aperture does not suffer any damage or modification and more important, the stencil aperture recovers the original size after FIB milling. This cleaned stencil was used for the deposition of 25 nm of Al and the deposited structure (Fig 1f) also recovers the size from the first deposition with the stencil (Fig 1b)

6.4 Double Angle Evaporation

Double-Angle Evaporation using Stencil Lithography

Process: Stencil Lithography (STEN)

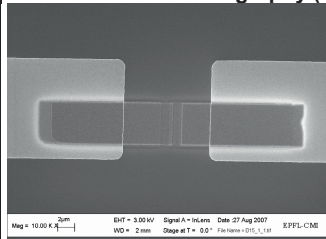


Figure:

An Al/AIO_x/Al tunnel junction fabricated by double angle evaporation through a stencil.

Process:

A first layer is deposited through the stencil from one material source. In situ, a second layer is deposited through the stencil from a second material source.

Application:

Nano electronics, material science, flexible electronics, etc.

Keywords: Stencil Lithography, Shadow Mask, Double Angle, Stencil Deposition

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Process: Stencil Lithography

Responsible: Marc van den Boogaart

E-mail: nanostencil@epfl.ch

Process description: Double angle evaporation of materials through stencils.

Purpose: In-situ deposition of multiple layers laterally offset by a controlled distance.

Major challenges: The offset between the two layers depends on the geometrical conditions during the deposition. For example, the substrate-stencil gap using a standard stencil exhibits a larger variation at full wafer scale than at the chip level (maximum of around 30 microns vs. 6 microns).

Major advantages:

The material overlaps obtained this way can be an order of magnitude and more smaller than the stencil apertures

Being an in situ process, it insures the cleanest interface between the deposited materials

Application and state-of-the-art: in-situ device fabrication (e.g. single electron transistors, tunnel junctions) compatible with large scale processing (e.g. CMOS).




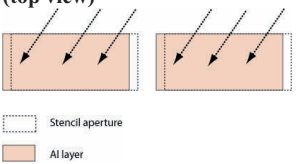
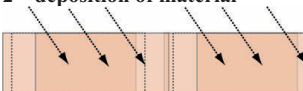
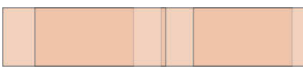
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LoP2007_STEN004_DoubleAngle. PDF

Double Angle Evaporation

Process: stencil lithography

	Process	Technical Parameters	Remarks
	What	how it should work	critical issues
1.0a	Process 1: Wafer preparation		
1.1	wafer selection and preparation	Any substrate can be used	<i>Topographic features on substrate will influence the minimum pattern resolution.</i>
	End of Process 1a		
1.0b	Process 1: Stencil Fabrication		
1.1	Membrane material definition	Deposition of Low Stressed SiN on Si wafer	
			
1.1	Aperture definition	Pattern the membrane apertures into the SiN via lithography and etching. Then open large windows on the back side using lithography and etching. The windows on the backside will define the membrane size.	
			
1.2	Wafer through etching	Etch all the way through the wafer to release the membrane form the bulk Si.	<i>SiN is an excellent etch mask for KOH etching.</i>
			
	End of process 1b		
2.0	Process 2: Double Angle Deposition through Stencil		
2.1	Place stencil on substrate	Place and fix the stencil with the membrane side on the substrate	
2.2a	1 st deposition of material (top view)	Place the stencil/substrate into deposition equipment and deposit a controlled amount of material from the 1 st source.	<i>Geometrical conditions will determine the minimum resolution of the deposited structures. A gap between stencil and substrate is necessary for double-angle depositions with non-zero offset between the two materials.</i>
			
2.2b	2 nd deposition of material	Deposit from the 2 nd material source.	<i>An intermediate oxidation step can for example be used in between the two depositions.</i>
			
2.3	Remove stencil from substrate	Remove the stencil from the substrate and characterize your devices.	
			
	End of process 2		

General remarks: The shift of the transferred pattern with respect to the openings depends on the evaporation angle α (with respect to the vertical of the substrate) and on the gap between the bridge and the substrate G (Fig. 2a). The evaporation angle can be computed from the distance between the (x,y) planes of the bridge and that of the evaporation source D , and the position of the source and the bridge in the (x,y) plane x,y with respect to the center (Fig. 2b). The junction width, $a1+a2$, can be computed as follows:

$$\tan \alpha 1 = \frac{a2}{G} = \frac{s2-x}{D} \Rightarrow a2 = G \frac{s2-x}{D},$$

$$\tan \alpha 2 = \frac{a1+A}{G} = \frac{s1+x-A}{D} \Rightarrow a1 = G \frac{s1+x-A}{D} - A$$

$$a1 + a2 = \frac{G}{D} (s1 + s2) - A$$

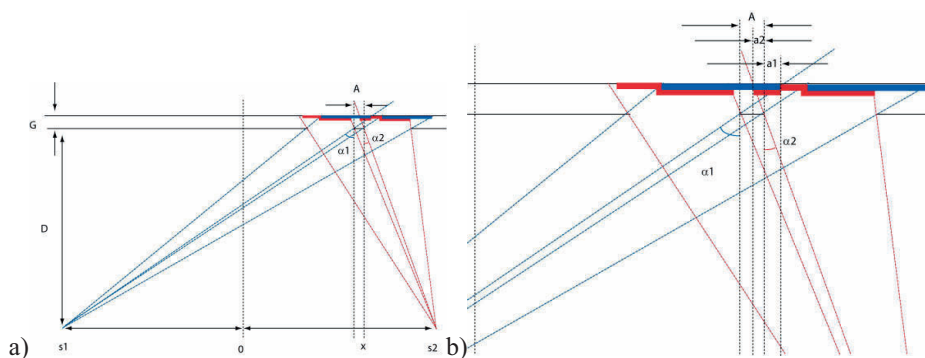


Figure 2. Geometrical schematic of the double-angle evaporation through a stencil: a) zoomed-out picture, and b) zoomed-in picture.

Examples:

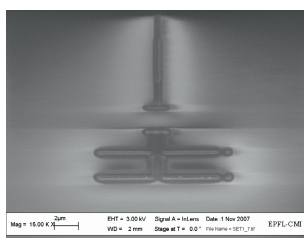
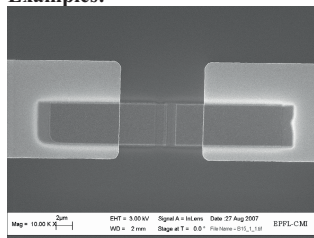


Figure 1: SEM images of structures obtained by double-angle deposition through a stencil. (a) An Al/AIOx/Al tunnel junction, where an intermediate in-situ oxidation step was introduced between the two Aluminum depositions; (b) An isolated single electron transistor (SET), containing two nano Al/AIOx/Al tunnel junctions fabricated using the same procedure as the micron junctions from Fig. 1a.

6.5 Dynamic Stencil

Fabrication of custom surface structures via (Quasi) Dynamic Stencil Lithography

Process: Stencil Lithography (STEN)

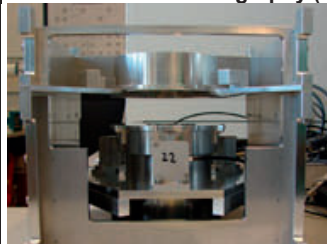


Figure:

Full wafer stencil (Quasi) Dynamic Stencil Lithography system (QDSLS).

Process:

The (Quasi) Dynamic Utilization of stencils during Stencil Lithography will allow the creation of multi-material, custom surface structures.

Application:

Life science, nano electronics, material science, flexible electronics, etc.

Keywords: Stencil Lithography, Shadow Mask, Stenciling, Stencil Deposition

Project leader: EPFL, Lausanne, Switzerland

Address: 1015 Lausanne, Switzerland

Web-Address: <http://lmis1.epfl.ch/>

Process: Stencil Lithography

Responsible: Marc van den Boogaart

E-mail: nanostencil@epfl.ch

Process description: Resistless patterning of custom micro and nano structures on any type of substrate using dynamic utilization of stencils.

Purpose: A process described in which a stencil is moved during or in-between depositions. This enables in-situ structuring of custom surface structures using simple stencil apertures. This process will also allow for tapered thin-film structures, stitched structures and closed loop structures such as a donut shape.

Major challenges: Pattern resolution is dependent on the geometrical conditions present during stencil lithography. Maintaining a constant gap over the full translation length is crucial to pattern size uniformity. Stencil aperture clogging is linked to the nominal thickness deposited while in dynamic stencil lithography deposited surface structure thickness is related to the scan speed, aperture size and deposition rate.

Major advantages: Stencil Lithography is a direct deposition technique where a controlled amount of material is deposited only where needed. No cyclic process steps are needed as seen in photolithography, which drastically increases its ease of use and lowers the risk of contamination associated with resist processing and material removal (i.e. etching). Dynamic Stencil Lithography will allow for in-situ, multi material and custom surface structures/devices while only using a simple stencil aperture.

Application and state-of-the-art: in-situ device fabrication (e.g. single electron transistors, organic electronics) compatible with large scale processing (e.g. CMOS).

References:


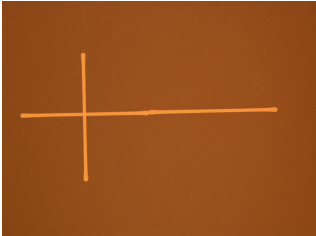
- [1] van den Boogaart, M. A. F. (2006). Stencil Lithography: An ancient technique for advanced micro- and nanopatterning. Konstanz, Hartung-Gorre Verlag. ISBN:3-86628-110-2
- [2] H. Guo, D. Martrou, T. Zambelli, J. Polesel-Maris, A. Piednoir, E. Dujardin, S. Gauthier, M.A.F. van den Boogaart, L.M. Doeswijk and J. Brugger, Nanostenciling for combinatorial fabrications and interconnections of nanopatterns and microelectrodes, Applied Physics Letters, 90 (2007) 093113 (3 pages).

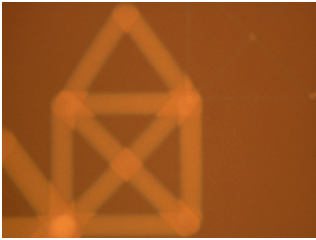
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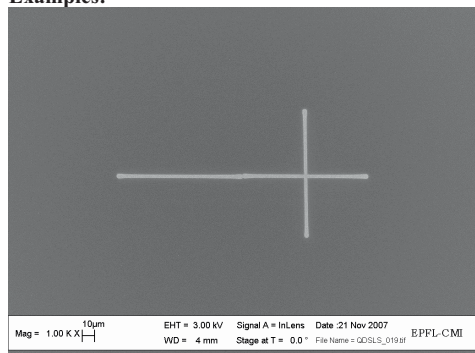
Process: stencil lithography

	Process	Technical Parameters	Remarks
	What	how it should work	critical issues
1.0a	Process 1: Wafer preparation		
1.1	wafer selection and preparation	Any substrate can be used (100mm)	<p><i>Topographic features on substrate will influence the minimum pattern resolution.</i></p> <p><i>Substrate (100mm) needs to be cut to a width of 60mm in current experimental set-up of EPFL-LMIS1.</i></p>
	End of Process 1a		
1.0b	Process 1: Stencil Preparation		
1.1	Membrane material definition 	Any stencil can be used (100mm) Place individual structures at known relative distances (e.g. horizontal and vertical lines)	<p><i>Stencil (100mm) needs to be cut to a width of 60mm in current experimental set-up of EPFL-LMIS1.</i></p>
	End of process 1b		
2.0	Process 2: (Quasi) Dynamic Stencil Lithography		
2.1	Place stencil and substrate into QDSLS	Place the stencil on the stencil holder. The stencil holder is mounted on a XYZ stage. Place and fix the substrate. Substrate does not move and remains static during structuring.	
2.3	Determine gap between stencil and substrate	Move the stencil and substrate towards each other and position them at a parallel and known gap.	<i>Due to wafer curvature and bowing the gap needs to be greater than approx. 30 μm during dynamic applications.</i>
2.4a	Step and repeat Stencil Lithography (Quasi Dynamic) 	Move to first position using XY actuators. Bring stencil in contact and deposited a controlled amount of material. Then, retract stencil to save distance (e.g. 50 μm). Move to second position and deposit second layer etc. etc.	<i>Nominal deposited thickness is nominal deposited structure height.</i>

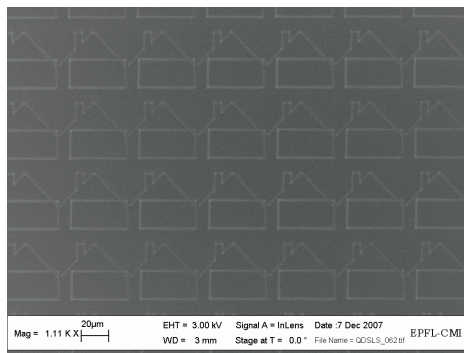
<p>2.4b</p>	<p>Dynamic Stencil Lithography</p> 	<p>Move to first position using XY actuators. Bring stencil to a controlled deposition gap and while depositing, move the stencil with your desired pattern using the XY actuators</p>	<p><i>Nominal deposited thickness is not the nominal deposited structure height. Structure height is a function of aperture size, XY actuation speed and deposition rate.</i></p>
<p>2.6</p>	<p>Remove substrate and stencil from QDSLS End of process 2</p>	<p>Remove substrate and stencil from QDSLS</p>	

General remarks:

Examples:



(a)



(b)

Figure 1: Surface structures made via vacuum deposition through QDSLS. (a): Surface structure made via step and Repeat Stencil Lithography. Image shows three successive depositions of one horizontal line and one vertical line shaped slit. The largest displacement to place the vertical line above a horizontal line was 900 μm. (b) Surface structure made via Dynamic Stencil Lithography. An array of 2 μm holes was moved during deposition forming a custom surface structure. The image shows a micro house made of two materials (Ag and Au).

6.6 OLED Device

Fabrication of OLED device by nanostencil method

Process: stencil lithography (STEN)

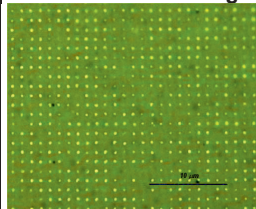


Figure:

Organic light emitting device
nanopatterned surfaces (resolution
1 μm and height 300 nm).

Process:

OLED device fabrication by nanostencil method.

Application:

Lighting systems and displays.

Keywords: OLED, nanostencil

Project leader: Centro Ricerche Fiat

Address: Strada Torino 50, 10043, Orbassano (TO)

Web-Address: <http://www.crf.it>

Process: OLED fabrication

Responsible: Vito Lambertini

E-mail: vitoguido.Lambertini@crf.it

Process description: A process is described to fabricate a light emitting devices based on organic materials deposited by HUV deposition and spin coating method.

Purpose: The aim of this process is demonstrate the increasing of efficiency more than 20% enhancing the light extraction.

Major challenges: deposition of charge injection layer trough nanometer stencils.

Application and state-of-the-art: the structuring of OLED device has been proposed in several work mainly based on microstructuring. Only in the last 2 years the introduction of sub-wavelength patterns has been proposed.

References:

- [1] Improvement of the external extraction efficiency of OLED by using a pyramid array, Stanley Electric Co., Ltd. (Japan)
- [2] Nanohole OLEDs embedded in the 2D periodic SiO₂ nanohole array. Yoon-Chang Kim R&D Center, Samsung SDI Co. Ltd., Young Rag Do Dep. of Chemistry, Kookmin Un., Seoul, 2005 Optical Society of America.

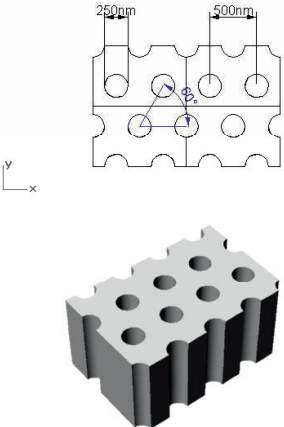
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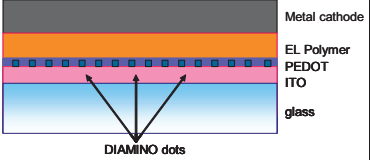

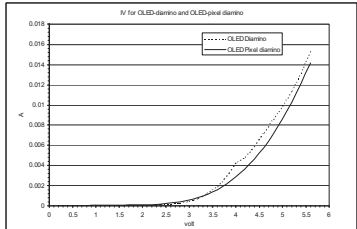
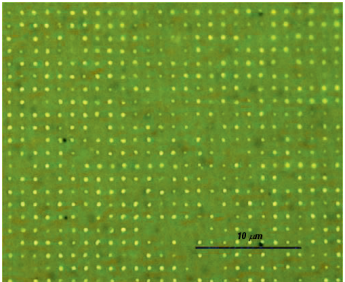
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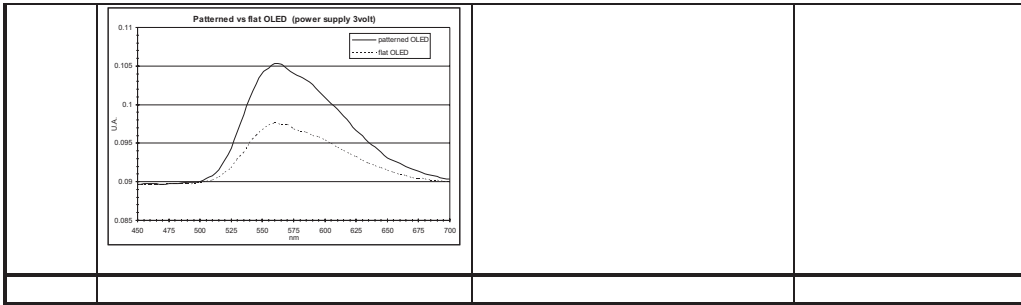
OLED - Device

Process: stencil lithography

	Process	Technical Parameters	Remarks
	What	how it should work	critical issues
1.0	Process 1: Substrate preparation		
1.1	wafer selection and preparation	transparent substrate with transparent conductive oxide layer (ITO) Glass substrate 35x45 mm Thickness 1 mm	
1.2	substrate preparation	Cleaning washing in Micro90 solution diluted (2%); ultrasonic baths cycles (5 min) in water and ethanol	
1.3	ITO patterning	UV-photolithography spin coating of UV-resist 2500 rpm soft bake 80°C for 1 min UV exposure for 20sec hard bake 120°C for 30 min KOH wet etching	
	End of Process 1		
2.0	Process 1: Stencil characterization and selection		
2.1	Pattern selection 	Different pitches, shapes and hole dimensions are chosen for nanostencil masks to obtain a regular arrangement of nanometer dots after physical depositions.	

<p>2.2</p>		<p>SEM/FIB/AFM characterization</p>	<p><i>Micrometer stencil with linking holes at nanometer scale is too hard to fabricate.</i></p>
<p>3.0 Process 3: OLED fabrication</p>			
<p>3.1</p>	<p>Charge-injection layers evaporation through nanostencil</p>	<p>Thermal vacuum evaporation Evaporation of charge injection layer -NN' Diphenyl-NN' bis(1Naphyl-4n Diamino) -1 Biphenil). AUTO306 coater Vacuum 9×10^{-6} mbarr Thickness 20-40 nm Evaporation rate 0.5 nm/min</p>	<p><i>Several evaporations through the nanostencil carry out clogging of nanostencil holes. Wet chemical cleaning is requested after 10-20 evaporation steps.</i></p>
<p>3.1a</p>	<p>Process control</p>	<p>Profilometer Thickness 20-30 nm Optical microscope</p>	
<p>3.2</p>	<p>Charge-injection layers deposition</p>	<p>Spin coating Karl Suss RC8 spin coater Double layer: PEDOT/PSS suspension (Bayer) no vacuum 2500 rpm 5000 rpm/s 20-40 nm</p>	
<p>3.2</p>	<p>Active layers deposition</p>	<p>Spin coating Karl Suss RC8 spin coater Double layer: PPVs (yellow/orange from Merck) no vacuum 2000-2500 rpm 5000 rpm/s 75-90 nm</p>	
<p>3.3</p>	<p>Cathode deposition</p>	<p>Thermal vacuum evaporation AUTO306 coater</p>	

		<p>Al (capping layer) Vacuum 9×10^{-6} mbarr 120 nm</p>	
<p>3.4</p>	<p>Packaging</p>	<p>Epoxy resin casting The liquid epoxy resin (UV or thermal) is placed directly onto the cathode and a thin glass (microscope glass) is used to close the device. The curing is made: Thermal Tamb 2 hours UV (spot light) : 60 mW/cm² 10 s</p>	<p><i>The contact of the device with oxygen degrades the device quickly; the oxygen exposition time has to be reduced as much as possible. The ideal condition is to use a glove box.</i></p>
<p>3.5</p>	<p>Measurement</p>  	<p>Electrical analysis I/V curves Home made software by Labview K2425 power supply</p>	
<p>3.5a</p>	<p>Measurement</p> 	<p>Electro-Optical analysis Efficiency curves (Lm/W) for light emission at 0° (normal to the emission surface) Coupling of Horiba-Jobin Yvon spectroradiometer and optical microscope by UV-VIS optical fiber Optical fiber range 200-800nm Home made software by Labview : K2425 power supply</p>	<p><i>Focus of emissive area through optical microscope lens onto optical fiber is hard.</i></p>

**General remarks:**

The architectures of devices with patterned electrode showed an increasing of external efficiency (at 0° degree in view) in OLED technology is in the range of 25-30%.

6.7 Integration of NEMS with CMOS

Direct integration of NEMS with CMOS using Stencil Litho

Process: Stencil Lithography (STEN)

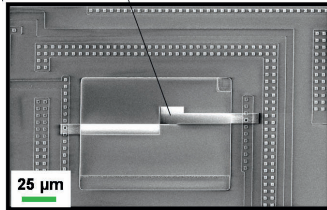


Figure:

Stencil alignment to CMOS substrate

Process:

Placing the stencil onto a substrate and simple deposited the wanted material through the stencil apertures onto the substrate.

Application:

Nanosensors for life science, nanoelectronics, material science, flexible electronics, etc.

Keywords: Stencil Lithography, Shadow Mask, Stenciling, Stencil Deposition, NEMS, CMOS

Project leader: EPFL, Lausanne, Switzerland

Address: 1015 Lausanne, Switzerland

Web-Address: <http://lmis1.epfl.ch/>

Process: Stencil Lithography

Responsible: Marc van den Boogaart

E-mail: nanostencil@epfl.ch

Partner: Centro Nacional de Microelectronica (CNM-CSIC)

Address: UAB Campus, 08193-Bellaterra, Spain

Web-Address: <http://www.cnm.es/>

Process: CMOS post processing

Responsible: Julien Arcamone

E-mail: nano@cnm.es

Process description: Resistless patterning of micro and nano-structures [1] on- and aligned to any type of substrate. In this example of process, the substrate is a pre-fabricated CMOS substrate.

Purpose: Full-wafer (100mm) stencil alignment to prefabricated CMOS substrates and structures.

Major challenges: A stencil aperture needs to be used as an alignment marker. If the stencil has already been used a couple of times, the membrane might be stressed which will cause a loss of alignment resolution. The trick is to make a membrane that is not sensitive to deformation due to thin film stresses. After alignment, stencil and substrate need to stay in their aligned position which can be achieved by placing the whole alignment chuck into the deposition equipment. After the deposition, the Al stenciled patterns are blurred. Therefore, a short corrective dry etch [2] is applied to them so that they recover nominal dimensions. Then, they need to be transferred into the active mechanical layer which is a given CMOS layer.

Major advantages: With Stencil Lithography a controlled amount of material is deposited only where needed. No cyclic process steps are needed unlike e-beam lithography which has demonstrated to cause perturbations in the CMOS circuitry operation.

Application and state-of-the-art: in-situ device fabrication (e.g. single electron transistors, organic electronics, tunable mechanical resonators [3]) compatible with large-scale processing (e.g. CMOS).

References:

- [1] van den Boogaart, M. A. F. (2006). Stencil Lithography: An ancient technique for advanced micro- and nanopatterning. Konstanz, Hartung-Gorre Verlag. ISBN:3-86628-110-2
- [2] J. Arcamone, A. Sánchez-Amores, J. Montserrat, M. A. F. van den Boogaart, J. Brugger, and F. Pérez-Murano *Dry etching for the correction of gap-induced blurring and improved pattern resolution in nanostencil lithography* J. Micro/Nanolith. MEMS MOEMS **6**, 013005 (2007)
- [3] J. Arcamone, B. Misischi, F. Serra-Graells, M.A.F. van den Boogaart, J. Brugger, F. Torres, G. Abadal, N. Barniol and F. Pérez-Murano, A Compact and Low-Power CMOS Circuit for Fully-Integrated NEMS Resonators, IEEE Transactions on Circuits and Systems II, 54 (2007) 377-381.

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LoP2007_STEN007_Integration of NEMS with CMOS.PDF

Direct integration of NEMS with CMOS using Stencil Litho

Process: Stencil lithography

	Process	Technical Parameters	Remarks
	What	how it should work	critical issues
1.0a	Process 1: CMOS preparation		
1.1	CMOS substrate. 	CMOS circuitry with a dedicated surface area (integration area) for the mechanical resonators. A set of alignment markers need to be present on substrate to which the stencil will be aligned.	<i>Topographic features on CMOS substrate will influence the minimum pattern resolution.</i> <i>Full wafer (100mm)</i>
	End of Process 1a		
1.0b	Process 1: Stencil Preparation		
1.1	Fabricate stencil 	Include a set of alignment markers in a membrane which will be used during alignment process	<i>Full wafer stencil (100mm)</i>
	End of process 1b		
2.0	Process 2: Fabrication of nano mechanical resonators integrated into a CMOS substrate		
2.1	Perform a stencil alignment 	Simply align the stencil to the CMOS substrate using stencil membrane and surface alignment markers present in the CMOS substrate.	<i>See Stencil Alignment process sheet.</i>
2.2	Aligned Stencil Lithography 	Place the aligned stencil-CMOS combination into an evaporator and evaporate a 80nm thick Al layer.	<i>The Al layer will serve as an hard etch mask during pattern transfer into the active layer designated in the CMOS.</i> <i>See Stencil Lithography Process sheet.</i>
2.3	Transfer Stencil pattern into CMOS layer by RIE 	Place the CMOS substrate into an etching chamber and use an appropriate etch recipe to etch into the structural layer. In this example fluorine chemistry was used.	Before the transfer, pattern blurring can be removed by a short corrective dry etch to recover nominal dimensions [1,2].
2.4	Releasing the resonators 	Remove the Al etch mask and release the resonators via a local selective etch. In this example a HF solution was used	<i>Protect the rest of the circuitry during the release by using e.g. a thick photo resist layer.</i>
	End of process 2		

Examples:

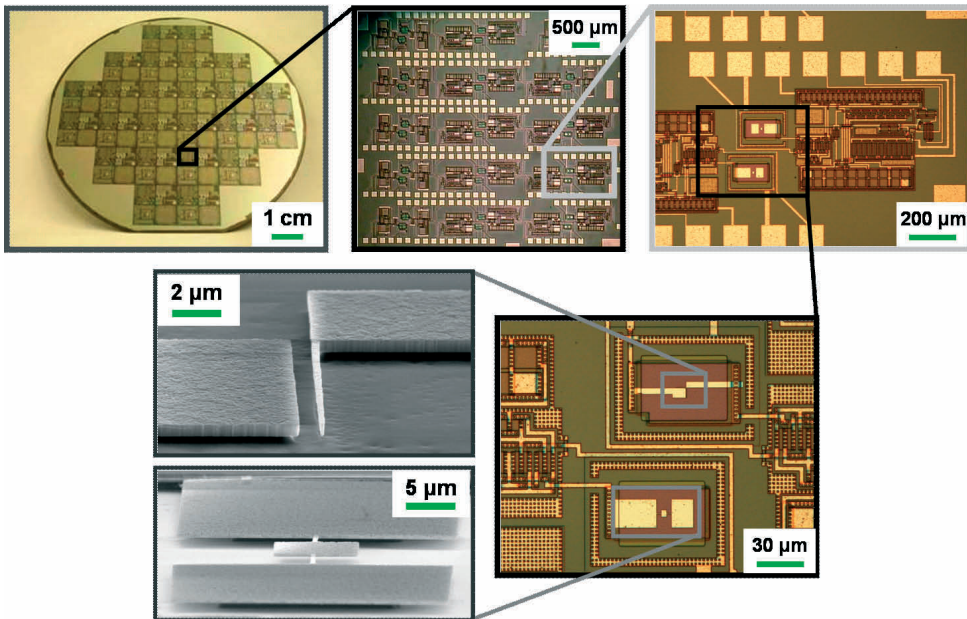


Figure 1: Full-wafer (100 mm) fabrication of diverse types of nanoresonators (~2000/wafer) patterned by nanostencil lithography and monolithically interconnected with CMOS circuitry for signal interfacing.

NaPa – Library of Processes

Nanopatterning and Applications

First edition with results of the NaPa-project, March 2008

Printed by micro resist technology GmbH Berlin, Germany

URL: <http://www.microresist.com>

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