Developement of a DC-DC Converter for the Mu3e Detector

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Sophie Gagneur

Erstgutachter: Prof. Dr. Niklaus Berger
Zweitgutachter: Jun.-Prof. Dr. Florian Hug

Institut für Kernphysik
Johannes Gutenberg-Universität

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Sophie Gagneur
2714773
AG Berger
Institut für Kernphysik
Staudingerweg 9
Johannes Gutenberg-Universität
D-55128 Mainz
sgagneur@students.uni-mainz.de

Abstract

The Mu3e experiment, planned at the Paul Scherer Institute in Villigen, Switzerland, searches for the lepton flavour violating decay of the muon into an electron and two positrons $\mu^+ \to e^+e^+e^-$. This process is strongly suppressed in the standard model of elementary particles and a detection would thus be a clear sign for physics beyond the standard model. Mu3e aims at a sensitivity level of 10^{-16} for the branching fraction.

A special challenge for the experiment is the powering scheme of the individual detector components. Power supplies in the experimental hall provide a voltage of 20 V, which is routed via long cables into the detector. Inside the detector the voltage is converted with the help of DC-DC converters into a lower voltage between 2.1 V and 3.6 V, depending on the requirement of the corresponding detector component. The DC-DC converters have to meet special requirements. Since they are located within a 1 T strong magnetic field, all components of the converter must be suitable for this environment. This also excludes the use of coils with iron cores, which requires the development of special air coils. The components must also be suitable for operation with very high currents (operation point at 20 A). Special conditions are also attached to the output quality of the converters. In order to ensure efficient performance of the detector components, the noise level of the output voltage must be as low as possible. An upper limit of 10 mV was set for the height of the output ripple.

A first version of the Mu3e Dc-DC converter has already been designed. The task of this thesis was to test the behaviour of the converter and to design a new, improved version based on the results. The performance of the first version could already be tested during a a test beam at DESY.

Zusammenfassung

Das Mu3e Experiment, geplant am Paul Scherer Institute in Villigen in der Schweiz, sucht nach dem Leptonfamilienzahl-verletzenden Zerfall des Myons in ein Elektron und zwei Positronen $\mu^+ \rightarrow e^+e^+e^-$. Dieser Prozess ist im Standardmodel der Elementarteilchen stark unterdrückt und ein Nachweis würde somit ein klares Zeichen für Physik jenseits des Standardmodels darstellen. Mu3e strebt dabei ein Sensitivität von 10^{-16} für das Verzweigungsverhältnis an.
Eine besondere Herausvorderung für das Experiment ist die Spannungsversorgung der einzelnen Detektokomponenten. Netzteile in der Experimentierhalle liefern eine Spannung von 20 V, die über lange Kabel ins Detektorinnere geleitet wird. Im Inneren wird die Spannung mit Hilfe von DC-DC Wandlern eine niedrigere Spannung zwischen 2.1 V und 3.6 V, je nach Anforderung der entsprechenden Detektorkomponente, umgewandelt.
Die DC-DC Wandler müssen dabei spezielle Anforderungen erfüllen. Da sie sich innerhalb eines 1 T starken Magnetfeldes befinden müssen alle Komponenten des Wandlers in dieser Umgebung auch funktionieren. Das schließt auch die Verwendung von Spulen mit Eisenkernen aus, was die Entwicklung von speziellen Luftspulen erfordert. Auch an die Ausgangsspannung der Wandler werden besondere Bedingungen geknüpft. Um einen effizienten Betrieb der zu versogrenden Detektorkomponenten zu gewährleisten, muss das Rauschen der Ausgangsspannung so gering wie möglich sein. Dabei wurde für die Höhe des Spannungsschwankungen am Ausgang eine Obergrenze von 10 mV gesetzt.
Eine erste Version des Mu3e DC-DC Wandlers wurde bereits entworfen. Aufgabe dieser Arbeit war es, die Funktion des Wandlers zu testen und auf Basis der Ergebnisse eine neues, verbessertes Design zu entwerfen. Die Funktion der ersten Version konnte bereits im Rahmen eines Testbeams am DESY getestet werden.

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Chapter 1

The Mu3e Experiment

1.1 Motivation

Many theories and discoveries made in particle physics during the last years and decades have resulted in a remarkable model: the Standard Model of particle physics. This model is a rigorous mathematical theory of all elementary particles and their interactions.
The Standard Model categorizes the fundamental particles into two groups as seen in figure 1.1: fermions and bosons. The bosons have integer spin and act as exchange particles of the fundamental interactions. Fermions can be understood as the building blocks of matter. They all have half-numbered spin and can be classified further into quarks and leptons. There are 6 quarks and 6 leptons and their corresponding antiparticles known. These can be divided into so-called "generations" or "families" according to their characteristics. One of these properties is called flavour. Each lepton has a corresponding flavour and they are parameterised with the flavour quantum number. This lepton flavour is conserved in the Standard Model [41].
Even if the Standard Model currently provides the best description of the subatomic world, it cannot explain all observed phenomena. For example, only three of the four fundamental forces can be adequately explained; gravity is not yet fully understood. Questions about dark matter, matter-antimatter asymmetry and about neutrino masses also remain open.

As mentioned before, lepton flavour is conserved in the Standard Model of elementary particle physics. The violation of lepton flavour conservation is nevertheless observed by various experiments in the neutrino sector, such as Super-Kamiokande [4], SNO [2] and KamLAND [17]. The phenomena of neutrino oscillation indicates that neutrinos have non-zero masses and therefore lepton flavour violation (LFV) is also expected in the realm of the charged leptons. However, in the Standard Model extended by massive neutrinos, charged LFV is heavily suppressed due to very small squares of the mass differences between neutrinos compared to the mass of the W-boson. If the existence of new particles beyond the Standard Model is brought into play, the whole situation changes. LFV effects are predicted in many models and are therefore considered a strong indication of new physics. For example, a high probability for LFV is predicted in models such as grand unified models, left-right symmetric models, supersymmetric models and models with an extended Higgs sector.[10]

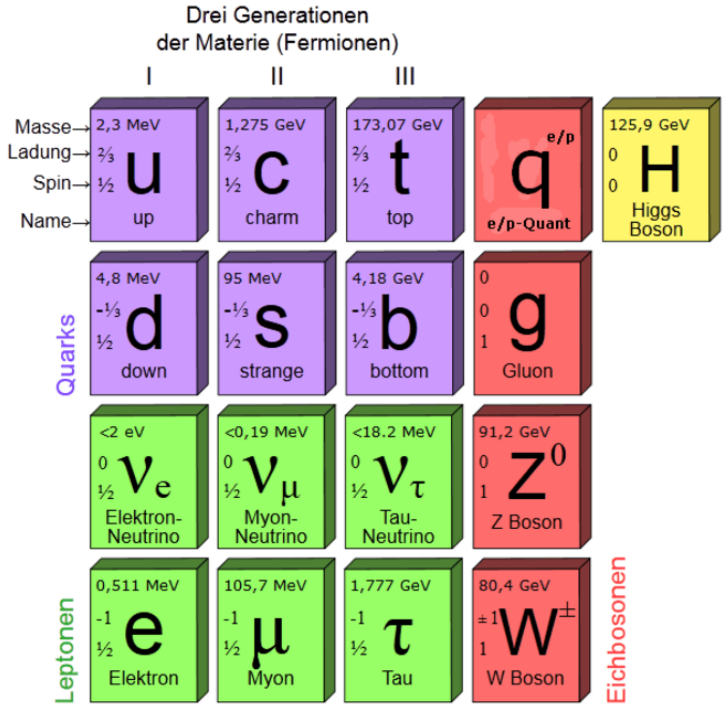


Figure 1.1: The Standard Model consists of three generations of matter particles and three gauge bosons associated with the fund force between them plus the higgs boson [63].

1.2 The Muon

The muon is a lepton with electrical charge and can be described as a heavy electron with similar properties. It has a mass of (105.658367±0.000004) MeV and a mean lifetime of (2.197034±0.00021)·10^{-6} s [24].
The Michel decay shown in figure 1.2 is the most likely decay mode for the muon with a branching ratio of nearly ∼100%. All other decays for the muon in the Standard Model are listed in table 1.1 [33].
Models that consider phenomena outside the limits of the Standard Model open up the possibility for even more decay modes than those shown in table 1.1. Decay processes like $\mu \to e$, $\mu \to e\gamma$ and $\mu \to eee$ become possible. Mu3e puts its focus on

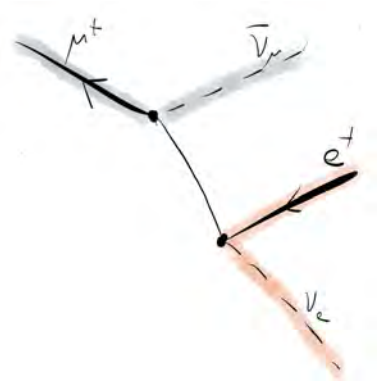
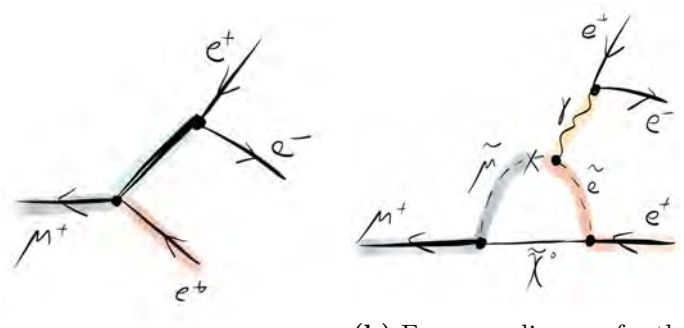


Figure 1.2: Feynman diagram of the Michel decay for a positively charged muon [60].

Decay mode	Branching ratio	References
$\mu^- \to e^- \bar{\nu}_e \nu_\mu$	100%	
$\mu^- \to e^- \bar{\nu}_e \nu_\mu \gamma$	$1.4 \pm 0.4\%$ (for $E_\gamma > 10\,\mathrm{MeV}$)	Crittenden, et al. (1961)
$\mu^- \to e^- \bar{\nu}_e \nu_\mu e^+ e^-$	$(3.4 \pm 0.4) \times 10^{-5}$	Bertl, et al. (1985)
$\mu^- \to e^- \nu_e \bar{\nu}_\mu$	$< 1.2\%$	Freedman, et al. (1993)
$\mu^- \to e^- \gamma$	$<1.2 \times 10^{-11}$	Brooks, et al. (1999)
$\mu^- \to e^- e^- e^+$	$<1.0 \times 10^{-12}$	Bellgardt, et al. (1988)
$\mu^- \to e^- \gamma \gamma$	$<7.2 \times 10^{-11}$	Bolton, et al. (1988)

Table 1.1: Muon decay modes with the corresponding branching ratios.



(a) Feynman diagram for the decay $\mu \to eee$ on tree level

(b) Feynman diagram for the decay $\mu \to eee$ via SUSY particles

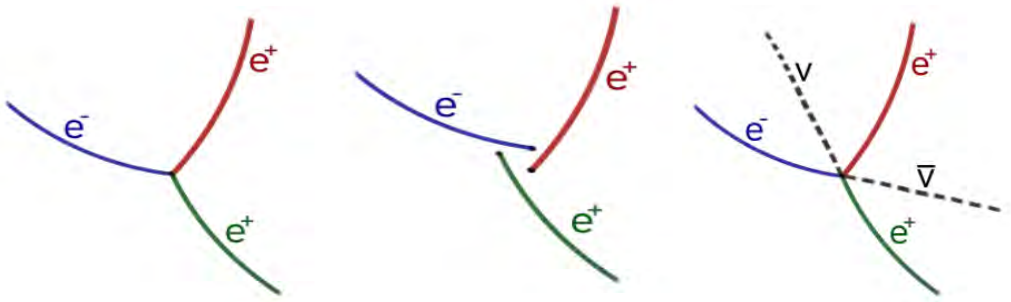
Figure 1.3: Possibilities for the LFV decay of the muon into three electrons in models of physics beyond the Standard Model [60].

the investigation of the process $\mu \to eee$.
The interest to study lepton flavour violating muon decays in order to find new physics or exclude particular models has grown in the recent decades. There are several predictions for the decay $\mu^+ \to e^+ e^+ e^-$, of which only a few are given here as examples.
LFV is explained in some theories by coupling on tree level as shown in figure 1.3a. An example for this is the model with a triplet Higgs field [29]. Here, the coupling with the Higgs triplet generates the neutrino mass and simultaneously induces the LFV process.
Another theory of lepton flavour violating decays is based on loop diagrams. Many such models are based on the proposal of super symmetric (SUSY) particles (see figure) 1.3b [34]. Supersymmetry links fermions with bosons; each particle is allocated to a supersymmetric partner whose spin differs by $\frac{1}{2}$ from that of the SM particle [31]. There are also models in which exotic non-SUSY particles appearing in loop diagrams [8],[6].

1.3 Challenges for the Experiment

1.3.1 Detector Acceptance and Resolution

The acceptance of the Mu3e experiment depends on its geometrical acceptance and momentum coverage. All detector properties must be optimized for a decay at rest



(a) Signal **(b)** Combinatorical background **(c)** Internal conversion

Figure 1.4: Signal and background topologies for the $\mu \to$ eee decay [10].

with three coincident particles.
In the case of a decay where the kinematics are not fully known, the detector acceptance must be as high as possible. To achieve this, the losses that are inevitably present due to the geometry of the detector must be reduced. Because the beam has to enter, no instruments for track reconstruction can be placed at this position. In addition, losses can occur due to non-reconstructed tracks if the number of transversed detector planes is too low [10].
The level of background suppression and thus the success of the experiment depends largely on the momentum resolution of the detector. The condition, for a decay at rest, for the vectorial sum of all momenta of the involved particles is

$$|\bar{p}_{tot}| = |\sum \bar{p}_i| = 0 \tag{1.1}$$

and the total energy has to be equal to the muon mass [10].
The average momentum resolution has to be better than 0.5 MeV to achieve the sensitivity goals of 10^{-16}. This is important for the distinguishability of the decays (see section 1.3.2). The main impact on the resolution of the detector is multiple Coulomb scattering in the detector material. Therefore the detector material must be as thin as possible [10].

1.3.2 Background

The sensitivity of the planned experiment depends strongly on the ability to reduce backgrounds. There are two types of background that are crucial for the Mu3e experiment: radiative decays with internal conversions that lead to an **irreducible background** and the **accidental background** [10].
The most serious background is the process of internal conversion $\mu^+ \to e^+e^+e^-\nu\nu$ with a branching fraction of $3.4 \cdot 10^{-5}$ presented in figure 1.4c. The differentiation against the process $\mu^+ \to e^+e^+e^-$ (figure 1.4a) is only possible by using momentum conservation to reconstruct the energy carried away by the neutrinos [10].
The accidental background or combinatorial background shown in figure 1.4b results from the superposition of processes that produce the same traces as the decay being searched for [10].

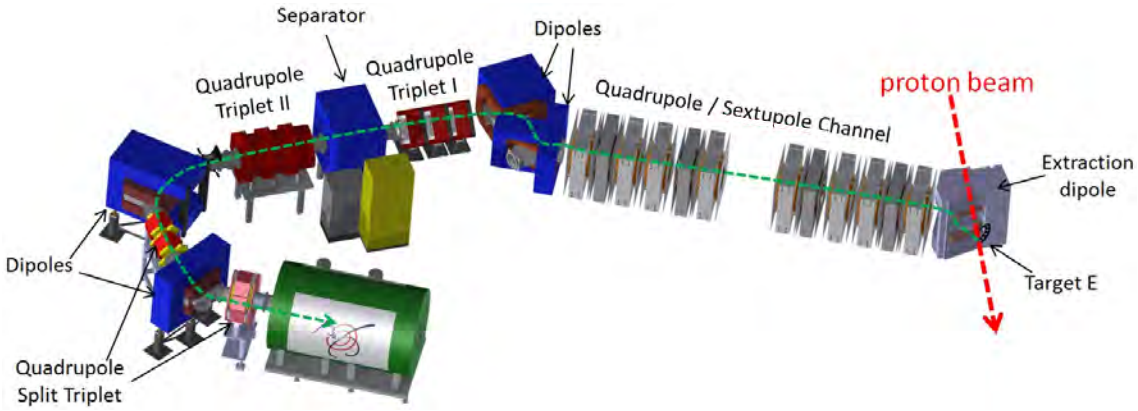


Figure 1.5: CAD model of the πE5 channel and the Mu3e beam line at the Paul Scherer Institute, Switzerland. [60]

1.4 The Experimental Setup

The setup of the Mu3e experiment is planned at the Paul Scherer Institute in Villigen, Switzerland. The experiment will be carried out in two phases. Phase I uses the PSI's high intensity muon beam of the πE5 channel. The Muon beam reaches intensities of $10^7 - 10^8$ muons per second, which is essential to reach the sensitivity goal of $2 \cdot 10^{-15}$. The Mu3e experiment shares the πE5 channel with the MEGII experiment [7]. A model of the Mu3e beam line is shown in figure 1.5. Phase II will use a new high intensity muon beam which is currently being studied at PSI with more than $2 \cdot 10^9$ muons per second. The Mu3e experiment wants to achieve a sensitivity of $\mathrm{B}(\mu \to \mathrm{eee}) \leqslant 10^{-16}$ [1] in this phase. In order to meet this goal, the detector acceptance in phase II has to be improved, which is achieved, for example, by extra tracking stations [10].

1.4.1 The Detector

The entire Mu3e detector is located in a 1 T strong magnetic field. See figure 1.6 for a schematic of the detector. The muons are stopped in a thin target in the middle of the setup. The magnetic field deflects the trajectories of the electrons and positrons. This allows the determination of the electron momentum and charge from the radius of the trajectory and the direction of curvature [10].
The Mu3e detector consists of three detector subsystems. The pixel detector is responsible for an accurate track and vertex reconstruction. Scintillating fibres and scintillating tiles are used for exact timing measurements of the decays [10].

The Mu3e Pixel Detector

The Mu3e pixel tracker consists of High Voltage Monolithic Active Pixel Sensors (HV-MAPS). The central pixel tracker consists of four tracking layers of these HV-MAPS which are called MuPix sensors in the context of the Mu3e experiment. The four layers, arranged as double layers, consist of mechanically robust modules and instrumented ladders are integrated on each module. These ladders form the smallest mechanical unit and are compounds of MuPix sensors which are glued to a

[1] Branching ratio

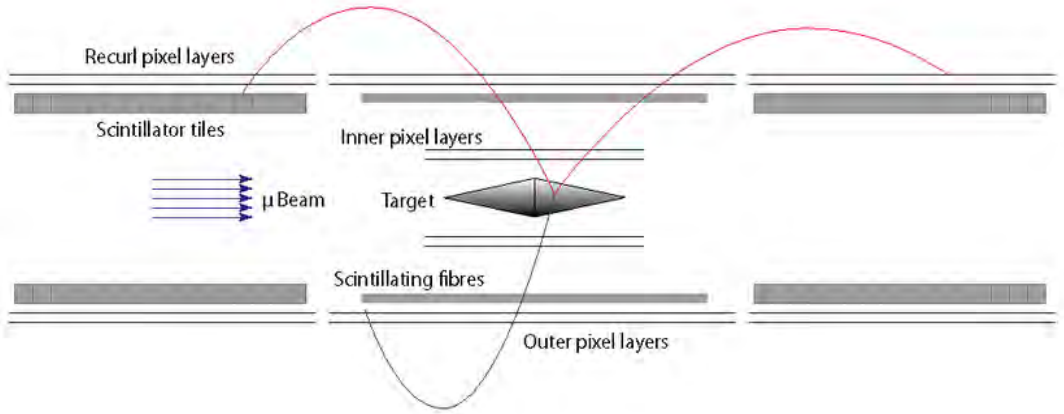


Figure 1.6: Schematic drawing of the Mu3e detector with pixel sensors, scintillating fibres and scintillating tiles [60].

layer	1	2	3	4
number of modules	2	2	6	7
number of ladders	8	10	24	28
# MuPix per ladder	6	6	17	18

Table 1.2: Number of modules, ladders and MuPix sensors per tacking layer.

thin support structure.The support structure is provided by Kapton flex-prints with aluminum traces for the signal and power lines. The number of MuPix sensors per ladder varies in different layers. An overview of this can be found in Table 1.2. In total, the four layers contain 2844 MuPix sensors. The sensors are thinned to 50 μm and thus the material budget is reduced to a radiation length of 1.1 ‰ per layer. To carry away the produced heat of the pixels the detector is cooled with helium gas [32]. The outer pixel sensor layers are extended with two additional detector stations to provide precise momentum measurements in an extended region with the help of recurling electrons and positrons.

High-Voltage Monolithic Active Pixel Sensors

The HV-MAPS technology was developed by Ivan Perić [40]. The sensors are manufactured in a commercial Complementary Metal-Oxide-Semiconductor (CMOS) process, qualified for high voltages up to 120 V.
The layout of an HV-MAPS is illustrated in Figure 1.7. A deep n-doped well is sitting in a p-doped substrate. The sensitive volume of the sensor is defined by the depletion zone created around the n-wells when a bias voltage is applied between the substrate and the wells. Due to the high voltage which can be applied, depletion zones of 10-50 μm thickness are possible and a fast charge collection via drift occurs. Because the rest of the p-substrate is not depleted, the sensor can be thinned down to 50 μm [25]. In the context of Mu3e, as series of HV-MAPS prototypes, the MuPix chips, were developed.

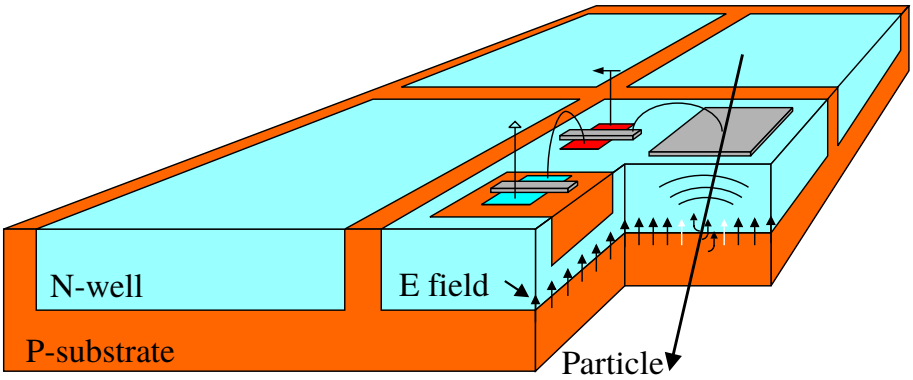


Figure 1.7: Layout of a HV-MAPS [60].

The Mu3e Fibre Detector

A cylindrical time of flight (ToF) detector is planned inside the outer pixel layers. It consists of scintillating fibres (Sci-Fi) with a length of 36 cm and a diameter of 250 μm, see figure 1.9a. The Sci-Fis are joined together in 3-5 layers to form a total of 24 ribbons (see figure 1.9c) [10].
The goal of the ToF system is to precisely measure the arrival time of the particles with a time resolution of 500 ps in order to compare them with hits in the silicon detectors. Thus a reduction of the accidental backgrounds can be achieved. Additionally, the direction of flight and thus the charge can be determined [10].
The read-out system of the fibres consists of Silicon Photomultipliers (SiPM) and the MuTRiG chips. The SiPM arrays are located at the ends of the SciFi and detect the scintillating light produced in the fibres. The SiPMs are connected via flexprints to the MuTRiG PCBs as shown in figure 1.8. The MuTRiG is a 32 channels mixed-signal Silicon Photomultiplier readout ASIC[2]. They are known for high timing precision and high event rate capability [11].

The Mu3e Tile Detector

The second component of the ToF hodoscope is a scintillating tile detector located in the recurl station on the inside of the recurl pixel layer (see figure 1.10). The detector consists of two modules with a diameter of 12 cm and a length of 34 cm. Each module consists of 52 rings and each ring consists of 56 tiles with a geometry of 6.3×6.2×5 mm.
To achieve a fast light response the tiles are made of plastic scintillator material. To effectively identify coincident signals and to suppress combinatoric background a time resolution of below 100 ps is required.
The readout is again performed by SiPMs, which are directly attached on the inside of the tile and connected to the MuTRiG [10].

1.4.2 Power Requirements

The power distribution of the individual detector components has to face several challenges: MuPix sensors and MuTRiG require relatively low voltages between 1 and 3.3 volts and the cables that lead into the detector are relatively long. Therefore,

[2]Application Specific Integrated Circuit

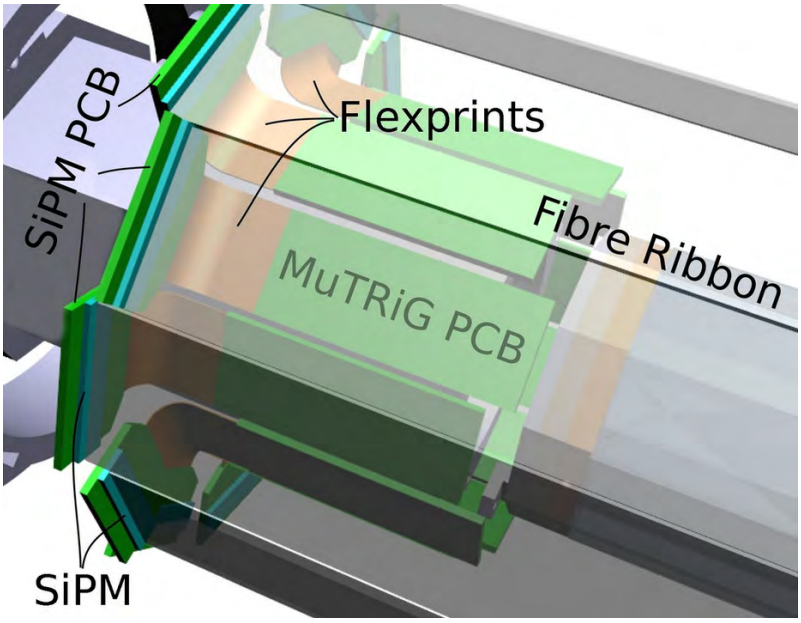
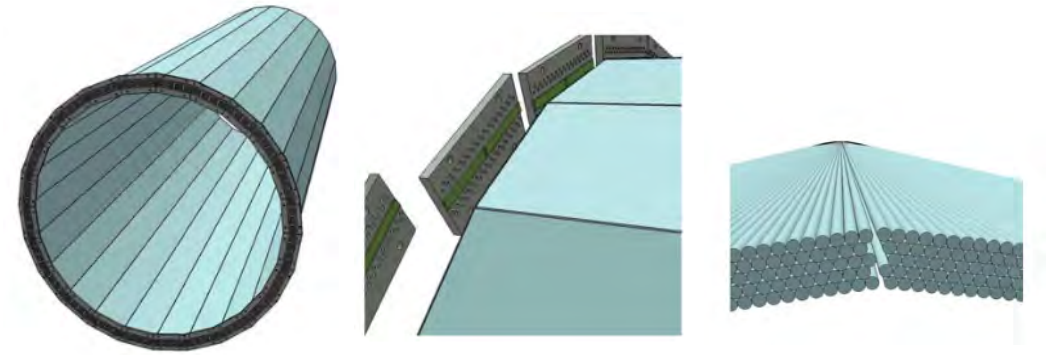


Figure 1.8: CAD model of the fibre read-out system with SiPMs connected via flexprints to the MuTRiG [60].



(a) Overall view of the SciFi ToF detector

(b) SiPM ceramic support structure

(c) SciFi ribbons

Figure 1.9: Drawings of the Mu3e fibre detector [60]

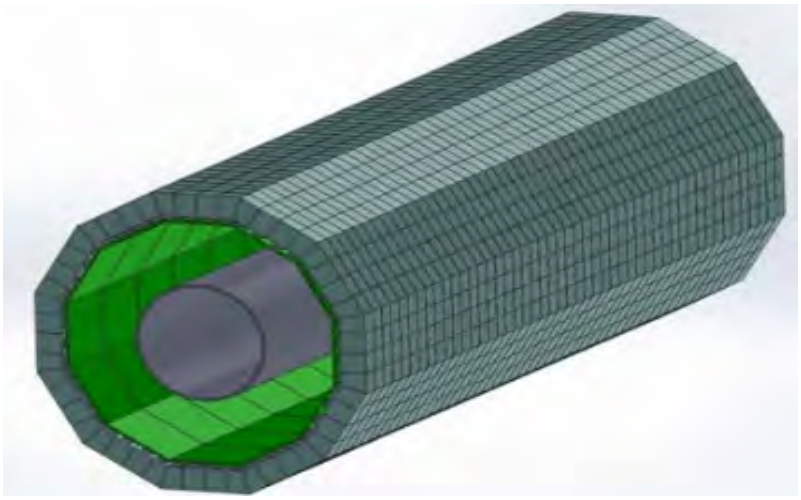


Figure 1.10: Schematic illustration of the Mu3e tile detector module [60].

Detector	ASIC	# partitions	V_{out}	typical current [A]
Pixel				
layer 1	MuPix	4	2.3-2.4	10.3
layer 2	MuPix	4	2.3-2.4	10.3
layer 3	MuPix	3×12	2.4-2.5	21.9
layer 4	MuPix	3×14	2.4-2.5	21.9
Fibre	MuTRiG	12	2.2+	7
Tile	MuTRiG	14	2.2+	9
		14	3.6+	3.1

Table 1.3: Number of power partitions for the different detector components [60].

the losses in the cables would be very large and there would not be enough power to reach the detector. On the one hand, this could be compensated by thicker cables, but this is not possible unlimitedly due to the little room inside the detector and the small material budget. The solution taken for the Mu3e experiment is to increase the voltage to 20 V in combination with the use of DC-DC step-down converters located as close as possible to the detector components. The converters ar located in a 1 T strong magnetic field, whereby certain conditions are linked to the design, and provide a power of 10 kW in total [10].
According to the design of the individual detectors, the power distribution is also segmented into different sections, the so-called power partitions. Each power partition consists of electronic components: one channel of a power supply located in the experimental area supplies the 20V voltage via robust copper cables. Through patch panels in the detector envelope, the power enters the detector. From there, the cables are connected to the DC-DC converters, which are located directly on the beam pipe and serve pixel, fibre and tile detector. Per power partition one DC-DC converter is required. A maximum of 16 boards is mounted in 2×8 **power crates**, each equipped with a controller with slow control and an interlock system. An overview of the distribution of partitions and converters is listed in table 1.3. A total of 126 DC-DC converters is required [10].

Chapter 2

DC-DC Converter

A DC-DC converter is a high-frequency power electronic device that transforms a DC [1] input voltage to a DC output voltage. DC-DC converter circuits consist of usually two switching elements like diodes or transistors and energy storage elements like capacitors or inductors. Closed feedback loops maintain a constant output voltage even when the input voltage and output currents are changing [65].
DC-DC converters usually achieve efficiencies above 90 % and are therefore significantly more efficient than linear regulators. The disadvantages are for example complexity and noise due to the switching action [65].
The output voltage of such an converter can be lower than the input voltage (**Buck Converter**) or vice versa (**Boost Converter**). As Mu3e uses only buck converters, the following chapters only refer to the function of these step-down converters.

2.1 Buck Converters

A buck or step-down converter is a DC to DC converter which converts a not regulated DC voltage from its input (supply) into a regulated DC output voltage (load) while stepping up the current. These regulators derive their voltage regulation from the high-frequency switching of a metal-oxide semiconductor field-effect transistor (MOSFET). The second semiconductor can be a diode or another transistor [65].
DC-DC converters with two power MOSFETs, like in the Mu3e experiment, are called **synchronous buck converters**. This type of buck converter is named after the control method of the two MOSFETs. The switching behaviour of these regulators is synchronised to prevent both transistors from being switched on at the same time, thus preventing short circuits [48]. Only in this way a regulated output voltage can be provided. Therefore a synchronous buck converter circuit has two sections. The first one is the power section which makes the energy conversion. The second one is the control section which tells the switches when to open or close [22].
A basic buck-switching regulator circuit is shown in figure 2.1. The upper MOSFET Q_1 is the high side MOSFET and the lower one Q_2 is the low side MOSFET.

2.1.1 Buck-Switching Regulator Operation

In order to analyse the operating principle of a converter, the system can be divided into two simpler circuits:

[1] DC $\widehat{=}$ direct current

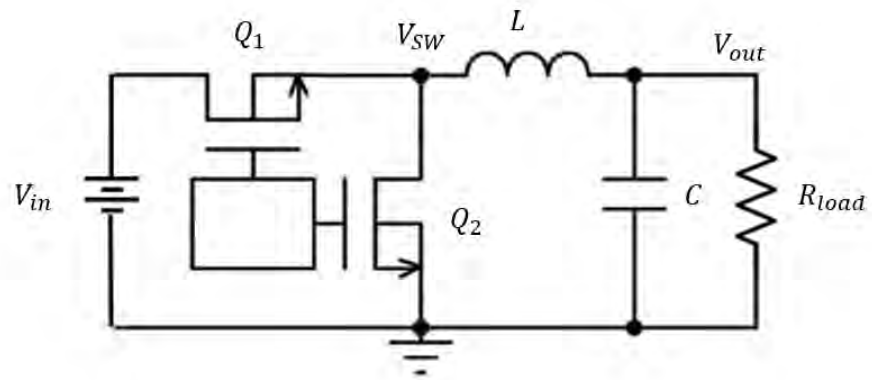


Figure 2.1: Schematic drawing of an DC-DC converter circuit [48].

1. Phase 1: The first MOSFET (Q_1) is on and the second MOSFET (Q_2) is off for a time t_{on} (see figure 2.3a)

2. Phase 2: The first MOSFET is off and the second MOSFET is on for a time t_{off} (see figure 2.3b)

The quotient between duty time t_{on} and period duration $T = t_{on} + t_{off}$ is called duty cycle [65]:

$$D = \frac{t_{on}}{T} \tag{2.1}$$

At the beginning when Q_1 is off the current in the circuit is zero. When Q_1 turns on for the first time and Q_2 is off, the current is flowing from the input through the load as in the red path shown in figure 2.3a. The current through the coil therefore increases linearly and a voltage of

$$V_L = V_{in} - V_o \tag{2.2}$$

is applied across the terminals of the coil [22].
The load asks for a certain amount of current which is provided by the coil. In the coil, however, more current is secured than is required by the load. The excess current is then stored in the capacitor.
In phase 2, Q_1 turns off and Q_2 turns on and so the voltage source is disconnected from the circuit. The current continues to flow through the coil in the same direction as in the red path in figure 2.3b. The current in the inductor decreases linearly and the voltage is now equal to [22]

$$V_L = -V_o \tag{2.3}$$

In this phase, the current from the coil is no longer sufficient. However, the current deficit can be compensated by the capacitor C. A high C-value ensures that the charge difference on the capacitor produces only a small voltage ripple.
The most important waveforms within a synchronous buck converter are shown in figure 2.2. Above the voltage behaviour of the two transistors can be seen. The transistor Q_1 is on when Q_2 is off and vice versa. The amplitude depends on the control unit of the converter and is called V_{drive}. The voltage on the switching node V_{SW} is also a rectangular voltage with an amplitude depending on the input voltage and the same switching behaviour as the MOSFET Q_1. V_{SW} is then smoothed by the inductor and the capacitor to produce a regulated output voltage. Coil

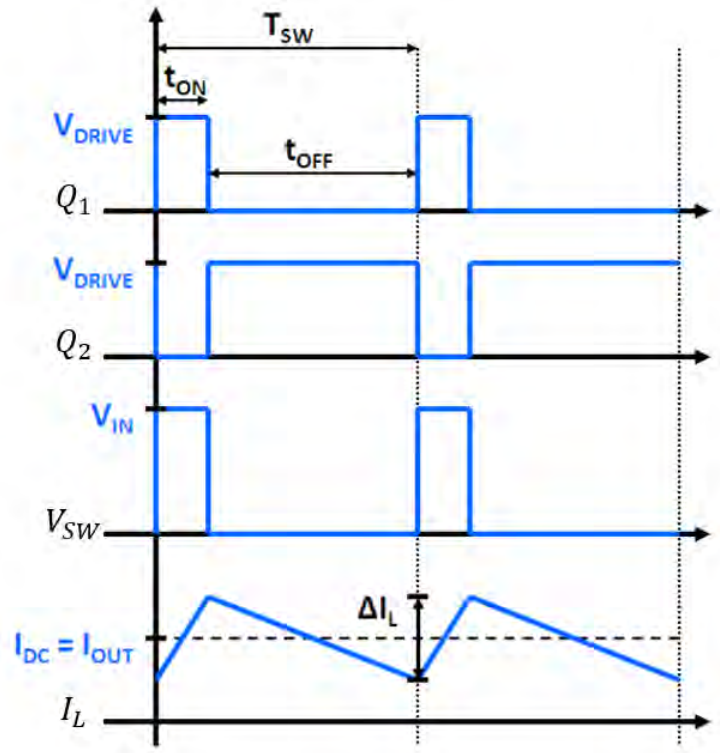
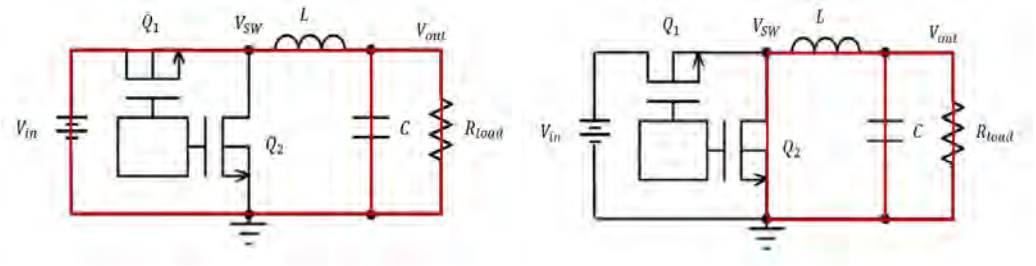


Figure 2.2: Most important waveforms od a buck converter [48].



(a) Circuit t_{on}: the upper switch is conducting. $t = (0, t_{on})$

(b) Circuit t_{off}: the lower switch is conducting. $t = (t_{on}, T)$

Figure 2.3: Current path in the two subcircuits of the DC-DC converter.

and capacitor thus build a low-pass filter of second order. Effectively, the down-conversion is achieved by filtering the direct current (DC) out of the square wave voltage. This arithmetic mean value can be adjusted by the duty cycle. The inductor current can be seen at the bottom. The change in the coil current ΔI_L is called peak-to-peak inductor current [48].
In this operation mode the inductor current never falls to zero so the circuit is always operating in the **continuous mode** [50].
If the amount of energy required by the load is too small, a threshold is reached where the inductor current reaches zero and the **discontinuous mode** is entered. In this case ringing can occur because the inductor resonates due to the high impedance at the junction of the two switches. The ringing can produce unacceptable levels of electromagnetic interference (EMI), thus this condition must be avoided if possible. Otherwise the ringing has to be reduced by damping with for a suitable filter [50].

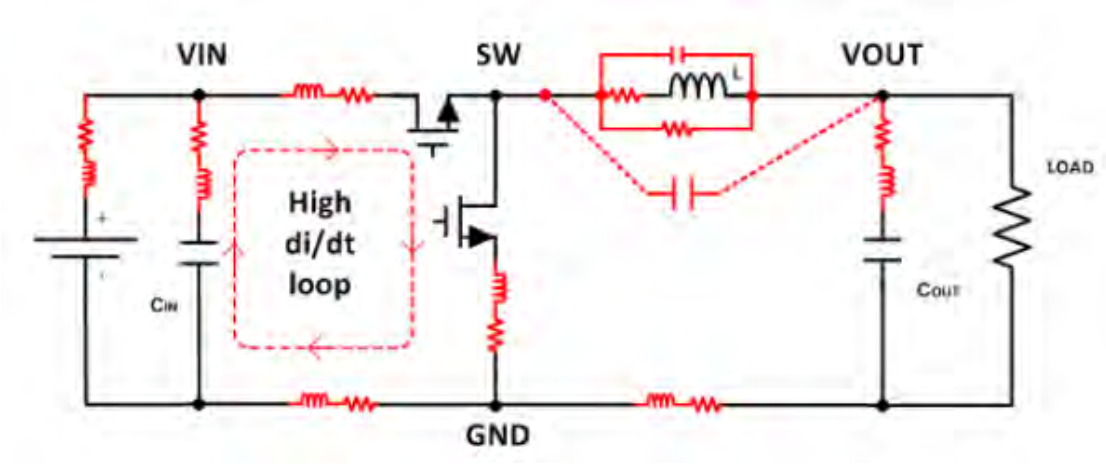


Figure 2.4: Realistic buck converter with parasitic elements; "free" components in red [28].

2.1.2 Noise in Switching Buck Converters

Noise must be taken into account in the realisation of all electronic circuits.
Figure 2.5 shows an example measurement for the AC coupled output voltage of a DC-DC converter. There are essentially three noise elements that can couple to the output signal: the high frequency (HF) noise, subdivided into HIGH-side and LOW-side HF noise and the low frequency (LF) ripple [28].
What always has to be considered in the design of a switching power supply are parasitic components. Every element in an electrical network always has a component that is not desirable for its intended purpose. For example, a capacitor always has unwanted electrical elements of equivalent series resistance (ESR) and equivalent series inductance (ESL). The same applies to inductors [28]. A DC-DC converter circuit with its parasitic components is shown in figure 2.4. The parasitic components can cause effects through which noise arises or is amplified within a buck converter. Parasitic elements must therefore always be taken into consideration and a careful selection of the used components and their properties is essential for an accurate converter design.

High Frequency Noise

The main cause for the development of HF noise is the influence of inductances and current loops on the switching behaviour of applications. When current flows in a loop, a magnetic field is generated. If changes occur in the current, the magnetic field also changes and an inductive voltage V_L is produced. With the help of Faraday's law V_L can be determined [62]:

$$V_L = -\frac{d\varphi}{dt} = -L\frac{di}{dt}, \tag{2.4}$$

$$\varphi = \int_A B \cdot dA = -L \cdot I \tag{2.5}$$

It becomes clear that L strongly depends on the geometry of the current loop. This means that even if the change in current (di/dt) is stable, the inductive voltage V_L increases due to a higher inductance coming from a larger loop area [62].

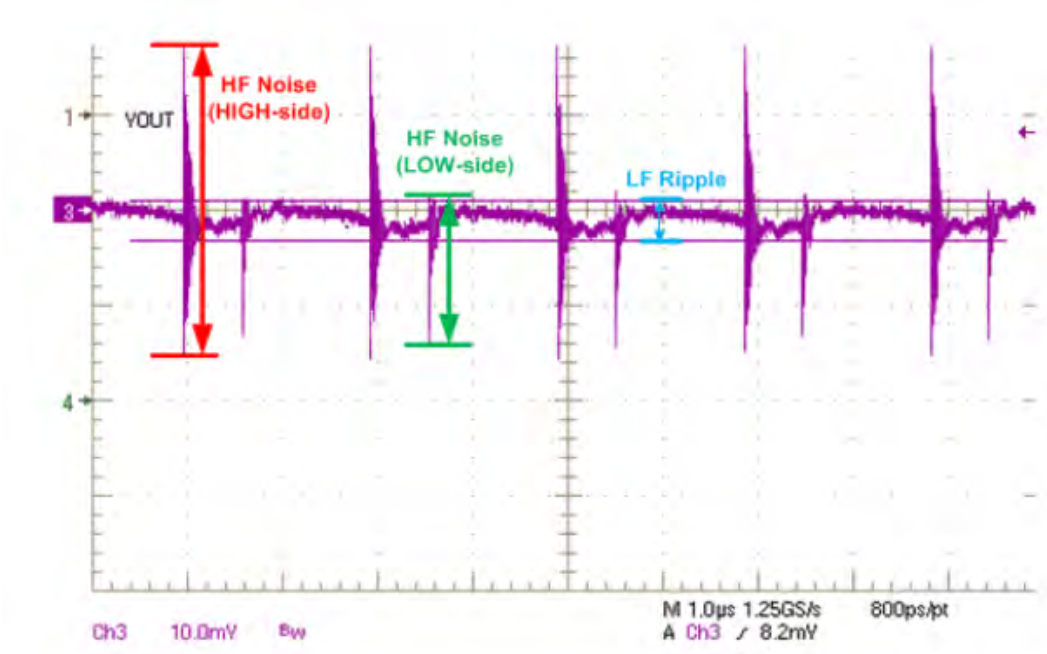


Figure 2.5: Noise contributions to a buck converter output signal. The noise can be divided into two contributions: high frequency (HF) noise and the low frequency (LF) ripple [28].

It follows that the area of the high di/dt loop spanned by the input capacitor and the power MOSFETs must be kept as small as possible to minimize noise. Due to the alternating switching of the transistors, high frequency noise can pollute the output voltage. The noise can be amplified by the following parasitic elements and can be coupled and propagated onto the output voltage. Again, the use of an LC filter can help to suppress the noise [28].

Low Frequency Ripple

The LF ripple is caused by a mixture of the inductor ripple current and output capacitor impedance. In particular, C_{out} represents a critical component primarily through the influence of its parasitic components, such as ESL and ESR, and electrostatic capacitance (C). As already described in section 2.1.1, triangular inductor current is generated by switching the MOSFETs. As shown in figure 2.6, the average current (DC component) of the inducer flows to the output. The triangular (AC) component, however, flows through the output capacitor. The voltages caused by this triangular capacitor current have different waveforms, depending upon ESL, ESR and the capacitance components (C) (see figure 2.7). A triangular wave voltage is generated by the ESR component. ESL creates a square wave and, based on its capacitance, a time constant is acquired. The capacitor current is thus converted into a composition of these three components [44]. Figure 2.8 shows an example of an output ripple waveform of a buck converter. The sharp rise is a consequence of the ESL and the following slight increase is caused by the ESR and C component. Together, this results in the height of the output ripple voltage. The ESL component therefore has a particularly high proportion in the ripple voltage [44]. In order to keep the LF ripple low, special emphasis must be placed on the selection of the

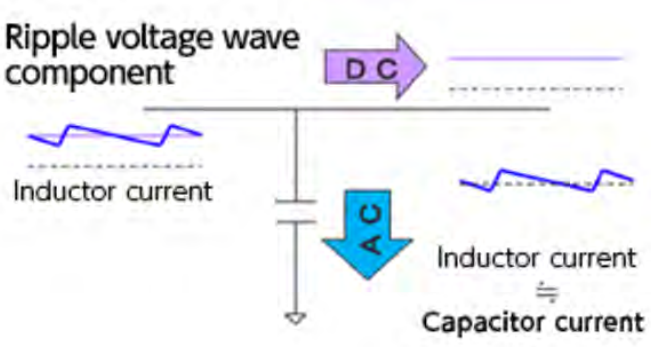


Figure 2.6: Flow of the inductor current through C_{out} and into the output [44].

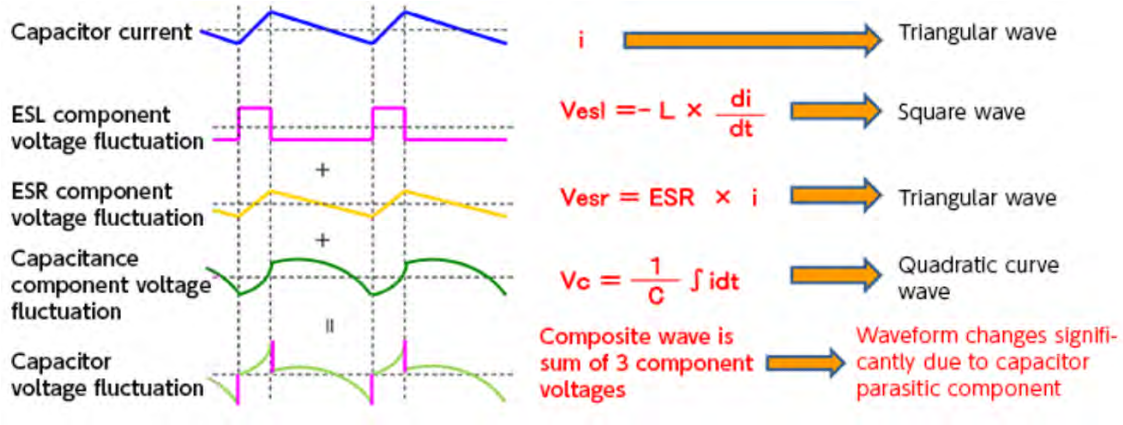


Figure 2.7: Capacitor voltage fluctuations due to its parasitic components [44].

ESL and ESR values of the output capacitors. If the reduction of the ESR portion is not possible due to technical limitations, for example the output capacitor can be divided into several smaller capacitors as this reduces the ESR [42]. A careful calculation of the inductance is also decisive as the triangular current can be reduced. In addition to the improvements in the individual components, the implementation of an another second stage LC filter can also minimize the LF ripple [28].

2.2 The Mu3e DC-DC Buck Converter

2.2.1 Specifications

The Mu3e DC-DC buck converter is designed to convert an input voltage of $V_{in} = 20\,V$ to an output voltage of $V_{out} = 2.1\,V$ at a load current of $I_{out} = 20\,A$. The whole system is operated at a switching frequency of $f_s = 1\,MHz$. The converter is equipped with an input capacitor of $C_{in} = 61.1\,\mu F$ and an output capacitor of $C_{out} = 394\,\mu F$. The capacitances were distributed to several capacitors to minimize noise as described in section 2.1.2. The inductor of the Mu3e DC-DC converter has a inductance of 550 nH and was calculated such that ΔI_L is about 30 % of the total current. The design offers the possibility to implement an additional LC filter to further improve the output signal.
The individual components of the regulator have to meet very specific requirements due to the external conditions. The DC-DC converters are located inside the detec-

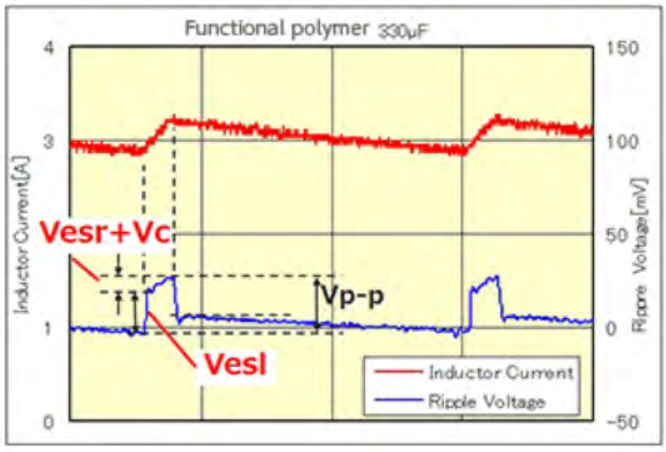


Figure 2.8: Waveform of the triangular inductor current and the output ripple voltage with its contributions V_{ESR}, V_{ESL} and V_C [44].

tor and thus all components should work within the 1 T strong magnetic field.
Another important aspect is the control over the converter. It is necessary to be able to check the parameters of the regulator and change them if necessary. Therefore, components were selected that provide a communication interface to enable the control of the converter. A description of these components and their application can be found in the sections 2.2.2 and 3.2.
An additional limiting factor in the selection of components is the space available in the detector. The space in the Mu3e detector is quite limited, so the converters cannot be arbitrarily large and the selected components must be relatively compact in size. In the following the characteristics of the most important components of the Mu3e DC-DC converters are described.

2.2.2 Components

In the following, the two largest component blocks, the switching and the energy storage elements are explained. In addition to these, capacitors and resistors represent the largest proportion of components. With these, it is important to find designs with the appropriate parameters for the application. For capacitors, for example, it is very important to pay attention to low ESL and ESR values to keep parasitic elements and thus noise as low as possible.

Switching Elements

The CSD86360Q5D

The CSD86360Q5D [52] Synchronous Buck NexFET^{TM} Power Block from Texas Instruments is a highly optimized product made for the use in a synchronous buck topology. These power blocks have been developed for applications requiring high frequency, high current and high efficiency. The CSD86360Q5D consists of two Field Effect Transistors (FET), a control and a synchronisation FET, optimized for switching performance and minimizing losses. The equivalent circuit diagram is shown in figure 2.9.

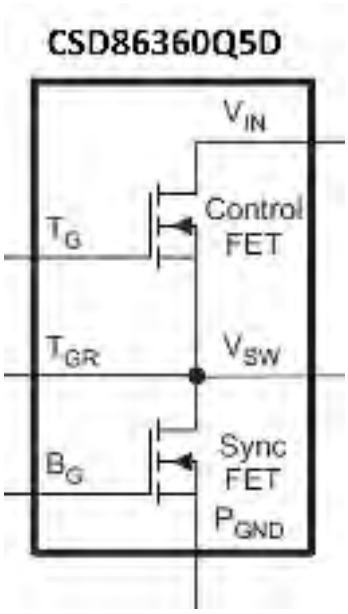


Figure 2.9: Equivalent circuit diagram of the CSD86360Q5D [52].

Another advantage over two discrete semiconductors is the optimized packing technology. This technique minimizes losses due to the fact that parasitic elements between the two FETs are eliminated [52].

The TPS53819A

The TPS53819A [58] is a single-channel, high-efficiency, synchronous buck regulator controller suitable for low output voltage and high current applications. This chip is therefore used to control the power MOSFETs. The device has a input voltage range from 3 V to 28 V, a 5.5 V LDO[2] output and drivers for the two gates [58].
To protect the DC-DC converter from overloading, short circuits and other defects, the device features **Over Voltage Protection** (OVP) and **Over Current Protection** (OCP). The TPS53819A uses the PMBus protocol [64] (see section 3.2 for further informations). This allows, for example, the switching frequency or the operating voltage to be changed.
The compressed size of the device helps to save space on the PCB while the programmability via PMBus simplifies the power supply design.

Energy Storage Element

The energy storage element in the Mu3e DC-DC converters is represented by a copper inductor. The conditions of the Mu3e experiment place special demands on the coils of the voltage regulators. Since the Mu3e experiment will be set up inside a 1 T magnetic field the use of coils with an iron core is impossible. The magnetic field would saturate the inductor cores and thus impair the function of the converter. Because of this, air coils are used, which, as the name suggests, do not have a core. There are two types of air core coils that can be used in the Mu3e experiment: solenoidal and toroidal air coils (see figure 2.10).

[2] A low-dropout (LDO) regulator is a linear DC voltage regulator that is generating stable output voltages with low noise and small packages.

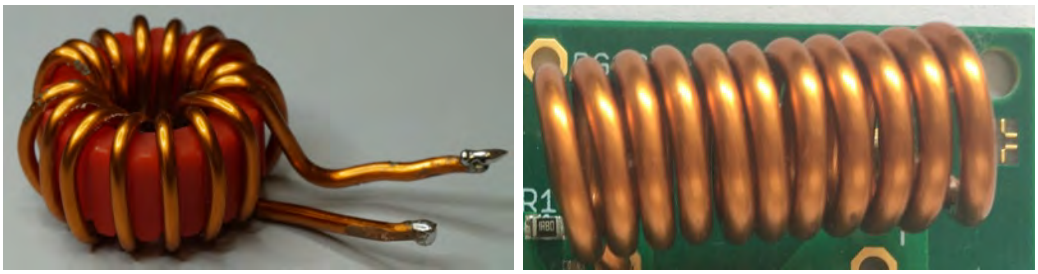


Figure 2.10: Solenoid and toroidal coil for the Mu3e DC-DC converter [26].

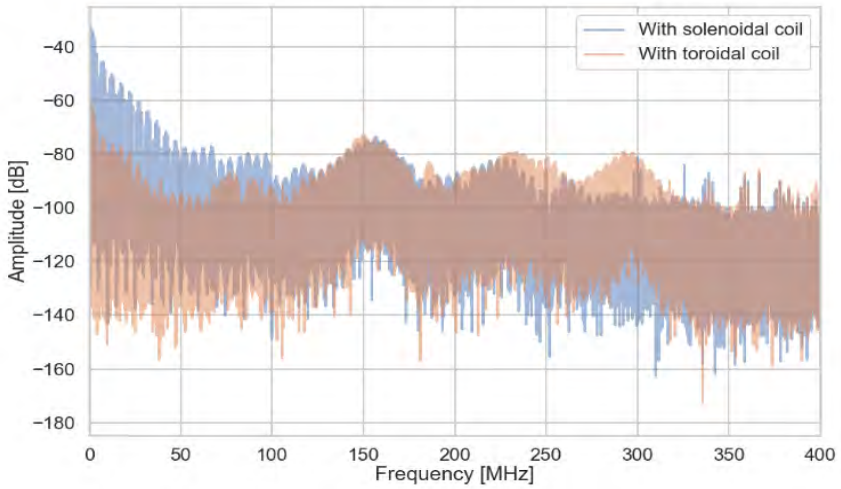


Figure 2.11: Spectrum of the radiated noise of the solenoidal and the toroidal coil [26].

Both types have been tested for efficiency and noise. It is expected that the efficiency of the toroid should be some less than the efficiency of the solenoid because the coil is wound from a longer wire and therefore has a higher DC resistance for the same inductance. However, this effect is relatively small and can be compensated by a slight increase in inductance.
A critical factor in the design of a DC-DC converter is the noise emitted from the coil. This has to be minimized. The radiated noise was measured by means of a magnetic near-field probe at a fixed distance from the coil. The result is shown in figure 2.11. A closer look at the relevant part of the spectrum at low frequencies is shown in figure 2.12. Here it becomes clear that the radiated power of the toroidal coil is reduced by 30dB compared to the cylindrical coil, which corresponds to a factor of 1000. Based on the results, it was decided to use the toroidal coils for the Mu3e experiment.
Further results details can be found in the Bachelor thesis of Moritz Hesping [26].

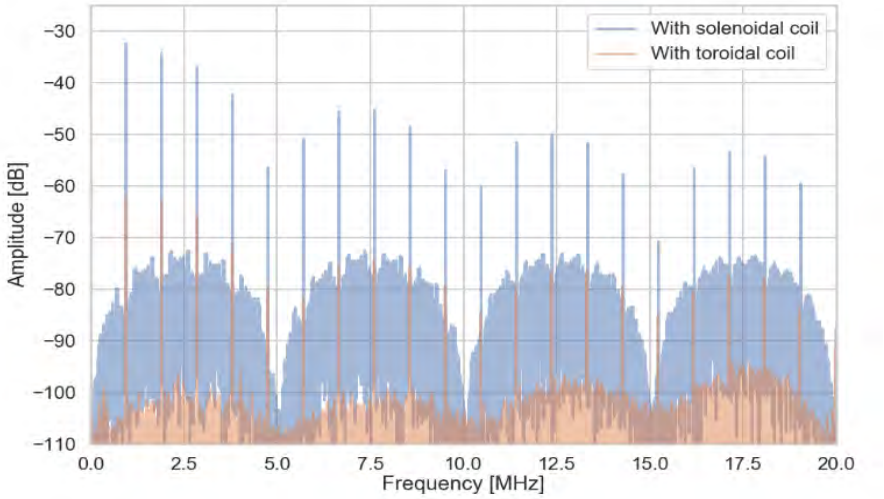


Figure 2.12: Close-up of the spectrum at low frequencies; a reduction of 30 dB of the toroidal coil in contrast to the solenoidal coil can be seen [26].

Chapter 3

Mu3e DC-DC Converter Version 1

The basis for the development of version 1 of the Mu3e DC-DC converter was the TPS53819AEVM-123 evaluation board from Texas Instruments. This evaluation board uses the TPS53819A and the CSD86360Q5D with the two power MOSFETs. With an input range of 8-14 [V], it provides an output voltage of 1.2 V at a load current of up to 25 A. This board was used for familiarization with the function of a DC-DC converter in general and with the function of the individual elements. Based on the experience with the evaluation board, a custom converter was designed that meets the requirements of the Mu3e experiment.
The Mu3e board itself has a size of $45 \times 70 \times 15$ mm and also features the TPS53819A and the CSD86360Q5D. The schematic can be found in the appendix (figures A.1-A.2). This converter was designed to collect experiences. It was made to test how, for example, the PCB layout affects the behaviour of the converter. The possibility was left open to implement and test input and output filters. With this board, also different coil designs were tested. For a better overview of the placement of the components, see figures 3.1 and 3.2.
The task of this thesis was to test version 1 and to develop a new version based on the results.

3.1 Lab Results

In the following section, version 1 of the Mu3e DC-DC converter was tested within the scope of laboratory measurements. For example, the efficiency and stress resistance were checked. The output signal was also tested in terms of quality.

3.1.1 Measurement Setup

The measurement setup includes the following components: The input voltage of 20V was supplied by a TENMA power supply. The output of the capacitor was connected with an adjustable electronic load. The various voltages were either measured with a multimeter or monitored with an oscilloscope. For the measurements with the oscilloscope, a measuring probe was used as shown in figure 3.3. This pigtail probe has the advantage that the ground loop is relatively small. A large loop acts like an antenna and contaminates the actual measurements [28]. This may, for example, have the consequence for the measurement of the output ripple that the results could be misinterpreted. In addition, the position of the pigtail probe

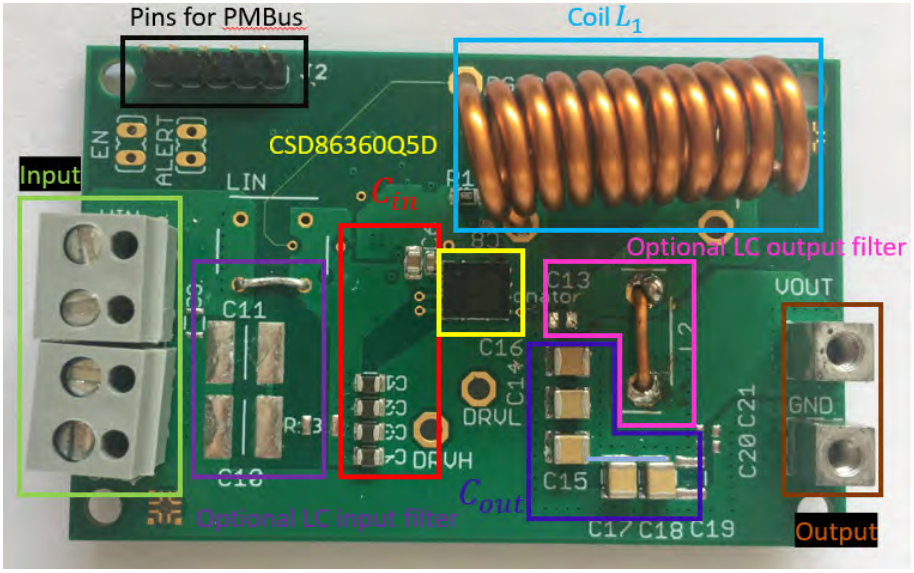


Figure 3.1: Front of the DC-DC converter version 1.

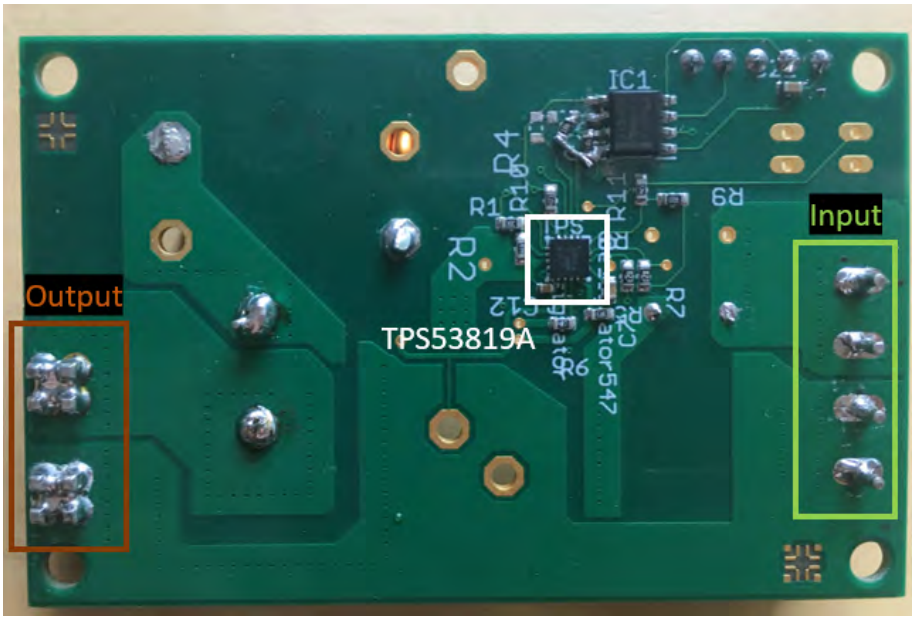


Figure 3.2: Back of the DC-DC converter version 1.

Figure 3.3: Pigtail probe for the oscilloscope for a proper measurement. The short distance of the non coaxial circuit reduces the pickup noise [12].

during the measurement is decisive. It can make a relative large difference whether the output signal is measured on the connectors of the converter or at the input of the load. Also the alignment, i.e. the angle of the probe changes the pickup of the noise. Particular care must therefore be taken during the measurements to ensure that the probe is always held in the same position.

3.1.2 The Efficiency

Switching regulators are generally known for their high efficiencies. The efficiency of a DC-DC converter describes the ratio between the power fed into the converter and the power taken out of the converter and is generally dependent on the respective operating condition. The DC-DC converter's efficiency can be written as

$$\eta = \frac{P_o}{P_{in}} \tag{3.1}$$

$P_{in} = V_{in} \cdot I_{in}$ is the input power and $P_o = V_o \cdot I_o$ is the output power of a buck converter. The efficiency of a converter is influenced by the power losses in its individual components. The following factors are mainly responsible for these losses [3]:

- Switching loss in the MOSFET,
- Operation loss caused by the IC control circuit,
- Conduction loss in the inductor,
- Loss in the capacitor

The efficiency of the Mu3e DC-DC converter was measured for three different input voltages 18 V, 19 V and 20 V. The load current was varied in steps of ±1.5 A around the 10 A. Although the converter was designed for an operating point of 20 A, the voltage in the laboratory measurements was limited to a maximum of 13 A due to the lack of cooling. The result can be seen in figure 3.4. The efficiency at the operational point lies between 87.0 % for an input voltage of 20 V and 87.8 % for an input voltage of 18 V. The efficiency is thus in a very good range.

3.1.3 Stress Test and Behaviour in a Magnetic Field

For a good DC-DC converter not only a faultless function during constant operation is crucial but also a resistance to frequent on and off switching. Therefore a

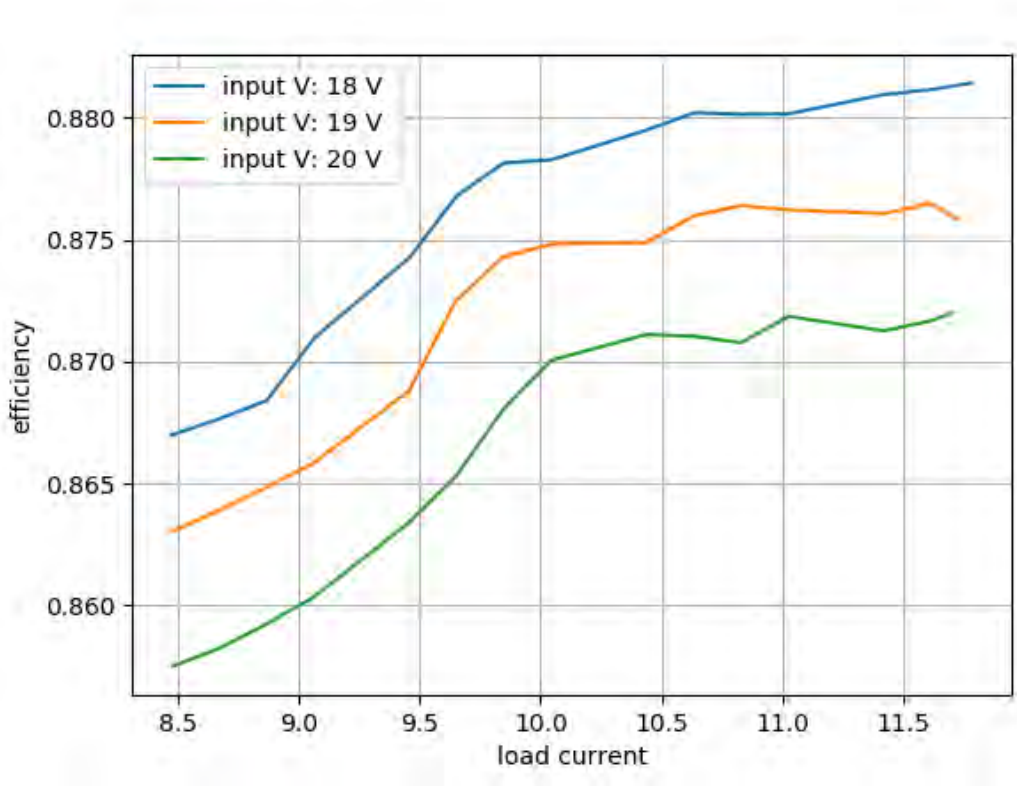


Figure 3.4: Efficiency of the Mu3e DC-DC converter. The efficiency was measured with steps of $\pm 1.5\,\mathrm{A}$ around the operating point of $10\,\mathrm{A}$ for three different input voltages.

stress test was carried out with the help of a Python script: After the converter has been switched on for the first time the efficiency is measured. The converter was then switched off and directly on again and the efficiency is measured again. The duration of the efficiency measurement was 10 seconds. This process was repeated for a total of 24 hours. This creates an efficiency map, shown in figure 3.5, on which the status of the efficiency during the procedure can be read. The average value of the efficiency is 83.65 % with small fluctuations. However, these fluctuations move within a frame of ±0.4 % and are therefore negligible. So it can be said that the efficiency does not change during the stress test.

The same test was used to test the behaviour of the converter in a magnetic field. In principle, all components are suitable for use in a magnetic field, but it is still important to check that the entire board is functioning correctly. Therefore the buck converter was placed in a 0.6 T strong magnetic field, created by a permanent magnet throughout the stress test. As mentioned above, the efficiency remains constant during the test. The magnetic field therefore has no negative influence on this parameter either.

3.1.4 Signal Shape and Output Filter

For the detector components which are supplied by the DC-DC converters it is extremely important that the output signal of the converter is as clean as possible. This means that the output ripple and noise must be sufficiently small. Figure 3.6 shows the output signal of the Mu3e converter at the parameters $V_{in} = 20\,\mathrm{V}$, $V_{out} = 2.1\,\mathrm{V}$, $I_{out} = 5\,\mathrm{A}$ and $f_s = 1\,\mathrm{MHz}$.
Figure 3.7 shows a section of the output signal in which the individual noise contributions discussed in section 2.1.2 are marked. One clearly recognizes the peaks of HF noise. The contributions of the LF ripple due to ESR and capacitance are relatively low. The main contribution occurs on the basis of inductive pick up thus the ESL components.

In conclusion, there is an output ripple height of $\sim 30\,\mathrm{mV}$ in this version of the converter. One requirement, especially of the MuPix sensors, was to reduce the ripple height to a value $\leq 10\,\mathrm{mV}$. Therefore the option to implement an output filter on the board was used. In this case it is a second stage LC filter which is often used due to its simple implementation.
Behind the inductor and capacitor of the regular buck converter circuit (L_1 and C_1) one more coil L_2 is connected in series and one more capacitor C_2 in parallel to the load as presented in figure 3.8. Since the coils are wound by hand, the inductances on the various test boards differ quite a lot by approximately 10-20 %. As a guide value, an inductance of 150 nH is used here for the inductor L_2. C_2 is now the output capacitor and thus receives the value $394\,\mu F$. C_1 is assigned the value $22\,\mu\mathrm{F}$.
Due to the parasitic DC resistance of the inductor and the load current a voltage drop across L_2 can occur. At high load currents like in the Mu3e experiment, the voltage drop can be so big that the output voltage drops below the required value. Therefore the LC filter is placed within the feedback loop so that the control unit can compensate for the loss.

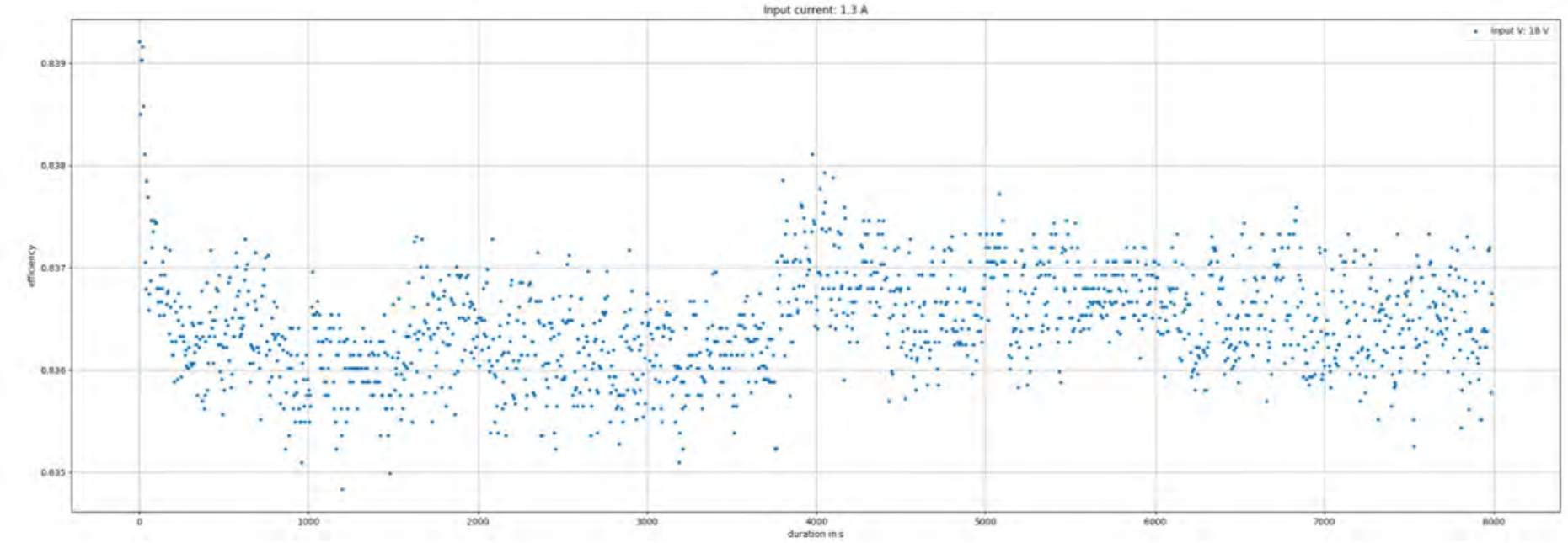


Figure 3.5: Results of the converter stress test. The efficiency was measured after every turn-off turn-on cycle and plotted against time. The measurements were performed in a 0.6 T strong magnetic field.

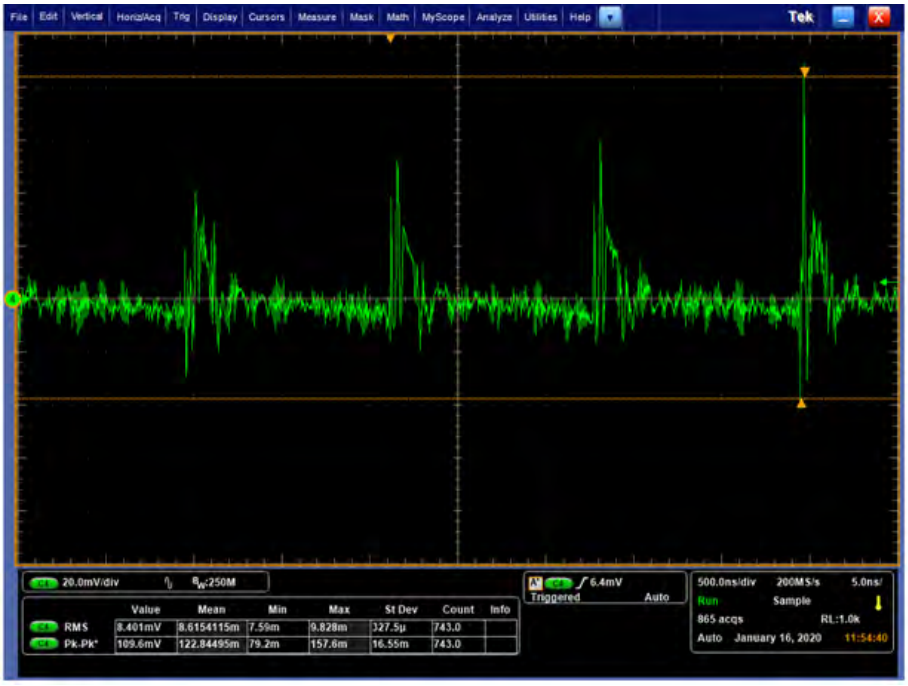


Figure 3.6: Output voltage signal of the Mu3e DC-DC convert without any filtering. Height of the LF ripple: 30 mV.

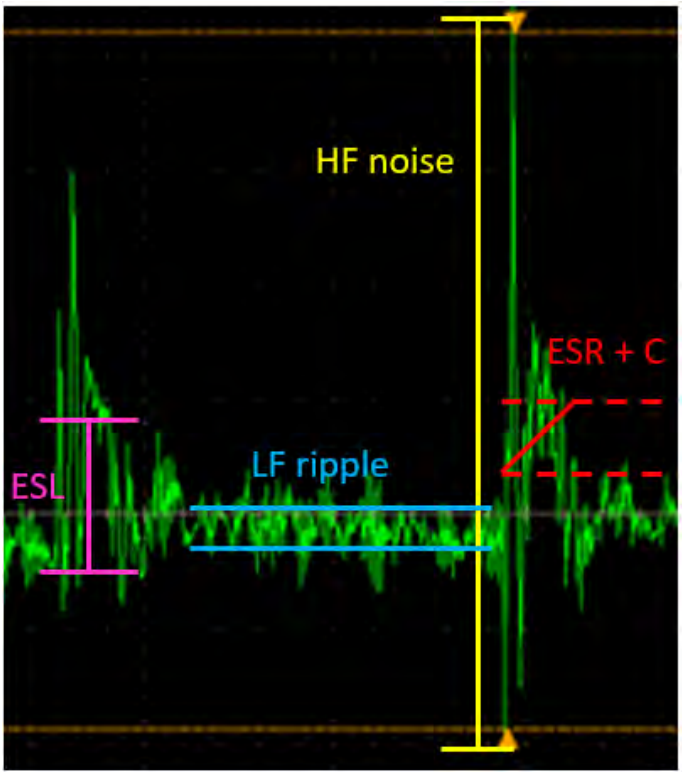


Figure 3.7: Section of the output signal of the DC-DC converter without a filter. The individual noise contributions are marked.

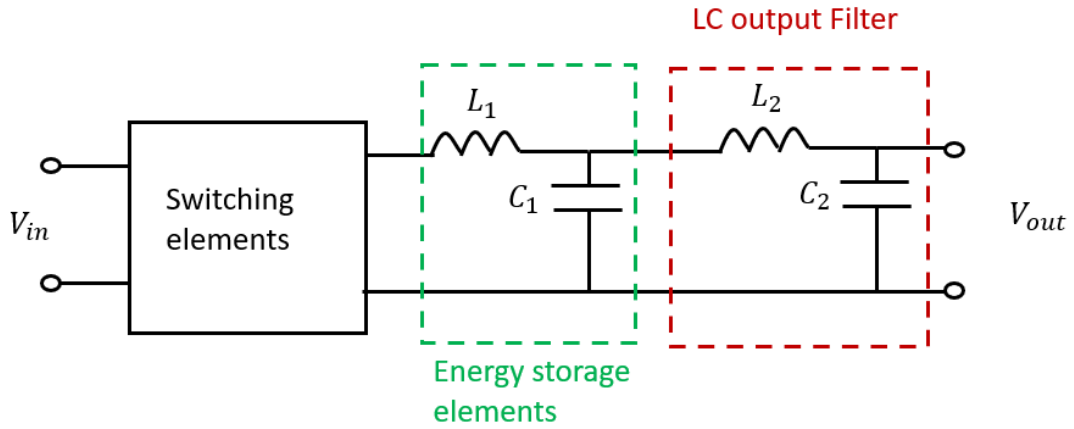


Figure 3.8: Schematic drawing of an DC-DC converter with a LC output filter.

An important parameter of a filter is the cutoff frequency [30]:

$$f_{cut} = \frac{1}{2\pi}\sqrt{\frac{C_1 + C_2}{L_2 C_1 C_2}} \tag{3.2}$$

Frequency noise in the frequency range above this value will be filtered out by the LC filter, all frequencies below can be amplified and pass through the filter. The appropriate selection of the values for L_2 and C_2 and thus the cutoff frequency is decisive for the desired function of the LC filter.
The realization of the LC filter on the Mu3e converter is shown in figure 3.9.
The output signal shape of the Mu3e DC-DC converter with the output filter can be seen in figure 3.10. The contributions of the ESR and C components could be reduced slightly compared to the version without filters, but the contributions of the ESL are still high. In addition to the intrinsic ESL of the components the output inductively picks up from L_1 and the switching nodes. The output ripple height is now at $\sim 15\,\text{mV}$ and could therefore be lowered by 15 mV which corresponds to a reduction by 50 %. The filter does not fully deliver the expected effect and does not reduce the ripple height below the required 10 mV. Reasons for this and a new design of the output filter are described in section 5.3.

3.2 Controlling

3.2.1 PMBus and I^{2}C

PMBus [64] is a two-wire communication protocol based on I^{2}C. It is a further development of the SMBus [19] protocol with the difference that it defines a considerable number of domain-specific commands [64].
I^{2}C [49] stands for Inter-Integrated Circuit and is a simple Master-Slave serial bus. It was invented by Philips Semiconductors (now NXP Semiconductors) in 1982.
The I^{2}C bus uses only a 2-wire connection. A serial data line (SDA) transmits data to and from slaves. A single serial clock (SCL) is used to clock data in or out of slave devices. All devices, master and slaves, are connected only by those two wires. An I^{2}C transmitter is a device that transmits data to the bus. The I2C receiver is

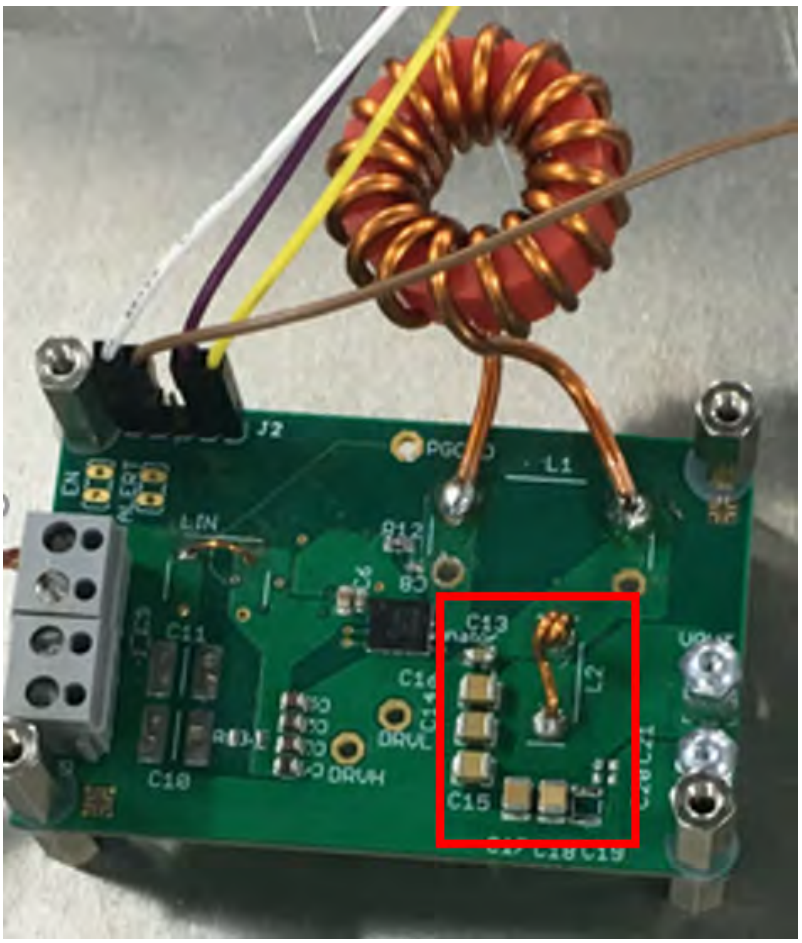


Figure 3.9: Implementation of the output filter on the DC-DC converter board.

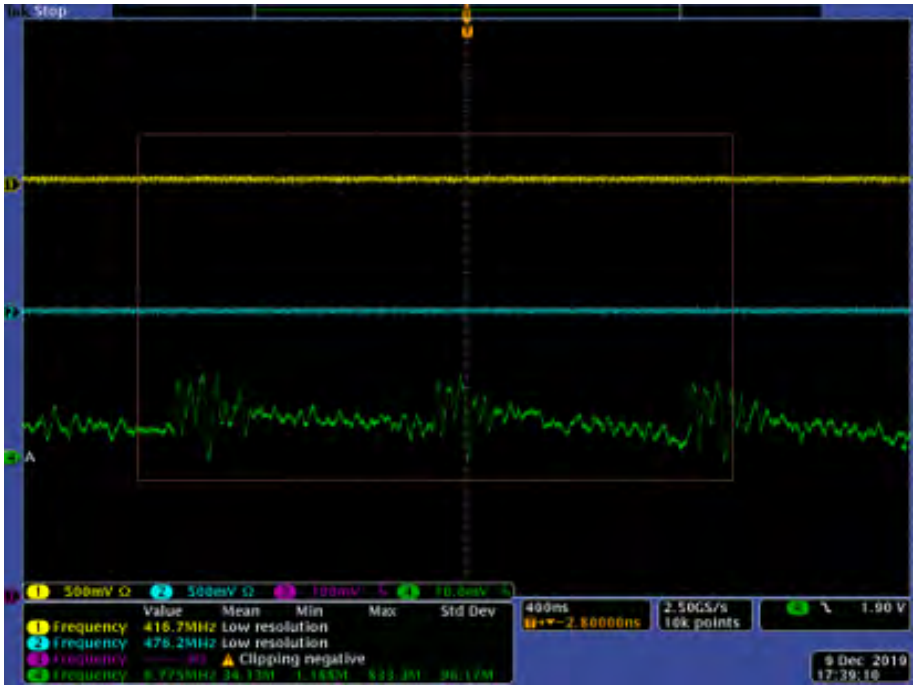


Figure 3.10: Output voltage signal of the Mu3e DC-DC convert with a additional LC output filter. Height of the LF ripple: 15 mV.

Command	Notes
OPERATION	Turn on or off switching converter only
ON_OFF_CONFIG	ON/OFF configuration
CLEAR_FAULTS	Clear all latched status flags
WRITE_PROTECT	Control writing to the PMBus device
STORE_DEFAULT_ALL	Store contents of user- accessible register to non-volatile memory cells
RESTORE_DEFAULT_ALL	Copy contents of non-volatile memory cells to user-accessible registers
STATUS_WORD	PMBus read-only status and flag bits
CUSTOM_REG	(Custom Register 0): Custom register
DELAY_CONTROLE	(Custom Register 1): Power on and power good delay times
MODE_SOFT_START_CONFIG	(Custom Register 2): Mode and soft-start time
FREQUENCY_CONFIG	(Custom Register 3): Switching frequency control
VOUT_ADJUSTMENT	(Custom Register 4): Output voltage adjustment control
VOUT_MARGIN	(Custom Register 5): Output voltage margin levels
UVLO_THRESHOLD	(Custom Register 6): Turn-on input voltage UVLO threshold

Table 3.1: PMBus commands supported by the TPS53819A [58].

the device that receives data on the bus from the transmitter [39].
The component that initiates communication on the bus and generates the SCL clock is called "master". The counterpart to the master is the slave responding to the commands on the bus. Master and slave can be both transmitter and receiver. Each slave has a unique 7-bit or 10-bit address to allow the master to communicate with a specific device. The master does not need a specific address because no commands are sent to it [39].
The signals are bidirectional. The electrical interface is therefore able to read and write on the SDA and SCL pins which are open-collector or open-drain. Three basic modes are supported by the I^2C bus specifications providing different levels of performance. The Standard Mode is the default mode and ranges from 0 up to 100 kbits/sec. The Fast Mode provides a speed upt to 400 kbits/sec and the High Speed mode even up to 3.4 Mbits/sec [39].

3.2.2 PMBus Commands Supported by the TPS53819A

The TPS53819A supports the PMBus protocol. The device has seven internal custom user-accessible 8-bit registers and can operate in the standard mode or fast mode. With this chip it is possible to communicate with up to 16 different devices via PMBus [58].
The TPS53819A supports only the commands shown in table 3.1 However, not all features of the several commands are supported. All other commands are not accepted by the device and can lead to error messages.
In the following only the commands most relevant for our purposes are described.

OPERATION

The OPERATION command is used to turn the regulator output on and off [58]. In addition to the possibility to activate the converter with the help of the PMBus command, there is also a hardware enable pin.

VOUT_ADJUSTMENT

The regulator output voltage can be adjusted via the VOUT_ADJUSTMENT command to e.g. compensate for voltage drops (see section 5.6). The adjustment can

be made in ±0.75% steps, with a total range of ±9% [58].

FREQUENCY_CONFIG

With the FREQUENCY_CONFIG command the switching frequency of the regulator can be varied. The default frequency value is 425 kHz [58].

UVLO_THRESHOLD

The UVLO_THRESHOLD command sets the under voltage lockout protection threshold. The default value is 4.25 V [58].

3.2.3 Technical Implementation in the Laboratory Measurements

The control of the TPS53819A was realized in the laboratory tests with a Raspberry Pi. Linux on the Raspberry Pi supports I^2C with its own subsystem and provides a dedicated I^2C client driver for this purpose [43]. To control the DC-DC converter with a Raspberry Pi, the pins on the board for SCL, SDA, V_{dd} and ground must be connected to the corresponding pins of the Raspberry Pi. This is done with jumper cables as shown in figure 3.11. In a Python script on the Raspberry Pi, the commands from section 3.2.2 are stored and the corresponding parameters can be changed. During the first tests with version 1 of the DC-DC converter a problem concerning the implementation of the PMBus interface occurred. The signal lines are protected by a bidirectional isolator (ISO1540-Q1 [55]) but the data was not getting through. Therefore, two 1.5 kΩ pull up resistors were used to connect SCL and SDA to the supply voltage of the interface on the side of the controller chip.

3.2.4 Controller Crate

Later in the experiment, the converters are to be controlled by a microcontroller. For this purpose, a control crate is designed on which, among other things, this microcontroller is located. One crate will then take over the control for 14-16 DC-DC converters. From here the PMBus interface is controlled and the converter can be switched off separately from each other. The crate also monitors voltages relevant to the operation of the converter (see chapter 5 for more details). In addition, the information from the safety interlock system is also processed on the control board.

3.3 Thermal Behaviour

The power output of the Mu3e converter is at $P_{out} = I_{out} \cdot V_{out} = 13\,A \cdot 2.1\,V = 27.3\,W$ and the power input at $P_{in} = I_{in} \cdot V_{in} = 1.7\,A \cdot 20\,V = 34\,W$ (during the lab measurements). The difference between power input and output (6.7 W) is dissipated in the board, which results in a large heat emission due to the relatively small size of the board. If a flat efficiency curve is assumed for higher currents, the radiated heat can be scaled to approximately 10 W at 20 A and 15 W at 30 A. Some of the components have a temperature limit that, if exceeded, will cause the unit to stop

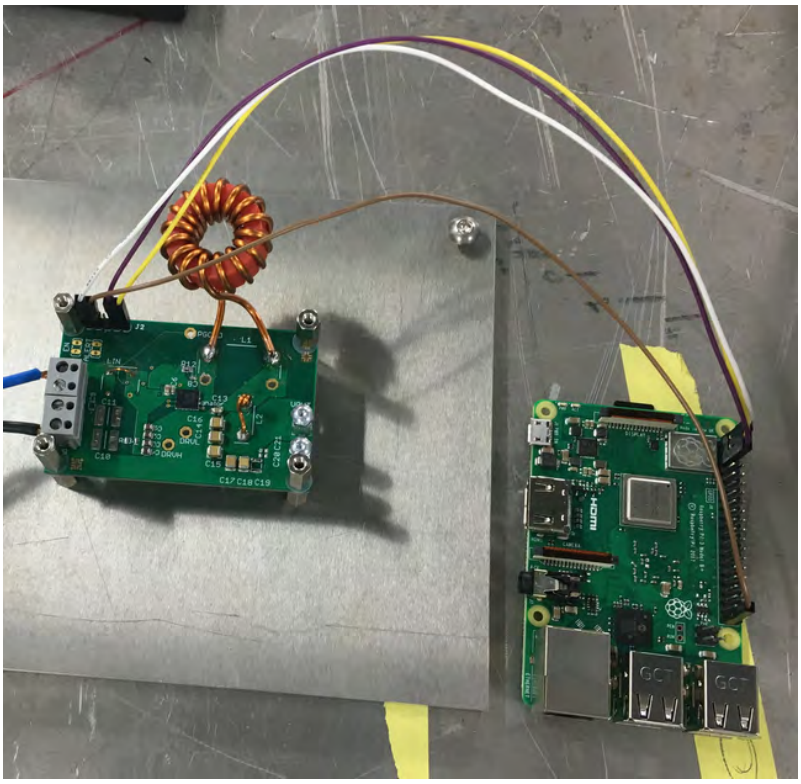


Figure 3.11: DC-DC converter with connection to the Raspberry Pi.

working reliably. Therefore the converter must be cooled later in the experiment. For laboratory tests, this means that the system cannot be operated under full load without being cooled. For the design of an effective cooling system, it is important to know the position of the hottest points and how fast they heat up. To investigate the thermal behaviour of the converter with respect to position of the hotspots and time, images were taken with an infrared camera [27] at different load currents and at different times. The largest heat radiation is expected from the two switching chips and the air coil.
Since different surface radiates heat to a different degrees [15], the PCB was sprayed with a black heat-resistant paint [35] specially produced for such applications to ensure comparable result (see figure 3.12).

3.3.1 Results

For the thermal imaging measurements the converter was operated at an input voltage of 20 V and a switching frequency of 1 MHz. Pictures were taken at three different times, 30 seconds, 5 minutes and 10 minutes after the converter was switched on. This was carried out at load currents of 5.5 A, 10 A and 13 A.
In the following, the results are presented as an example for I=10 A. All other results can be found in the appendix B.
When looking at the hot spots on the PCB, first of all a striking point is noticed on the front, which is by far the hottest (see figure 3.13). As expected, this point is the chip with the two integrated power MOSFETs (For a better orientation on the board see figures 3.1 and 3.2) . Due to the high load current, the air coil also develops a noticeable heat due to the ohmic losses. On the back side in figure 3.14, the control

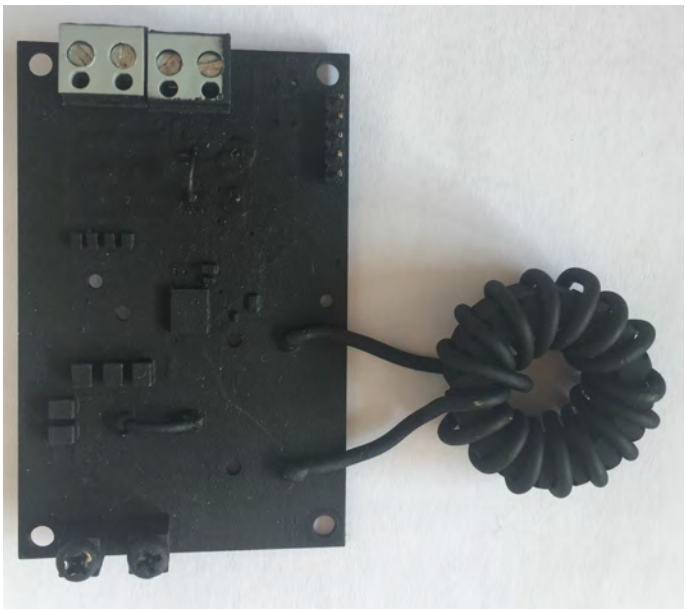
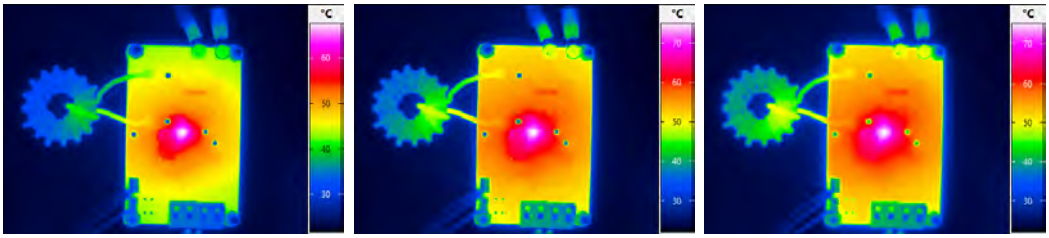


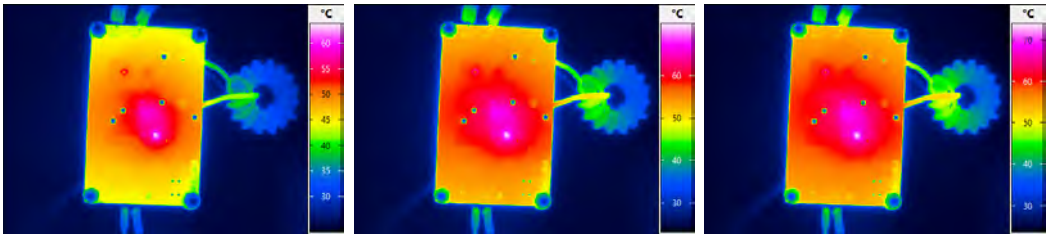
Figure 3.12: DC-DC board sprayed with an infrared paint.

chip for the two transistors is the element with the greatest heat radiation. On this side of the PCB another phenomenon becomes visible, but only with a load current of 13 A. In figure 3.15 another hot spot is visible after 10 minutes. It is coming from the transistor chip on the front. This is connected by thermal vias to the back of the PCB in order to be able to dissipate the heat through here. A thermal via is build by a penetrating hole in the PCB. A copper foil then connects the top and bottom surface of the board. This increases volume and area available for heat dissipation and radiation.
Figure 3.13 clearly shows that heat generation is relatively fast. After only 30 seconds, a temperature of 68 °C is reached. After 5 minutes the temperature has increased by another 5 °C. Between the measuring times of 5 and 10 minutes there is hardly any difference in temperature. The same applies to the back of the PCB (see figure 3.14). The temperature rises very quickly into the high 60's and reaches a maximum temperature of about 75 °C. The propagation of heat in the PCB that emanates from the chips also hardly changes after reaching the maximum temperature. It can be said that the temperature on the PCB increases very quickly and the heat generation is completed within about 1 minute. Cooling of the converter must therefore be guaranteed from the outside. It is planned to use water cooling for this purpose. A more detailed description of the planned cooling system can be found in section 5.10.



(a) After 30 seconds. **(b)** After 5 minutes. **(c)** After 10 minutes.

Figure 3.13: Infrared images of the front of the converter board running at $I_{load} = 10\,A$.



(a) After 30 seconds. **(b)** After 5 minutes. **(c)** After 10 minutes.

Figure 3.14: Infrared images of the back side of the converter board running at $I_{load} = 10\,A$.

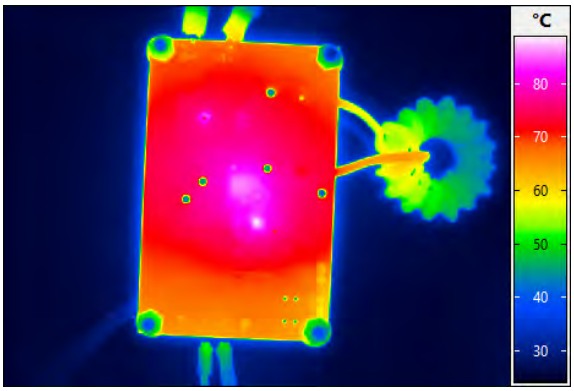


Figure 3.15: Image of the backside after 10 minutes at $I_{load} = 13\,A$. A second hot spot becomes visible due to the transistor chip of the front which is connected with thermal vias to the back.

Chapter 4

Test Beam

The Mu3e DC-DC converters version 1 were tested as power supply for the MuPix8 [5] sensors in cooperation with the University of Heidelberg. These tests were carried out as part of a test beam at DESY [14]. In preparation for the test beam, the behaviour of the MuPix8 sensor was investigated in laboratory studies.
The power lines of the DC-DC Converter were connected directly to the sensors and the MuPix8 motherboard was modified such that no active filter components were present on the module to bring the setup as close as possible to the final Mu3e conditions.

4.1 Setup

The following section describes the setup for laboratory studies and in large parts also for the test beam measurements. The changes for the test beam are described in section 4.3.
The DC-DC converters were supplied with the input voltage of 20 V by a HAMEG power supply. The sensor has 3 input voltages, VDD, VDDA and VSSA, which is why the output signal of the DC-DC converter has been split. VDD and VDDA were supplied directly with the output of the converter and require a voltage of 1.9 V. The output voltage of the converter was therefore adjusted using a Raspberry Pi and the PMBus interface. The basic voltage for VSSA is 1.0 V and was generated by a voltage divider. In the final Mu3e experiment, the sensors are supposed to generate the different voltages on the chip, which means that only one supply channel is required [61].
In addition, an electronic load was connected to the DC-DC converter in parallel to the sensors. This was necessary because the converters were designed to supply fully equipped detector modules. The load generated by a single sensor is not sufficient to ensure a stable functioning of the converter. Therefore, an additional load current of 5 A was created to stabilize the system.

4.2 Lab Studies

In the laboratory studies, the behaviour of the MuPix8 sensors in terms of signal strength and the reliability of data transmission measured by the 8b10b error counter, was studied. Three different powering schemes were compared to check if

the DC-DC converter has a negative effect on the performance of the sensor:

1. Powering with HAMEG supply; standard motherboard (capacitive filters)
2. Powering with HAMEG supply; no-filter motherboard
3. Powering with DC-DC converter; no-filter motherboard

The height of the in-pixel amplifier output (AmpOut), which gives information about the signal strength, was determined and compared for injection signals and a ^{55}Fe source. The results can be seen in table 4.1.

Configuration	AmpOut (Inj.)	AmpOut (^{55}Fe)
1	(188 ± 6) mV	(100 ± 14) mV
2	(164 ± 7) mV	(83 ± 8) mV
3	(171 ± 8) mV	(95 ± 11) mV

Table 4.1: AmpOut for injection signals and ^{55}Fe source [61].

The results show only small differences between the individual powering schemes. From this it can be concluded that powering the MuPix8 sensor with a DC-DC converter has no significant influence on the signal strength and thus on the signal performance. Also with regard to data transmission no 8b10b errors could be found. If the DC-DC converter negatively affects the quality of the data transmission, i. e. if there were a significant ripple on the data output of the sensor, this would be noticeable in the 8b10b error counter. Since the MuPix8 sensor could also run at low thresholds during the laboratory studies a high degree of efficiency can be expected when using a DC-DC converter for powering a MuPix8 sensor.

4.3 Test Beam Measurements and Results

Efficiency and noise rate of the MuPix8 sensor powered by a DC-DC converter has been measured during the "December 2019 test beam campaign" at DESY, where a 4 GeV strong electron beam was used for the measurements. On the basis of the laboratory studies carried out previously, a high efficiency was expected.
The setup was essentially identical with that from the laboratory studies. The MuPix8 sensor supplied with the DC-DC converter was placed between 3 reference layers in a MuPix telescope [36] consisting of MuPix8 sensors on regular motherboards and two scintillating tiles for timing (see figure 4.2. DC-DC converter and Raspberry Pi were placed about 1 m away on a table next to the stage with the telescope as shown in figure 4.1. The distribution board and voltage divider were attached to the telescope support structure (see figure 4.3). The voltage level of the converter was monitored throughout the measurements by a webcam directed at an oscilloscope.
In order to determine the efficiency and the noise level, threshold scans were performed [61]. If a signal is detected in a pixel and this signal is above a certain threshold voltage, then the hit is registered. This means that the lower the threshold, the higher the efficiency, as less relevant signals are discarded. But a lower threshold also means that the system reaches a higher noise level. One scan was performed with a DC-DC converter without an additional LC filter and one scan

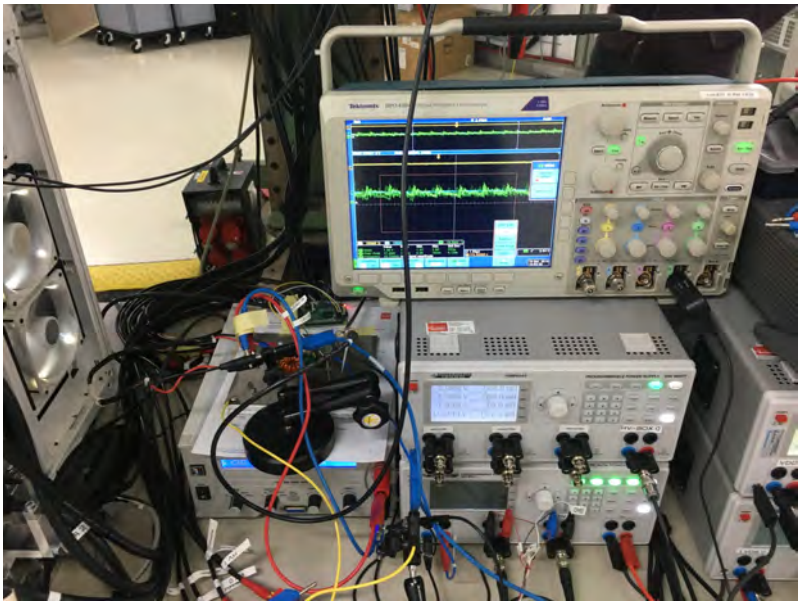


Figure 4.1: DC-DC converter and Raspberry Pi were placed on a table text to the stage with the MuPix8 telescope. HAMEG power supply, electrical load and oscilloscope for monitoring were located on the table too.

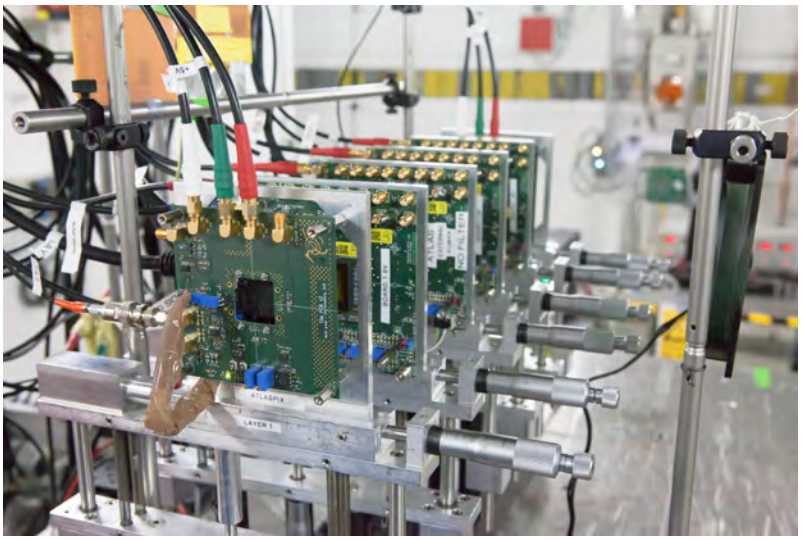


Figure 4.2: The MuPix8 telescope: one scintillating tile at front and back for timing; 4 modules with MuPix8 sensors, the second is powered by the DC-DC converter [61].

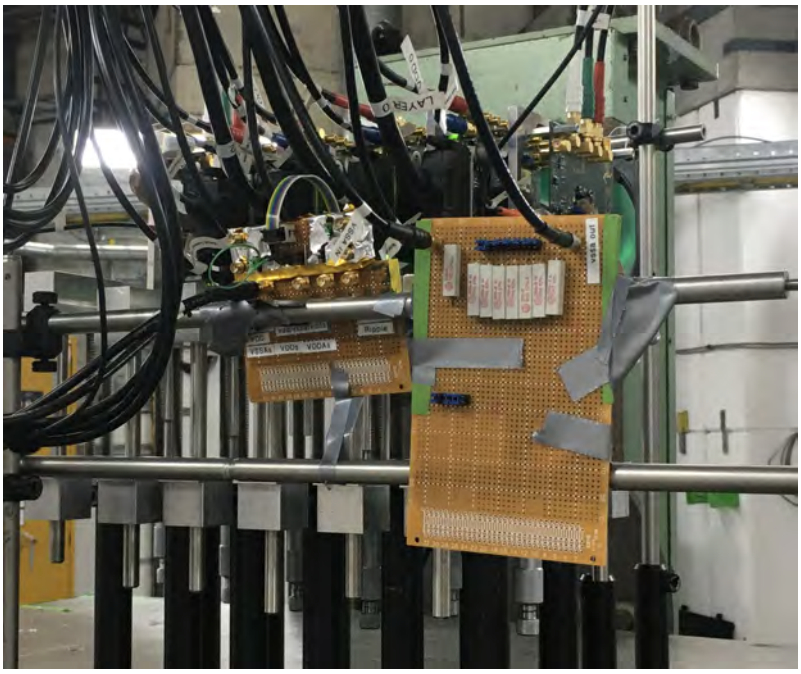
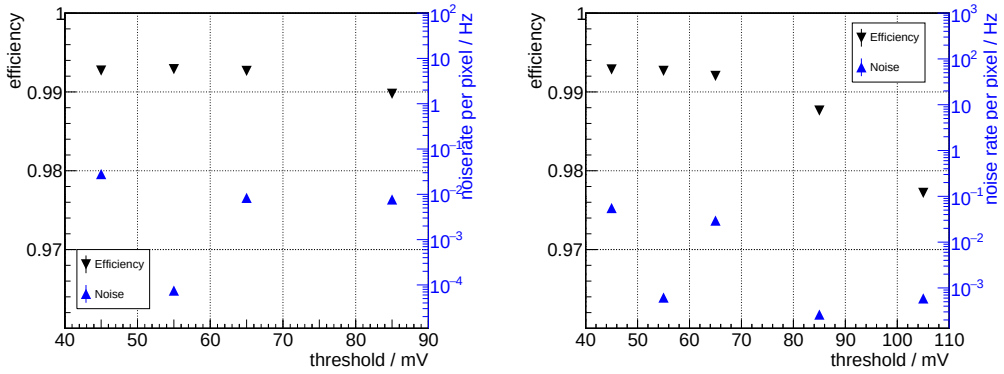


Figure 4.3: Distribution board (left) and voltage divider (right) were mounted to the telescope support structure.

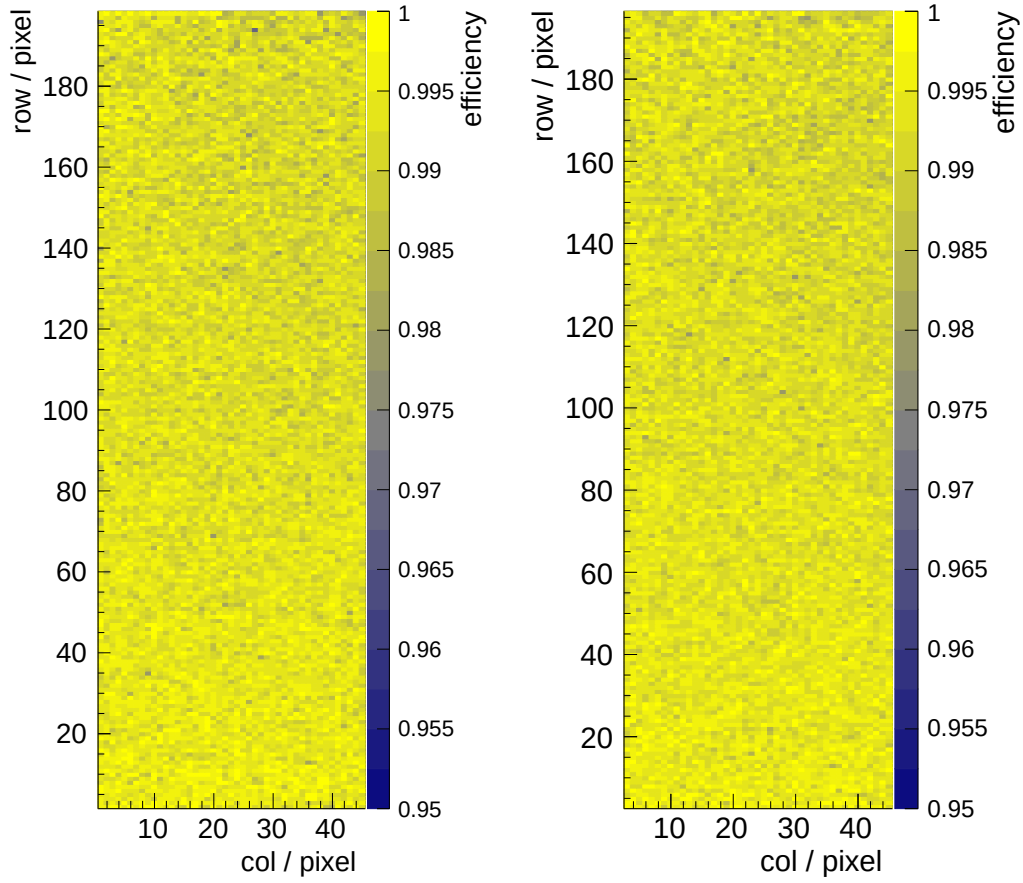
with a converter with filter. Due to the time restriction, more measurements could not be carried out, which is why statistics and number of measurement points are low.
The threshold scans are shown in figure 4.4. For low thresholds, the overall efficiency is 99.3 %. The MuPix8 sensor therefore operates highly efficient when powered by a DC-DC converter. Also in the efficiency maps created for a very low threshold of 45 mV no gradients or patterns could be observed (see figure 4.5).The noise rate per pixel, also shown in figure 4.4, is always below the required value of ≤ 1 Hz which, however, should be considered with caution in view of the low level of statistics [61]. This holds for both DC-DC converters: the one with additional LC filter and also to the converter without a filter. Thus, no difference in the behaviour of the MuPix8 sensor by powering with different voltage ripple heights could be detected.
The results are an important step in the development of the Mu3e DC-DC converter and shows that it is on a good way. Nevertheless, it is of course necessary to improve the DC-DC converter and in particular its output signal, since only one MuPix sensor was powered in this test beam. How the powering of several sensors and later on the entire system affects the quality of the output voltage of the DC-DC converter is not yet clear.



(a) Powered by a DC-DC converter without the second stage LC filter.

(b) Powered by a DC-DC converter with the second stage LC filter.

Figure 4.4: Threshold scans for efficiency and noise [61].



(a) Without filter.

(b) With filter.

Figure 4.5: Efficiency map for scans with and without second stage LC filter. Threshold at 45 mV [61].

Chapter 5

Mu3e DC-DC Converter Version 2

From the results of the tests in chapters 3 and 4 valuable conclusions can be drawn about necessary changes and improvements for the new version of the Mu3e DC-DC converter. However, these measures should be checked beforehand to avoid unnecessary errors in the next version. For this purpose, the method of circuit simulation was chosen. The program Tina TI from Texas Instruments based on SPICE was selected in version 9.3.200.277 SF-TI [51].

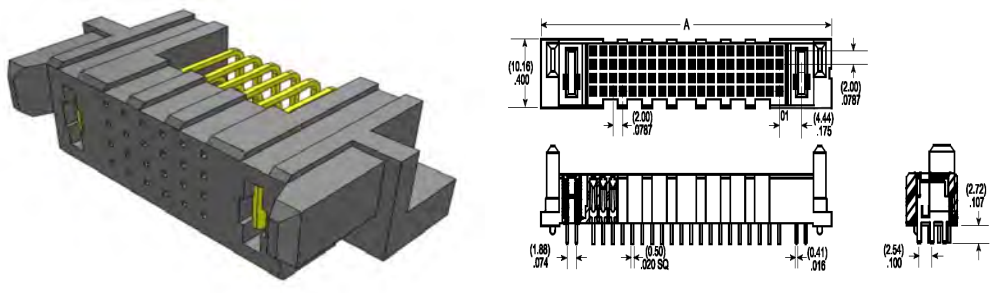
5.1 Circuit simulations with SPICE

The basis of almost all modern circuit simulation programs is SPICE [38] which is an acronym for "Simulation Program with Integrated Circuit Emphasis". SPICE1 was developed at the Electronics Research Laboratory of the University of California in Berkley and was first presented to the public in 1973. The improved versions SPICE2 and SPICE3 were released in 1975 and 1989.
SPICE is an open-source circuit simulator for analog, digital and mixed electronic circuits. It was developed to check the functionality of circuit designs and to make predictions about the behaviour of the circuit.

A circuit simulation program essentially consists of 5 main subprograms: input, setup, analysis, output and utility. The input subprogram reads the input file and generates a data structure that represents a complete description of the circuit. This data structure is first searched for user errors in order to eliminate them. Subsequently, further data structures are constructed by the subprogram setup, which are necessary for the analysis program. The analysis program is the core of the system and performs the circuit analysis specified by the input file. Subsequently, the output is generated which can contain graphs and tabular listings of predefined values. The utility subprogram creates and updates libraries with new element models and circuits [37].

5.1.1 Working Principle of SPICE

The analysis program of SPICE uses a mathematical representation of the circuit to calculate a numerical solution of the system. Each element of the circuit is described by mathematical models just like the connections between the elements. The circuit equations are a system of algebraic-differential equations [37]. This



(a) CAD model **(b)** Drawings

Figure 5.1: MPTC-01-24-01-01-01-L-RA-LC from Samtec Inc. :Input connector for version 2 [47].

system of equations is established with the help of Kirchhoff's rules and has the form:

$$G \cdot V = I \tag{5.1}$$

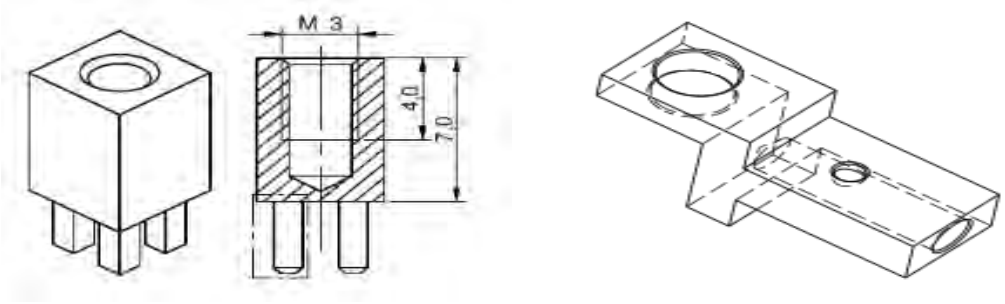
G is the nodal admittance matrix, V the vector of the node voltage to be determined and I the vector of the independent current source [**abc**]. For the calculation of the linear equations SPICE uses the method of LU decomposition [23].
This solution method can only be applied to linear circuits. Systems with non-linear elements must be linearized beforehand. This is done with the help of the Newton-Raphson algorithm [13], which approximates each non-linearity by a first order Taylor series [37].
With the analysis program, 4 different numerical procedures can be performed: the **DC Analysis** to calculate the operating point of the circuit, the **AC Analysis** as a small signal AC analysis and the **Transient Analysis** which measures the response of the circuit in the time domain over an interval (0,T) [**abc**].

5.2 New Components

Input and output Connector

The input connector of the new Mu3e DC-DC converter is going to be a signal and power combination system. This device is a rectangular connector header with 26 male pins and a current rating of 28 A per contact. It has 1 power pin per end and 24 signal pins in 4 rows between them [47].

The connectors of the output voltage, the REDCUBE PRESS-FIT with internal thread from Würth Elektronik GmbH & Co.KG, Germany do not change in the new design. These are cube-shaped power elements with 4 poles, an internal M3 thread and a rated current of maximum 70 A at 20 °C [67]. The mechanical workshop of the University of Heidelberg has designed a special cable shoe for the connection of the connectors with the leading-edge cables. A drawing of the cable shoe is shown in figure 5.2.



(a) Output connector [67] **(b)** Cable shoe

Figure 5.2: Output connector system for the Mu3e DC-DC converter.

Figure 5.3: Coil design for the filter inductor L_2 from Würth Elektronik GmbH & Co.KG, Germany [68].

Coil L_1 and L_2

It should be clear that winding the coils by hand is not an option for an application with such precision requirements. A solution has already been found for the smaller coil of the filter L_2. For this purpose, small copper coils of the company Würth Elektronik GmbH & Co.KG, Germany are used [68] (see figure 5.3), which are already implemented in the new PCB design. For the large coil L_1 it is much more difficult to find a suitable device. Most coils in the order of size either have an iron core or are not suitable for applications at high currents. As a next step, a custom design has now to be made and manufacturers must be contacted. Therefore, the hand-wound coils must first be used for the laboratory measurements as described in section 2.2.2.

5.3 Filter

The output signal of the Mu3e DC-DC converter is set to certain conditions to ensure a reliable function of the following detector components. This means above all that the high-frequency noise and the output ripple of the signal must be as small as possible, the upper limit for the ripple has been set at 10mV. This was not achieved with the version 1, which is why the output filter should be improved in the new version. However, the results of the test beam have shown that a stable function of the MuPix sensor is also possible with 15mV ripple. This led to the conclusion that

although an improvement of the output signal is to be achieved, it does not have to be massive changes which may then cause problems with the available space and heat development. When designing an LC filter, it is necessary to observe a few rules in order not to endanger the stability of the system in addition to the desired filter effect. Above all, it is important to consider the values of the first LC pair of the regular buck converter. The principle of a LC filter was presented before in section 3.1.4. As a reference for the designation of the components, see figure 3.8.
The first step is the determination of the inductance of the filter coil. The inductor L_1 should be much larger to limit the currents from the power MOSFETs. As a guideline L_2 should be about one tenth smaller than L_1 [16] which is in this case:

$$L_2 = \frac{1}{10} \cdot L_1 = \frac{1}{10} \cdot 550\,\text{nH} = 55\,\text{nH} \tag{5.2}$$

The manufacturer that was selected for the filter coils offers a variant with 46.5 nH which fits the requirements.
Next, the values of the capacitors must be set. It is not possible to simply hang an LC filter behind the output capacitor because this can lead to major stability problems. The second capacitor block should be much larger than the capacitor between the two inductors. If this were not the case, the system would be very sensitive to capacitive loading and could become unstable [16]. In addition, C_2 should be very large so that the capacitance of the load does not change the time constant of the system. C_2 was set to 541 μF, a slightly higher value than in the old version of the filter (394 μF) to reduce the ripple even further. For the capacitor C_1 a value that is about twenty times smaller than that of C_2 is recommended [16]. Therefore, the value for C1 was set to 47 μF.
Finally, it is extremely important to check the stability of the filter system. For this purpose, the frequencies of the converter should be examined more closely, in particular the relation between the cutoff frequency of the filter and the switching frequency. Figure 5.4 shows an example of how the frequencies in a DC-DC converter with an LC filter should be set to create a stable system. The cutoff frequency of the filter should therefore be about 1 tenth less than the switching frequency [1]. The crossover frequency, at which the loop gain equals one (0 dB) should then be again one decade lower than the cutoff frequency. To proof the stability of the system the condition

$$f_{cut} = \frac{f_{sw}}{10} = \frac{1MHz}{10} = 100\,\text{kHz} \tag{5.3}$$

should apply [1].
In addition to L_2 and C_2, the capacitor C_1 is taken into account for the calculation of f_{cut} and the whole system is considered as a pi filter. Therefore, the cutoff frequencies can be determined by [30]:

$$f_{cut} = \frac{1}{2\pi}\sqrt{\frac{C_1 + C_2}{L_2 C_1 C_2}} \tag{5.4}$$

The previously selected values $C_1 = 47\,\mu$F, $C_2 = 541\,\mu$F and $L_2 = 46.5\,$nH correspond to a cutoff frequency of:

$$f_{cut} \approx 112\,\text{kHz}. \tag{5.5}$$

If the result is compared with equation 5.3, it becomes clear that the cutoff frequency is of the same size as one tenth of the switching frequency and stability condition is

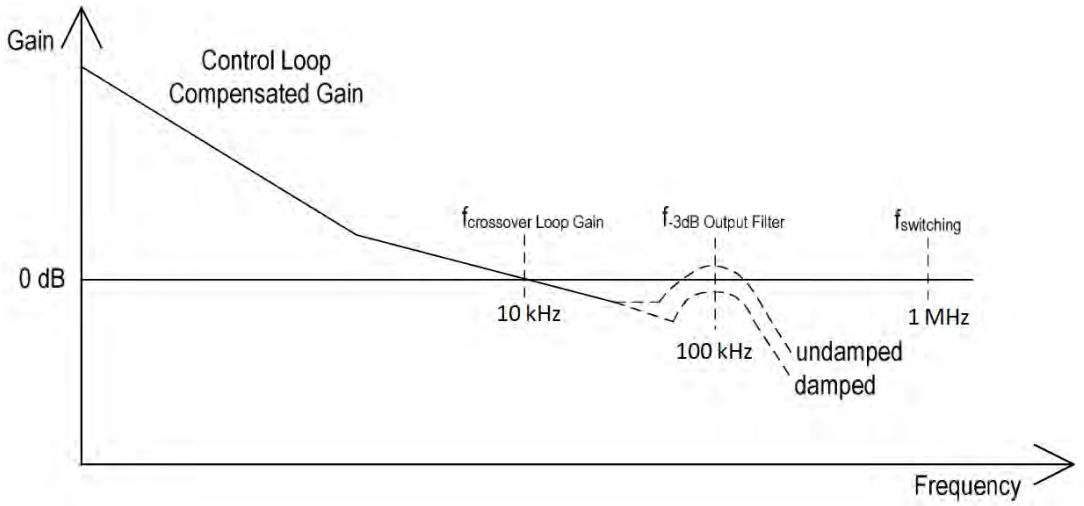


Figure 5.4: Setting the frequency values of a DC-DC converter with LC filter in relation to the switching frequency [1].

fulfilled.
In figure 5.4 a damped and an undamped case is shown. Damping can help to stabilize the circuit and is achieved by adding a damping resistor in parallel to L_2. On the PCB of version 2 of the DC-DC converter the option for an additional damping resistor is kept free.

5.3.1 Simulation of the Output Filter

To see if the newly designed filter also brings the desired effect, the circuit of the entire converter was simulated. In figure 5.5 the output signal of the DC-DC converter with an average voltage of $V_{out} = 2.1\,V$ is presented. The low overshoot at the beginning of the signal is probably a product of the simulation. It could not be confirmed in the laboratory measurements.
First of all, the ripple height was determined for the case without an output filter as a reference. The result in figure 5.6 shows a ripple height of 43.62 mV. The simulation for the designed LC filter with the parameters $C_1 = 47\,\mu F$, $C_2 = 541\,\mu F$, $L_1 = 550\,nH$ and $L_2 = 46.5\,nH$ shows a ripple height of 7.51 mV. The filter thus improves the output signal by 82.78 %; the target for the height of the output ripple $\leq 10\,mV$ is reached.
However, the simulation results should be evaluated with caution. Although, for example, parasitic components for the capacitors were taken into account, a simulation always only shows the optimal case. The result can change in reality by factors not taken into account and external influences, especially by the innovations described in the following chapters.
The option to implement an input filter was not used because the output filter turned out to be sufficient.

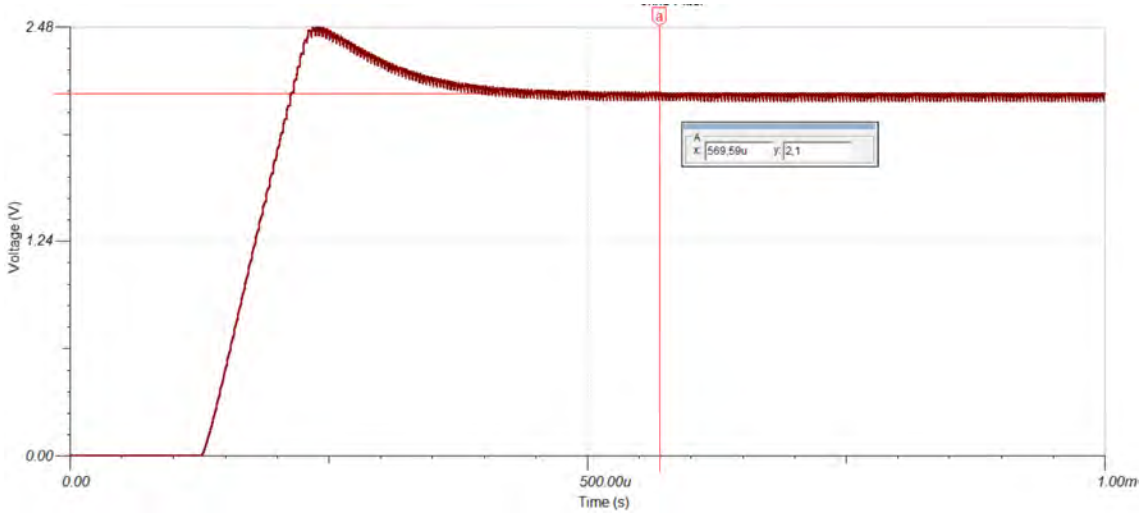


Figure 5.5: Simulation of the output signal of the Mu3e DC-DC converter without an output filter. The overshoot can not be seen in the laboratory measurements.

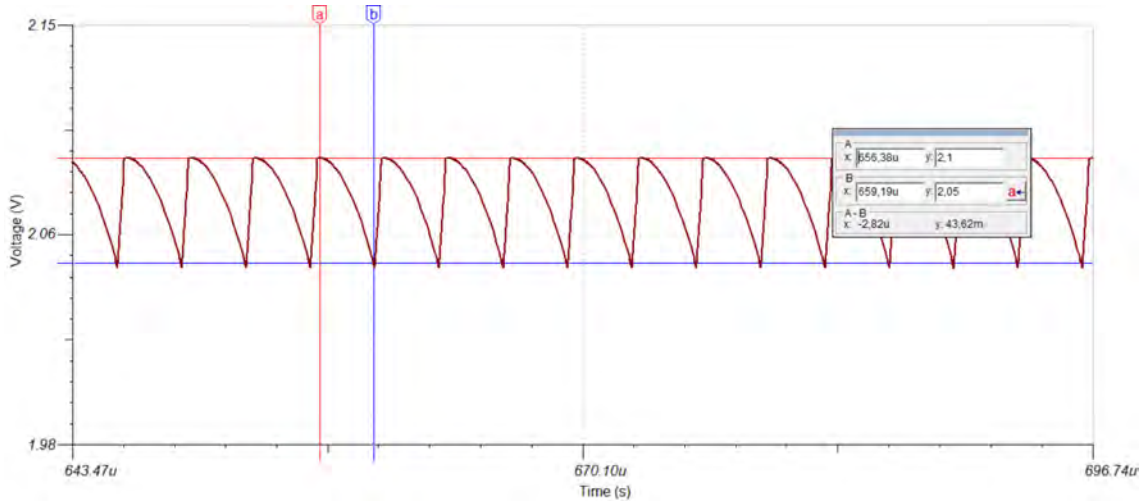


Figure 5.6: Simulation of the output ripple height of the converter without an output filter. The ripple is about 43.62 mV high.

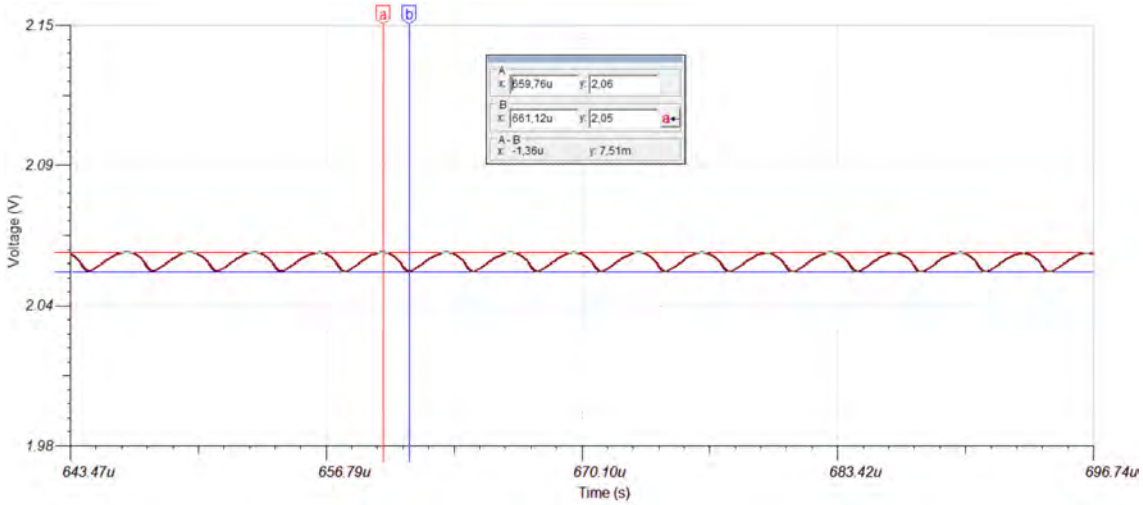


Figure 5.7: Simulation of the output ripple height of the converter with an output filter. The ripple is about 7.51 mV high.

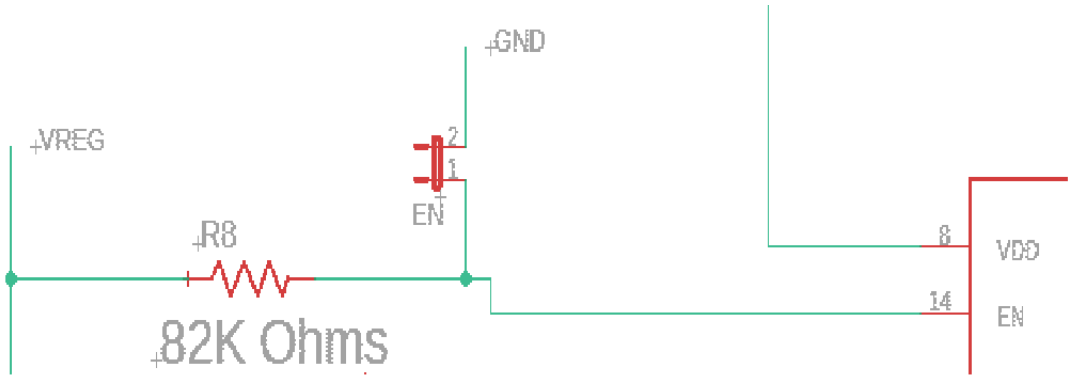


Figure 5.8: The voltage V_{en} can be pulled to ground by a jumper connection. In this case the converter is disabled. This circuit is only valid for version 1 of the converter.

5.4 Temperature Interlock System

For all experiments, especially for those with power ratings like the Mu3e experiment, a safety system that prevents damage to the individual components is absolutely necessary. High power always means a strong heat development, which is why all detector systems must also be cooled. The task of the interlock system is to ensure that the detector components are only switched on when the cooling systems are running and if they fail the detector is also switched off. Of course there will be an overall system for the experiment that connects all the individual components, but that is not part of this thesis. But in the new version of the DC-DC converter there should be a system that protects the MuPix sensors from overheating by the converter. For this purpose a temperature diode is used which is implemented in the MuPix sensors. This is to ensure that the DC-DC converter switches off if the module is too hot, independent of the chip status. Or the other way round, it should be prevented that the converter turns on if the module is too hot. This can be achieved by switching the enable voltage V_{en} a low voltage, using the information from the temperature diode of the MuPix sensor. At a high voltage V_{en} the converter works normally and at a low ($< 0.5\,V$) voltage it is disabled. Up to now a deactivation was only possible when a jumper connection was used to pull the voltage V_{en} to ground (see figure 5.8).

5.4.1 MuPix Temperature Diode

The temperature diode is build by a p-implant embedded in the deep n-well which is connected to V_{dd}-mupix which is the voltage provided by the DC-DC converter (see figure 5.9). If a defined constant current is injected into the diode, the measurable voltage drop across the diode is temperature dependent. The relationship between the voltage drop across the diode and the temperature is anti-proportional as shown in figure 5.10. The voltage drop is very low at high temperatures and vice versa [32]. The results were approximated with a linear fit. The fit function can then be used to create a formula for the temperature of the Mupix module depending on the diode voltage [32]:

$$T_{MuPix} = 228.0°C - 0.332°C/mV \cdot V_{bias,diode}. \tag{5.6}$$

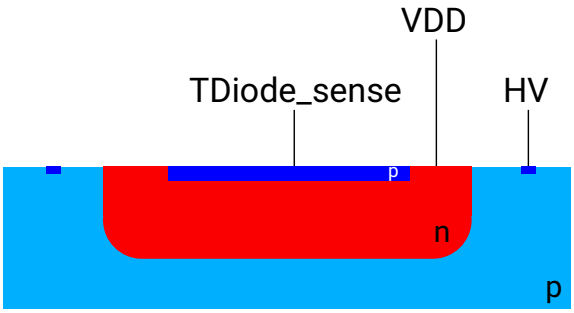


Figure 5.9: Temperature diode of the MuPix sensor [60]. The diode consists of a p-implant embedded in a deep n-well.

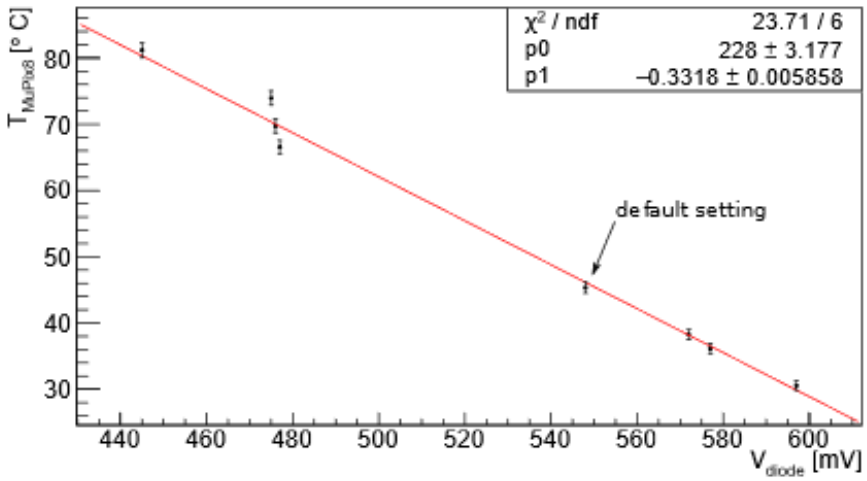


Figure 5.10: The voltage drop across the temperature diode is temperature dependent. A low voltage drop corresponds to a high temperature and vice versa [32].

5.4.2 Interlock System with 3 Operational Amplifiers

The heart of this system are 3 operational amplifiers (OPA2333P [56]) with a supply voltage of 5 V. The circuit diagram of the interlock system is shown in figure 5.11. The first two amplifiers (Part 1) form a source follower and a differential amplifier, thus determining the voltage difference V_{diff} between V_{diod} and V_{dd}-mupix. The system is supplied with a supply voltage of 5 V, provided by V_{REG} of the control chip, from which a threshold voltage V_{thresh} is generated by a voltage divider. V_{thresh} is then compared to V_{diff} by the third amplifier (part 2) which acts as a comparator. Behind this amplifier is a npn-transistor with a connection to a 100 Ω pull-up resistor to 5 V where the enable voltage V_{en} is measured. If the voltage V_{diff} is above the given threshold voltage, the output of the comparator is small and the transistor is closed and V_{en} is at 5 V. If the temperature of the MuPix module rises, V_{diod} drops and so does V_{diff}. If the differential voltage then falls below V_{thresh} the comparator output becomes high and the transistor is conducting. V_{en} then gets shortened to ground and goes to 0 V, disabling the converter. The threshold voltage has been set such that it disables the converter when a bias voltage is applied to the diode which corresponds to a temperature of 70 °C. According to equation 5.6, 70 °C correspond to a bias voltage of 476 mV. With the help of the equation for the voltage divider

$$V_2 = \frac{V_{ges} \cdot R_2}{R_1 + R_2} \tag{5.7}$$

the resistances $R_1 = 21\,k\Omega$ and $R_2 = 2.2\,k\Omega$ can be determined [18].
The operation of this structure was simulated with the help of Tina Ti. For this purpose the following settings were made: The supply voltage of all parts and of the system itself is 5 V. Since the system should function independently of the MuPix settings, two different scenarios were simulated: The supply voltage of the MuPix was set to 0 V once and once to its maximum value of 2 V. For the bias voltage of the diode 600 mV were chosen. The diode voltage V_{diod} is actually the diode bias voltage plus V_{dd}-mupix and thus has the values 0.6 V and 2.6 V. The following two simulations were carried out:

	parameters 1 [V]	parameters 2 [V]
V_{dd}-mupix	0	2
V_{diod}	0.6	2.6

In order to simulate a temperature increase of the module and thus a voltage drop at the diode, V_{diod} was configured so that the proportion of the bias voltage drops constantly within a time interval of 2 ms.
The results of the simulations are shown in the figures 5.12 and 5.13. The voltages V_{dd}-mupix, V_{diod}, V_{thresh} and V_{en} were recorded. The threshold voltage is at 474 mV as expected and the enable voltage V_{en} is switched when the threshold is reached. The system works as expected for both V_{dd}-mupix =0 V and V_{dd}-mupix =2 V.

5.4.3 Interlock System with 2 Amplifiers

It is possible to replace part 1 completely by a single instrumentation amplifier that combines the characteristics of the source follower and the differential follower. The INA326 [54] from Texas Instruments was chosen in this case.

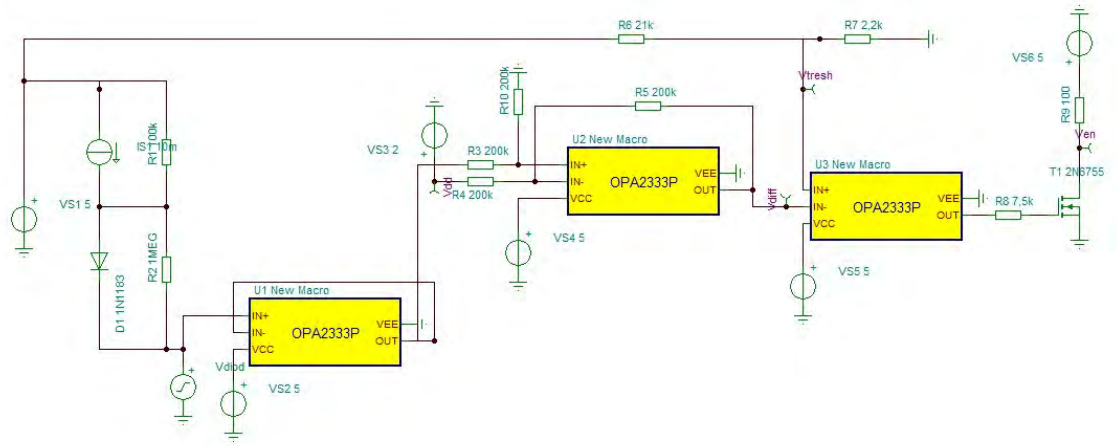


Figure 5.11: Temperature diode interlock system with 3 operational amplifiers.

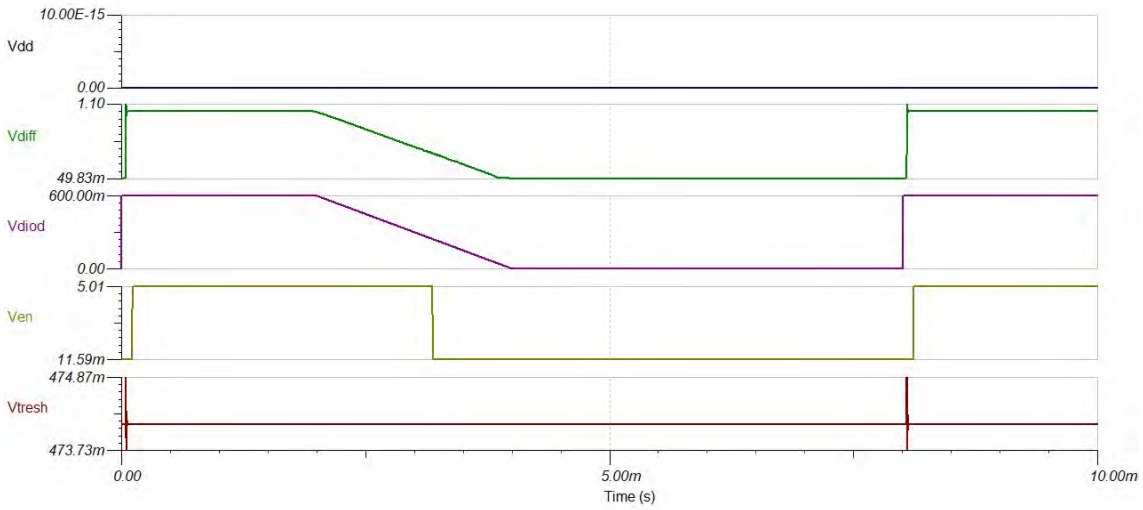


Figure 5.12: Simulation results for V_{dd}-mupix = 0 V with 3 operational amplifiers.

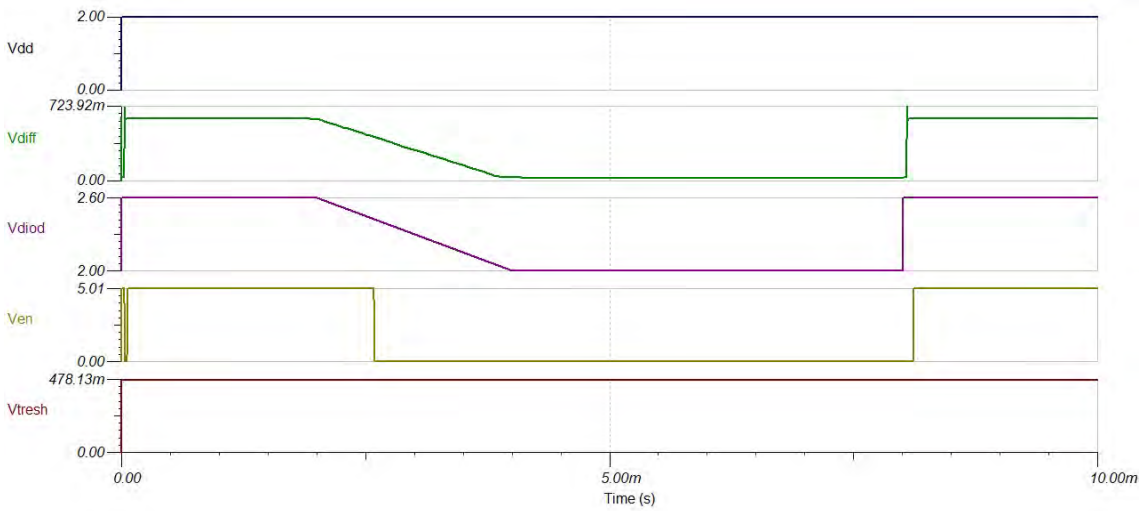


Figure 5.13: Simulation results for V_{dd}-mupix = 2 V with 3 operational amplifiers.

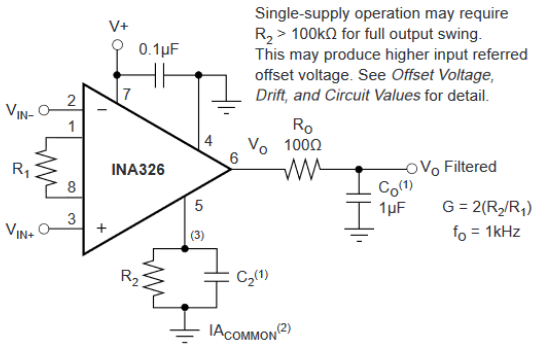


Figure 5.14: Basic connections for the operation of the INA326 [54].

The INA326 is a high performance, precision, 2-stage instrumentation amplifier. The basic connections for operating this amplifier are shown in figure 5.14. For high accuracy a 0.1 μF capacitor close to the power supply pins is strongly recommended. An output filter is built by R_0 and C_0 to minimize auto correction circuitry noise. The two gain stages are set by R_1 and R_2 and the overall gain can be expressed by [54]

$$G = 2 \cdot \frac{R_2}{R_1} \tag{5.8}$$

The resistor values for frequently used gains are shown in figure 5.15.
This variant brings a space saving which is an advantage due to the small size of the board, but it must be checked whether the function and especially the stability of the system is still guaranteed. Therefore, the simulations from section 5.4.2 have been updated with the new circuit diagram (see figure 5.16). The results are shown in the figures 5.17 and 5.18. Apart from a light RC filter effect, the system works just like the interlock with 3 amplifiers. Therefore, the space-saving variant with the instrumentation amplifier was chosen.

5.4.4 Technical Implementation in the Circuit Design

In the new design enabling the converter will not be achieved by pulling a plug like in version 1, but by the external controller. If the temperature interlock would be implemented with a pull-up resistor of 100 Ω it would overrule the external controller. This problem is presented in figure 5.19a. If the controller disables the board (here represented by an open switch) the system would still pull the 5 V from V_{REG} and the converter would stay on. The solution is to use a much higher pull-up resistor of about 1 MΩ as shown in figure 5.19b. Under these conditions, the converter cannot be switched on by the temperature interlock if the external controller has deactivated the converter.

5.5 Current Sense

A further addition will be an additional current measurement in the second version of the Mu3e DC-DC converter. This allows the output current and thus the applied load to be constantly checked. This is realized in the most common way by sensing the voltage drop across a current-sense or shunt resistor. The voltage drop V_{drop}

DESIRED GAIN	R_1 (Ω)	$R_2 \parallel C_2$ (Ω || nF)
0.1	400k	20k || 5
0.2	400k	40k || 2.5
0.5	400k	100k || 1
1	400k	200k || 0.5
2	200k	200k || 0.5
5	80k	200k || 0.5
10	40k	200k || 0.5
20	20k	200k || 0.5
50	8k	200k || 0.5
100	4k	200k || 0.5
200	2k	200k || 0.5
500	2k	500k || 0.2
1000	2k	1M || 0.1
2000	2k	2M || 0.05
5000	2k	5M || 0.02
10000	2k	10M || 0.01

Figure 5.15: Resistor values for frequently used gains [54].

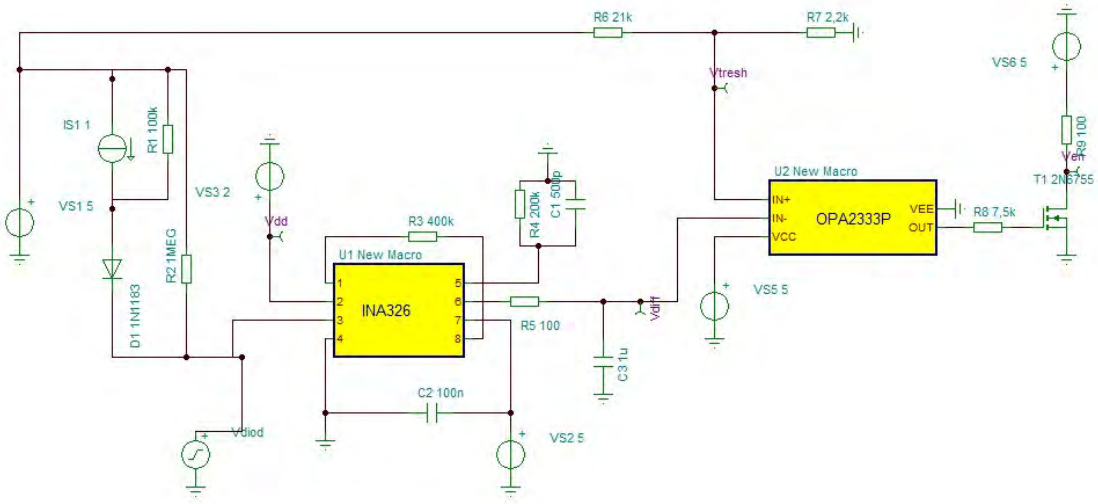


Figure 5.16: Temperature diode interlock system with an instrumentation amplifier INA326.

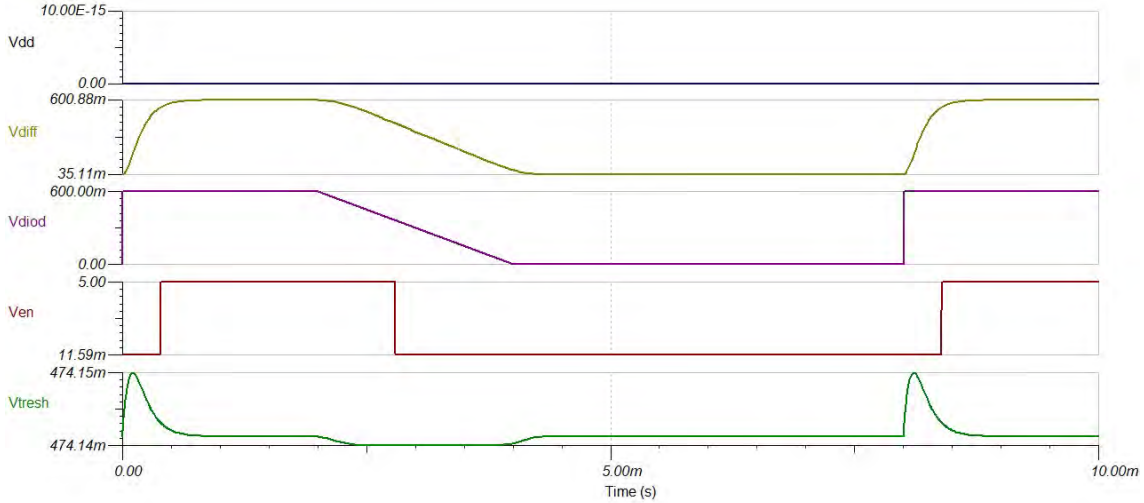


Figure 5.17: Simulation results for V_{dd}-mupix = 0 V with INA316.

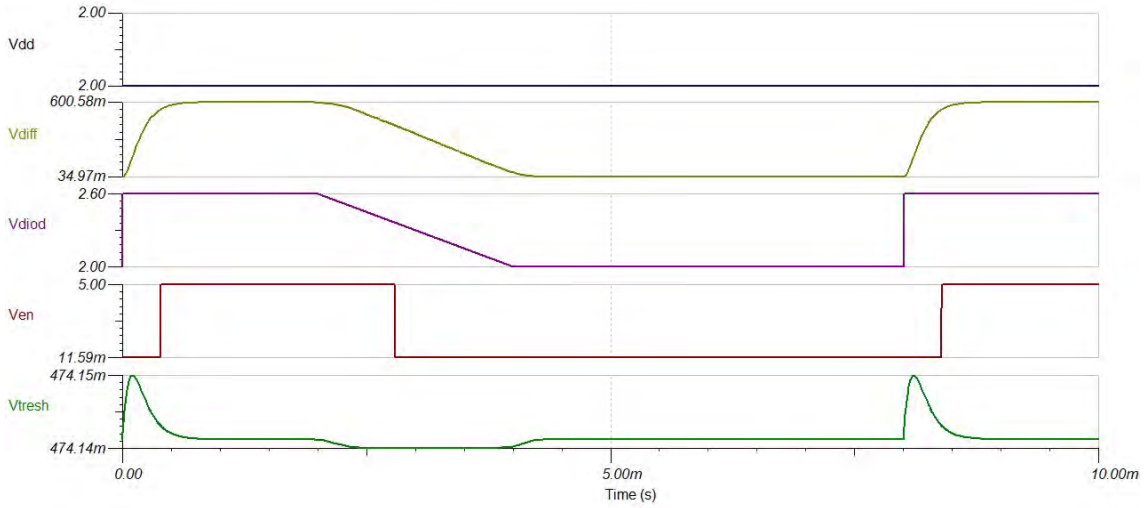
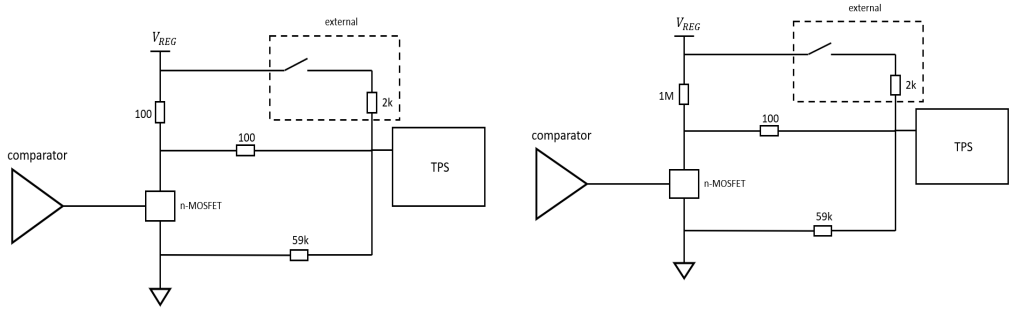


Figure 5.18: Simulation results for V_{dd}-mupix = 2 V with INA326.



(a) The temperature interlock would overrule the external controler.

(b) The converter is just enabled if the switch is closed and the output of the temperature interlock is high.

Figure 5.19: Implementation of the temperature interlock in the circuit design of the Mu3e DC-DC converter.

can then be converted into a value for the current $I = \frac{U}{R}$, with R the value for the shunt resistor.
The first step in the development of a current measurement is the choice for a current-sense resistor, its value and its wattage. The definition of a resistance value depends on the desired voltage drop at the highest expected current. A voltage drop of 50 mV was selected for this application. This corresponds to a load current of 20 A, a resistance of 2.5 mΩ and a power dissipation of 2 W. The current measurement is placed before the feedback node to have some headroom to compensate for the voltage loss. To amplify the small voltage drop the instrumentation amplifier INA326 is used with a gain of 20. This value will then be read out by the slow control system by an external ADC. The functionality was tested via simulations.

5.5.1 Results of the Simulation

The test circuit is shown in figure 5.20. The simulation was running once with a current of 10 A, as it is usually used in laboratory measurements, and once with the highest expected current in the experiment of 20 A. For the simulation with I = 10 A a voltage drop of $V_{drop} = 20$ mV at R = 2 mΩ is expected. At a gain of 20 this means a voltage of 400 mV at the output of the amplifier. A current of I = 20 A has consequently an amplified voltage of 800 mV.
The simulation results are presented in the figures 5.21 and 5.22.
A critical point in the layout of the current-sense measurement is the connection of the shunt resistor and the current-sense amplifier. A bad or faulty connection can reduce the accuracy of the measurement [57]. There are current-sense amplifiers with integrated shunt resistors existing which are recommendable to use to avoid errors in the connection. One example is the INA250 [53] from Texas Instruments. The INA250 is a voltage-output, current sensing amplifier and features a 2 mΩ shunt resistor with a tolerance of 0.1 % (max). The amplifier is available with four different gain stages (200 mV/A, 500 mV/A, 800 mV/A, 2 V/A) [53]. The functional block diagram of the INA250 is shown in figure 5.23. The disadvantage of this device is that it is only suitable for applications with a maximum of 15 A for which reason a parallel summing configuration of two INA2501 has to be used (see figure 5.24). For testing the INA250A1 was chosen with a gain of 200 mV/A. Again two simulations with currents of 10 A and 20 A were performed.
For version 2 of the Mu3e DC-DC Converter, the decision was made to use the version without integrated shunt again, since only one amplifier is required. The variant with integrated resistor will be saved as backup in case of connection problems in the application of the chosen variant.

5.6 Feedback Loop

The output voltage of a DC-DC converter is not always 100% stable in terms of its amount. Due to component variations and thermal effects, small deviations are constantly occurring. Variations in the applied load can also influence the output voltage. Since the detector components supplied by the Mu3e DC-DC converters require an extremely stable voltage, a control mechanism that stabilizes the output voltage of the converter is necessary. This is usually done through feedback control.

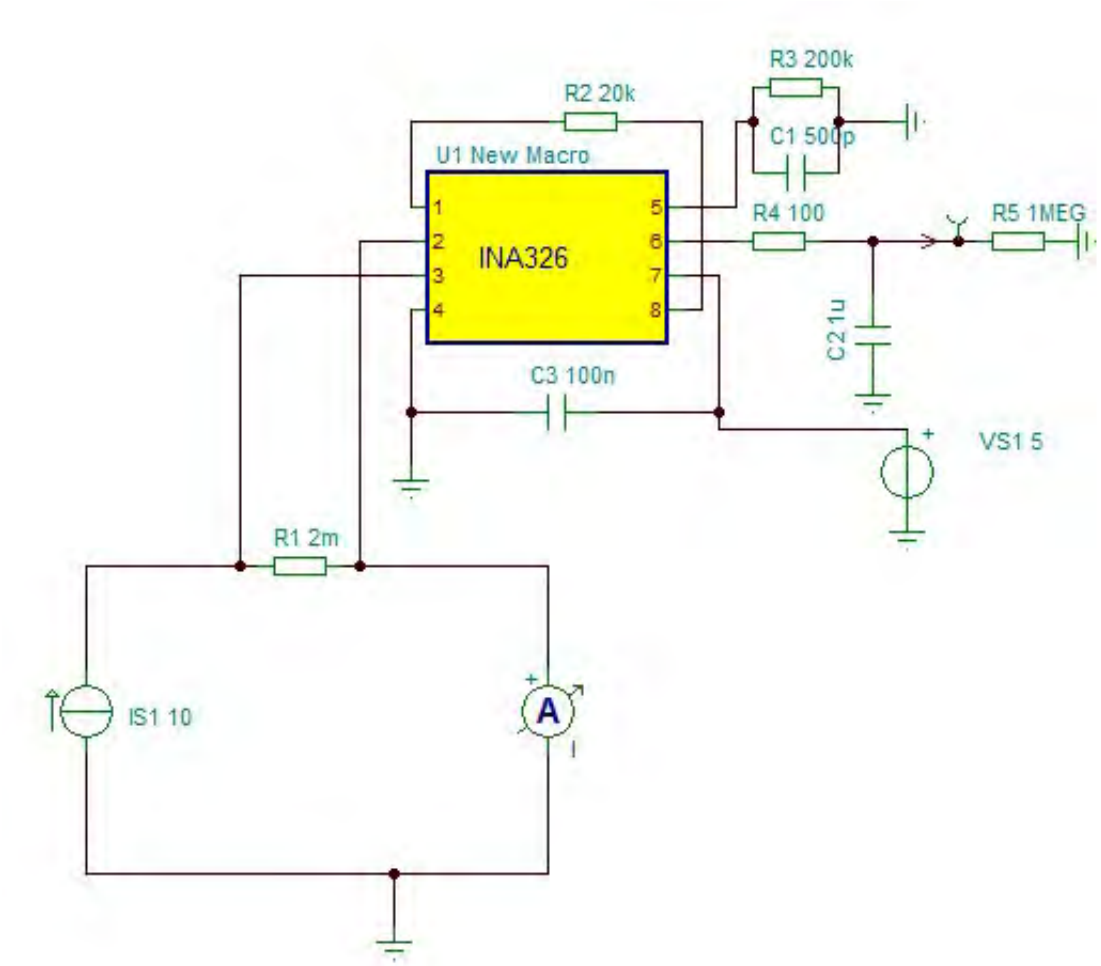


Figure 5.20: Current measuring: The voltage drop across a shunt resistor is measured with an instrumentation amplifier.

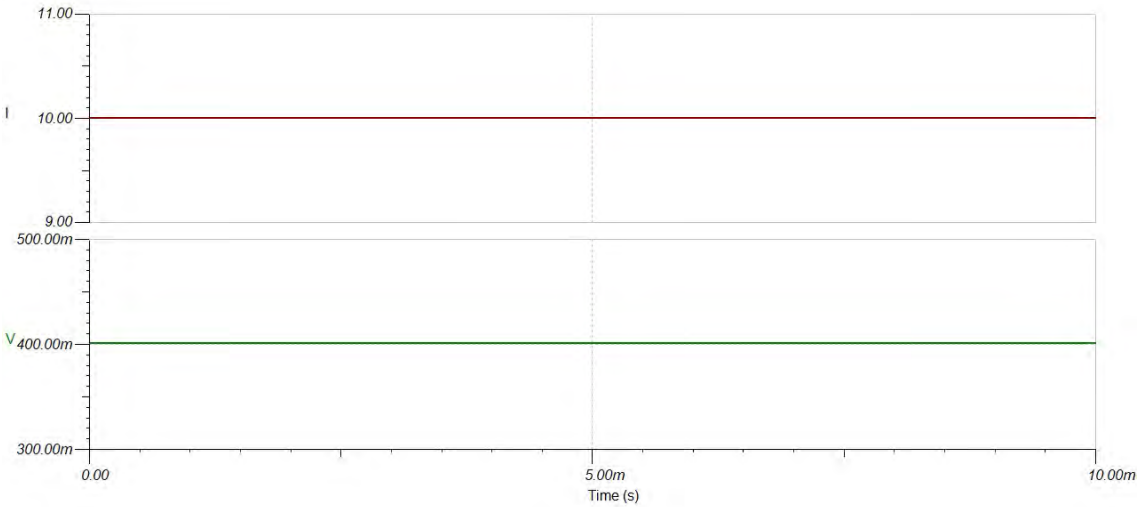


Figure 5.21: Simulation of the current measurement with the INA326 at a current of 10 A.

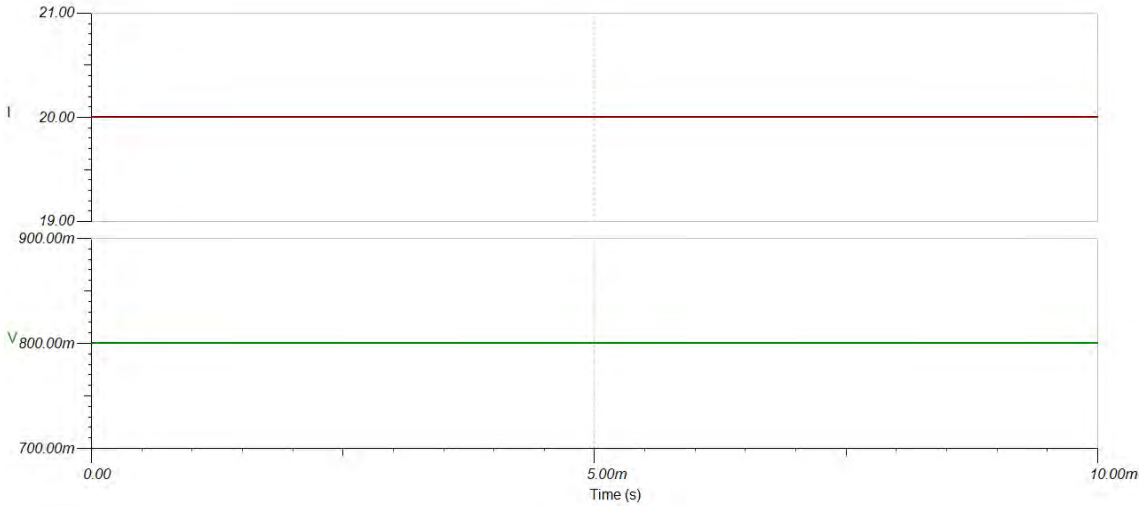


Figure 5.22: Simulation of the current measurement with the INA326 at a current of 20 A.

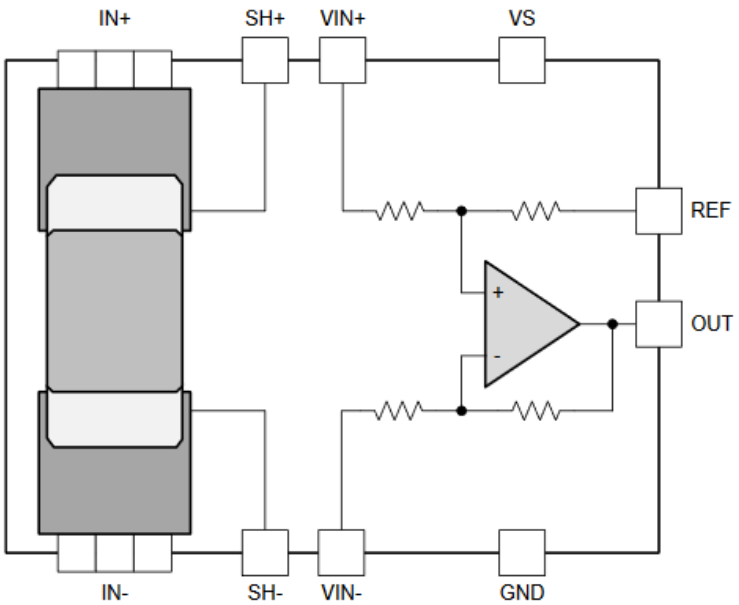


Figure 5.23: Functional block diagram of the INA250 [53].

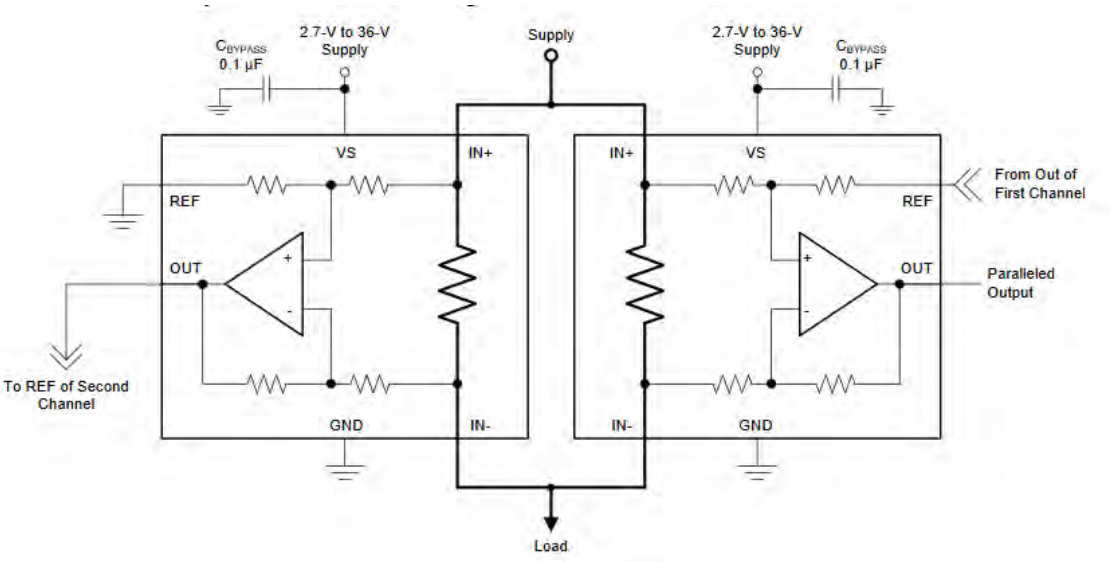


Figure 5.24: Parallel summing configuration for applications with higher currents for the INA250 [53].

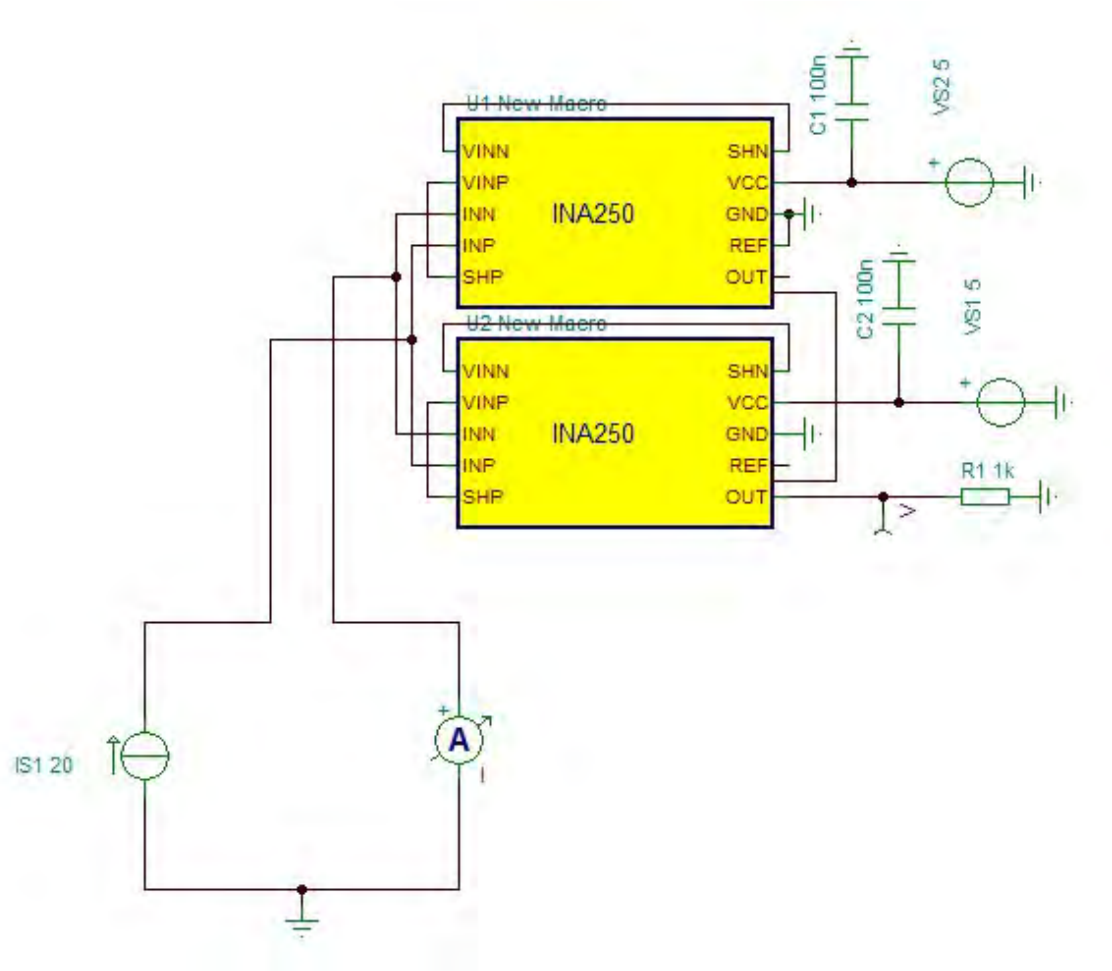


Figure 5.25: Simulation circuit for the current measurement with current-sense amplifiers.

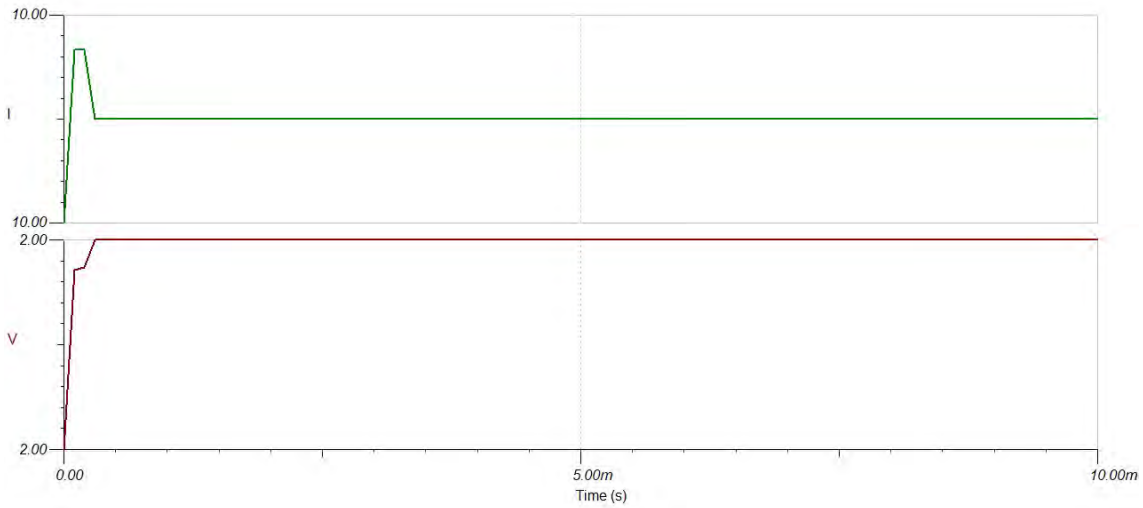


Figure 5.26: Simulation of the current measurement with the current-sense amplifier at a current of 10 A.

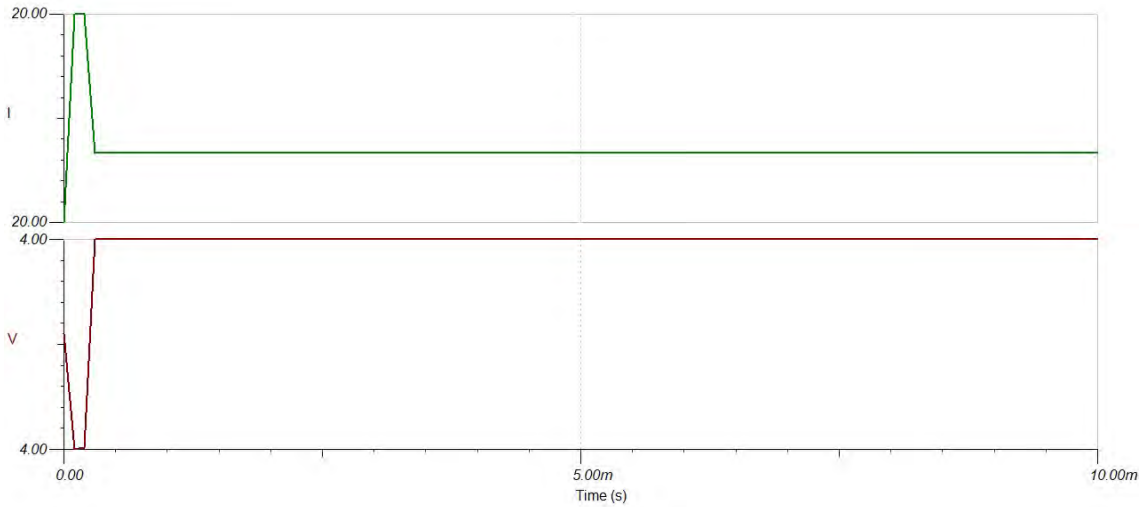


Figure 5.27: Simulation of the current measurement with the current-sense amplifier at a current of 20 A.

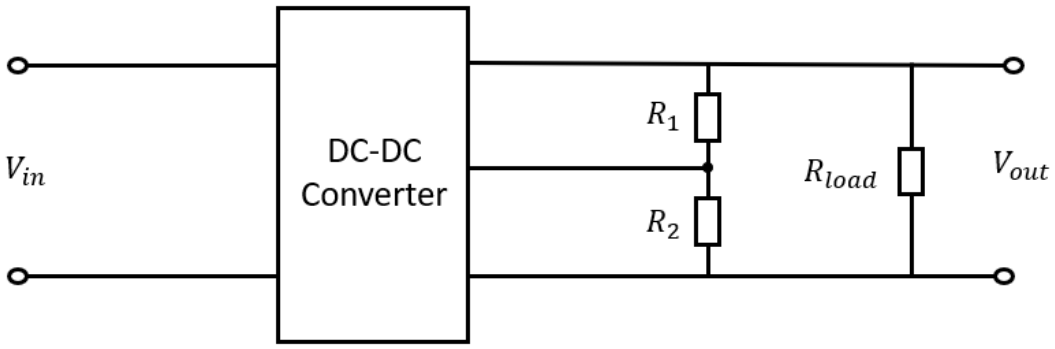


Figure 5.28: Principle of a feedback loop realized with a voltage divider.

The feedback loop is realized by a voltage divider placed between V_{out} and ground before the output of the converter shown in figure 5.28. A fraction of the output voltage is fed back to the feedback pin of the TPS53819A. The control chip then compares this voltage V_{FB} to the target voltage of 0.6 V. If V_{FB} is not equal to the target voltage the output voltage can be regulated by switching the power MOSFETs and thus adjusting the duty cycle to keep V_{out} stabel.

In version 2 of the Mu3e DC-DC Converter the feedback loop will be extended by a further feature. The voltage transport from the converter to the detector components takes place via various different media. The voltage drop is not known for all elements of this cable chain and depends on the varying current drawn by the load. The transport media to MuPix and MuTrig also differ in their type and length. Additionally load changes and thus changes in the output voltage of the converter can occur if not all detector elements are in operation. To illustrate this, figure 5.29 lists the previously known voltage drops of the individual sections of the connection between DC-DC converter and MuPix sensor. Assuming the system runs under full load, we have voltage drops of at least 340 mV. With the help of the PMBus interface, the output voltage can be varied by ±9 % which at 2 V corresponds to a voltage difference of 180 mV. The limits of the remote tuning range are thus reached. In order to take into account at least some of the voltage drops, sensor wires are used to take the voltage between DC-DC converter and Mupix module as a reference for the feedback loop. V_{dd} is already present on the converter because the voltage is already needed for the temperature interlock. The ground wire comes either from a MuPix sensor (the same from which V_{dd} is coming) or it is fastened between the two flexprints. The two sensor wires are then fed into an instrumentation amplifier, the difference is determined and the output of the amplifier can be fed into the feedback loop. A combination of jumper pins before the resistance R1 of the voltage divider then provides the possibility either to use the original feedback loop or to test the new variant. The implementation is shown in figure 5.30. A jumper connection makes it easy to switch between the two variants of the feedback loop if it should turn out that the new version should cause problems, for example by making the system unstable.

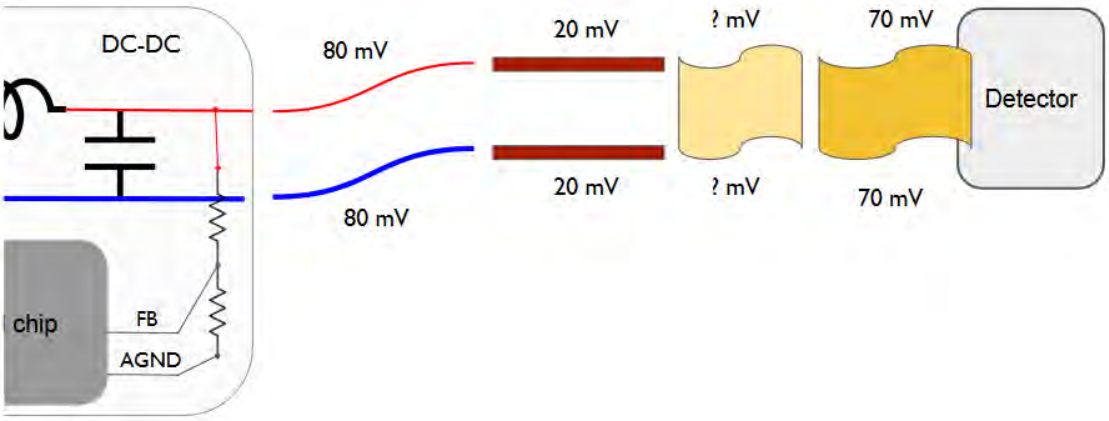


Figure 5.29: Voltage drops of the single cable sections between the DC-DC converter and a MuPix sensor. Not all voltage drops are known at the moment [21].

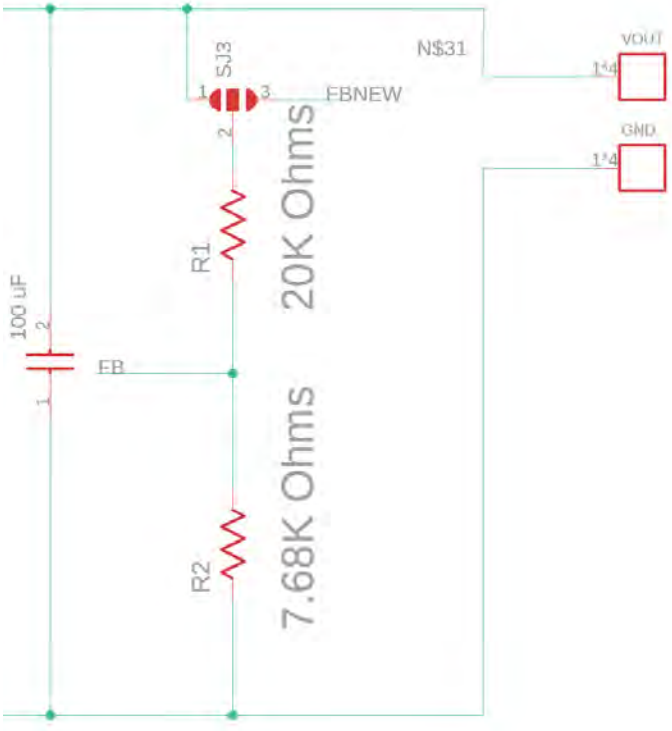


Figure 5.30: New implementation of the feedback loop in version 2 of the Mu3e DC-DC converter. With a solder jumper it possible to connect the voltage divider either with the output signal of the converter (connection to the left) or with the new version with the sense wires. (connection to the right).

5.7 Grounding Scheme

The grounding scheme will also be changed in the new version of the Mu3e DC-DC converter.
In version 1 the power board ground was isolated from the outside. The reference of a power partition was located on the return line (V_{in}^-) in front of the power board. V_{in}^- was the power ground (PGND) and was connected to the analog ground (AGND) on the board. V_{in}^+ was connected to V_{dd} of the TPS53819A, which generates V_{REG} for all control circuits.
In the new version the AGND of the control circuit is connected to the slow control GND from the outside. The slow control GND is delivered by a common (virtual) ground plane in the detector. The power partition ground is now referenced at the connection of AGND and PGND. The V_{dd} of the control chip will be powered separately from the outside.
This has the advantage that the TPS53819A chip can be powered before the 20 V input power is turned on. Therefore all slow control settings can be set and checked before the board gets powered.

5.8 Schematic

The following section presents the schematic of the Mu3e DC-DC converter version 2. Due to space constraints, the circuit diagram was divided into several sections. The main circuit is shown in figures 5.31 and 5.32, along with the current measurement. Figure 5.33 shows the temperature interlock with the new enable scheme. The second variant of the feedback loop is shown in figure 5.34. Figure 5.35 shows the implementation of the PMBus interface and a 1-wire temperature sensor for monitoring the temperature of the DC-DC converter.
A Bill of Material (BOM) can be seen in the appendix C.

5.9 PCB design

Results from section 3 have shown that the largest part of the output ripple is caused by inductive coupling. In addition to an improvement of the output filter, two ways to reduce this are the PCB design and shielding (shielding is described further in section 5.10). A well-designed PCB can contribute significantly to the signal quality of a circuit. The coupling and propagation of noise can be minimized by careful placement of the components.
Decisive for DC-DC converters are the position of the input and output capacitors, the wiring of the signal lines and the division of the ground. For version 1 of the Mu3e DC-DC converters, the main consideration was the size of the PCB. It has been compressed to the smallest possible size because the space inside the detector is limited. In the meantime the size relationships have been clarified and there is space for DC-DC PCBs of size $50 \times 90 \times 35$ mm. In the following the most important aspects of the PCB design are listed which can contribute to improve the output signal.

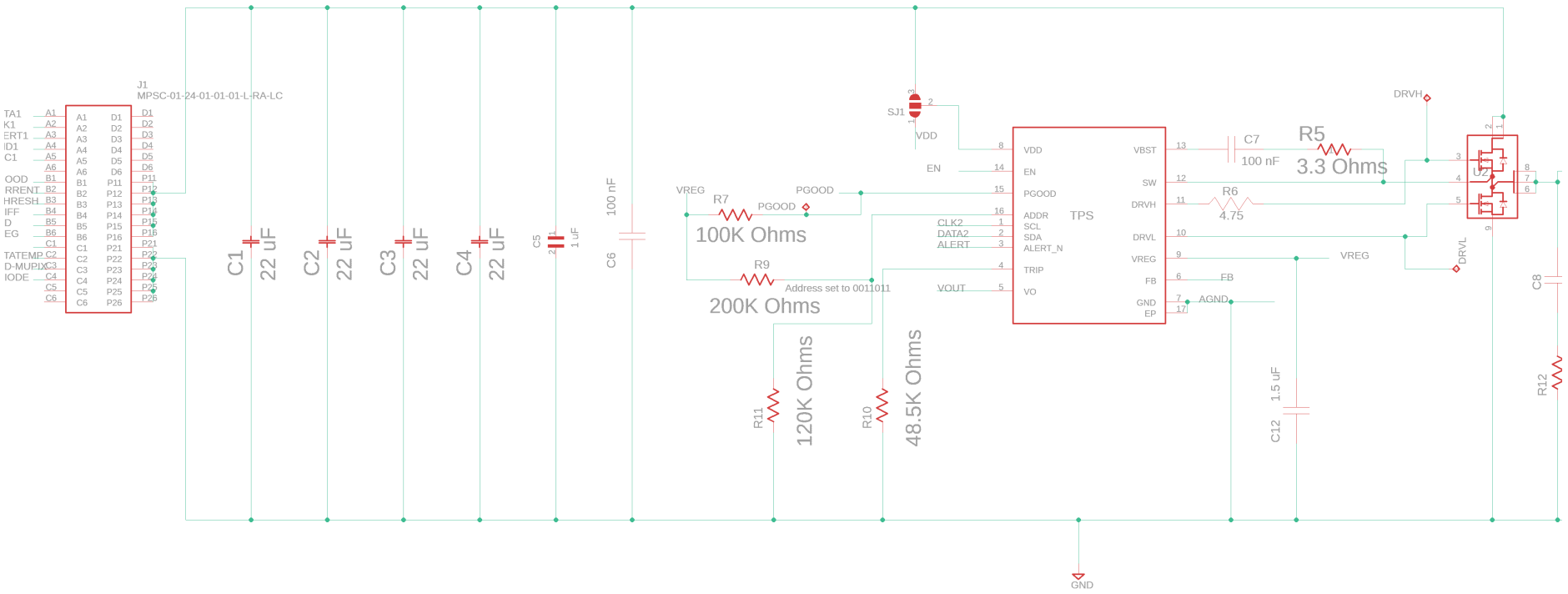


Figure 5.31: Schematic of the Mu3e DC-DC converter version 2 part 1: Input connector; input capacitors; TPS53819A; CSD86360Q5D.

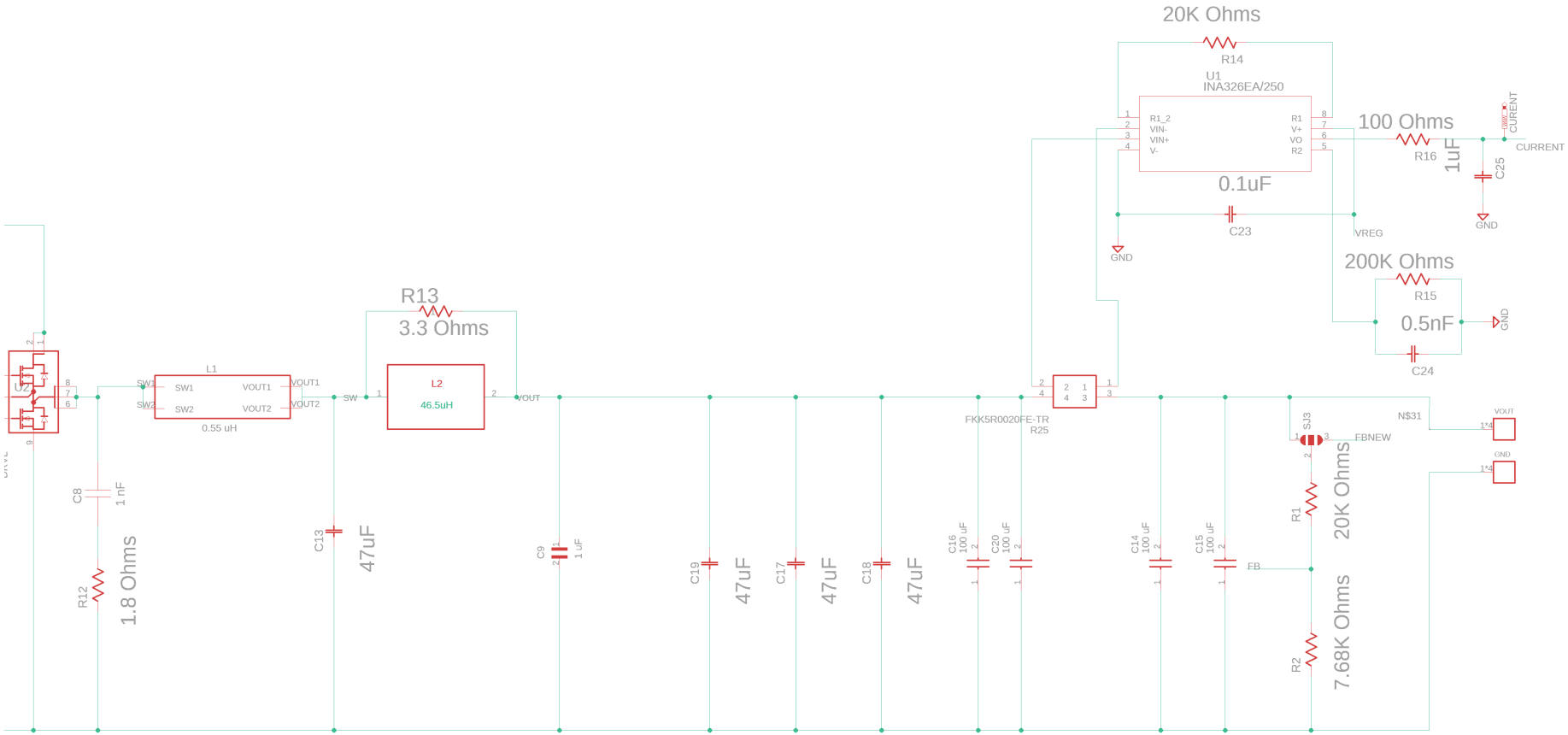


Figure 5.32: Schematic of the Mu3e DC-DC converter version 2 part 2: CSD86360Q5D; second LC filter; current sense measurement; output connectors.

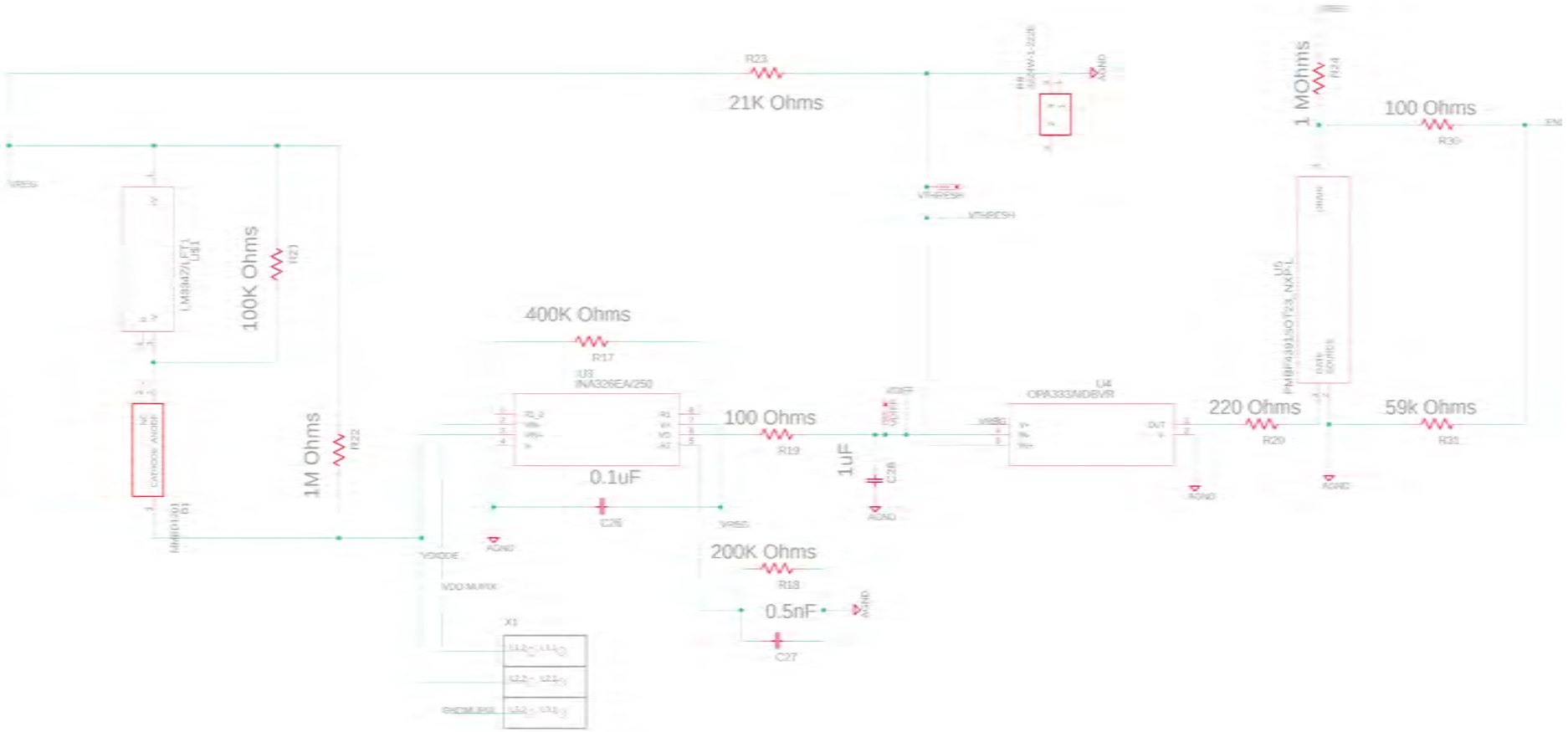


Figure 5.33: Temperature interlock system.

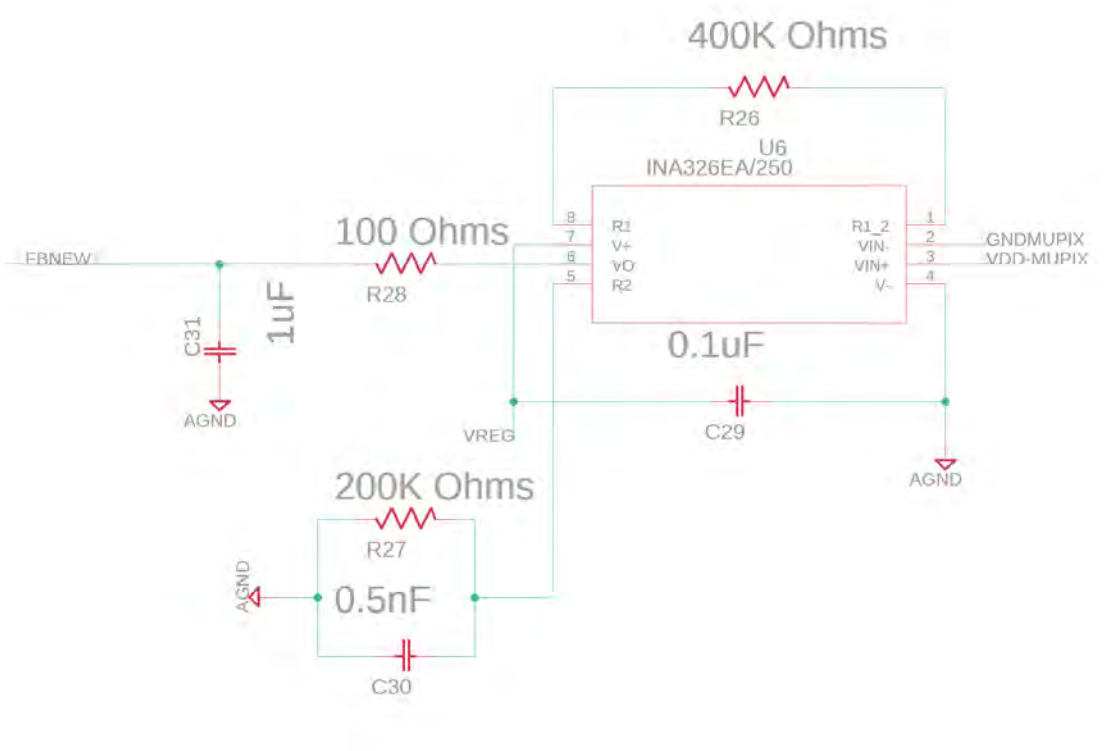


Figure 5.34: New version of the feedback loop with two sense wires from the MuPix sensor.

5.9.1 Placement of Input and Output Capacitors

The capacitors that form C_{in} should be placed on the power side. In addition, C_{in} should also be placed as close as possible to the input pins of the power MOSFETs, as this will reduce the high di/dt loop and thus reduce the noise as discussed in section 2.1.2.
A sharply rising and falling current flows through C_{in}, causing high-frequency ringing in the range of several hundred megahertz which can propagate into the ground patterns. If the connections of C_{in} and C_{out} to the ground are too close together, the noise from the input could pass through C_{out} and be coupled to the output signal. However, by placing the ground side of C_{out} at least 1-2 cm from C_{in}, one can take advantage of the properties of the otherwise undesirable parasitic components. The inductance and resistance of the thin film wiring can act as a kind of filter and reduce the HF noise [45].

Due to the presented design guidelines some changes in the PCB of the old version are necessary. The input capacitors are relatively far away from the transistors. The flow of the current from the input of the converter through the capacitors to the MOSFETs is also not straight (see figure 5.36). As a result, the di/dt loop is unnecessarily high and the HF noise is amplified. The same applies to the output capacitors. They are arranged L-shaped shown in figure 5.37 so that no direct current flow is given. This creates a kind of current loop which becomes visible in the output signal described in section 3.1.4 in the form of inductive pick up.

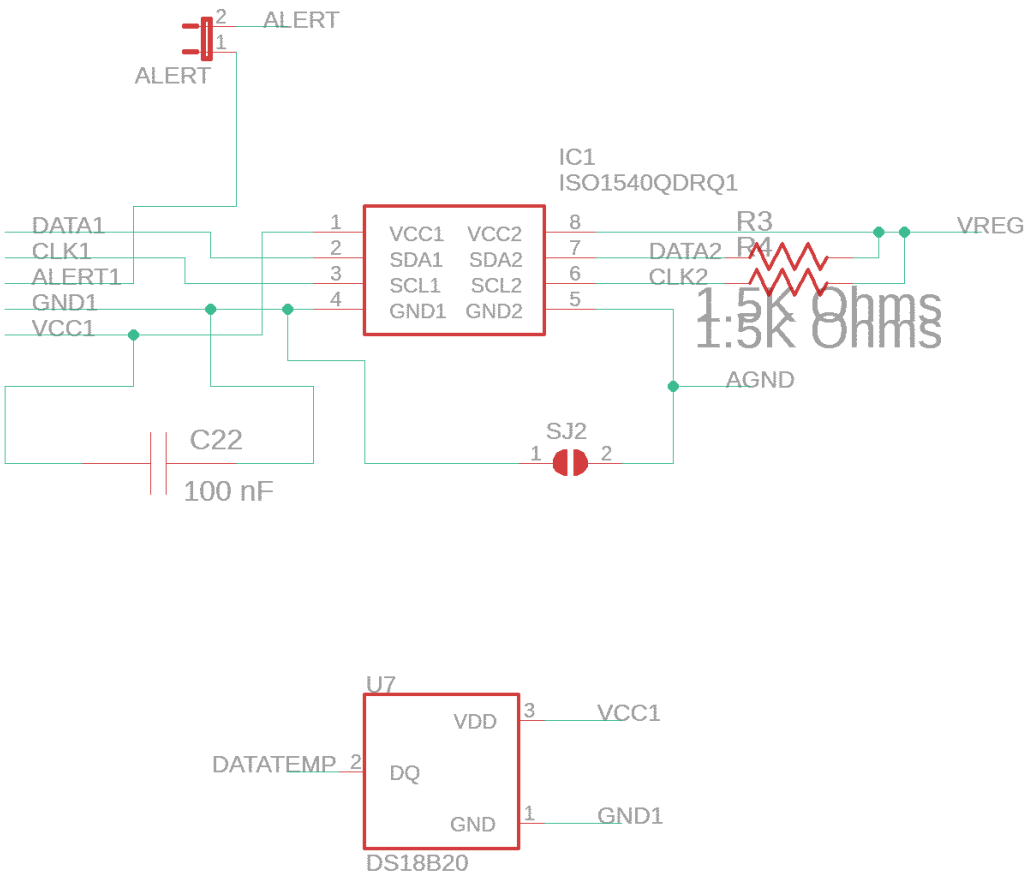


Figure 5.35: PMBus implementation and the a temperature sensor to monitor the temperature of the DC-DC converter.

5.9.2 Placement of Inductor

When positioning the inductor, special attention must be paid to the area below the device. A coil always generates a magnetic field and its magnetic lines of force could pass through the copper foil below the inductor. This generates eddy currents that cause two different problems. On the one hand, the eddy currents can compensate the magnetic field and thus reduce the inductance. On the other hand, problems can arise in adjacent electrically conducting components. If the copper trace is a signal line, this can have a negative effect on the circuit operation as the noise can propagate through the signal. The same applies to ground layers located under the inductor. In addition, the copper pads the inductor is connected with should be as small as possible, otherwise they could act as antennas and amplify EMI noise.
These considerations also apply to the switching node. This is a critical point because it switches continuously between 0 V and V_{in}. The plate under the switching node should therefore also be as small as possible to minimize noise [45].

5.9.3 Feedback Wiring

Special attention must be paid to a correct wiring of the feedback loop as fluctuations in the feedback path can cause oscillations and an accurate output stabilization is

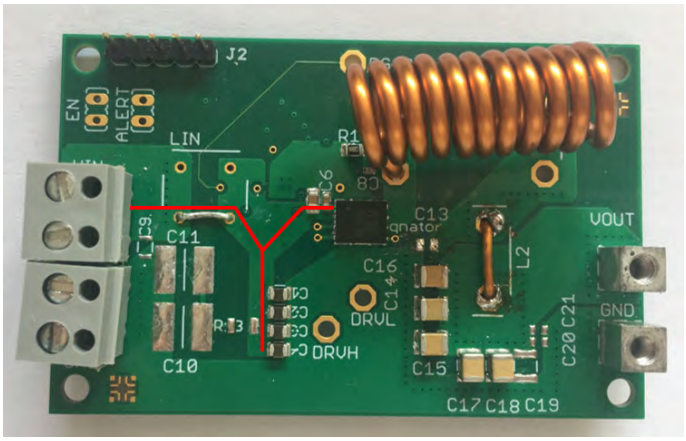


Figure 5.36: The course of the input current is not direct and produces a high di/dt loop.

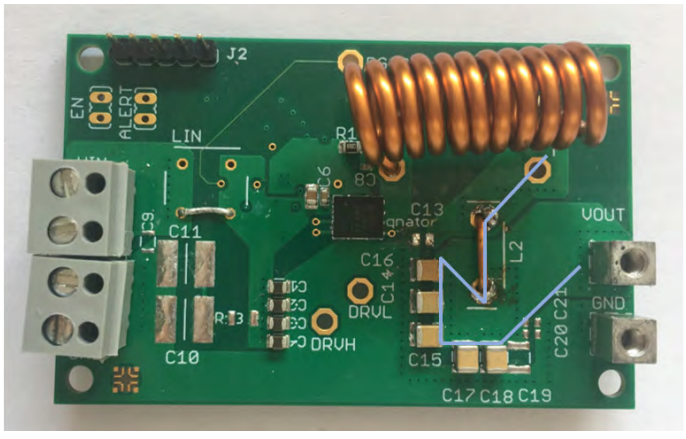


Figure 5.37: The output capacitors are L-shaped and noise can be amplified.

no longer guaranteed. Therefore the feedback node should be placed after C_{out} to feed a maximally filtered signal into the loop. In addition, cables should be kept as short as possible to minimize the probability of picking up noise and the effect of parasitic components. The cables running from V^+ and ground to the two voltage divider resistors should run parallel to each other and be very close together to again minimize the picked up noise. Last but not least it must be ensured that the feedback path is far away from all switching nodes and not below the inductor [45].

5.10 Cooling and Support Structure

The development of the cooling system and the integration of the Mu3e DC-DC converter into the support structure of the detector are still under development, but for the sake of completeness, they are be briefly presented here.
The support structure of the Mu3e detector is mounted on large wheels that can be pulled out of the detector and are located at both ends of the detector tube. The DC-DC converters are arranged in power crates as shown in figure 5.39. There are 4 power crates per support wheel. Each crate carries 16 DC-DC converters plus one control board. The size of the DC-DC converters is limited to $50 \times 90 \times 35\,\text{mm}$ and the boards should be water-cooled.
The support and cooling structure of the converters is shown in figure 5.38. The boards are mechanically clamped into H-shaped beams which are made of aluminium and through which the water is to flow for cooling. Over the hottest components of the converter a kind of box is attached which has contact to the H-beams. This box covers the large coil and the chip with the power MOSFETs and is intended to transport the heat produced there to the cooled holders. At the same time, the components where high currents are switched are shielded. This is to shield the other components from the HF switching noise.
In order to further advance the development of the cooling and support system, a first step is the development of a mockup PCB of the converter. A suitable support structure can then be developed.

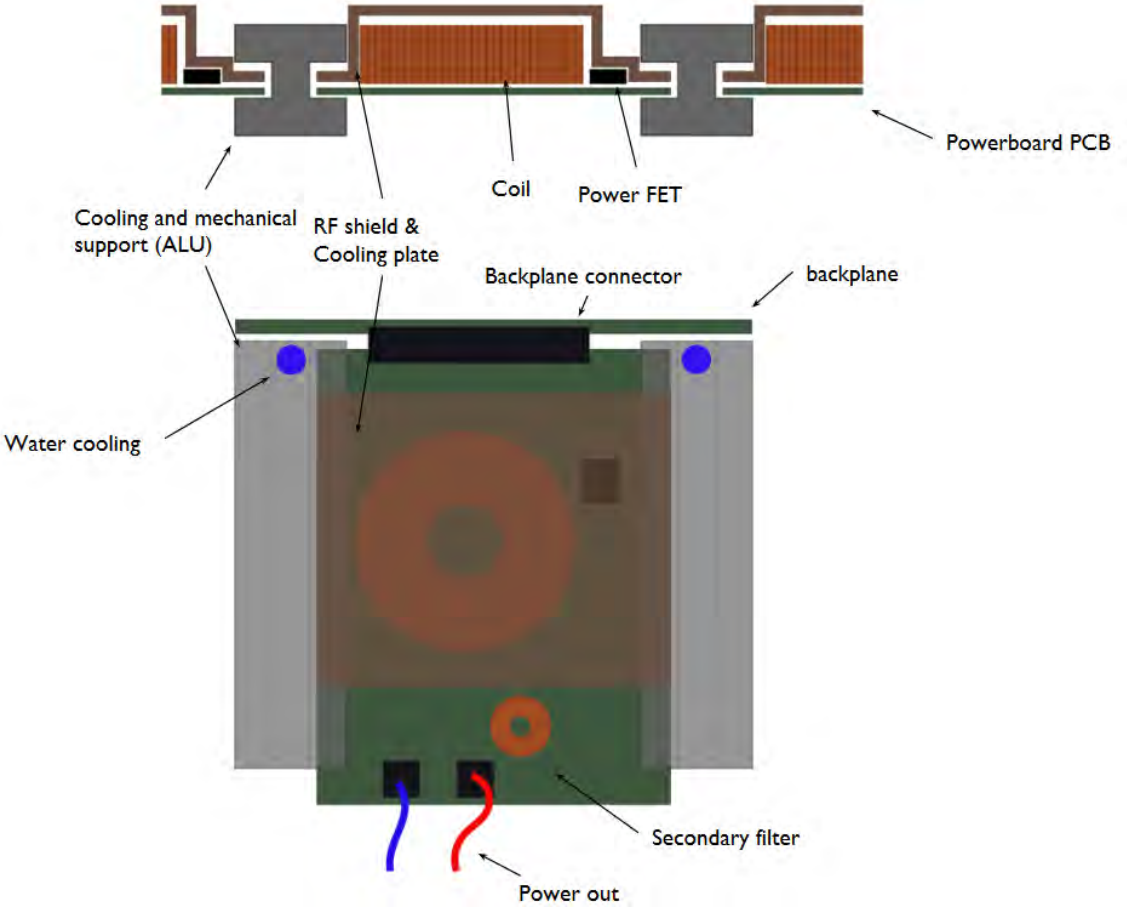


Figure 5.38: The support structure of the DC-DC converter is water-cooled [21]. A box above the hot components of the converter with contact to the holders derives the produced heat. At the same time, the box serves to shield HF switching noise.

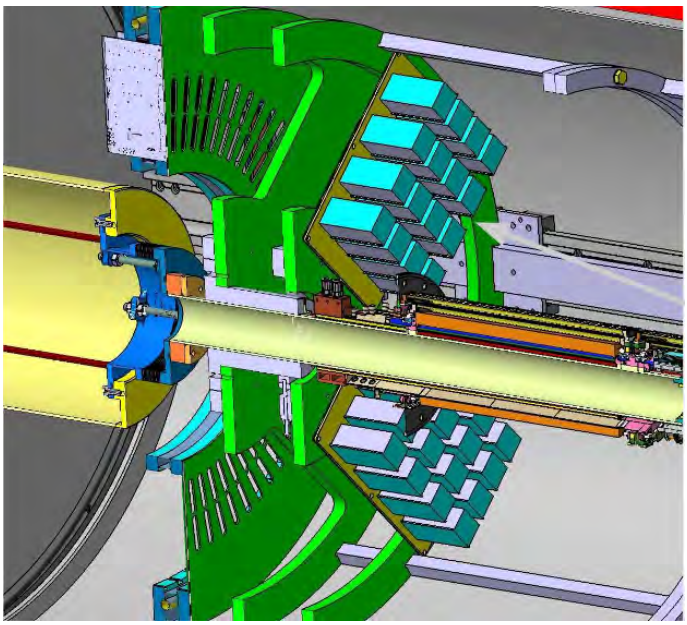


Figure 5.39: Implementation of the DC-DC converters in the support structure of the detector [21]. Shown are the 2 of the total 8 power crates on which 14-16 DC-DC converters and a control crate are located. The beam enters from the left, stopping target is just of-screen on the right.

Chapter 6

Conclusion and Outlook

The version 1 of the Mu3e DC-DC converter was able to achieve good results in the laboratory tests. The efficiency of 87.0 % at 10 A is in a very good range. The function of the converter is not impaired even under high loads such as the constant switching off of the controller. It was also checked that the individual components work reliably in a magnetic field.
The TPS53819A makes the converter controllable. With the help of the PMBus interface, important parameters of the converter can be set. For example, after starting the controller, the switching frequency must first be set to 1 MHz as this is not the default value. In addition, the PMBus commands provide the possibility to change the output voltage by ±9 %. This is important because always slight load fluctuations can occur which require an adjustment of the output voltage.
An important step was the investigation of the thermal behaviour of the board. It has been shown that the heating of the PCB is completed after a maximum of one minute. The hot spots of the design are as expected the switching chips and the coil. These informations are important for the development of an effective cooling system.
In a test beam it was investigated whether the MuPix sensors also work efficiently with power supplied by the DC-DC converter and if so, how well. The measurements were carried out with a converter without an output filter as well as the converter with an output filter. The results showed that the operation of MuPix sensor is not impaired. This is important information for the further development steps of the Mu3e DC-DC converters.
For version 2 of the Mu3e DC-DC converter, several innovations and improvements were designed and tested with the help of the simulation software Tine TI from Texas Instruments. For example, a new LC output filter was designed to reduce the height of the output ripples to $\leq 10\,\mathrm{mV}$.
In the new version there is also the possibility to monitor the current at the output of the converter in order to have a better information basis and thus a better control over the DC-DC converter. For this purpose, the voltage drop over a current-sense resistor is determined with the help of an instrumentation amplifier. Another new feature is a temperature interlock system. Here the DC-DC converter can be deactivated by a temperature diode on the MuPix module if the module becomes too hot regardless of the status of the sensor.
A new variant of the feedback loop now allows the consideration of the voltage drops in the connections between the converter and the detector components. Sense wires

are used to measure the voltage at a point in the cable chain and thus enable a more precise control of the output voltage. Furthermore, the grounding scheme is adapted such that the signal and power ground are separated from each other to prevent the noise from spreading through the ground plate. For all improvements in the second version of the DC-DC converter, it is possible to switch between the new and the old version. Unfortunately, due to the corona crisis that occurred in the final phase of this thesis, further tests in the laboratory could not be carried out. Therefore, the simulations became particularly important for the development. In particular, the cooling tests could not be completed. If an adequate cooling of the boron in the laboratory would have been possible, the performance of the converter could have been tested at the operating point of $I_{load} = 20\,A$.

On the way to the final version of the Mu3e DC-DC converter, there are still a few steps to do. As a first step it is necessary to create a module for the PCB of version 2 and to coordinate this with the workshops that are responsible for the mechanical design of the detector. The space provided for the DC-DC converter is very limited, which is why a precise agreement about the position of the large components such as coils or input and output plugs is extremely important for an optimal implementation of the regulator. At the same time, this model is also important for the development of a cooling system. The studies on the thermal development of the board have shown that cooling of the converter is absolutely necessary. The plan is to use an aluminium block with contact to the hottest components. This block has a connection to the carrier rails of the converter through which cold water runs and thus cools the board. The aluminium block also serves as shielding for the switching elements.
An important next step is of course the testing of the new DC-DC converter board. It must be checked whether the desired effects and parameters have been achieved and what influence the new elements have on the operation of the converter.
It is also important to test the new converter in a helium environment because the gas is located inside the detector and thus also encloses the converters.
A big step towards the operation within the experiment is the development of the controlling crates. All elements controlling the DC-DC converter are combined here. These include, for example, a microcontroller for the I^2C interface and the safety interlock systems.

Appendix A

Schematics Mu3e DC-DC Converter Version 1

Schematics of the Mu3e DC-Dc converter version 1. Due to space constraints, the circuit diagram was divided into several sections.

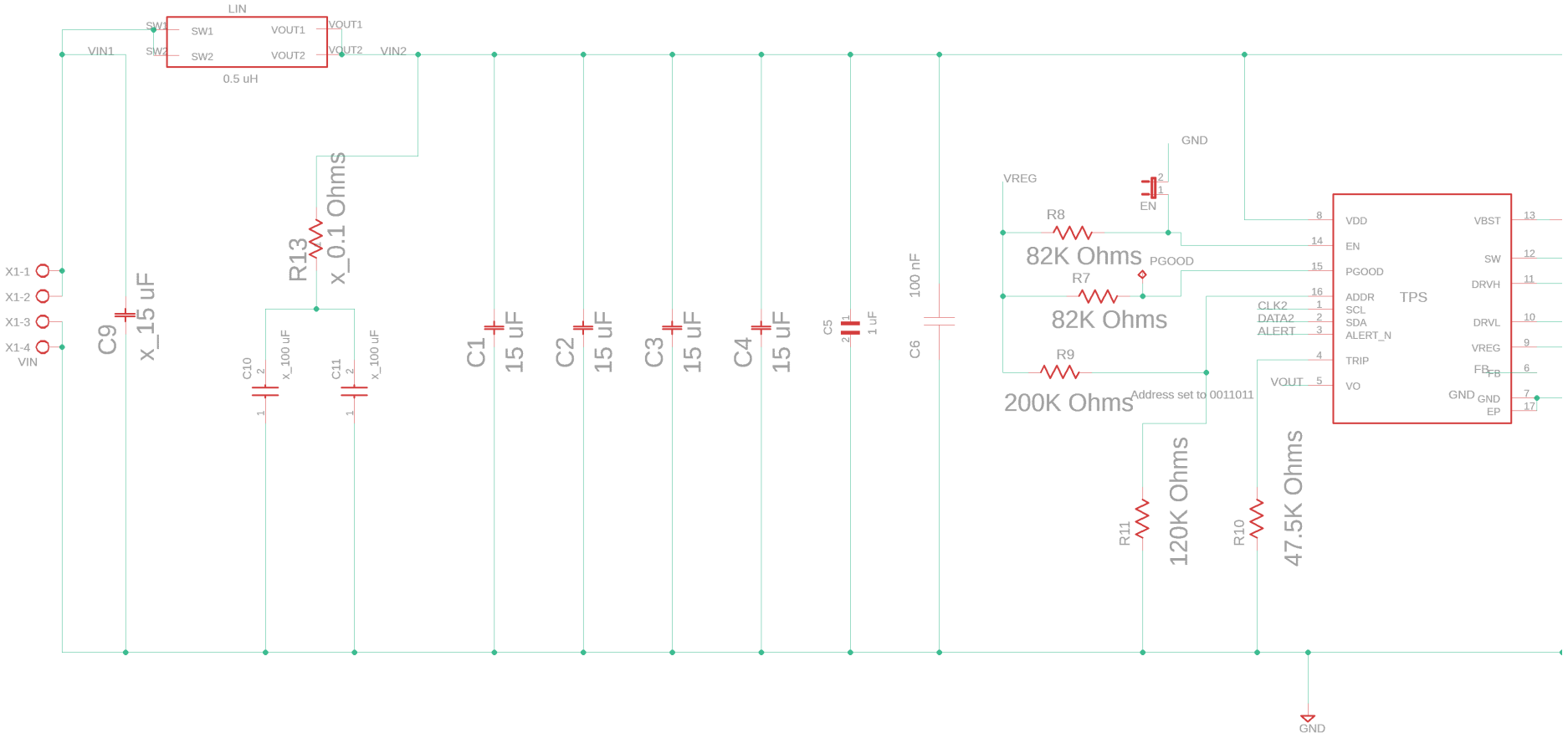


Figure A.1: Schematic of the Mu3e DC-DC converter version 1 part 1: Input connector; input capacitors; optional input LC filter; TPS53819A.

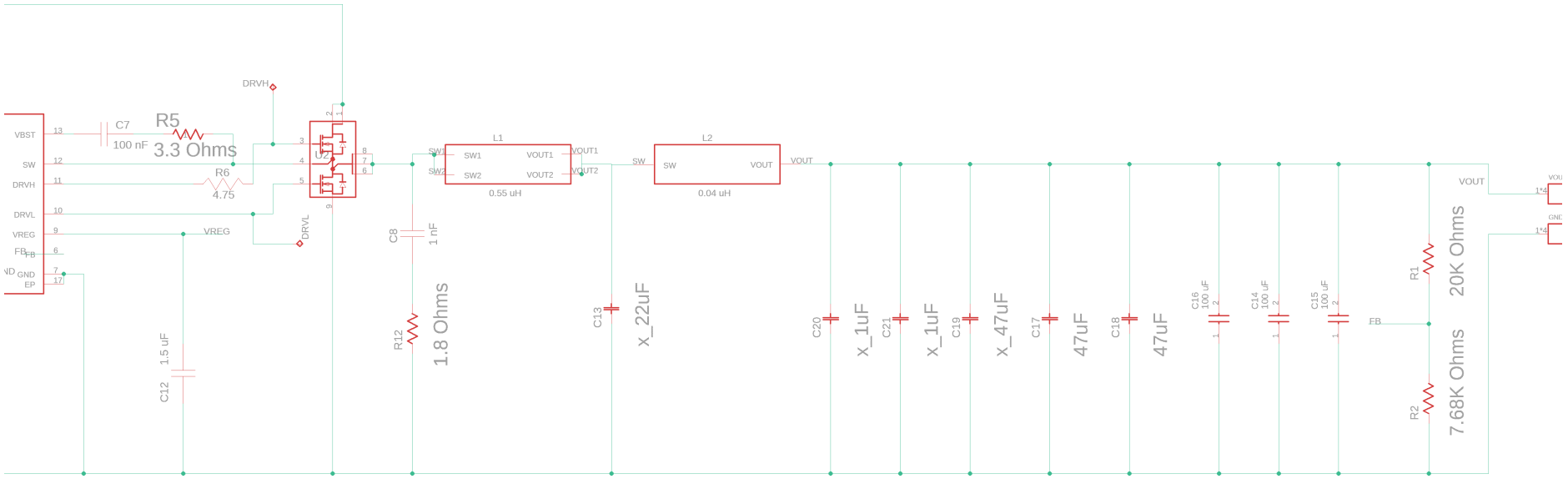


Figure A.2: Schematic of the Mu3e DC-DC converter version 1 part 2: TPS53819A; CSD86360Q5D; coil ; second LC filter; output connectors.

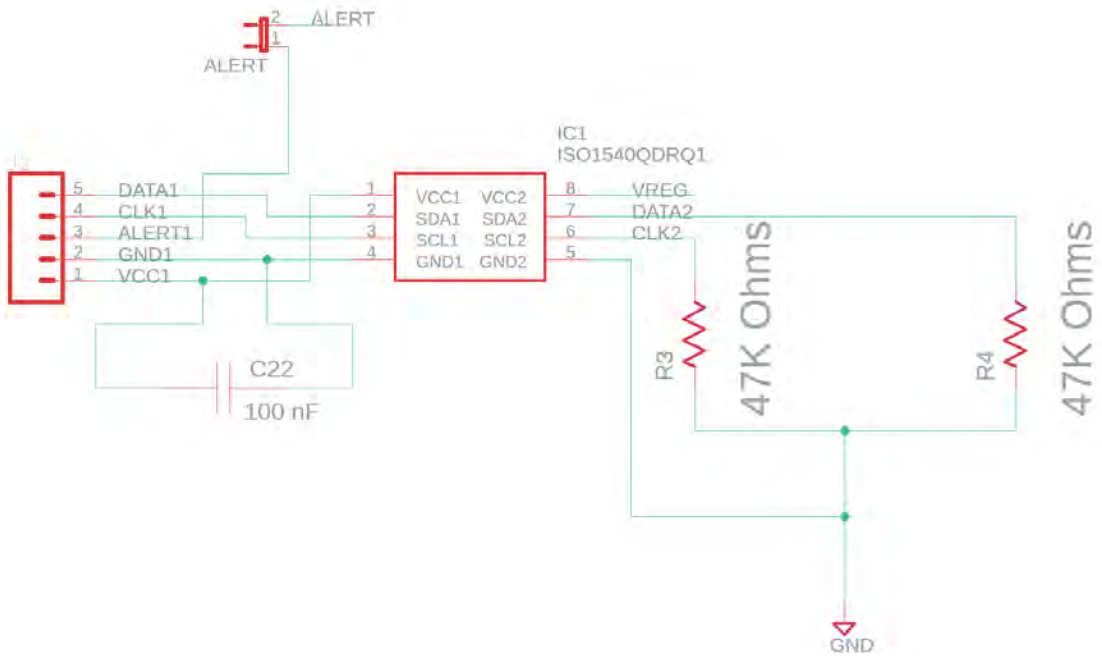


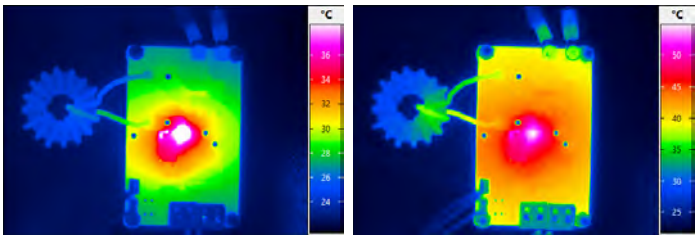
Figure A.3: Implementation of the PMBus interface.

Appendix B

Thermal Behaviour

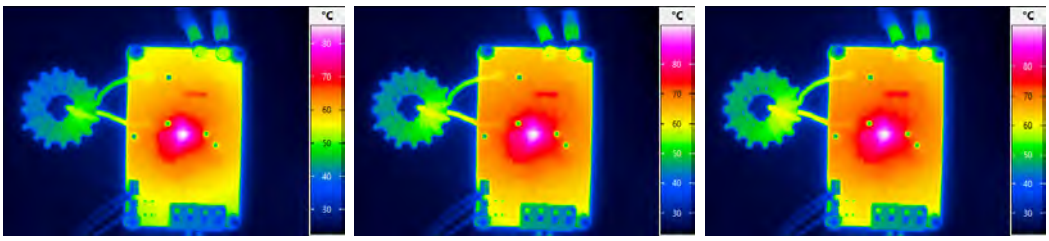
Infrared images of the Mu3e DC-DC converter.

B.1 Frontside



(a) After 30 seconds. **(b)** After 5 minutes.

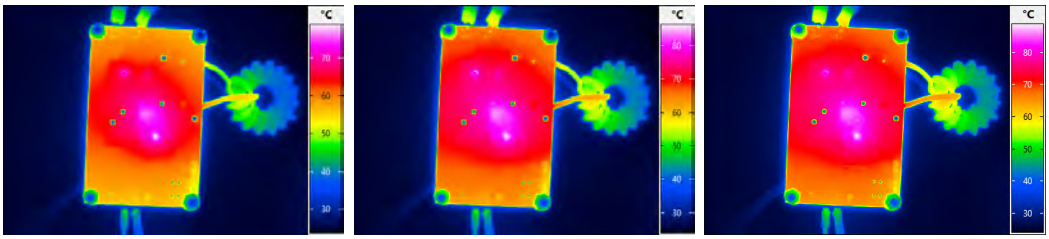
Figure B.1: Infra red images of the front at $I_{load} = 5.5\,A$.



(a) After 30 seconds. **(b)** After 5 minutes. **(c)** After 10 minutes.

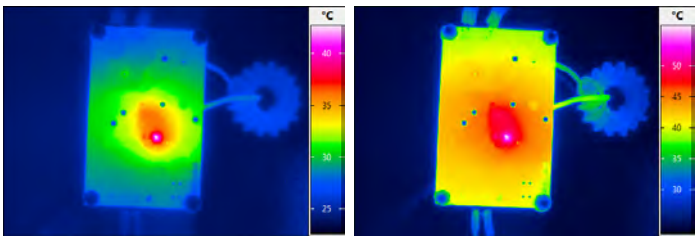
Figure B.2: Infra red images of the front at $I_{load} = 13\,A$.

B.2 Backside



(a) After 30 seconds. **(b)** After 5 minutes. **(c)** After 10 minutes.

Figure B.3: Infra red images of the backside at $I_{load} = 13\,A$.



(a) After 5 minutes. **(b)** After 10 minutes.

Figure B.4: Infra red images of the backside at $I_{load} = 5.5\,A$.

Appendix C

Bill of Material for the Mu3e DC-DC Converter Version 2

Part		Value	Device
ALERT			JP1E
C1		22 uF	C2012X5R1V156M125AC
C2		22 uF	C2012X5R1V156M125AC
C3		22 uF	C2012X5R1V156M125AC
C4		22 uF	C2012X5R1V156M125AC
C5		1 uF	C2012X6S1H105M125AB
C6		100 nF	CGA3E3X7S2A104K080AB
C7		100 nF	CGA3E3X7S2A104K080AB
C8		1 nF	CGA2B2X7R1H102K050BA
C9		1 uF	C2012X6S1H105M125AB
C12		1.5 uF	C1005X6S1C155K050BC
C13		47uF	GRM32ER60J476ME20L
C14		100 uF	GRM32ER60J107ME20L
C15		100 uF	GRM32ER60J107ME20L
C16		100 uF	GRM32ER60J107ME20L
C17		47uF	GRM32ER60J476ME20L
C18		47uF	GRM32ER60J476ME20L
C19		47uF	GRM32ER60J476ME20L
C20		100 uF	GRM32ER60J107ME20L
C22		100 nF	CGA3E3X7S2A104K080AB
C23		0.1uF	GRM188R60J105KA01D
C24		0.5nF	GRM188R60J105KA01D
C25		1uF	GRM188R60J105KA01D
C26		0.1uF	GRM188R60J105KA01D
C27		0.5nF	GRM188R60J105KA01D
C28		1uF	GRM188R60J105KA01D
C29		0.1uF	GRM188R60J105KA01D
C30		0.5nF	GRM188R60J105KA01D
C31		1uF	GRM188R60J105KA01D
CUREN	T	PTR1B2,54	PTR1B2,54
D1		MMBD1201	MMBD1201
DRVH		TPPAD1-20	TPPAD1-20
DRVL		TPPAD1-20	TPPAD1-20
GND			WP-BUFU_7462810
IC1		ISO1540QDRQ1	ISO1540QDRQ1
J1		MPSC-01-24-01-01-01-L-RA	#NAME?
L1		0.55 uH	MAIN_COIL
PGOOD		TPPAD1-20	TPPAD1-20
R1		20K Ohms	RC0603FR-0720KL
R2		7.68K Ohms	RC0603FR-077K68L
R3		1.5K Ohms	RC0603FR-0782KL
R4		1.5K Ohms	RC0603FR-0782KL
R5		3.3 Ohms	CRCW06033R30FKEA
R6		4.75 Ohms	CRCW06034R75FKEA
R7		100K Ohms	RC0603FR-0782KL
R8		3224W-1-222E	3224W-1-222E
R9		200K Ohms	RC0603FR-07200KL
R10		48.5K Ohms	RC0603FR-0747K5L

R11		120K Ohms	RC0603FR-07120KL
R12		1.8 Ohms	RC0805FR-071R8L
R13		3.3 Ohms	CRCW06033R30FKEA
R14		20K Ohms	RC0603FR-077K68L
R15		200K Ohms	RC0603FR-077K68L
R16		100 Ohms	RC0603FR-077K68L
R17		400K Ohms	RC0603FR-077K68L
R18		200K Ohms	RC0603FR-077K68L
R19		100 Ohms	RC0603FR-077K68L
R20		220 Ohms	RC0603FR-077K68L
R21		100K Ohms	RC0603FR-077K68L
R22		1M Ohms	RC0603FR-077K68L
R23		21K Ohms	RC0603FR-077K68L
R24		1 MOhms	RC0603FR-077K68L
R25		FKK5R0020FE-TR	FKK5R0020FE-TR
R26		400K Ohms	RC0603FR-077K68L
R27		200K Ohms	RC0603FR-077K68L
R28		100 Ohms	RC0603FR-077K68L
R30		100 Ohms	RC0603FR-077K68L
R31		59k Ohms	RC0603FR-077K68L
SJ1			SJ2WW
SJ2			SJW
SJ3			SJ2WW
TPS			TPS53819ARGTR
U$1		LM334Z/LFT1	LM334Z/LFT1
U$2		L2	L2
U1		INA326EA/250	INA326EA/250
U2			CSD86360Q5D
U3		INA326EA/250	INA326EA/250
U4		OPA333AIDBVR	OPA333AIDBVR
U5		PMBF4391SOT23_NXP-L	PMBF4391SOT23_NXP-L
U6		INA326EA/250	INA326EA/250
U7		DS18B20	DS18B20
VDIFF		PTR1B2,54	PTR1B2,54
VOUT			WP-BUFU_7462810
VTHRE	SH	PTR1B2,54	PTR1B2,54
X1		2059-303/998-403	2059-303/998-403

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