Department of Physics and Astronomy

University of Heidelberg

Bachelor Thesis in Physics

submitted by

Paul Vincent Wolf

born in Berlin-Spandau (Germany)

July 2023

On-chip temperature measurements and studies of temperature effects on the pulse shaping of the MuPix11

— Updated version from 29 July 2023 —

This Bachelor Thesis has been carried out
by Paul Wolf at the
Physikalisches Institut of the University of Heidelberg
under the supervision of
Prof. Dr. André Schöning

Abstract

The Mu3e experiment searches for the charged lepton flavour violating decay $\mu^+ \to e^+e^-e^+$ with an unprecedented single event sensitivity of 2×10^{-15} in phase I. To achieve this goal, the detector needs to provide excellent vertex, time and momentum resolution for low momentum particles at high muon rates of 1×10^8 Hz. The technology of choice are high voltage monolithic active pixel sensor (HV-MAPS) which allows to build ultra-thin sensors that minimise multiple Coulomb scattering with a thickness 0.115 % of the radiation length per layer. For phase I of the Mu3e experiment, the MuPix11 pixel sensor is used in the tracking detector.

In this thesis, on-chip temperature measurements were performed and the temperature effect on the signal shaping of the MuPix11 was studied. As active pixel sensors dissipate heat, both reliable monitoring of chip temperatures and understanding of temperature effects on the detector are critical. Therefore, measurements were carried out in a climatic chamber at ambient temperatures in a range from $-10\,^\circ$C to $+70\,^\circ$C.

Calibration methods for the on-chip temperature sensors has been developed which enables absolute temperature measurements. These measurements provide insight into the heat distribution within the MuPix11 sensor. For the first time, digital temperature measurements have been successfully implemented using the on-chip analogue-to-digital converter and the digital readout. Furthermore, investigation of the signal shaping shows significant temperature effects on the width of the signals. The analysis of the temperature dependence of the Time-over-Threshold spectrum of 100 pixels reveals a linear decrease in pixel-to-pixel variation with increasing temperature, particularly at low thresholds. In addition, the functionality of the bandgap current reference circuit designed to compensate for first-order temperature effects is verified.

Based on these results, suggestions are made for possible temperature calibration methods in the Mu3e experiment and the limitations of digital temperature measurements are discussed. These findings will contribute to the optimisation and successful implementation of the MuPix11 in the Mu3e experiment.

Kurzzusammenfassung

Das Mu3e-Experiment sucht nach dem geladenen leptonenfamilienzahlverletzenden Zerfall $\mu^+ \to e^+e^-e^+$ mit einer Einzelereignisempfindlichkeit von 2×10^{-15} in Phase I. Um dieses Ziel zu erreichen, muss der Detektor eine hervorragende Orts-, Zeit- und Impulsauflösung für Teilchen mit geringem Impuls von hohen Myonenraten von 1×10^8 Hz bieten. Dies wird mit hochspannungsbetriebenen monolitischen aktiven Pixelsensoren (HV-MAPS) erreicht. Diese Technologie ermöglicht ultradünne Sensoren, die die Coulomb-Vielfachstreuung mit einer Materialdicke von 0.115 % einer Strahlenlänge pro Detektor-Lage minimieren.

In dieser Arbeit wurden auf dem Chip Temperaturmessungen durchgeführt und der Temperatureffekt auf die Signalformung des MuPix11 untersucht. Da aktive Pixelsensoren Wärme erzeugen, sind sowohl die zuverlässige Überwachung der Chiptemperaturen als auch das Verständnis der Temperatureffekte auf den Detektor von entscheidender Bedeutung. Daher wurden Messungen in einer Klimakammer bei Umgebungstemperaturen in einem Bereich von $-10\,^\circ$C to $+70\,^\circ$C durchgeführt.

Es wurde eine Kalibrierungsmethode für die integrierten Temperatursensoren entwickelt, die absolute Temperaturmessungen ermöglicht. Diese Messungen geben Aufschluss über die Wärmeverteilung im Inneren des MuPix11-Sensors. Mit dem integrierten Analog-Digital-Wandler und der Auslese über den Datenstrom ist es erstmals gelungen, digitale Temperaturmessungen zu realisieren. Darüber hinaus zeigt die Untersuchung der Signalformung signifikante Temperaturauswirkungen auf die Breite der Signale. Die Analyse der Temperaturabhängigkeit des Time-over-Threshold-Spektrums von 100 Pixeln zeigt eine lineare Abnahme der Pixel-zu-Pixel-Variation mit steigender Temperatur, insbesondere bei niedrigen Schwellenwerten. Darüber hinaus wird die Funktionalität der Bandlückenstrom-Referenzschaltung zur Kompensation von Temperatureffekten erster Ordnung verifiziert.

Auf der Grundlage dieser Ergebnisse werden Vorschläge für mögliche Methoden zur Temperaturkalibrierung im Mu3e-Experiment gemacht und die Grenzen digitaler Temperaturmessungen diskutiert. Diese Erkenntnisse werden zur Optimierung und erfolgreichen Implementierung des MuPix11 im Mu3e-Experiment beitragen.

Contents

1 Introduction

The Standard Model of Particle Physics (SM) is the best-known theory describing all visible matter in the universe and its interactions. Its precise predictions, confirmed by experiments around the world - most recently the discovery of the Higgs boson [1, 2] - have been a major success in particle physics in recent decades [3].

However, the SM still leaves open questions that motivate scientists to continue to challenge our understanding of the universe: It fails to incorporate gravity as the fourth known fundamental force, it does not explain the matter-antimatter asymmetry that formed the universe nor does it solve the mystery of dark matter. With the experimental confirmation of neutrino oscillation [4, 5, 6], it had to be extended to account for the mass of neutrinos.

This drives physicists to come up with new theories beyond the SM to explain such phenomena. Some of these include new heavier particles that have yet to be discovered. This is the main focus of large-scale experiments such as the Large Hadron Collider [7] or the Future Circular Collider [8], which is planned to provide centre-of-mass energy scales of 100 TeV.

In parallel, experiments are being carried out to search for rare phenomena that are not predicted by the SM. The Mu3e experiment aims to study a decay that is heavily suppressed in the SM, but is predicted in higher rates by theories beyond the SM: $\mu^+ \to e^+e^-e^+$[9]. For this purpose, a novel high-voltage monolithic active pixel sensor (HV-MAPS) detector has been developed in recent years. It provides excellent energy resolution for high rates of low-momentum charged particles due to minimal material budget of the sensors. Therefore, this decay can be tracked with an unprecedented single event sensitivity of 1×10^{-16}[10].

As active pixel sensors dissipate heat, cooling and temperature monitoring are required to prevent overheating of the detector. This thesis characterises the final HV-MAPS sensor MuPix11 that will be used in the tracking detector of the Mu3e experiment. The first and second parts of this thesis deal with the physical background and the setup for the measurements. Part III focuses on the integrated temperature sensors of the chip. Their calibration is performed and temperature measurements are examined, giving an insight into the heat distribution on the chip. Additionally, possible applications of the temperature sensors in the Mu3e experiment are discussed. The last part focuses on the performance of the MuPix11 under temperature changes.

1.1 Physics Motivation

To understand what the Mu3e experiment is searching for, some background in particle physics is required. This chapter covers the basic concepts of particle physics and motivates the search for charged lepton flavour violation.

1.1.1 Standard Model of Particle Physics

The Standard Model of Particle Physics is a quantum field theory that describes all known elementary particles in the universe and their interactions. It successfully unifies the electromagnetic and weak interactions and combines them with the strong interaction. It classifies particles into fermions (spin-1/2 particles) and bosons (spin-1 particles), as shown in Figure 1.1.

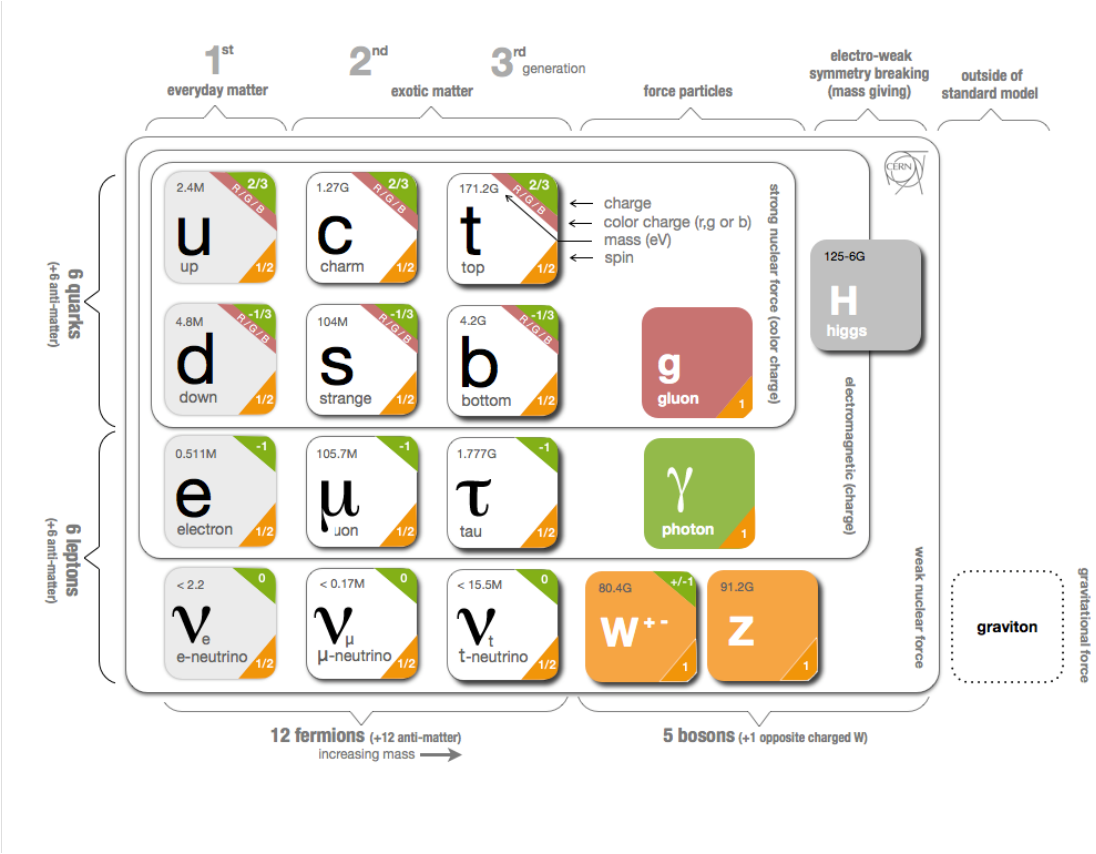


Figure 1.1: Diagram of the Standard Model of Particle Physics [11]

The fermions are further subdivided into 3 generations of quarks and leptons. In each generation, there is a lepton with the electric charge of -1 (electron, muon, tauon) and one with charge 0 called neutrinos. All fermions have associated anti-fermions with opposite quantum numbers. The two quarks of each generation have charges of $+2/3$ and $-1/3$ respectively. While the other generations are copies of

the first one with slightly increasing mass for each particle, the quarks of the first generation and the electron make up all the known matter around us.

The known bosons are classified into the only scalar boson (spin = 0), gauge bosons (spin = 1). The only spin-0 boson, the Higgs boson, can be described as an excitation of the Higgs field whose interaction provides mass to particles via the Higgs mechanism [12, 13]. The gauge bosons carry the fundamental forces: The photon couples to electric charge and mediates the electromagnetic force. The massive gauge bosons Z, $W^{+/-}$ carry the weak force and couple to the weak isospin. The strong force is mediated by gluons. They couple to colour charge, which only quarks and gluons carry.

As known from other areas of physics, there are conserved quantities such as energy and momentum. In addition, in SM there are conserved quantum numbers like the electric charge or the baryon number. A baryon is a particle that is composed of an odd number (usually three) of valence quarks. The baryon number B is calculated from the number of quarks n_q and the number of antiquarks $n_{\overline{q}}$: $B = 1/3(n_q - n_{\overline{q}})$. Since the baryon number is conserved, there is no known process in where the baryon number of the initial and final particles is different.

In classical SM, both the lepton number and the lepton flavour are conserved. The lepton number of a system L is defined as the number of leptons n_l minus the number of anitleptons $n_{\overline{l}}$. In addition, lepton family numbers (lepton flavors) are introduced, which divide the lepton number into the electron number L_e for electrons and electron neutrinos, the muon number L_μ for muons and muon neutrinos, and the tau number L_τ for tauons and tau neutrinos.

1.1.2 Charged Lepton Flavor Violation

The discovery of neutrino oscillation challenges the lepton flavour conservation of the SM. It was shown that neutrinos change their lepton number with periodic probability as they propagate through space [5, 6]. Thus, the SM has been extended to allow neutrinos to carry mass and to allow lepton flavour violation (LFV) for neutral leptons (neutrinos), while still conserving the total lepton number L [14]. With this extension, charged lepton flavour violation (CLFV) via loop with neutrino oscillation would also be possible, as shown in Figure 1.2. However, these processes are still strongly suppressed by $\sim O(10^{-50})$.

Other theories such as supersymmetry models or extended gauge theories inherently include LFV [15]. They allow charged lepton flavor violation processes that are much less suppressed than predicted by SM. In the search for validation of the CLFV predictions of beyond SM theories, muon decays have been studied in several

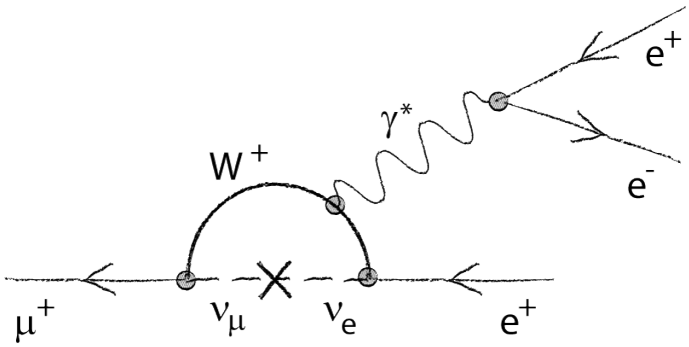


Figure 1.2: Feynman diagram of the CLFV decay $\mu^+ \to e^+e^-e^+$ via loop that is allowed by the SM including neutrino oscillation.

Decay	current limit	future experiment	projected SES
$\mu \to eee$	1.0×10^{-12} [16]	Mu3e (phase I)	2×10^{-15}
		Mu3e (phase II) [10]	$\leq 1 \times 10^{-16}$
$\mu \to e\gamma$	4.2×10^{-13} [17]	MEG-II [18]	6×10^{-14}
$\mu N \to eN$	7.0×10^{-13} [19]	COMET (phase II) [20]	2.6×10^{-17}
		Mu2e [21]	3×10^{-17}

Table 1.1: Overview of current limits for lepton flavour violation experiments with muon decays and projected SES in future experiments. Taken from [22].

experiments. There are trhee possible muon decays to search for CLFV:

$$\begin{aligned} &N\mu \to Ne. \\ &\mu \to e + e + e, \quad \text{and} \\ &\mu \to \gamma + e \end{aligned} \tag{1.1}$$

Current experimental limits and predicted single event sensitivities (SES) for future experiments investigating these decays are given in Table 1.1.

1.2 The Mu3e Experiment

The Mu3e experiment aims to search for the CLFV decay $\mu^+ \to e^+e^-e^+$ or to set a new branching fraction exclusion limit of $> 1 \times 10^{-16}$ with 90 % confidence level [9, 10]. At present, no existing muon beam can provide the required rate of 1×10^9 Hz needed for the targeted sensitivity for phase II. Therefore, the phase I of the experiment is planned to achieve an SES of 2×10^{-15} over a one-year runtime with the currently available beam rate of 1×10^8 Hz at the Paul Scherrer Institute (PSI). For phase II, a more intense beam is needed to provide the required muon stopping rate, which is still under development at PSI [23].

1.2.1 The $\mu^+ \to e^+e^-e^+$ decay

The $\mu^+ \to e^+e^-e^+$ decay is possible in the extended SM via loop including neutrino oscillation, as shown in Figure 1.2. However, its branching ratio is suppressed to $< 1 \times 10^{-54}$ [24]. In beyond SM theories, the branching ratio can be enhanced. Any observation of this decay would be a sign of beyond SM physics.

In the MU3E experiment, background events can occur that mimic the signal topology. There are several background processes that produce electrons and positrons without violating the lepton flavour conservation and could be misinterpreted as a $\mu^+ \to e^+e^-e^+$ decay.

Combinatorial background comes from multiple processes that reproduces the searched decay topology. The Michel decay

$$\mu^+ \to e^+\nu_e\bar{\nu_\mu} \tag{1.2}$$

has a branching ratio of $\approx 100\,\%$. This decay can combine with a Bhabha scattering of the decay positron with an electron in the stopping target. This can recreate the signal topology ${}^+e^-e^+$. Both processes do not share the same vertex or decay time. Thus, this background can be suppressed with high vertex and time resolutions that can distinguish the two decays.

Irreducible background describes the production of the same particle signature within a single process. An example is the decay:

$$\mu^+ \to e^-\bar{\nu_e}\,\nu_\mu e^+e^-. \tag{1.3}$$

It has a branching ratio of $(3.4 \pm 0.4) \times 10^{-5}$ [15] and produces two additional neutrinos that cannot be detected by the detector. The conservation of energy and momentum is used to filter out this background. When the muons decay at rest, the total momentum of the particles produced also vanishes. Due to the energy conversion, the invariant mass must remain the same:

$$|\vec{p}_{tot}| = |\sum \vec{p}_i| = 0 \quad \Rightarrow \quad m_{inv} = \sum E_i = m_\mu c^2 \approx 105.66\,\mathrm{MeV} \tag{1.4}$$

with i, all the decay particles are indexed. The remaining energy of the muon is shared by the decay particles. With sufficient energy resolution, it is possible to identify the energy carried away by undetected neutrinos. This allows the irreducible background to be excluded from the measurement.

Therefore, the tracking detector of the MU3E experiment requires a mass resolution better than 1 MeV, which is one of the main challenges for the MU3E detector.

1.2.2 The Mu3e Experimental Setup

The design concept of the phase I experiment is shown in Figure 1.3. The beam hits a hollow double-cone target, which stops the muons. The tracking detector consists of four layers of pixel sensors radially surrounding the target. The two inner layers act as vertex detectors. Together with the 1 T solenoidal magnetic field aligned along the beam axis, the outer layers act as momentum detectors by determining the bending radius of the deflected particles. Particles that bend back and reenter the outer layers allow improved momentum resolution and better reconstruction of their tracks, as their bend radius can be more accurately determined and more hits are provided. The recurl layers are added to increase the number of reentering particles.

The momentum resolution is mainly constrained by multiple Coulomb scattering in the detector which makes it crucial to minimise the material budget of the detector. Therefore, High-Voltage Monolithic Active Pixel (HV-MAPS) technology is used(see subsection 1.3.3). The ultra-thin silicon pixel sensors allow for relative radiation lengths of approximately $X/X_0 = 0.115\,\%$ per layer in the tracking detector. Their main requirements for the Mu3e experiment are listed in Table 1.2.

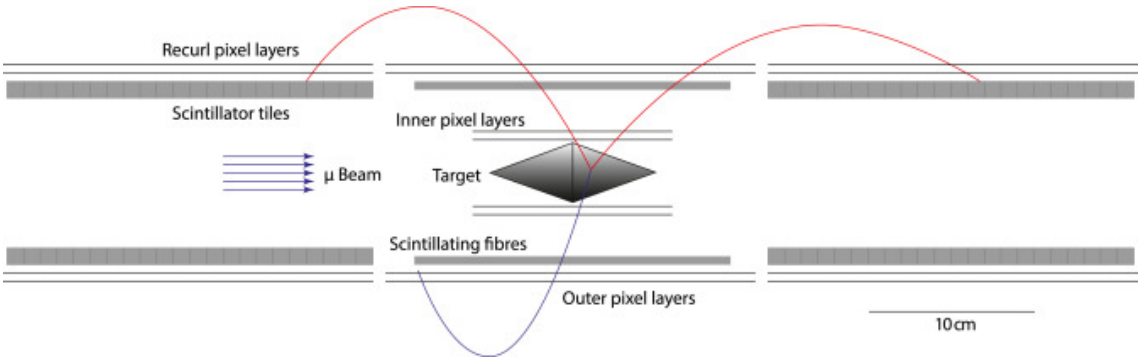
thickness [µm]	≤ 50
spacial resolution [µm]	≤ 30
time resolution [ns]	≤ 20
hit efficiency [%]	≥ 99
# LVDS links (inner layers)	1 (3)
bandwidth per link [Gbit/s]	≥ 1.25
power density of sensors [mW/cm^2]	≤ 350
operation temperature range [°C]	0 to 70

Table 1.2: Mu3e pixel sensor requirements. Taken from [10].

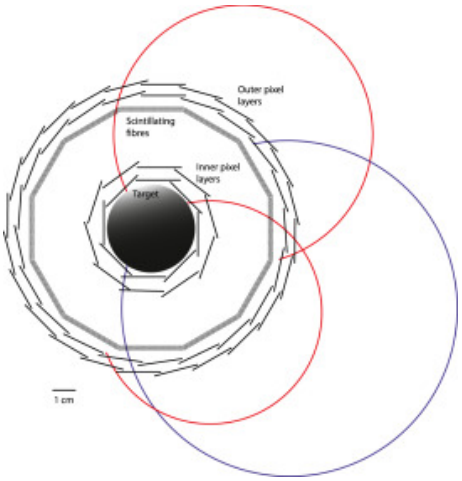
The time detection is covered by scintillating fibres and scintillating tiles. They are responsible for determining the charge of the traversing particles in the case of recurl. The time resolution of the tracking detector is not sufficient to identify the time sequence of hits within a track. The tracks are extrapolated and assigned to hits in the fibre and tile detectors. This allows the direction of rotation of recurling particles to be determined, which corresponds to the charge [10].

1.2.3 Detector Cooling and Temperature Monitoring

All active detector systems dissipate heat. The tracking pixel sensor at Mu3e is assumed to have a power consumption of ~ 200 mW/cm^2 to 400 mW/cm^2. Without considering the surrounding material, a conservative calculation for 350 mW/cm^2 leads to chip temperatures of up to > 140 °C without cooling [22].



(a)



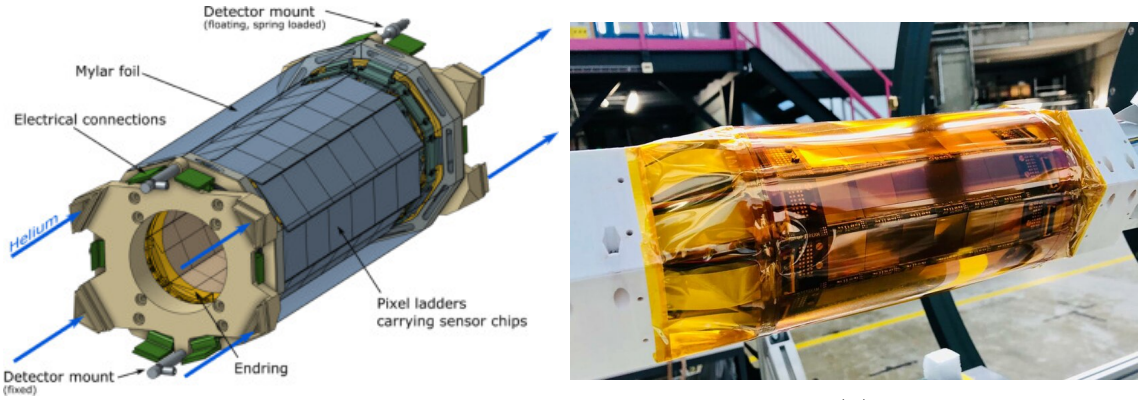
(b)

Figure 1.3: Schematic view of the MU3E experimental setup for phase I. a) Side view cut along the muon beam axis. b) Front view cut transverse to the beam axis. Taken from [10].

For pixel particle detectors, high temperatures increase radiation damages in the substrate for non-ionising energy loss processes (NIEL-effects) [25]. For the MU3E experiment, this bulk damage in the silicon is negligible because the radiation from the traversing particles will be predominantly ionising. Therefore, the temperature limitations for the tracking detector are defined by construction requirements. The chips are be bonded to and glued on aluminum-polyimide laminate ladders, each carrying six sensors in a row (see Figure 1.4a). Hence, their temperature must not exceed the adhesives' glass transition temperatures of 70 °C [10].

This makes a cooling system and temperature monitoring indispensable. The timing detector's readout electronics and front-end boards are cooled by a water cooling system. Conventionally, liquid cooling is also used for active pixel detectors. However, their tubing and high-density cooling substrate are not compatible with the discussed requirements of a low material detector budget to minimise multiple Coulomb scattering. Therefore, an ambient pressure helium cooling system has

been developed using commercially available turbo compressors [26]. They supply the three outer stations each with 16 g/s each and the vertex detector with 2 g/s of cooled helium at 0 °C as a baseline temperature and ambient pressure [22]. The images in Figure 1.4 show the CAD rendering of the vertex barrel and a prototype.



(a) (b)

Figure 1.4: Model and prototype of the vertex barrel for the tracking detector. a) Schematic view of the vertex detector. Eight inner and ten outer ladders carry six chips each. The maylar foil has been cut out for better visibility. Taken from [10]. b) The vertex barrel prototype that was tested with helium cooling. The polyimide foil confines the outer helium flow. Taken from [22].

For temperature monitoring, the chips themselves contain integrated temperature sensors in the periphery (see subsection 1.4.3). The construction temperature limitations apply to an average temperature of the active pixel matrix, where the chips are glued to a ladder. Hot spots in the periphery are expected to exceed the average temperature, which poses the challenge of correctly estimating the active matrix temperature from measurements in the periphery. This is discussed further in this thesis (see chapter 3).

1.3 Technological Choice of the Tracking Detector

The requirement for processing hit rates of 5 MHz and excellent momentum resolution of 1 MeV for the tracking detector in the Mu3e experiment is met by HV-MAPS technology. This cutting-edge technology has been developed over the last 20 years and promises to be well suited to future particle detectors. For the Mu3e experiment, the MuPix series was developed, with the MuPix11 being the final version to be used in the tracking detector in phase I. This section gives an introduction to semiconductor physics and pixel detectors. It then outlines the key concepts of HV-MAPS technology and describes the MuPix11 chip itself.

1.3.1 Semiconductor Physics

Based on their electrical properties, materials can be classified as conductors, resistors or semiconductors. In semiconductors, the gap between the valence and conduction bands is so small that electrons can cross it by thermal excitation. This makes the resistivity of semiconductors highly temperature dependent. It falls with rising temperatures and rises with decreasing temperatures [27].

To artificially enhance the resistivity of a semiconductor, impurity atoms with a small difference in valence electrons (usually one) can be added to the lattice. This is called doping. If impurity atoms with a higher valence electron number are introduced into the semiconductor, this is called n-doping. They act as donors because they carry an electron that isn't used in the covalent bonds of the lattice and can therefore be easily thermally excited. Doping with atoms with lower valence electrons (acceptors) is called p-doping and leaves electron holes in the lattice.

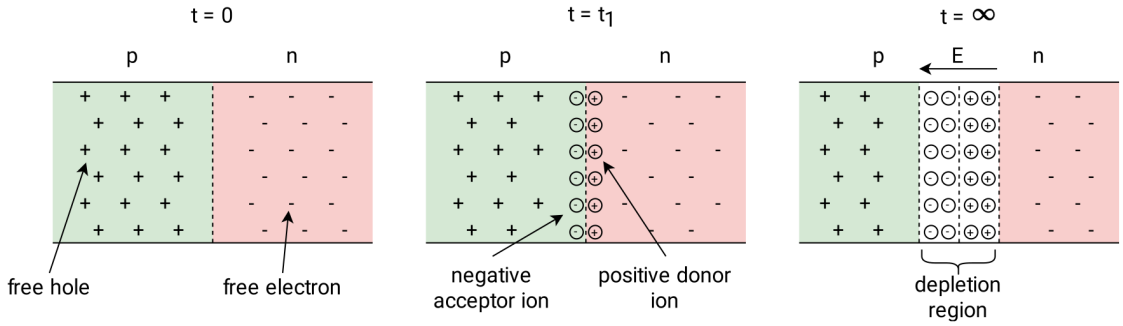


Figure 1.5: Schematic of a pn-junction. Electrons and holes diffuse towards the interface at $t = t_1$. Here, they recombine, leaving behind ionised donors and acceptors that generate an E-field. Equilibrium is reached at $t = \infty$ and a depletion zone is formed. Based on [28]

When a p-doped and a n-doped semiconductor meet, it is called pn-junction or diode. The free electrons in the n-doped substrate diffuse into the p-doped substrate. There, they meet diffusing holes, creating a zone of no free charge carriers, called depletion zone, as shown in Figure 1.5. The current generated by the diffusing charge carriers is called diffusion current. The positively charged donors which are left behind by the electrons in the n-doped material create an electric field together with the negatively charged p-doped side. This field itself generates a drift current with randomly generated electron-hole pairs from thermal excitation. This current is only dependent on temperature and opposes the diffusion current resulting in an equilibrium for long enough time scales. The in-built potential U_b created by the field and the length of the depletion zone are two of the main characteristics of a pn-junction.

For solid silicon, which forms four valence bonds in a diamond-like crystal struc-

ture, a typical value for the U_b is:

$$U_b = \frac{k_B T}{e} \cdot \log\left(\frac{N_A N_D}{n_i^2}\right) \overset{Si}{\approx} 0.6 - 0.8\,V \tag{1.5}$$

with the Boltzmann constant k_B, the acceptor and donor concentration N_A and N_D, the intrinsic charge carrier density n_i^2, the temperature T and the elementary charge e [25]. For highly doped silicon as in the MuPix sensors, the internal voltage exceeds 1 V.

An external voltage U_{ext} will affect the current balance and change the electrical properties depending on the direction. A voltage applied opposing the in-built potential is called forward bias. The depletion zone will shorten, and the current will increase significantly with voltage. If the external voltage is aligned with the in-built potential (reverse bias) the depletion zone will increase in size. Only the drift current will then flow, while the diffusion charges cannot overcome the increased potential.

The width of the depletion zone d is then given by

$$d \approx \sqrt{\frac{2\epsilon\epsilon_0}{e}\frac{1}{N_D}(U_b + U_{ext})} \tag{1.6}$$

with the dielectric constants for vacuum ϵ_0 and for the semiconductor material ϵ [25].

1.3.2 Semiconductor Particle Detectors

When a charged particle traverses through silicon, it deposits some of its energy by generating electron-hole pairs along its path through ionisation. This mechanism is used to detect passing charged particles in silicon pixel sensors, where pn-junctions act as charge collecting diodes. The electron-hole pairs can diffuse into the depleted region or be generated within it, where they get separated by the electric field and drift towards the collector electrodes. This results in an electrical signal that can be amplified and measured.

Typically, the charge collection diode is a thin p- or n-doped layer with a lower doped substrate acting as the depleted volume. A pixel sensor consists of a 2-dimensional array of charge collector diodes sitting in a common n-well. The readout electronics typically consist of an amplifier that makes the signals sufficiently large for further processing. The signal is fed into a comparator which determines whether the signal exceeds the selected threshold. If it does so, the comparator sends out a digital signal indicating a hit.

The chip's readout electronics assign the pixel position and time stamp to the signal. It is then sent in a data stream to the data acquisition system for further analysis. In addition to the pixel address and time stamp, modern sensors can also provide information about the signal size by measuring the time the signal surpasses the threshold. This is know as the Time-over-Threshold (ToT) measurement.

1.3.3 HV-MAPS

Monolithic pixel sensors combine the readout electronics with the active detection area in a single unit. Each pixel cell contains a complementary metal-oxide-semiconductor (CMOS) amplifier itself as an integrated circuit. It is embedded in a deep n-well in a p-substrate, which shields it from the substrate potential. At the same time, the deep n-well acts as a charge-collecting diode for the pixel sensor, as shown in Figure 1.6. Processes for manufacturing such chip architectures are commercially available, so that monolithic pixel sensors can be produced cost-effectively.

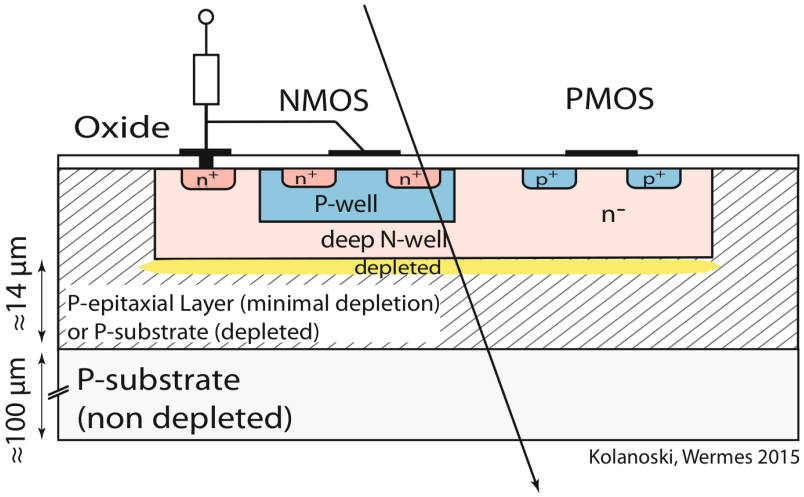


Figure 1.6: Schematic of a HV-MAPS particle detector. The deep n-well in a p-substrate forms a diode. Charged particles that generate electron-hole pairs will induce a current that can be measured. The readout electronics are integrated circuits within the charge collection diode itself. Taken from [25].

In high voltage monolithic active pixel sensors, a high voltage is applied in reverse bias. This increases the depleted volume and enables faster charge collection completely via drift. This leads to a faster readout, a better time resolution and larger signals because most of the electron-hole pairs are generated directly inside the depleted region. With low ohmic substrates $\leq 200\,\Omega$cm and bias voltages of 20 V to 80 V, the depth of the depletion region can be controlled to $\approx 30\,\mu$m to $40\,\mu$m [29].

The rest of the p-substrate volume isn't needed for signal generation. Therefore, it is possible to reduce the material budget by cutting off unused volume resulting in a chip thickness of $\leq 50\,\mu$m. In this way, HV-MAPS technology provides low material budget that enables excellent energy resolution by minimising multiple Coulomb scattering in the detector itself. Together with its very fast readout and excellent time resolution, it is the perfect technology for the Mu3e experiment.

pixel size [μm^2]	80×80
sensor size [mm^2]	20.66×23.18
columns $\times$ rows	256×250
active area [mm^2]	20.48×20

Table 1.3: MuPix11 sensor dimensions. Taken from [29].

1.3.4 MuPix11

The MuPix11 is the latest version of the HV-MAPS MuPix series and will be the operating chip in the Mu3e experiment. The met main requirements are listed in Table 1.2 and the dimensions of the MuPix11 in Table 1.3.

The sensor architecture is sketched in Figure 1.7. Each pixel's charge collecting n-well contains a charge sensitive amplifier (CSA) and a source follower as a line driver. For test purposes, the amplifier input can also be used to inject charges via a capacitor. In this way, an ionising particle can be simulated and the signal can be read out. The amplifier requires a separate supply voltage of 1.0 to 1.2 V, which is different from the chip supply voltage of ~ 1.9 V. This separate voltage is generated on-chip by a regulator in the periphery. This increases power consumption and heating of the chip.

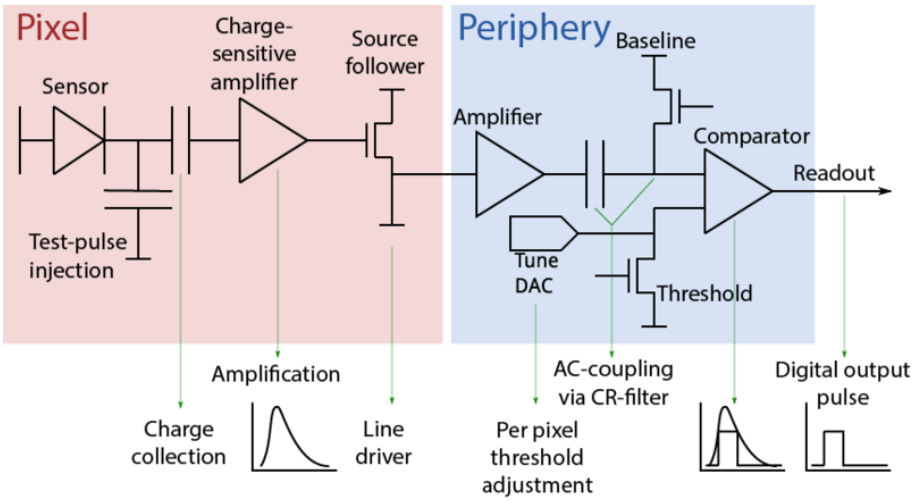


Figure 1.7: Electronic structure of the MuPix chip. Taken from [29].

A configurable feedback circuit produces a constant current to reset the charge collection. This gives the signal with a linear falling edge. The pulse height is then proportional to the pulse length. In this way, the ToT measurement provides information about the amplitude of the signal, hence the deposited energy. A metal line connects the pixel to the digital part in the periphery. For each pixel there is a set of two comparators whose thresholds can be set separately.

As all comparators operate slightly differently due to manufacturing process variation, a 3-bit adjustment "tuning" is possible for each comparator. The digitised signals are read out in a column-drain fashion and processed by the on-chip state machine. From there, the data is sent over in up to three links at 1.25 Gbit/s. This data stream is 8-bit/10-bit encoded. Free data slots are used to send values from on-chip voltage measurements, e.g. from temperature sensors.

1.4 Microelectronic Temperature Sensors

Measuring the temperature of silicon chips to monitor temperature and cooling is very important in modern microelectronics. As mentioned above, the electronic properties of semiconductors are naturally temperature dependent, which presents a challenge for some of their applications. For temperature measurement, however, this can be exploited in relatively simple circuits to create temperature sensors on a microelectronic scale. This chapter explains the working principles of two possible temperature sensor architectures and their implementation in the MuPix11.

1.4.1 The MuPix11 Temperature Diode

A temperature diode is a simple pn-junction. As discussed in subsection 1.3.1, the diffusion current and the drift current establish an equilibrium when no external voltage is applied. For the diffusion current density j_d^0 and the drift (or field) current density j_f^0 holds [27]:

$$j_d^0 + j_f^0 = 0. \tag{1.7}$$

The zeros indicate that no external voltage is applied. The amplitude of the diffusion current depends on the number of charge carriers that successfully diffuse against the in-built voltage. This is given by the Boltzmann statistics:

$$|j_d^0| = |j_f^0| = \tilde{\alpha}(T) \cdot e^{-eU_b/(k_B T)} \tag{1.8}$$

with the Boltzmann constant k_B and the temperature T. The prefactor $\tilde{\alpha}(T)$ is negligibly dependent on temperature compared to the exponential [27]. In the following, it is written as $\tilde{\alpha}$.

When an external voltage U_{ext} is applied, the two currents no longer compensate each other. In forward bias, the charge carriers have less potential to overcome when diffusing. If the external voltage is defined to be positive when opposing the in-built voltage (forward bias), the diffusion current is given by:

$$\begin{aligned} j_d &= \tilde{\alpha} \cdot e^{-e(U_b - U_{ext})/(k_B T)} \\ &= j_d^0 \cdot e^{eU/(k_B T)}. \end{aligned} \tag{1.9}$$

The drift current is limited solely by the generation of electron-hole pairs within the electric field of the depletion zone and not by the strength of the field. It is therefore independent of the applied voltage and can be assumed to be

$$j_f \approx j_f^0. \tag{1.10}$$

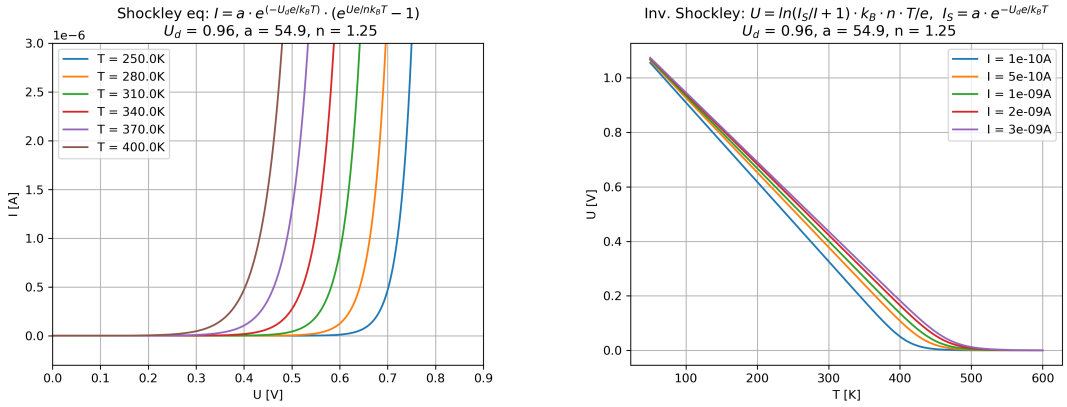
The total current density of the two opposing currents will then be described by the Shockley equation:

$$\begin{aligned} j(U) &= j_d(U) - j_f \\ &= j_d^0 \cdot e^{eU/k_BT} - j_f^0 \\ &= j_d^0 \cdot \left(e^{eU/k_BT} - 1\right) \\ &= \tilde{\alpha} \cdot e^{-eU_b/k_BT} \left(e^{eU/(k_BT)} - 1\right) \end{aligned} \tag{1.11}$$

For real applications an "ideality factor" n is added. It is a measure of how well the diode follows the theoretical equation, since its derivation makes certain assumptions. Depending on the semiconductor, the usual values are in a range of ~ 1 to 2. The current I in the diode is then described by the Shockley equation:

$$I = \alpha \cdot e^{-eU_b/(k_BT)} \left(e^{eU/(nk_BT)} - 1\right). \tag{1.12}$$

Figure 1.8a shows the course of the function for different temperatures and typical values for a silicon diode.



(a) (b)

Figure 1.8: Theoretical plots with parameters chosen close to the MuPix11 diode characteristics. a) Current–voltage characteristic (I-V curve) of a diode according to the Shockley equation. b) Temperature dependence of voltage at constant current in a diode.

Figure 1.8b shows the temperature dependence of the voltage at one constant current. In the operating temperature range of the chip of +0 °C to + 70 °C, the

function can be assumed to be linear. When a constant current is applied, the measured voltage will be proportional to the temperature of the diode. This shows, that it is not necessary to measure the whole curve for a temperature measurement. In to obtain true chip temperatures, a calibration of the used diode must be performed. For the temperature diode in MuPix11 this is be described in subsection 3.1.1.

1.4.2 Current Mirror Temperature Sensor (VTemp) and Bandgap Voltage Reference

The second microelectronic temperature sensor technology implemented in the MuPix11 uses the temperature dependence of transistors in sub-threshold conduction. The circuit is based on a Wilson current mirror consisting of four transistors as shown in Figure 1.9. Given an input voltage, this circuit reaches equilibrium with a constant current flow in both lines. The ratio of the currents is defined by the characteristics of the transistors: its width and lenght.

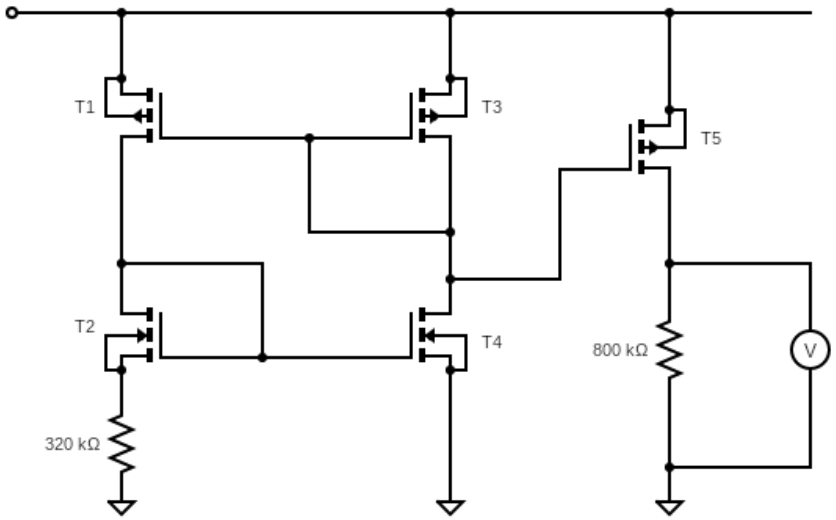


Figure 1.9: Schematic of the current mirror temperature sensor (VTemp). The 4 transistors T1, T2, T3 and T4 act as a Wilson current mirror. They produce a current proportional to the absolute temperature. This current is reproduced by T5 and forced through a resistor to measure the voltage drop.

In the sub-threshold region, the current through the transistor is mainly generated by diffusion current between source and drain (weak inversion current). This current is highly temperature dependent.

T2 in the current mirror is very wide, allowing a subthreshold current. All the other characteristics of the transistor are chosen so that the sub-threshold transistor

will change the equilibrium current of the circuit in a linear way with the temperature. This current is then reproduced by T5, which forces the current through a high ohmic resistor. The voltage drop across the resistor can be measured and is proportional to the temperature of the circuit. This circuit therefore provides a current source proportional to absolute temperature (PTAT).

When not used as a temperature sensor, the temperature dependence of silicon circuit currents is undesirable. For this reason, so-called bandgap voltage reference circuits are used. It is possible to use current changes of multiple transistors to cancel first-order (linear component) temperature dependencies. This is also implemented in the MuPix11 sensor to provide a current reference whose linear temperature dependence is minimised in a range of $+0\,^{\circ}\mathrm{C}$ to $+\,80\,^{\circ}\mathrm{C}$. The current fo reach circuit on the chip is derived from that reference current. Therefore, change in the reference current influences the current flow of the whole chip. The operation and the impact of the bandgap current reference is also investigated in this thesis.

1.4.3 Temperature Sensors in the MuPix11

The MuPix11 sensor contains three temperature sensors as integrated circuits. They are used to monitor the temperature of the chips during the Mu3e experiment. One of them is a temperature diode and the other two are Wilson current mirror temperature sensors, referred to as VTemp1 and VTemp2. They are all located at the periphery of the chip, as shown in Figure 1.10.

The periphery will have the hottest spots on the chip, as the readout electronics and voltage generation are concentrated in this small part of the chip. Since it is not possible to integrate the temperature sensors into the pixel cells themselves, the challenge is to gain insight into the actual temperatures of the matrix. The three sensors were chosen to be located in different regions in order to get a better understanding of the heat distribution in the periphery and to develop suitable temperature measurement methods for the Mu3e experiment.

The temperature diode is located next to one of the VSSA voltage generators. It is at a fairly short distance to the left of the readout state machine. One of the current mirror temperature sensors, VTemp2, sits to the right of the readout state machine, next to the Low Voltage Differential Signalling (LVDS) drivers that send the data stream to the Field Programmable Gate Array (FPGA). These two locations are considered to be two of the hottest areas on a running MuPix11 chip. VTemp1 was placed close to the bias block and the voltage digital-to-analogue converters (DAC) further away from the hotter areas. By not being exposed to the main heat sources of the peripherals, this location is intended to mimic a realistic matrix temperature.

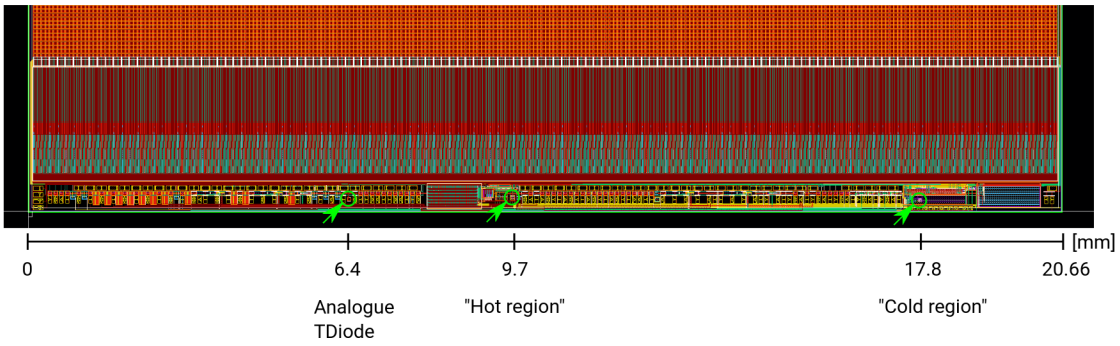


Figure 1.10: Position of the temperature sensors in the MuPix11 periphery. The "hot region" refers to VTemp2 and "cold region" refers to VTemp1. "Analogue TDiode refers to the temperature diode

2 Setup

In order to study the HV-MAPS chips in the laboratory, some hardware is required. The setup used includes the chip itself, which is glued to a printed circuit board (PCB). This is called an insert PCB, to which the chip is wire bonded. This PCB can then be inserted into another larger PCB, called the MuPix motherboard, as shown in Figure 2.1. The insert PCB provides pads for analogue measurement of internal voltages and contains the power connector for the chip's operating voltage, called 'low voltage' (LV). The high voltage (HV) is applied via the motherboard, which alos connects the chip to a Field Programmable Gate Array (FPGA). The data acquisition system (DAQ) allows configuration of the FPGA and the chip via an graphical user interface (GUI).

This chapter gives an overview of the setup for the temperature measurements that were carried out for this thesis.

2.1 Temperature Diode Measurement

The temperature diode is designed for analogue measurements that are independent of the stability of the chip. Therefore, it is not connected to any other on-chip readout electronics but solely connects to a bond pad. In the Mu3e experiment, this allows it to be used for a interlock system which shuts down the power if temperature diodes indicate overheating. This works even when the chips are not responding digitally. For the measurement in this thesis, two methods are used to make measurements with the diode which are discussed in the following sections.

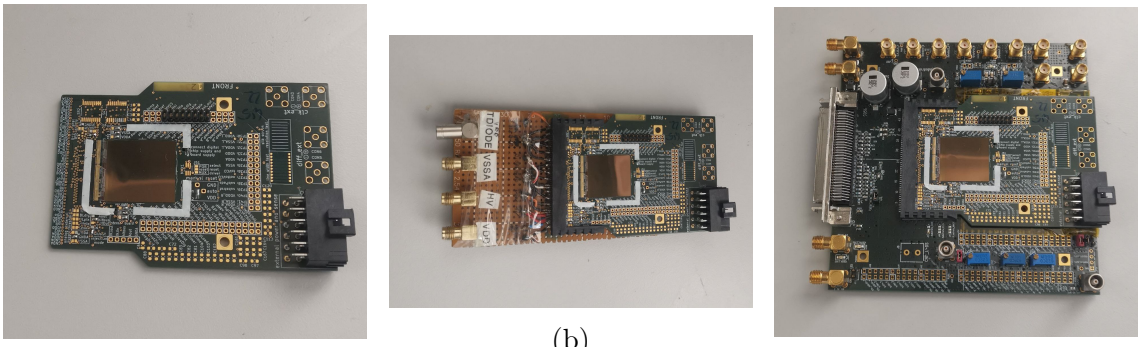
2.1.1 Diode Measurements with the Diode-Board

The first method does not include the standard MuPix motherboard to reduce the number of interconnections. A 'diode board' (Figure 2.1b) is used, which allows a power supply to be connected to the temperature diode bond pad on the chip. By providing different currents and measuring the voltage across the diode with the power supply, the current-voltage (I-V) characteristics can be obtained.

In this setup, it is not possible to configure the chip, so it used for most only one measurements in this thesis to verify that the diode behaves accordingly to the Shockley equation (Equation 1.12). However, it is a realistic realisation of the temperature diode measurement in the Mu3e experiment.

2.1.2 Diode Measurements with the MuPix Motherboard

The second method involves the MuPix motherboard. It provides a current via a digital-to-analogue converter (DAC) that is connected to the temperature diode on the chip. The DAQ allows to perform a current scan through the diode and measure the voltage at the same time. The voltages across the diode are measured via an analogue-to-digital converter. Non-linearities in the ADC and the DAC have an impact on the accuracy of this measurement method. This method is used throughout the experiment because it allowed measurements to be taken while the chip was running.



(a) (b) (c)

Figure 2.1: Pictures of the hardware in the lab for MuPix measurements. a): Shows a MuPix11 chip glued and bonded to an insert PCB. b): The PCB from a) is inserted into the diode board for the temperature diode scans. c): The PCB is inserted into the MuPix motherboard used to operate the chips.

2.2 VTemp Measurement

As described in subsection 1.4.2, the VTemp sensors generate a current proportional to the absolute temperature of the transistors. To measure this current, it flows through a high ohmic resistor (800 kΩ within the chip. The voltage drop across the resistor can then be measured. In the laboratory, this can be done in two ways which are described in this chapter. For temperature measurements in this thesis, both methods are used simultaneously.

2.2.1 Analogue VTemp Temperature Measurement via the TestOut Pad

On the printed circuit board to which the MuPix11 is bonded, several pads can be used to measure voltages across the chip, e.g. the VDDA supply voltage or the thresholds for the comparators. The 'TestOut' pad is connected directly to a

multiplexer (MUX) on the chip. A MUX can route a selected input line to an output line. The TestOut MUX has been integrated for laboratory testing. It is possible to select a variety of input lines such as VTemp1, analogue ground level GNDA, the analogue voltage level VDDA or the slow control MUX. This allows the voltage of the selected input lines to be measured with a voltmeter in the laboratory. For the TestOut measurements, one measurement of the VTemp1 was directly done via its input line of the TestOut MUX. However, it is not possible to measure VTemp2 as the TestOut MUX is not directly connected to it.

VTemp2 is only connected to the slow control MUX. This MUX selects the lines for the slow control digital readout (see subsection 2.2.2). It is also connected to VTemp1. To measure VTemp2, the slow control MUX needs to forward the VTemp2 signal to the TestOut MUX. From here, it can be read out via the TestOut pad. Through this detour it is possible to also make a analogue measurement of VTemp2.

In the same manner, a reference measurement of VTemp1 is taken. This way a comparison can be done between the measurement via the TestOut MUX and the measurement in which the signal additionally went through the slow control MUX. This gives insight into possible systematic errors induced by this transit through an additional MUX.

Voltages are measured using a high ohmic KEITHLEY power supply. Therefore, the forced current flow is selected to be zero. The actual currents are in the order of a few nA. A high ohmic voltage measurement is crucial as the voltage drop over a 800 kΩ resistance is measured. Measuring with voltmeters that have internal resistances of ~ 1 MΩ creates a parallel connection and results in a lower voltage drop across the resistance in the VTemp circuit.

2.2.2 Digital VTemp Measurement via the Data Stream

Digital measurements of the VTemp temperature sensors is realised via the slow control system of the chip. The voltage measurements are performed on-chip and the results are written into free slots in the data stream. This way, continuous measurements can be conducted during operation of the chip, as will be done in the Mu3e experiment. In single or alternating mode, one or more voltage levels can be selected in the slow control MUX e.g. the VTemp sensors, the baseline voltage or the threshold voltages of the comparators. It passes the signal to an 8-bit analogue-to-digital converter which converts the analogue voltage to a digital value. The ADC divides the supply voltage VDDA ~ 1.9 V into 256 equally spaced parts. It then compares the input voltage with each 256^{th} fraction of the supply voltage in ascending order until the input signal exceeds it. The corresponding 8-bit value is included into the 1.25 Gbit/s data stream, which holds enough space for these measurements.

For the measurements in this thesis, a small program was written to extract the measurement data from the data stream. The mean and standard deviation of multiple values are calculated and used for further analysis. The measurements in this thesis took 12 FPGA memory readouts and measured VTemp1, VTemp2 and

the baseline in the alternating mode. This resulted in 40 to 60 measurement values for each. In addition to the standard deviation σ_{ADC} of multiple measurements, the resolution of the binary signals is included. The total uncertainty of the digital values is then determined by

$$\Delta_{ADC} = \sqrt{\left(\frac{1}{\sqrt{12}}\right)^2 + \sigma_{ADC}^2}. \tag{2.1}$$

2.3 Climate Chamber and Infrared Camera

2.3.1 Climate Chamber

The Binder MK53 [30] climatic chamber is used to regulate the ambient temperature of the chip. It acts as a thermal reservoir for the measurements. A GUI on an external PC allows the temperature, fan speed and condensation protection to be selected. For all runs, the dew protection is enabled to prevent short circuits to the electronics and the fan was set to maximum speed.

The MuPix motherboard, which contains the circuit board with the chip, is placed on a ceramic plate which acts as an electrical insulator. The cables are fed through a hole at the top, which is sealed with a rubber plug. Figure 2.2b shows the setup.

The temperature in the chamber is verified using a PT-100 thermometer [31]. In the following chapters the selected temperature of the climate chamber is used as a reference. The PT-100 readings are used for calibration. A maximum deviation of 1 K is observed. For temperatures in the range of +5 °C to + 25 °C, the chamber constantly switches between heating and cooling, resulting in a periodic temperature change. For these temperatures, additional uncertainties of 1 K are added accordingly.

2.3.2 The Infrared Camera

To investigate the temperature distribution on the chip, a thermographic camera is used (ThermaCAM™ S40 [32]). It is placed on a tripod pointing down towards the table on which the motherboard is mounted. The top of the chip is covered with a seal that reflects all electromagnetic waves quite well. For this reason, the camera lens is aligned slightly transversal. In this way, double reflection effects do not distort the measurements. The reflection from the ceiling of the laboratory is assumed to be constant over the course of the measurements.

The infrared images should not be taken as accurate temperature measurements of the chip. The temperature scale provided by the program is inaccurate for the surface material of the chip and would require to be accurately calibrated. More importantly, it is unclear how much heat of the substrate of the is transported to the surface which radiates. The images are intended to be an estimate of the heat

(a) (b)

Figure 2.2: Pictures of the setup with the climate chamber in the lab. a) Shows the whole setup with the PC and the power supplies on the right hand side and the climate chamber on the left hand side. b) Shows the opened climate chamber with the MuPix11 sensor inserted into the motherboard and the oscilloscope on top.

distribution in the chip, not an accurate measurement of the temperature.

2.4 MuPix11 Signal Generation and Data Acquisition

In addition to the measurements of the temperature sensors, the effect of temperature on the output signals produced by the chip in the pixel matrix is also investigated. The setup discussed in the previous chapter does not include the actual commissioning of the chip as a particle detector. This is discussed in this chapter.

2.4.1 Signal Generation

Each pixel in the matrix contains a test pulse injection infrastructure as shown in Figure 1.7. It can generate charge pulses in a selection of pixels via a capacitance $C_f \approx 1.6\,\mathrm{fF}$, which are detected by the charge collector diode and processed as a signal. In this way, it is possible to study the chip's signal measurement without detecting the actual energy deposition of charged particles. An injection voltage of $0.7\,\mathrm{V}$ is used at a rate of $1000\,\mathrm{Hz}$ and a delay of $5000 \times 8\,\mathrm{ns}$. This produces a pulse equal to $(1.6\,\mathrm{fF} \times 0.7\,\mathrm{V}) \approx 6990\,e$.

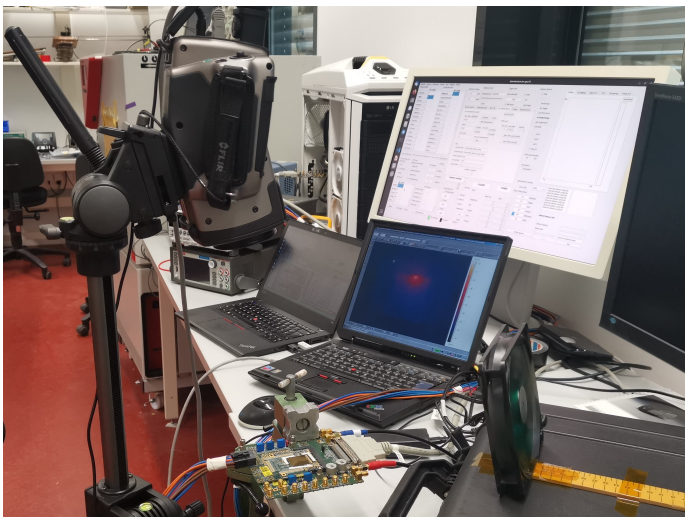


Figure 2.3: Setup of the infrared camera taking images of MuPix11 sensors.

For analogue measurements via the oscilloscope, the signal generated by the amplifier (AmpOut signal) inside of the pixels is driven to the digital cell of the periphery. Here, for each pixel, a compactor (ThLow) processes the signal and produces the digital 'Hitbus' signal. When the signal reaches the threshold, the start of the Hitbus signal is determined. When the signal falls below the threshold the end of the Hitbus signal is indicated.

In the case of digital readout via the data stream, the signal generated by the amplifier (AmpOut signal) is also driven to the digital cell of the periphery. Here, for each pixel, two compactors process the signal and produce the digital comparator output signal. When the signal reaches the 'ThLow' threshold, the start of the Hitbus signal is determined. When the signal falls below the 'ThHigh' threshold the end of the Hitbus signal is indicated. The digital signal is then interpreted by the periphery and sent out to the FPGAs for data acquisition.

2.4.2 Data Acquisition

The data stream contains any signal that has reaches the selected and is therefore recognised as a hit. It provides information on the pixel coordinates and timestamps of the signals that crossed the thresholds. This can be used to determine the Time-over-Threshold, the time between the signal surpassed the first threshold and the time it fell below the second threshold. The raw data is then analysed using Corryvreckan and ROOT. Corryvreckan is an agile and highly configurable software used for the reconstruction and analysis of particle detector data [33]. ROOT is a powerful analysis software package developed for high energy particle physics [34].

The setup provides an analogue measurement outputs for a selectable pixel in the bottom row. It is possible to measure the injection pulse, the AmpOut signal and the digital Hitbus signal. All three signals can be fed into an oscilloscope to study

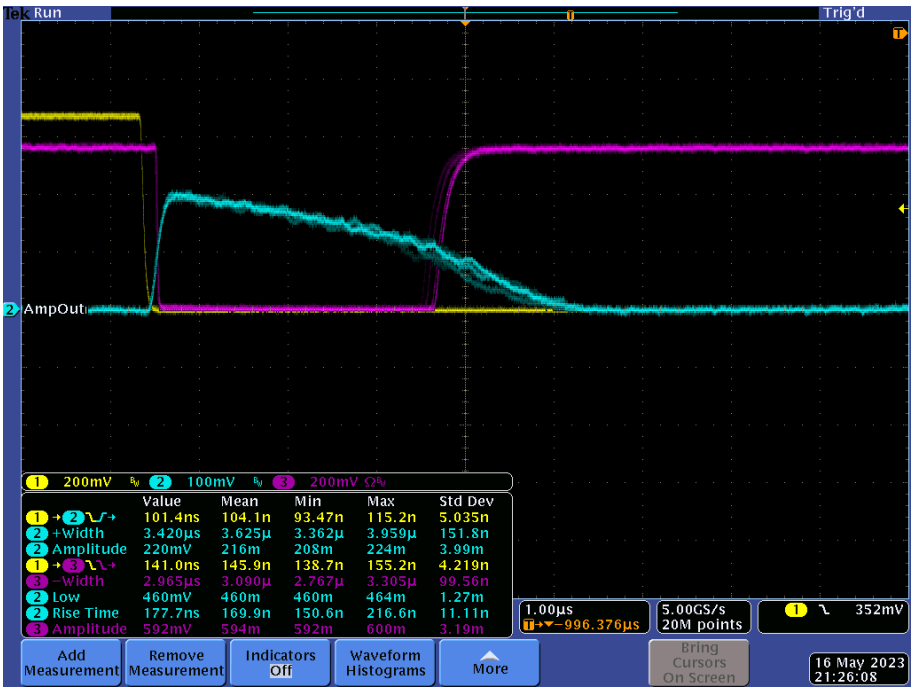


Figure 2.4: Example of oscilloscope measurements: Yellow is the injection signal, blue is the AmpOut signal and purple is the Hitbus signal.

their characteristics.

The measurements are performed with a Tektronix© DPO 4104B Digital Phosphor Oscilloscope. Measurements of single pixel signal shaping due to temperature changes are carried out. To do this, images are taken and the following characteristics are calculated and displayed on the oscilloscope: The delay between injection and the AmpOut signal, the width of the AmpOut signal, the amplitude of the AmpOut signal, the low level (baseline) of the AmpOut signal, the delay between injection and the Hitbus signal and the width of the Hitbus signal. For the delays, amplitudes and widths, the signal threshold of 30 % of the amplitude is used. For the AmpOut and Injection signals, a determination of 1 MΩ is chosen, while the Hitbus is determined with 50 Ω. The DAC values for the source followers of the AmpOut and Hitbus signal are: VNHB = 0x14 and VPFoll = 0x3f. Figure 2.4 shows an example picture.

The ToT measurement is conducted with a binning setting: ckdivend = 0x3f and a timer delay of: VPTimerDel = 0x1 to ensure no cutoff for large signals. This results in a binning size of 512 ns.

3 Sensor Calibration and Temperature Measurements

This chapter of the thesis focuses on the integrated temperature sensors of the MuPix11 the temperature measurements conducted with them. Therefore, all three sensors – the diode and both VTemp sensors – are calibrated individually. The temperature measurements are then presented and discussed. They provide insight into the heat distribution on the chip and the main heat sources, which are verified with infrared images. Finally, the applications and operation of the temperature circuits in the Mu3e experiment are discussed. The following measurements are performed with two different sensor thicknesses: 50 µm (chip ID: 327-01-09) and 739 µm (chip ID: 327-01-04).

3.1 Calibration of Temperature Sensors

This chapter deals with the calibration of the temperature diode and VTemp sensors. Therefore, the chips were placed in the climate chamber at different temperatures from $-10\,^{\circ}\mathrm{C}$ to $+70\,^{\circ}\mathrm{C}$. To minimise the effects of self-heating, an 'all-zero' setting is used for measurements with the in-chip temperature sensors. In this setting, all power consuming entities on the chip are turned off, while still maintaining the reference voltage levels. This is necessary for the operation of the VTemp temperature sensors and the MuPix motherboard. Depending on the temperature, the measured current flow is 4 mA to 6 mA resulting in a power consumption of 7.6 mW to 11.4 mW at a low voltage level of 1.9 V. The heat dissipation is almost 100 times lower than durin normal operation. Thus, it is assumed to be negligible. The ambient temperature inside the chamber is measured with a pt-100 sensor and used as the reference temperature for the chips.

3.1.1 Temperature Diode

In the following, two different approaches are discussed. Firstly, the diode is studied with an analogue current-voltage scan via a power supply that allowed for a precise I-V characteristics. This is done to verify that the diode behaves according to the Shockley equation (Equation 1.12). Secondly, the MuPix motherboard is used to conduct automated I-V scans at different temperatures. As this is the only way to perform measurements while the chip is running, this method is used for all following temperature measurements in this thesis.

The analogue measurement is conducted utilising the 'diode-board' mentioned in subsection 2.1.1. Therefore, the chip was completely unpowered. Figure 3.1a shows five current scans at chamber temperatures of (−10, +10, +30, +50 and +70)°C. The curves show an exponential behaviour. The lower the temperature the further the curves are shifted towards higher voltages.

In Figure 3.1b the Shockley equation (Equation 1.12) is fitted to each scan. U_d, a and n are chosen as free parameters with fixed temperatures for each curve. The fitted curves agree well with the data, confirming that the diode behaves according to Equation 1.12. The high temperature scans deviate slightly to from the fit towards higher voltages at low currents. This could be due to the temperature dependence of the free parameters U_d, a and n, which have the same value for all temperatures.

In Figure 3.1c the voltages at a given current level are plotted against the chamber temperature. The data shows linearity and is fitted with a linear function for each current. This verifies that a linear temperature calibration of the diode is possible for constant currents from 0.6 µA to 3 µA at temperatures of −10 °C to + 70 °C.

The automated I-V scans are performed with the MuPix motherboard as described in subsection 2.1.2. For each measurement, the motherboard supplies a current for the diode and measures the voltage. It provides values of arbitrary unit for the currents. Therefore, the currents generated by the MuPix motherboard for the I-V scans are measured with a Keithley power supply once. The two largest currents in the scans are 800.5 nA and 823.8 nA. The smallest currents shown in the plot are are 80.7 nA and 145 nA.

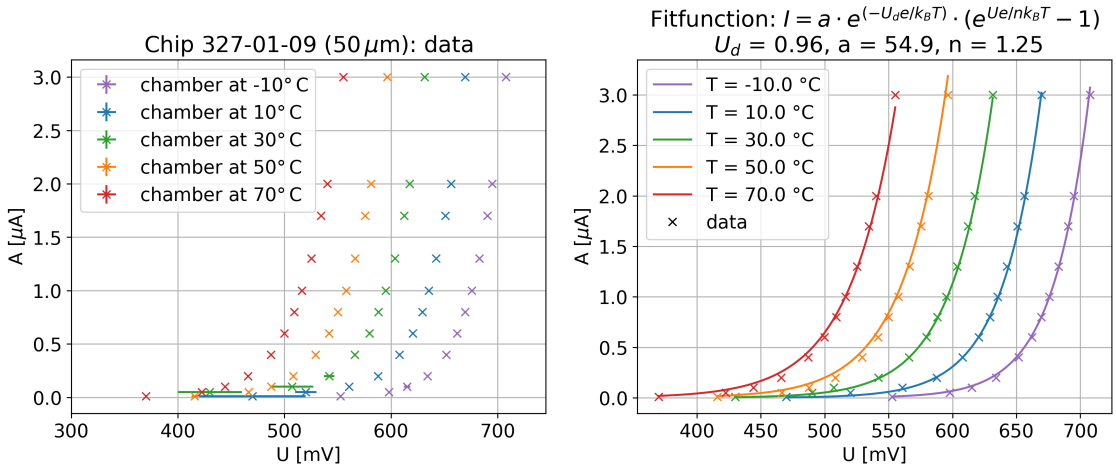
The results of the current scans and voltage measurements are shown in Figure 3.2a and Figure 3.2b. At high currents, the curves show similar behaviour as the 'diode-board' scans. For low currents, the curves have an offset towards higher voltages compared to the theoretical Shockley curve. This might be due to non-linearities in the ADC and the DAC of the MuPix motherboard, especially at low currents in the range of a few 100 nA.

The corresponding calibration curves with a linear fit for the both chips are displayed in Figure 3.2c and Figure 3.2d. For these, the second largest current in the scan are used which corresponds to 800.5 nA. It is chosen because with higher currents the curve gets more steep and the variation in voltage decreases and the last current sometimes showed outliers. In this regime, the voltage difference of two measurements at different temperature is the greatest, ensuring maximal possible accuracy for the calibration.

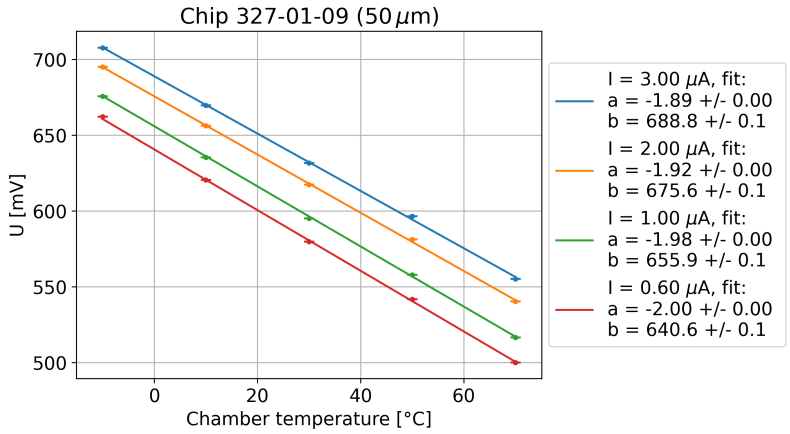
Both chip diode calibration curves are fitted with a linear function, resulting in the calibration formulae:

$$T^{09}_{diode} = \frac{U^{09}_{diode} - 708.6\,\mathrm{mV}}{-1.90\,\mathrm{mV/°C}} \quad \text{for chip 327-01-09 and} \tag{3.1}$$

$$T^{04}_{diode} = \frac{U^{04}_{diode} - 714.8\,\mathrm{mV}}{-1.85\,\mathrm{mV/°C}} \quad \text{for chip 327-01-04.} \tag{3.2}$$



(a) (b)



(c)

Figure 3.1: Temperature diode measurements with the chip 327-01-09 (thickness: 50 µm) via the 'diode-board' at "all zero" settings (LV current: ~ 5 mA. a) I-V characteristics for different chamber temperatures. b) Shockley fits with U_d, a and n as free parameters. The temperature parameter is fixed to the chamber temperatures. c) Calibration curves: data and linear fits for the temperature diode voltage vs chamber temperature for constant current.

The corresponding errors are given by:

$$\Delta T = \sqrt{\frac{1}{a^2}\Delta U^2 + \left(\frac{U-b}{a}\right)^2 \Delta a^2 + \frac{1}{a^2}\Delta b^2} \tag{3.3}$$

Where U is the measured voltage and a and b are the corresponding linear fit parameters of the calibration curves. ΔU is the error of the measured voltage. It is determined to be 1 mV coming from fluctuations observed in this range. For the tem-

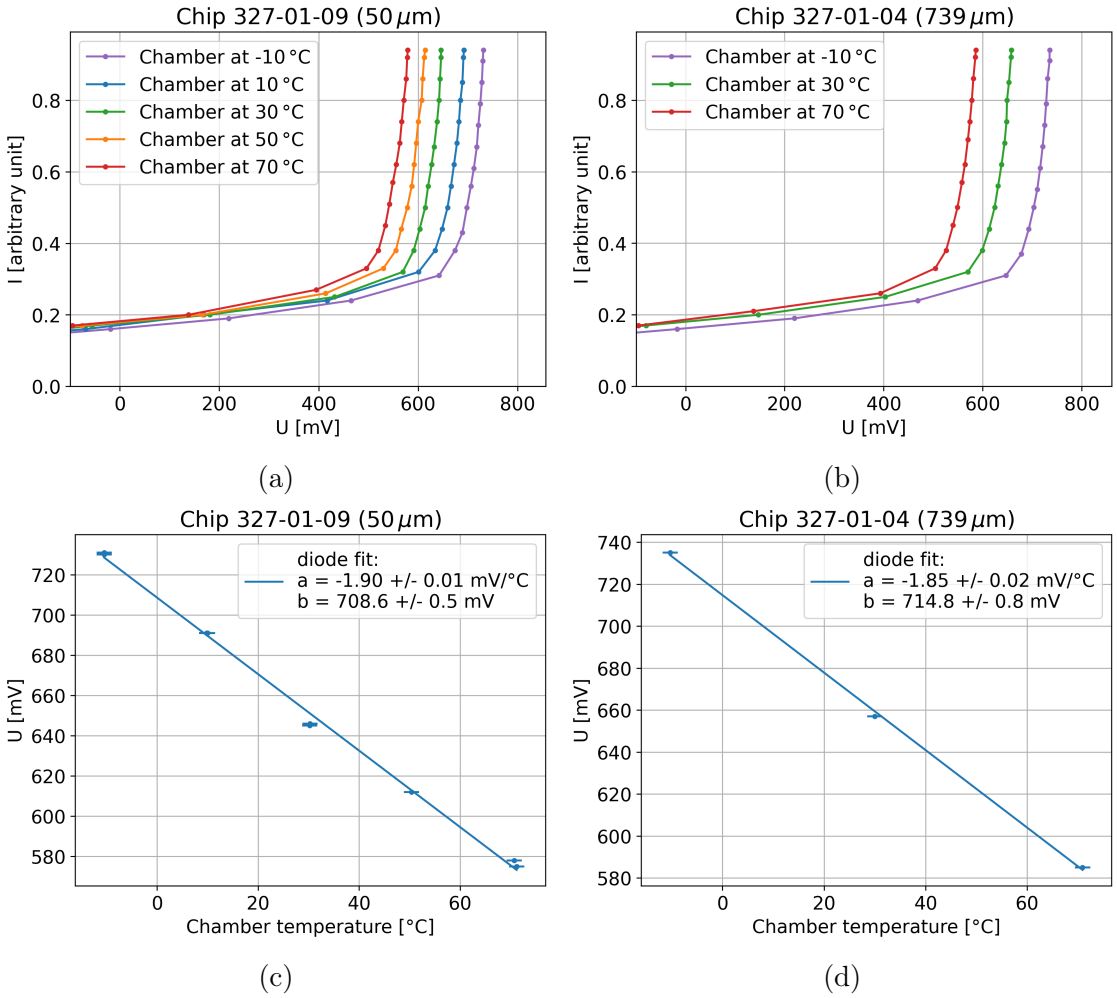


Figure 3.2: Temperature diode measurements via the MuPix motherboard: a) IV-scans of chip 327-01-09 (50 µm) and b) of 327-01-04 (739 µm) and c) calibration fit with the penultimate measurement point in the scan with the 327-01-09 and d) with the 327-01-04.

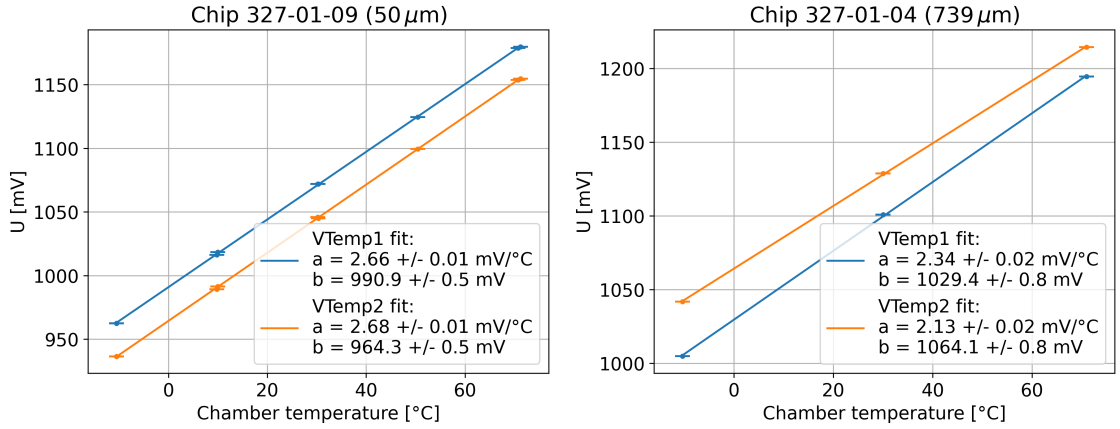
perature measurements in this thesis, ΔT_{diode} is in the range from 0.69 K to 1.30 K for the thick chip and from 0.58 K to 0.98 K for the thin chip. The smaller value corresponds to the measurement at $-10\,^{\circ}$C and the larger value from the measurement at $+70\,^{\circ}$C chamber temperature.

Since most of the temperature measurements in the thesis require the chip to be running, the diode measurements are performed with the MuPix motherboard. Therefore, the calibration in Equation 3.1 is used for the thesis to extract the total temperatures. This way, self-heating effects at different operation settings can be studied.

3.1.2 Calibration of the VTemp sensors

The calibration and measurements of the VTemp sensors are carried out with analogue measurements via the TestOut pad on the insert PCB. The measurements the chip itself provides via the digital readout that will be used in the Mu3e experiment, is discussed in section 3.3.

As for the diode calibration, the measurements are carried out in the 'all zero' settings for temperatures of (−10, +10, +30, +50 and +70)°C in the climate chamber. Figure 3.3 shows the calibration curves for VTemp1 and VTemp2 for each chip with linear fits.



(a) (b)

Figure 3.3: VTemp measurements via the TestOut pad with linear calibration fits for a) the chip 327-01-09 (50 µm) and b) the chip 327-01-4 (739 µm).

The measurements are in good agreement with the expected linear behaviour, confirming the correct operation of the circuits. The following calibration formulae are obtained for VTemp1 and VTemp2 of each chip:

$$\left.\begin{aligned} T^{09}_{VTemp1} &= \frac{U^{09}_{Vtemp1} - 990.9\,\mathrm{mV}}{2.66\,\mathrm{mV/°C}} \\ T^{09}_{VTemp2} &= \frac{U^{09}_{Vtemp2} - 964.3\,\mathrm{mV}}{2.68\,\mathrm{mV/°C}} \end{aligned}\right\} \text{for chip 327-01-09}$$

$$\left.\begin{aligned} T^{04}_{VTemp1} &= \frac{U^{04}_{Vtemp1} - 1029.4\,\mathrm{mV}}{2.34\,\mathrm{mV/°C}} \\ T^{04}_{VTemp2} &= \frac{U^{04}_{Vtemp2} - 1064.1\,\mathrm{mV}}{2.13\,\mathrm{mV/°C}} \end{aligned}\right\} \text{for chip 327-01-04} \tag{3.4}$$

with the measured VTemp voltages U^{XX}_{VTemp}. The corresponding errors are calculated according to Equation 3.3. The voltage errors ΔU of 0.5 mV to 1 mV were taken individually for each measurement, based on observed voltage fluctuations of that

magnitude. For the temperature measurements in this thesis, ΔT_{VTemp} is in the range from 1.33 K to 1.61 K for the thick chip and from 0.41 K to 1.22 K for the thin chip. The smaller value corresponds to the measurement at $-10\,^{\circ}$C and the larger value from the measurement at $+70\,^{\circ}$C chamber temperature.

From just one sample of two chips, the deviation in the calibration parameter is clearly visible. Although the design of the four circuits is the same, process variations appear to have a significant effect on the absolute temperature calibration. To obtain an absolute temperature calibration, each VTemp sensor would have to be calibrated individually.

3.2 Temperature Measurements

The calibration of the temperature sensors allows absolute temperature measurements of all three sensors on the chip. These measurements are presented and discussed in this section. First, the estimated power consumption distribution is calculated and the measurement methods are presented. Then the temperature differences of the three sensors and the effect of the heating of the pixel matrix are discussed. Finally, the heat distributions of the 739 µm and the thinned 50 µm chips are compared.

3.2.1 Power Consumption Distribution

Before the temperature measurements, a rough estimate of the heat dissipation and distribution on the MuPix11 is shown in Figure 3.4. The chip can be divided into three main parts with different power consumption. There is the matrix of the chip ($20.00 \times 20.66\,\mathrm{mm}^2$), the digital part of the periphery which contains the comparators ($20.00 \times 2.54\,\mathrm{mm}^2$) and the lower part of the periphery which contains the readout electronics ($\sim 20.00 \times 0.6\,\mathrm{mm}^2$).

The current in both studied chips (ID 327-01-09 and 327-01-04) is 400 mA for a LV supply of 1.9 V. By turning off components in the pixel matrix and the periphery and tracking the current, the power consumption of each part can be estimated. The current is divided into ~ 200 mA in the matrix, ~ 100 mA in the comparators and another ~ 100 mA in the readout electronics. This results in a area power density of $92\,\mathrm{mW/cm}^2$, $362\,\mathrm{mW/cm}^2$ and $1533\,\mathrm{mW/cm}^2$ respectively.

Although some of the power put into the chip is used to drive signals or generate electromagnetic waves, most of it is dissipated as heat. The calculation shows that the periphery, and especially the readout electronics, will be the main heat sources determining the heat distribution on the chip. Note that the readout electronics consume most of the power put into the orange part in Figure 3.4. However, it is not distributed over the whole length of the periphery, but is much more localised. This is indicated by the red spot. Therefore, the area power density is assumed to be even higher in this region.

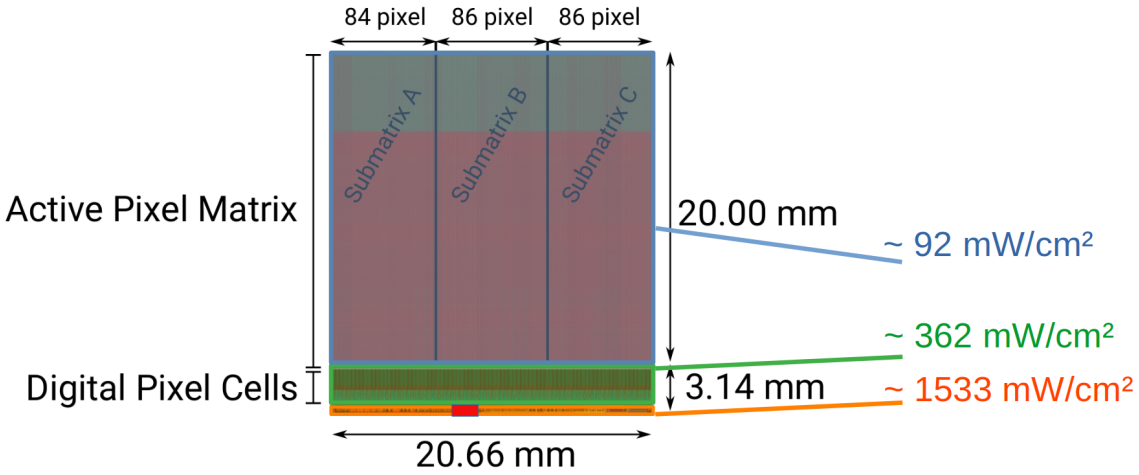


Figure 3.4: MuPix11 chip dimensions and rough power consumption estimation. Blue: the active pixel matrix. Green: the digital pixel cell with the comparators. Orange: the lower part of the periphery. The red square indicates the position of the state machine that is expected to be the hottest part of the whole chip.

3.2.2 Configuration Settings and Comparator Power Scans

There are two main settings used for temperature measurements. The 'default' setting is an operating setting optimised for the MuPix11 and runs at ~ 400 mA with 1.9 V LV supply voltage. Secondly, a 'low current' setting is used to minimise the power consumption of a chip while still producing a data stream. The matrix is therefore switched off and the digital readout electronics operate at minimum stability. In this setting, the chip is unable to track hits, but can provide digital VTemp measurements via the data stream. In addition, a measurement was made in the 'matrix off' setting. In this setting, the pixels in the matrix are switched off while the readout electronics operate as in the 'default' settings. The DAC values for all settings can be found in Table B.1

It is possible to select DAC values for the current supply of the comparators in the periphery. This allows the comparators to be utilised as a controllable heat source. The evenly distributed heat dissipation is used to heat up the periphery. The comparator DAC 'VComp2' is used for this purpose, controlling half of the implemented comparators. Temperature measurements are performed for increasing comparator DAC values. The results of these comparator power scans are presented and the observations discussed below.

Figure 3.5 shows the temperature measurements at 'default' and 'low current' setting for both chips at −10 °C chamber temperature. Measurements for other chamber temperatures can be found in Figure A.1, Figure A.2 and Figure A.3. In each plot the absolute temperatures of the diode and VTemp circuits after calibration are plotted against the low voltage supply current. The first measurement in each plot (at ~ 5 mA) is the 'all zero' setting measurement. This was used for calibration

and is indicated by the top x-axis entry 'az'. The other data points are comparator scan measurements for a given DAC value, shown on the top x-axis. The comparator DAC values were scanned in steps of 16 from 0 to the maximum value of 63 (in decimals).

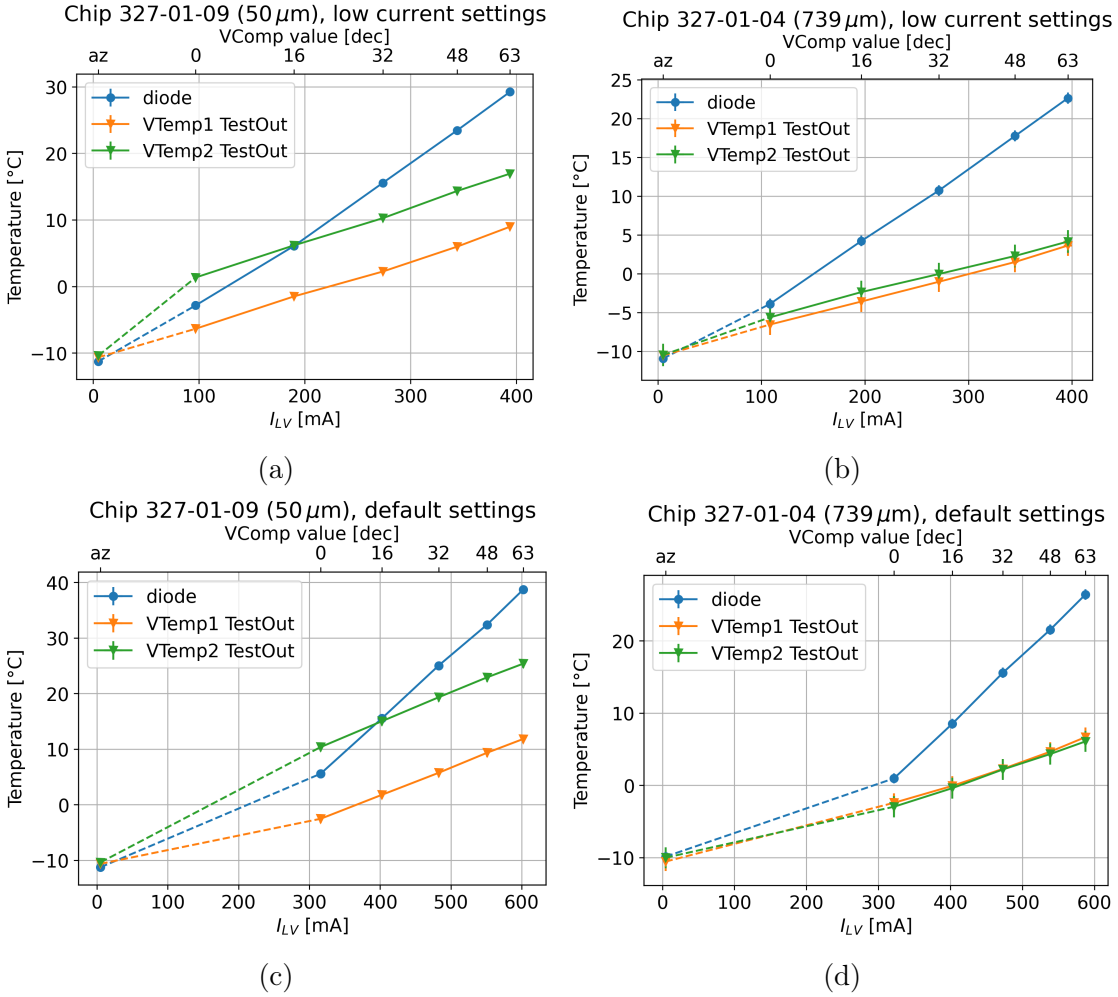


Figure 3.5: Comparator scan (VComp2) temperature measurements. The diode and VTemp measurements are plotted against the low voltage supply current at $-10\,^{\circ}$C chamber temperature for the thin chip 327-01-09 (a/c) and the thick chip 327-01-04 (b/d).

The quality of the comparators as a consistent heat source for different settings is evaluated. In Figure 3.6 measurements for different setting are shown in a common plot. In this plot, the 'low current' setting measurements are shifted in both temperature and current for better comparability of the curves. The top x-axes displays the LV current for the 'low current' measurement while the bottom x-axis is the LV current for the 'default' settings. For all sensors the temperature rise with supply current is linear. The slopes of each temperature sensor are similar when comparing

both settings. The linearity holds for all of the measurements performed at chamber temperatures of (−10, +10, +30, +50 and +70)°C and for both chips.

This shows that the scanning of the comparators is a reliable heat source that increases the chip temperature linearly with power consumption. Other observations such as the steeper slope for the diode or differences in the VTemp measurements of the two chips are discussed in subsection 3.2.3, subsection 3.2.4 and subsection 3.2.5.

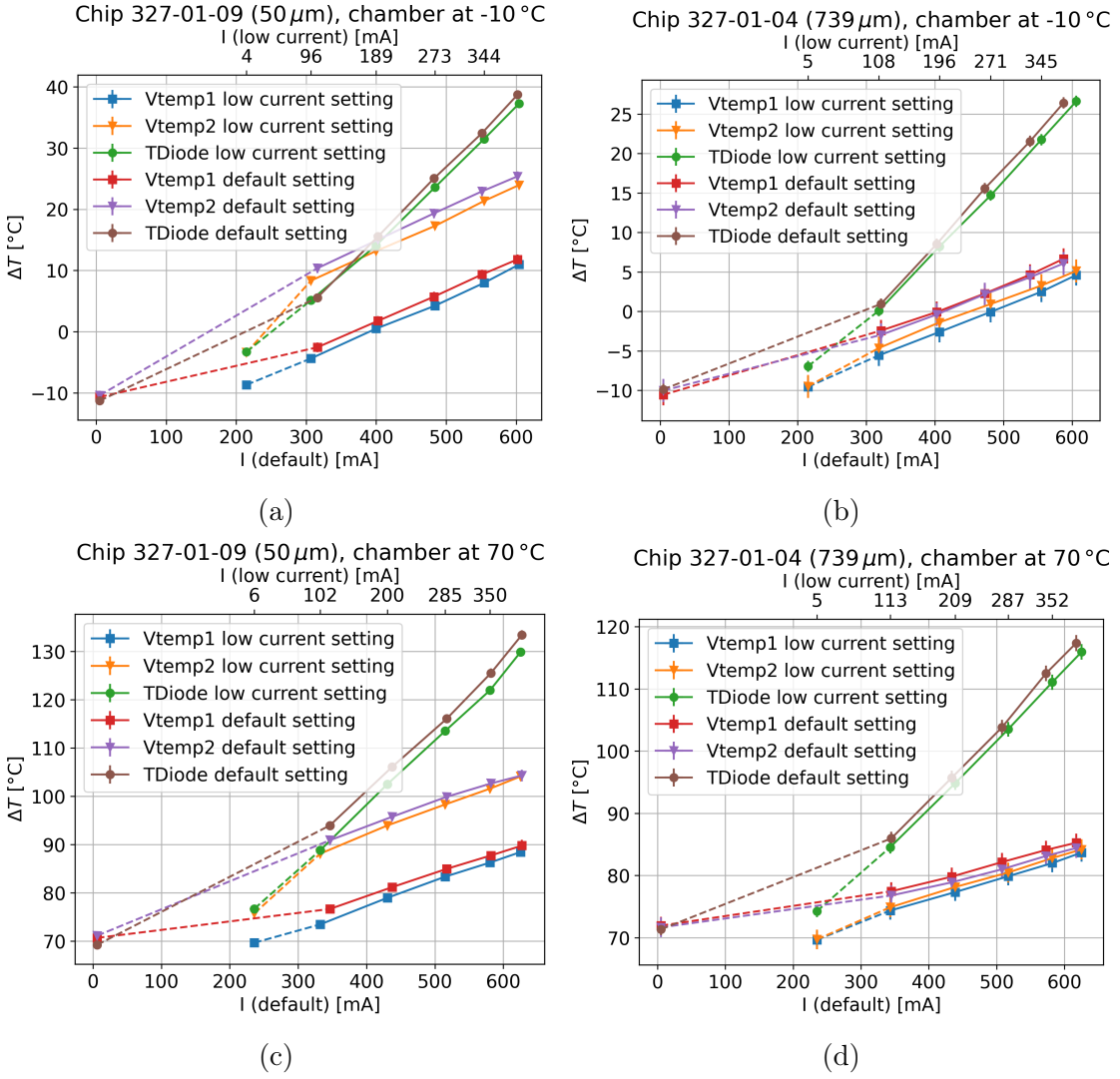


Figure 3.6: Comparison between 'low current' and 'default' setting comparator scans (VComp2) with the climate chamber at −10 °C (a, b) and at +70 °C (c,d). All temperature measurements of the 'low current' settings are shifted on both axes for better comparability of the slopes. The LV current of 'low current' measurements is given by the top x-axis. The LV current of the 'default' measurements is given by the bottom x-axis.

3.2.3 High Temperatures at the Temperature Diode

In each measurement, the temperature diode shows considerably higher temperature increases than the VTemp sensors for the comparator scan (see Figure A.1, Figure A.2 and Figure A.3). At low VComp2 DAC values of around 10 to 20, the diode of the thin chip and VTemp2 measure comparable temperatures (14 K to 16 K above ambient for 'default' settings). With the increased heat dissipation of the comparators at higher DAC values, the temperature diode heats up to significantly higher temperatures than the VTemp sensors.

The absolute temperature of a given spot is determined not only by the heat dissipation around it, but more importantly by its ability to distribute that heat. Around hot spots, heat is transferred to other parts of the chip where it can flow into the temperature reservoir of the surrounding environmental chamber, e.g. by radiation or thermal convection. In this way, areas that are better thermally connected to the rest of the chip will dissipate produced heat and be cooler in equilibrium. Since the thermal conductivity of the substrates ($\kappa_{silicon} \approx 150\,\mathrm{W/(mK)}$) is lower than the thermal conductivity of the electrical traces ($\kappa_{aluminium} \approx 250\,\mathrm{W/(mK)}$), electronically connected components will remain cooler than the surrounding substrate.

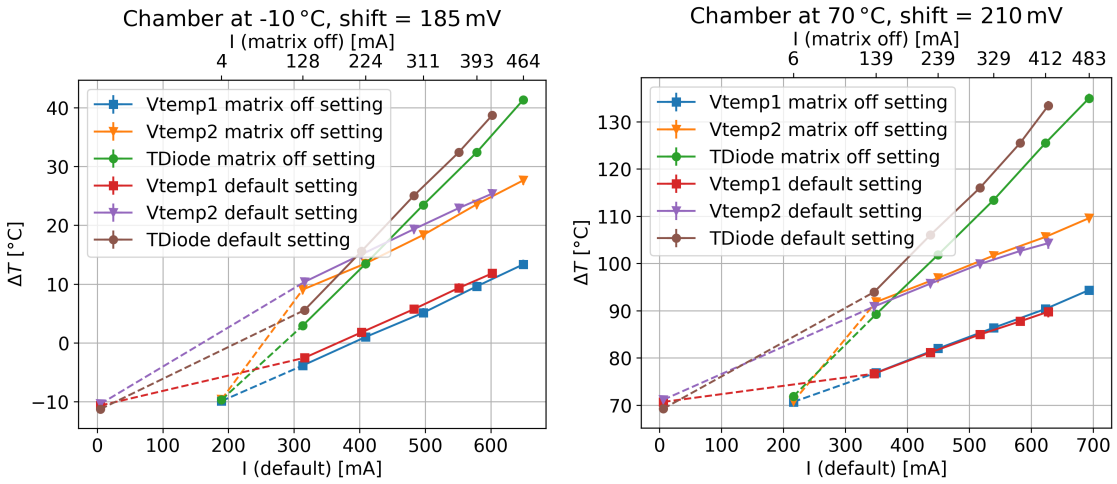
The VTemps circuits consist of many transistors which are electronically connected to a variety of surrounding electrical components via the aluminium traces, e.g. the ADC MUX, the TestOut MUX and especially the VDDA power lines. They will therefore dissipate the nearby produced better than the surrounding substrate. The temperature diode, on the other hand, is separated from other electronics. Apart from the measurement trace connected to the bond pad, it is rather thermally isolated. It mostly uses the surrounding silicon to dissipate the heat, which is less conductive. This explains its greater temperature rise when performing comparator scans. Therefore, the diode measurements reflect the temperature of the substrate in the periphery that cannot distribute the produced heat into the chip via trace connections.

3.2.4 Impact of Pixel Matrix Heating

By switching off the pixel matrix in the aforementioned 'matrix off' settings, its impact on the periphery's temperature can be studied. The 'matrix off' setting is compared to the 'default' setting in Figure 3.7 for chamber temperatures of $-10\,^{\circ}\mathrm{C}$ and $+70\,^{\circ}\mathrm{C}$. In the plots, the 'matrix off' setting measurements are shifted in current for better comparability of the temperatures. It is shifted by the amount of current that additionally flows through the chip when the matrix is switched on. Therefore, the top x-axis provides the LV current of the 'matrix off' measurements while the bottom x-axis gives the LV current of the 'default' settings.

At an ambient temperature of $-10\,^{\circ}\mathrm{C}$, switching on the matrix will increase the current by 185 mA. At $+70\,^{\circ}\mathrm{C}$ it increased by $\sim$ 210 mA. The 'matrix off' settings differed by $<$ 4 mA. This suggests that the increase in current through the chips at

higher temperatures is due to leakage currents in the matrix electronics. This will be discussed further in subsection 4.1.1.



(a) (b)

Figure 3.7: Comparator scan (VComp2) temperature measurement comparison between 'default' settings with the matrix turned on and off. The 'matrix off' measurements are shifted on the x-axis for better visibility. a) −10 °C, b) +70 °C. The LV current of 'matrix off' measurements is given by the top x-axis. The LV current of the 'default' measurements is given by the bottom x-axis.

For the VTemp sensors, the temperature difference between the two settings is 0 K to 1.5 K. When the pixels are turned on, they dissipate heat evenly throughout the matrix. This will immediately raise the temperature. If there was little or no temperature gradient between the matrix and the periphery due to sufficient thermal coupling, this would raise the periphery temperature significantly. However, little to no difference is observed.

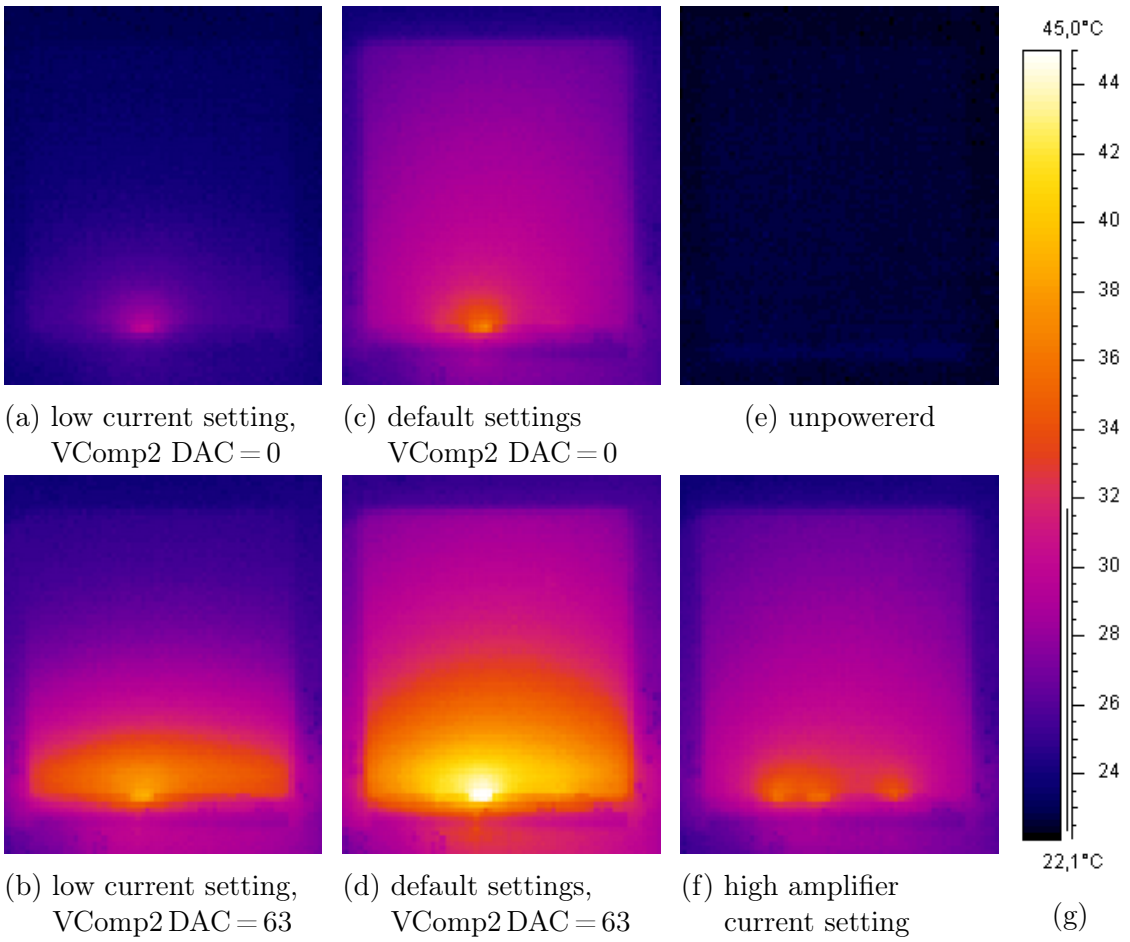
Therefore, significant temperature gradients between the matrix and the periphery can be expected. Hotter areas are less affected by heat dissipation in cooler areas because the temperature gradient is greater. The infrared images in Figure 3.8 support this conclusion: The state machine in the periphery is visible as a clear hot spot in all images. It heats the surrounding material with a circular temperature gradient. Although the infrared camera does not show the temperature of the substrate underneath the sealing layer, the heat distribution clearly matches the temperature measurements of the sensors that indicate a temperature gradient of > 12 K between VTemp1 and VTemp2 in the periphery.

At the same time, most of the cooling of the chip is provided by thermal convection through the contact with the insert PCB. In this setup, the entire backside of the chip has been glued to the PCB, giving the matrix enough contact to transfer

produced heat before it can reach the periphery. This is another reason why the additional heat generated in the matrix has little effect on the peripheral temperature.

The temperature diode shows an increase in temperature of ~ 4 K when the matrix is switched on. Conclusions from the VTemp measurements suggest that this heating is not due to heat dissipation from the matrix. The diode is placed close to one of the VSSA regulators which provides the reference voltage for all the pixel amplifiers. When the matrix is turned on, the regulator will dissipate heat very locally. In Figure 3.8f you can see this effect. For this image, a setting was chosen that exceeds the normal amplifier current. Therefore, the heat dissipation is also visible on the surface as two additional hot spots next to the state machine. The left hot spot is exactly where the diode is located, indicating that the regulator is responsible for the 4 K increase when the matrix is turned on. As discussed in subsection 3.2.3, the diode is not able to dissipate this additional heat like VTemp2. So this temperature increase is reasonable.

This also shows that the temperature of the diode can be mainly attributed to the operation of the state machine as it heats up the diode of > 20 K in 'matrix off' settings. The VSSA regulator only account for an additional heating of ~ 4 K.



(a) low current setting, VComp2 DAC = 0

(c) default settings VComp2 DAC = 0

(e) unpowererd

(b) low current setting, VComp2 DAC = 63

(d) default settings, VComp2 DAC = 63

(f) high amplifier current setting

(g)

Figure 3.8: Infrared images of chip 327-01-09 (50 µm) for different settings. a) and b) show 'low current' settings (in which the pixel matrix is turned off) with the lowest and highest comparator DAC (VComp2) values. c) and d) show this in 'default' settings (in which the pixel matrix is turned on) accordingly. e) is the reference image of the unpowered chip. f) shows a setting with high amplifier current provided by the VSSA regulators in the periphery. This can be seen as 2 additional hot spots next to the state machine. g) is the colour map legend provided by the camera.

3.2.5 Comparison of Thin and Thick Chips

In Figure 3.9, each sensor temperature measurements of the 739 µm thick chip are compared with those of the thinned 50 µm one for −10 °C ambient temperature. Measurements for chamber temperatures of +30 °C and +70 °C can be found in the appendix: Figure A.4, Figure A.5.

For all three sensors, the thick sensor measurements show lower total temperatures than the thin sensor measurements. For the first and last measurement points of the comparator scan (values 0 and 63), the measured temperature differences between the thick and thin chips are displayed in Table 3.1.

Setting	Comp DAC [dec]	ΔT_{diode} [K]	ΔT_{VTemp1} [K]	ΔT_{VTemp2} [K]
low current	0	1.1	0.2	7.0
	63	6.6	5.4	12.8
default	0	4.6	-0.1	13.3
	63	12.3	5.2	19.3

Table 3.1: Temperature deviation between the 739 µm thick 327-01-04 and the 50 µm thin 327-01-09 chip temperature sensors for different settings. (From the measurements in Figure 3.9).

With the comparator switched off, the VTemp1 sensors on both chips measure similar temperatures, differing by only 0.2 K. The diode of the thin chip is moderately hotter ~ 1.1 K to 4.6 K. The most pronounced change was measured with VTemp2 for both 'low current' and 'default' settings. Figure 3.5 shows that the VTemp1 and VTemp2 temperatures are almost the same for the thick chip.

As the power consumption of the comparators increases, the sensors of the thick chip show smaller temperature increases. VTemp1 of the thick chip heats up 3.5 K per 100 mA, which is only 69.1 % of the heating of VTemp1 of the thin chip of 5.1 K per 100 mA. The diode of the thick chip shows 84 % of the heating of the thin chip, the VTemp2 64 % accordingly.

This indicates a much more uniform distribution of heat in the thicker chip. The more than 14-fold increase in silicon substrate greatly enhances heat transfer throughout the chip. The combination of the aluminium traces and the thick substrate allows an equal heat distribution at the periphery between VTemp1 and VTemp2.

The temperature diode is also affected and shows lower temperatures than in the thin chip. However, the inability to conduct additional heat through the aluminium traces discussed in subsection 3.2.3 still holds. These results also agree well with the infrared images shown in Figure 3.10. Compared to the thin chip, the thick chip shows a very even heat distribution for both settings.

In terms of pixel matrix temperatures, the higher temperatures measured on the thin chip can be misleading. Even though the periphery shows relatively higher temperatures, the average matrix temperature can be assumed to be cooler than that of the thick chip. The small amount of substrate of the thin chip prevents the heat – even in equilibrium – from being distributed within the matrix before being dissipated to the surroundings by thermal convection and radiation. This results in cooler pixels far from the periphery, as can be seen in Figure 3.10.

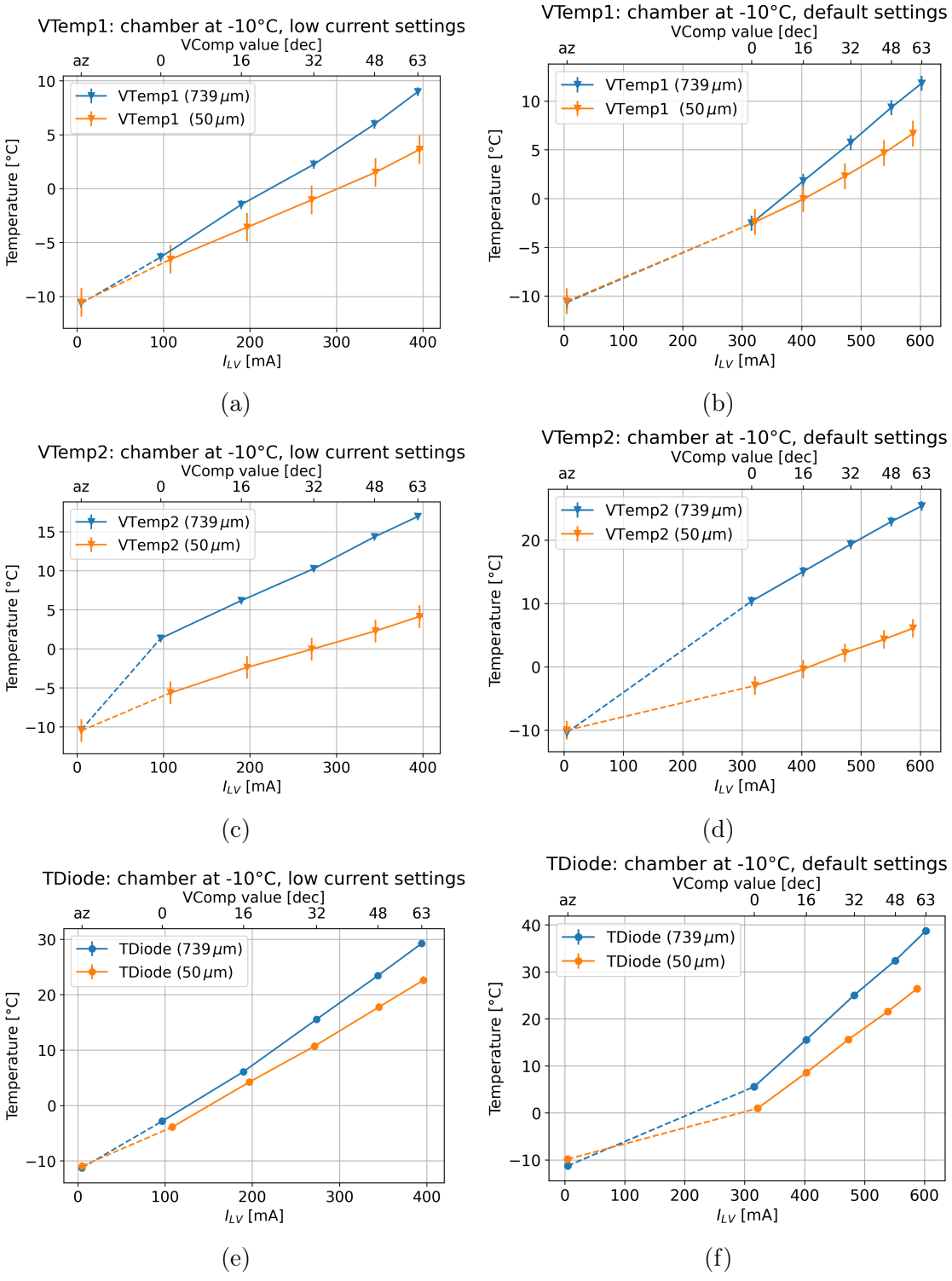
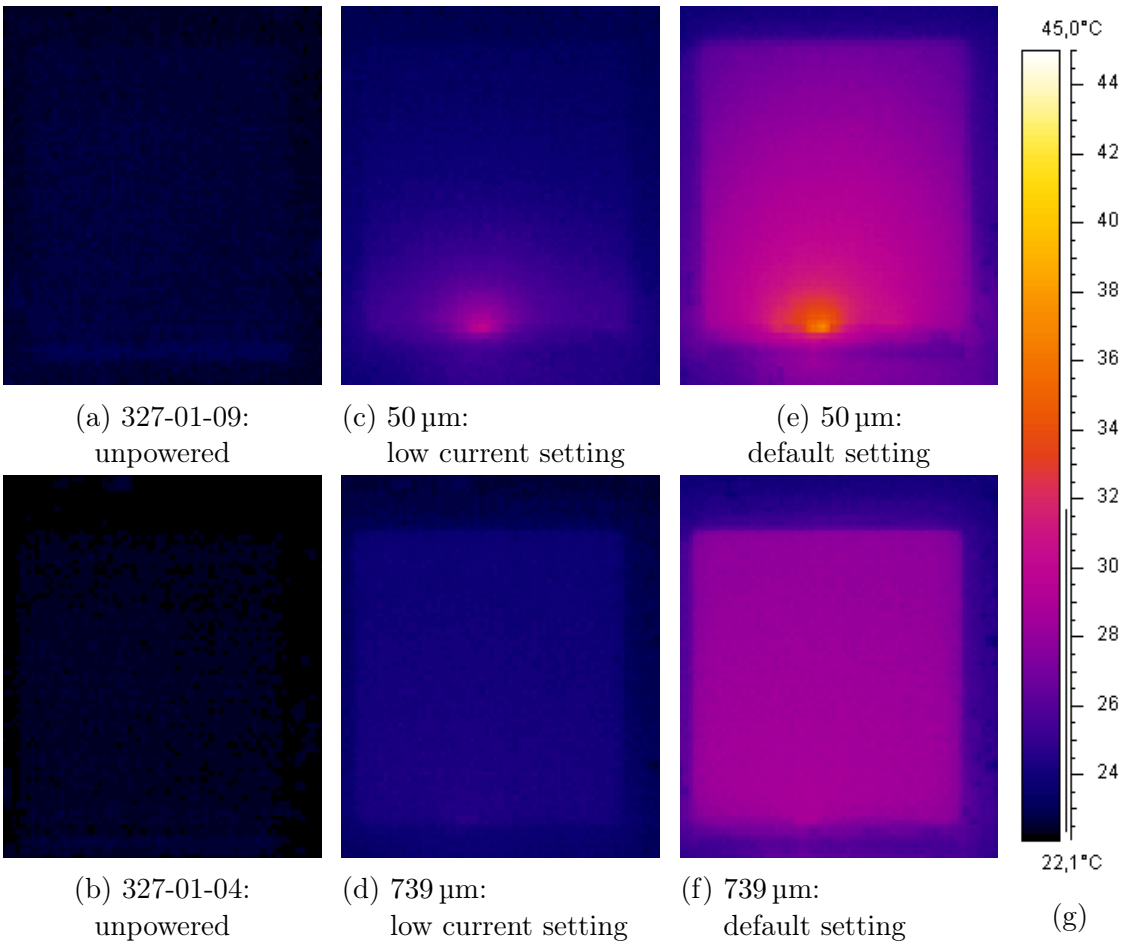


Figure 3.9: Comparison of temperature measurements between the 327-01-04 (739 µm) and the 327-01-09 (50 µm) chip at −10 °C chamber temperature. For each temperature sensor a 'low current' and a 'default' setting is compared.



(a) 327-01-09: unpowered
(c) 50 µm: low current setting
(e) 50 µm: default setting
(b) 327-01-04: unpowered
(d) 739 µm: low current setting
(f) 739 µm: default setting
(g)

Figure 3.10: Infrared images of chip 327-01-04 (739 µm) and 327-01-09 (50 µm) for different settings with the comparators turned off. a) and b) show reference images of the unpowered chips, c) and d) the 'low current' settings, and e) and f) the 'default' settings. g) is the colour map legend provided by the camera.

3.3 VTemp Digital Readout and ADC Calibration

In the Mu3e experiment, there is not enough space on the chip ladders for another readout channel. Thus, the temperatures measurements with the VTemp sensors are conducted entirely digital. An analogue-to-digital converter measures the VTemp voltages on-chip and produces corresponding digital values. These are stored in free data slots in the data stream. For all temperature measurements in section 3.2, this digital readout is also conducted. This chapter focuses on these results. The on-chip ADC is calibrated and its temperature dependence is studied. Finally, the digital measurements are compared with the analogue measurements shown in the previous chapter and possible sources of error are discussed.

3.3.1 ThPix Scans

To convert the digital values from the data stream into voltages, ADC calibration is required. Therefore, a 'ThPix scan' was performed. ThPix is a voltage that can be generated by a voltage digital to analogue converter on the chip. It is used as this voltage is not connected to any power consuming entity which is why it is not influenced by the configuration of the chip. When a ThPix DAC value is selected, the generated voltage can be measured digitally by the ADC and analogue via the TestOut pads. This allows the ADC to be calibrated by making a direct comparison between the analogue voltage and the digital values. The 'ThPix scan' consists of a series of these analogue and digital measurements for increasing 'ThPix' DAC values.

ThPix scans for different ambient temperatures of $-10\,^{\circ}\mathrm{C}$ to $+70\,^{\circ}\mathrm{C}$ are performed for both 'low current' and 'default' settings. Each measurement in the scan takes at least 70 ADC values. The mean of all values is calculated, therefore mon-integer numbers appear in the plot. The uncertainty is calculated as the binary resolution propagated with the standard deviation of all ADC values. For each measurement, three relations are discussed: First, the digital ADC values versus the analogue TestOut voltages (a). This is the calibration curve of the ADC and the data is fitted with linear functions. Second, the selected DAC input values against the digital ADC values (c). Third, the selected DAC input values versus the analogue TestOut voltages (e). This data is also fitted linearly. In the following plots in Figure 3.11 and Figure A.6, all three relations are plotted on the left. On the right hand side the fitted residuals (b, f) and the difference between the DAC and ADC values (d) are shown respectively. Figure 3.11 compares the 'ThPix scan' of the 'low current' setting with the 'default' setting. Figure 3.12 compares scans of ambient temperatures of $-10\,^{\circ}\mathrm{C}$, $+30\,^{\circ}\mathrm{C}$ and $+70\,^{\circ}\mathrm{C}$ at 'default' settings. These measurements are taken with the thin 327-01-09 chip. The same measurements of the thick 327-01-04 chip can be found in Figure A.6 and Figure A.7.

The calibration curve fits return slopes that correspond to binnings of $7.1\,\mathrm{mV/bin}$ to $7.4\,\mathrm{mV/bin}$. The difference in the slopes for the calibration curves in the top left plots (a) for varying settings and temperatures are discussed in the next section.

The focus of this section is the quality of the linear behaviour of the ADC. The top right plots (b) show the absolute fit residuals of the linear fit. It shows maximum deviations < 1 bin which corresponds to < 7.1 mV to 7.4 mV. For most voltages the variations are < 0.5 bins $\triangleq$ 3.5 mV to 3.7 mV.

The same structures in the residuals are observed within every measurement and for both chips. There is a clear downward peak with a maximum at measured ADC values of 152 corresponding to TestOut voltages of 1100 mV to 1140 mV depending on settings and temperature. The residual at the peak is < 0.9 bins bin for $+70\,^{\circ}$C ambient temperature and reduces to < 0.4 bins for $-10\,^{\circ}$C in Figure 3.12. The peak for 'low current' settings Figure 3.12 is at 0.4 bins and > 0.7 bins for the 'default' setting at $+30\,^{\circ}$C chamber temperature. For these voltages, the fit overestimates the ADC value for the analogue TestOut voltage.

To investigate this, the relations between the input DAC values and the measured ADC values, as well as the analogue TestOut voltages are taken into account. The difference between input DAC values and digital ADC values is plotted in the middle right plot (d). The residuals of the linear fit of the input DAC values versus analogue TestOut voltages are shown in the lower right plot (f). Comparing them with (a), a pattern can be observed. The ADC calibration residuals are composed of the DAC-ADC difference (d) and the DAC-TestOut residuals (f). The downward peak originates from the TestOut measurements as it is not visible in the ADC-DAC comparison.

Therefore, the downward peaks in the residuals do not corrupt the digital measurements via the ADC. They are due to the analogue TestOut measurement infrastructure. Some residual structure remains that cannot be attributed to either the DAC or the ADC. The remaining deviations of ~ 0.4 bins $\triangleq$ 2.8 mV to 3.0 mV are in the order of the resolution of binary signals of ~ 0.3 bins. Therefore, its precision as a voltmeter is ~ 0.5 bin which corresponds to 3.5 mV to 3.65 mV.

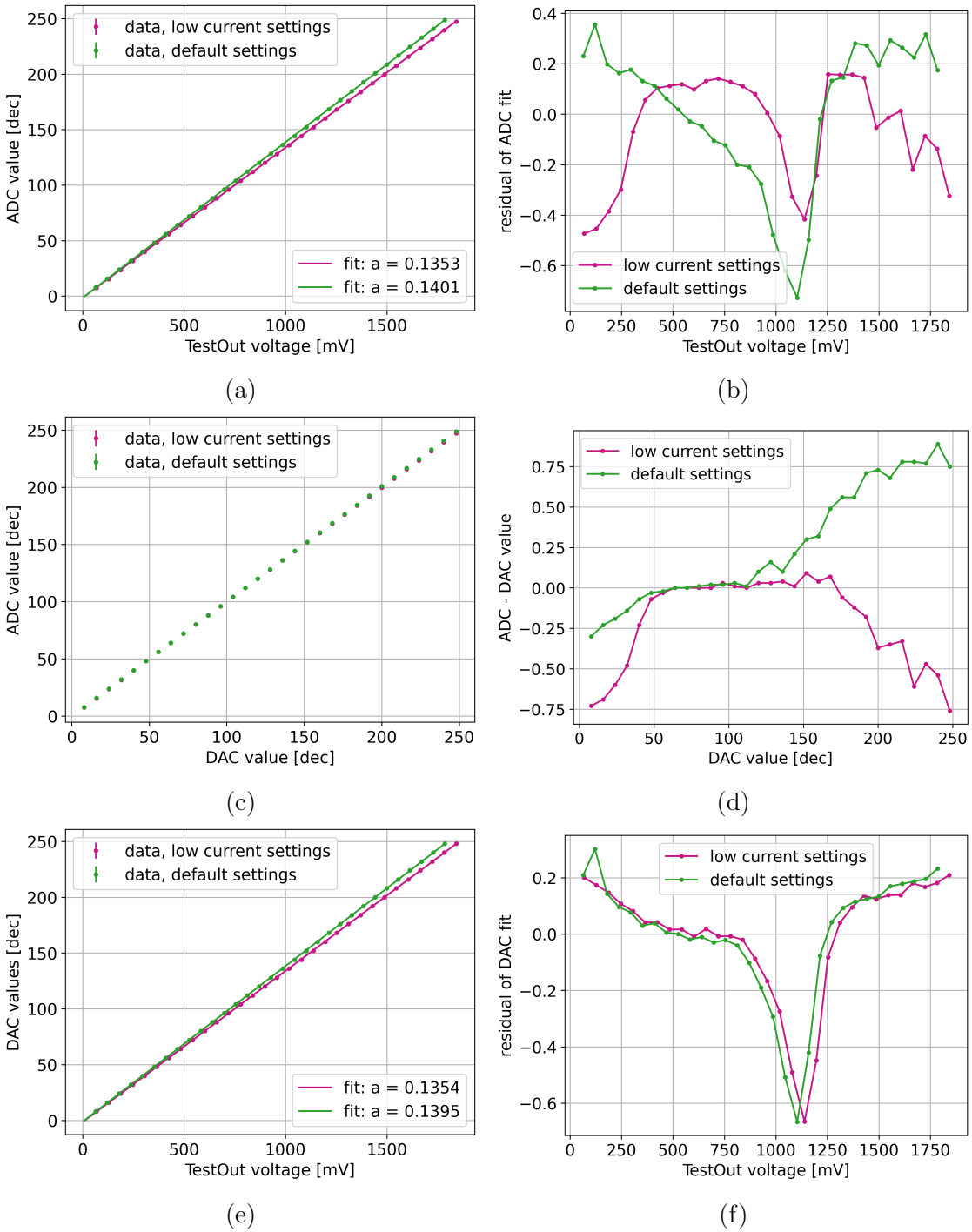


Figure 3.11: ThPix scans of chip 327-01-09 (50 µm) at +30 °C chamber temperature for 'low current' and 'default' settings. The digital ADC values are calculated as the mean of > 70 measured values. Different relations are plotted. In a): the data of the digital ADC values versus the analogue TestOut voltages and their linear fit. Its residuals are shown in b). In c): the selected DAC input values against the digital ADC values. Their deviation is shown in d). In e): the selected DAC input values versus the analogue TestOut voltages and its linear fit. Its residuals are shown in f).

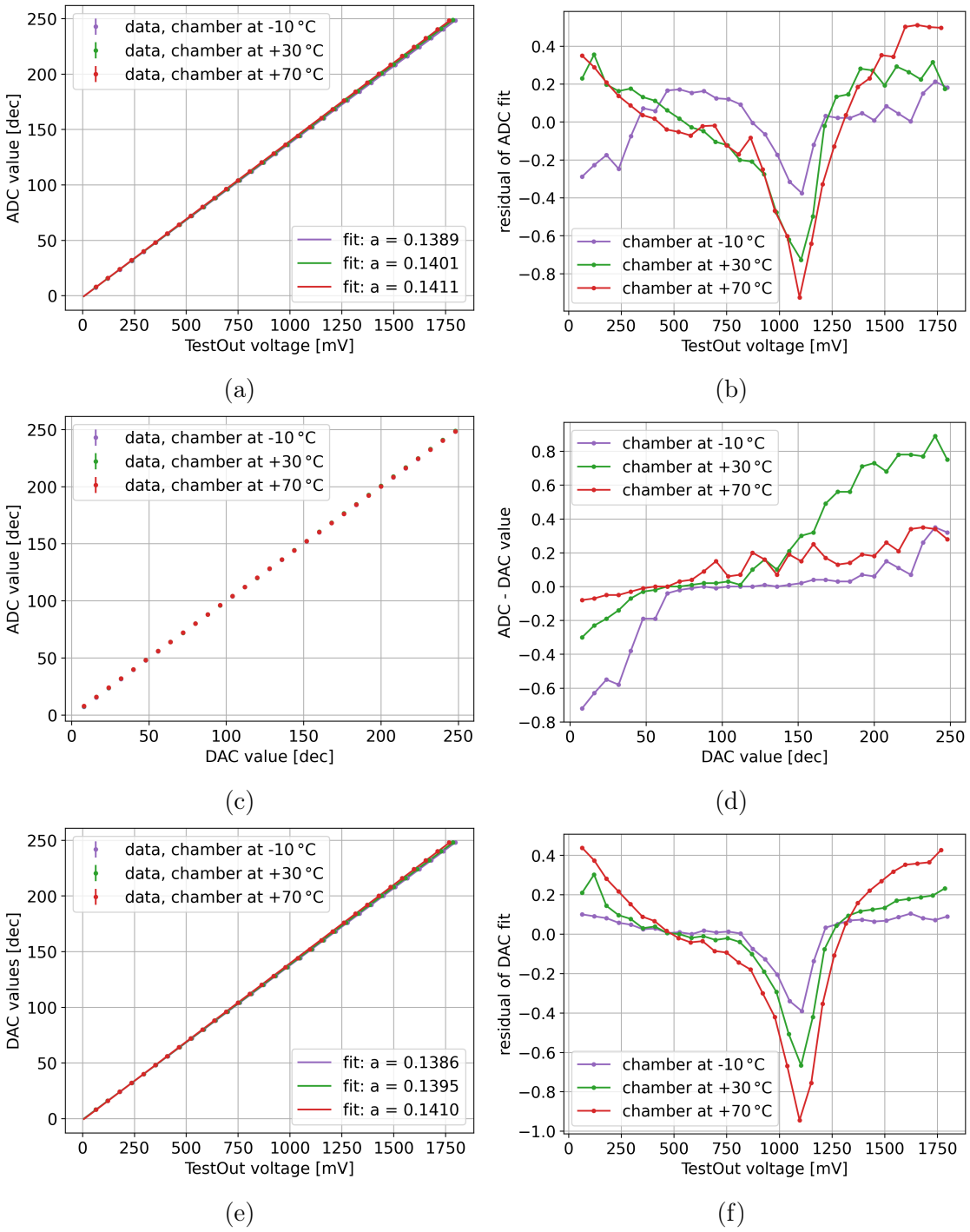


Figure 3.12: ThPix scans of chip 327-01-09 50 µm at 'default' settings for chamber temperatures of −10 °C, +30 °C and +70 °C. The digital ADC values are calculated as the mean of > 70 measured values. Different relations are plotted. In a): the data of the digital ADC values versus the analogue TestOut voltages and their linear fit. Its residuals are shown in b). In c): the selected DAC input values against the digital ADC values. Their deviation is shown in d). In e): the selected DAC input values versus the analogue TestOut voltages and its linear fit. Its residuals are shown in f).

3.3.2 ADC Temperature Dependence

In Figure 3.11a and Figure 3.12a a dependence on temperature and settings of the slopes can be observed for the thin chip 327-01-09. At 'default' (df) settings, the calibration fits return slopes a corresponding to a binning $(1/a)$ of:

$$U^{df}_{ThPix} = 7.20\,\mathrm{mV/bin} \cdot v_{ADC} \quad \text{at } -10\,^{\circ}\mathrm{C} \text{ ambient temperature,} \tag{3.5}$$
$$U_{ThPix}df = 7.14\,\mathrm{mV/bin} \cdot v_{ADC} \quad \text{at } +30\,^{\circ}\mathrm{C} \text{ ambient temperature and} \tag{3.6}$$
$$U_{ThPix}df = 7.09\,\mathrm{mV/bin} \cdot v_{ADC} \quad \text{at } +70\,^{\circ}\mathrm{C} \text{ ambient temperature} \tag{3.7}$$

with the ADC values v_{ADC}. Higher temperatures lead to increased calibration fit slopes a, which corresponds to a decreasing bin size at 'default' settings. At 'low current' (lc) settings the calibration fits return slopes corresponding to binning of:

$$U^{lc}_{ThPix} = 7.40\,\mathrm{mV/bin} \cdot v_{ADC} \quad \text{at } -10\,^{\circ}\mathrm{C} \text{ ambient temperature,} \tag{3.8}$$
$$U^{lc}_{ThPix} = 7.40\,\mathrm{mV/bin} \cdot v_{ADC} \quad \text{at } +30\,^{\circ}\mathrm{C} \text{ ambient temperature and} \tag{3.9}$$
$$U^{lc}_{ThPix} = 7.38\,\mathrm{mV/bin} \cdot v_{ADC} \quad \text{at } +70\,^{\circ}\mathrm{C} \text{ ambient temperature.} \tag{3.10}$$

The temperature effect on the 'low current' settings is negligible. The same behaviour is observed for the thick chip 327-01-04.

The operating voltage of the ADC is the VDDA analogue domain. It powers most of the pixel electronics, such as the amplifier and signal driver. Its initial voltage is given by the low voltage (LV) supply of 1.9 V which also provides for the VDD digital domain. When the pixels are in operation, they consume power, resulting in an on-chip voltage drop in VDDA. Firstly, this depends on the pixel configuration, i.e. the settings used. Secondly, the operating points of the pixel electronics will shift as the temperature changes, resulting in a change in LV current. This also affects the VDDA level in the 'default' settings.

Therefore, the VDDA level may vary depending on settings and temperature. If the supply voltage for an ADC changes, its binning will change accordingly. Consider the following calculation for different supply voltages:

$$\begin{aligned} \frac{1}{a_1} &= \frac{1.9\,\mathrm{V}}{256\,\mathrm{bins}} \approx 7.42\,\mathrm{mV/bin} \\ \frac{1}{a_2} &= \frac{1.8\,\mathrm{V}}{256\,\mathrm{bins}} \approx 7.03\,\mathrm{mV/bin} \end{aligned} \tag{3.11}$$

Figure 3.13 plots the ADC calibration fit parameters against the measured VDDA voltage. The VDDA voltage is is determined as the difference between the VDDA level (vdda1) and the VDDA ground level (gnda1) via the voltage pads on the insert PCB. It cannot be measured digitally on-chip as it it the reference voltage for the ADC. Also it is not reachable in the Mu3e experiment, as there is not enough space on the ladders for another readout channel. In all four plots, the six measurement

points at lower the VDDA voltages > 1850 mV are at 'default' settings where the pixels are operated. This results in large temperature dependent voltage drops. The 'low current' settings are at VDDA voltages close to 1.9 V and show small voltage drops.

The temperature dependence of the on-chip voltage drop in VDDA is clearly visible. The VDDA voltage at +70 °C is 1821 mV and increases linearly to 1849 mV at +70 °C for 'default' settings with disabled bandgap for chip 327-01-09. For each temperature and setting, a measurement is also made with the bandgap switched on. As the bandgap circuit compensates for temperature effects on the reference current for many entities, the measurements are performed to test if the VDDA voltage drops can be reduced. However, the enabling of the bandgap only shifted the VDDA voltage to higher values by 5 mV for each temperature. For all of the measurements, temperature dependence of the slope remains the same. This means, the currents that induce the voltage drop in VDDA are independent of the currents the bandgap circuit supplies for the chip.

The slopes a of the ADC calibration fit show linear behaviour with the VDDA voltage. A linear function is fitted to the data. In addition, the theoretical values are calculated according to Equation 3.11. The ADC calibration fit offset b shows no dependence on the VDDA level.

This shows that the on-chip VDDA voltage drop must be taken in to account when calibrating the ADC. In the laboratory this can be achieved by simply tracking the VDDA voltage for each temperature measurement. As discussed, the Mu3e experiment, this is not possible as the VDDA cannot directly be measured. The next section focuses on the digital VTemp measurements in the laboratory and discusses the impact of the temperature dependency of the ADC calibration. In subsection 3.4.3 the implications for the Mu3e are further discussed.

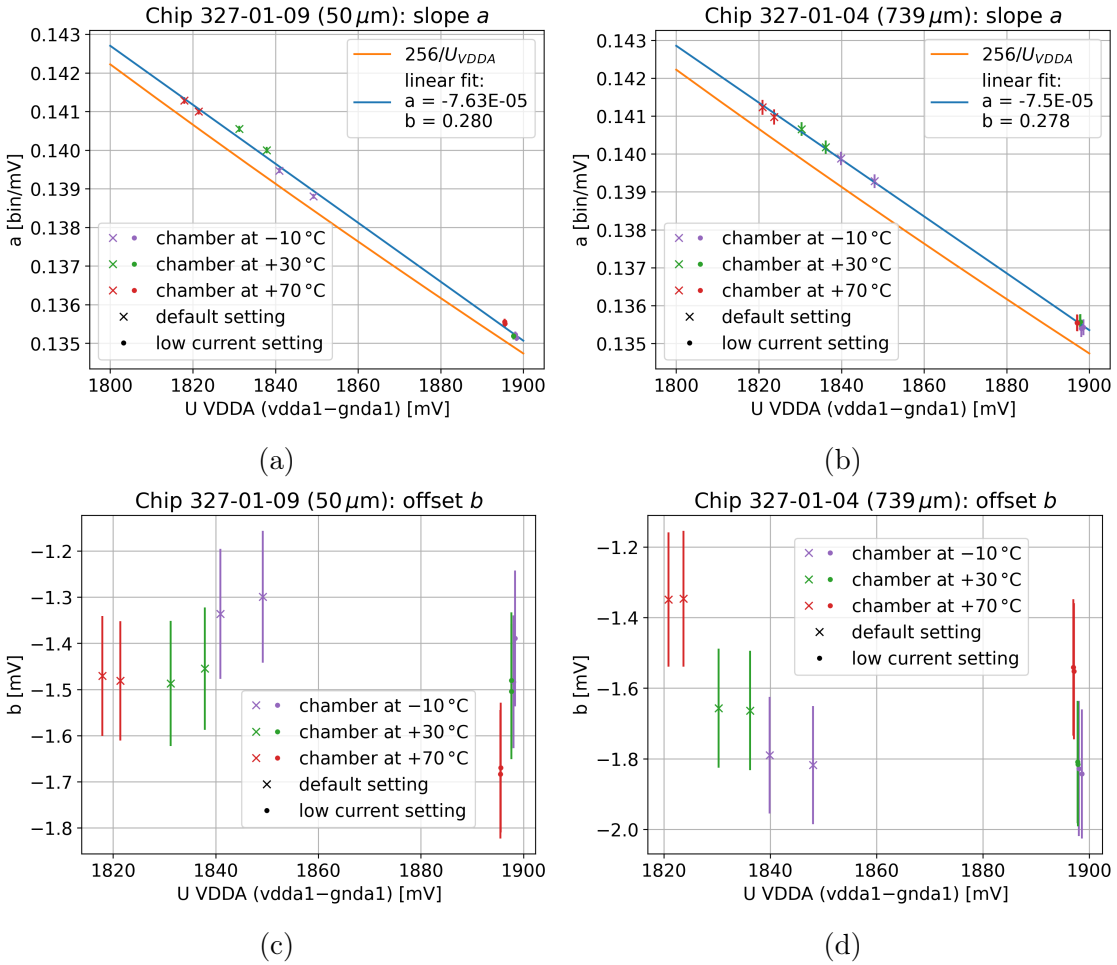


Figure 3.13: Linear fit parameters of the ADC calibration against the VDDA level for different temperatures and settings. (a,b) depict the slope of the ADC calibration fit and (c, d) the offset. The slopes in a) and b) are linearly fitted and the plot also shows the theoretical curve for the ADC binning the VDDA level in 256 steps without offset.

3.3.3 Digital VTemp Temperature Measurements

To take the VDDA voltage drop into account when calibration the ADC, each digital temperature measurement of the VTemp sensors also requires a VDDA voltage drop measurement. Then the calibration slope a and thus the binning $1/a$ can be determined with Figure 3.13 to convert the ADC values into voltages. The offset b is determined by the average of the fit parameters for 'low current' and 'default'. The VTemp temperature calibrations from Equation 3.4 then returns the absolute temperatures.

This is done for all of the comparator power scan temperature measurements from

section 3.2. For the 'default' settings this gives bin sizes p^{09} of:

$$p^{09}_{min} = 2.649\,\mathrm{K/bin} \quad \text{for VTemp1 at } -10\,^{\circ}\mathrm{C} \text{ chamber temperature and} \tag{3.12}$$

$$p^{09}_{max} = 2.709\,\mathrm{K/bin} \quad \text{for VTemp2 at } +70\,^{\circ}\mathrm{C} \text{ chamber temperature} \tag{3.13}$$

for the thin chip 327-01-09 and bin sizes p^{04} of:

$$p^{09}_{min} = 3.034\,\mathrm{K/bin} \quad \text{for VTemp2 at } -10\,^{\circ}\mathrm{C} \text{ chamber temperature and} \tag{3.14}$$

$$p^{09}_{max} = 3.373\,\mathrm{K/bin} \quad \text{for VTemp1 at } +70\,^{\circ}\mathrm{C} \text{ chamber temperature} \tag{3.15}$$

for the thick chip 327-01-04.

In Figure 3.14 the digital VTemp temperature measurements of the comparator scans are compared to the analogue ones via the TestOut at $+70\,^{\circ}$C chamber temperature. Measurements at $-10\,^{\circ}$C and $+30\,^{\circ}$C chamber temperature can be found in Figure A.8 and Figure A.9.

The 50 µm thin chip (327-01-09) shows significant deviations between the digital and analogue measurements. The temperatures obtained from the data stream are of the order of 5 K lower for both 'default' and 'low current' settings at chamber temperatures of $+70\,^{\circ}$C. This reduces slightly to < 4 K at $-10\,^{\circ}$C chamber temperature.

The digital measurements from the 739 µm chip 327-01-04 are of the order of 4 K larger than the analogue measurements at $+70\,^{\circ}$C ambient temperature. However, at lower chamber temperatures of $-10\,^{\circ}$C and $+30\,^{\circ}$C both measurements agree within < 2 K deviation (see Figure A.8 and Figure A.9).

To investigate this discrepancy between the digital and the analogue measurements, the VTemp measurements from the comparator power scans are directly compared to the 'ThPix' scan from subsection 3.3.1 used for ADC calibration. This is shown in Figure 3.15.

The VTemp1 sensor of the thin chip shows significant deviations from the 'ThPix' scans for all ambient temperatures. For both 'low current' (Figure 3.15a) and 'default' settings, (Figure 3.15d) either the measured TestOut voltages are too high (by ~ 15 mV) or the ADC values from the data stream are too low (by ~ 2 bins) in order for them to agree. The mismatch in Figure 3.15 clearly indicates a systematic offset for chip 327-01-09. Chip 327-01-04 shows better fitting results for both settings at $-10\,^{\circ}$C and $+30\,^{\circ}$C ambient temperature. However, at $+70\,^{\circ}$C the measured TestOut voltages are either too low (by ~ 7 mV) or the ADC values from the data stream are too high (by ~ 1 bins). These discrepancies at high chamber temperatures for the thick chip 327-01-04 are opposite to the systematic offset produced by the thin chip 327-01-09. They most likely come from different sources.

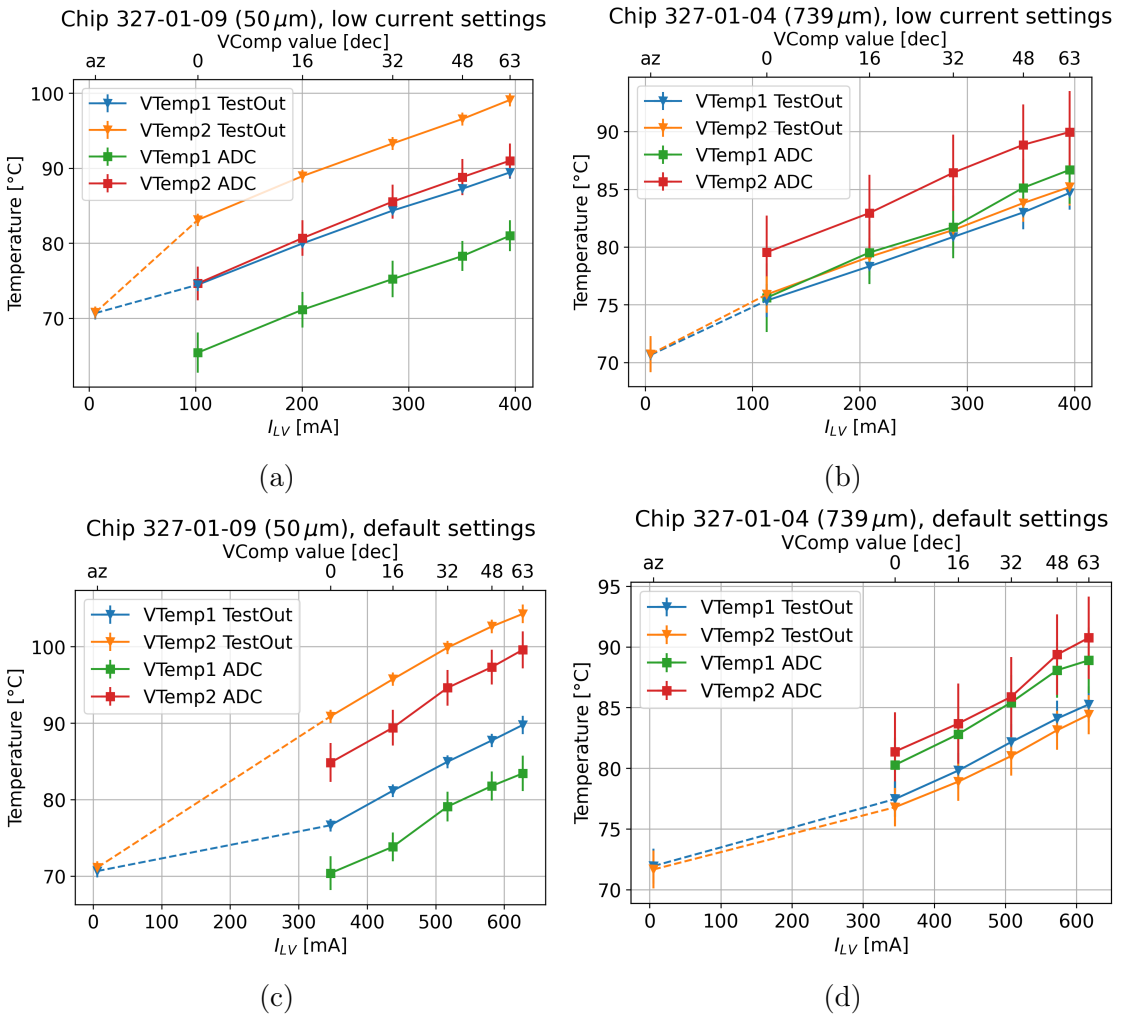


Figure 3.14: Comparator scan (VComp2) temperature measurement comparison of VTemp measurements: analogue via the TestOut and digital via data stream after ADC calibration for different settings at +70 °C chamber temperature.

There are three possible reasons for the systematic discrepancy between the two measurements. The first is related to the analogue meter. The current produced by the VTemp transistors is forced through a 800 kΩ resistor, as shown in subsection 1.4.2. The voltage drop across this resistor is then measured. For analogue measurements via the TestOut pad, a high ohmic voltmeter is required which does not create parallel currents and thus lower the measured voltage, as described in subsection 2.2.1. Even if a power supply has been used that allows currents of the order of nA to flow, this can still be a problem. Any parasitic resistance of the order of MΩ in the circuit would lower the measured voltage values. However, the systematic error for chip 327-01-09 indicates that the TestOut voltages are too high. In addition, a systematic offset coming from the voltmeter is expected to be the

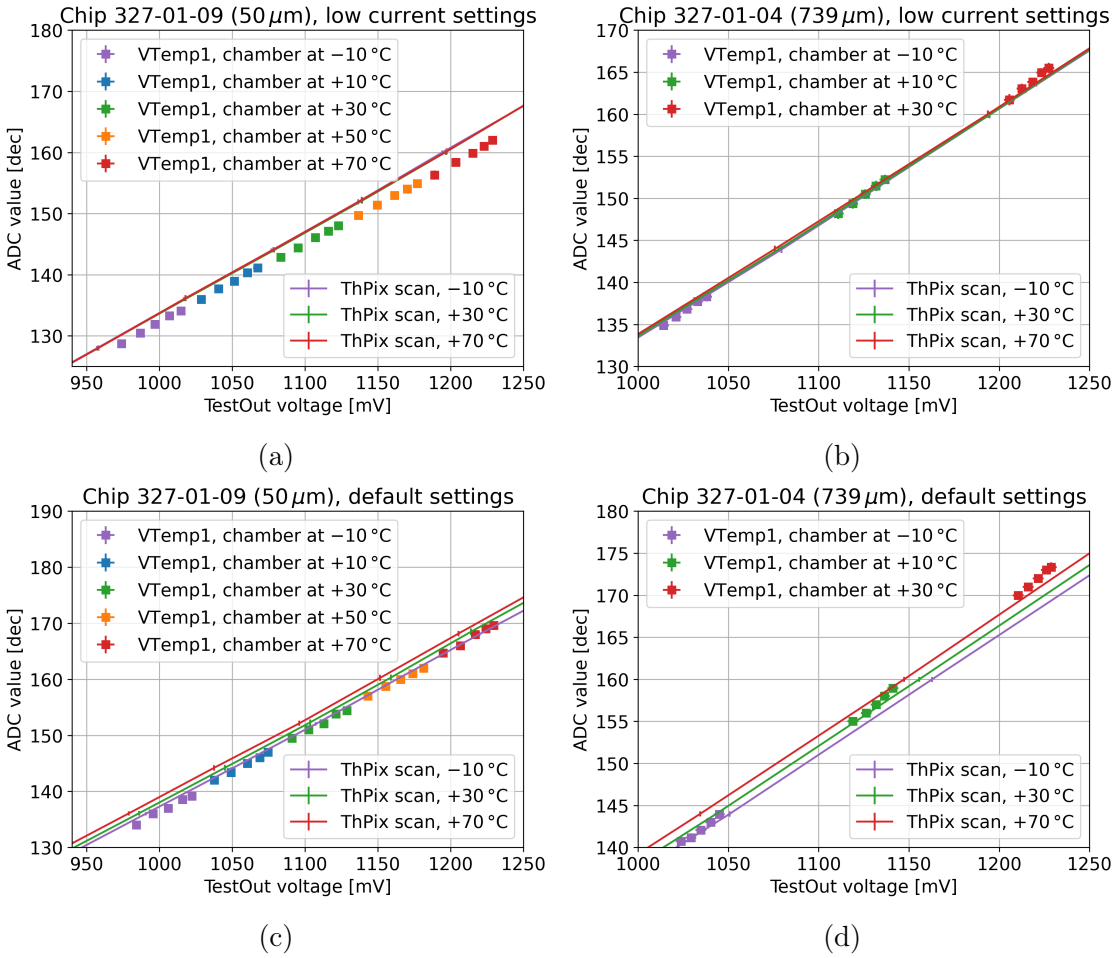


Figure 3.15: Comparison of the ThPix scans used for ADC calibration and the VTemp1 measurements for different settings. The analogue TestOut voltage is plotted against the digital ADC value. For the ADC value the mean of > 70 measurements is used. The same plots for VTemp2 can be found in Figure A.10

same for both chips which is not the case. It is therefore unlikely that this source of error is responsible for the large systematic error observed in Figure 3.15a and Figure 3.15d.

Of course, the ADC faces the same challenge when measuring the high ohmic VTemp voltage. If its internal resistance is of the order of MΩ, it would measure lower voltages as described above. The resulting ADC values would be lower than the high ohmic measurements via TestOut as shown in Figure 3.15a and Figure 3.15d. However, both chips would be equally affected by a fault caused by a parasitic resistance in the ADC. Either process variations in the ADC are causing different ohmic ADCs, or the offset is elsewhere.

Another error source are the multiplexers. As described in subsection 1.4.2, the voltage for the TestOut measurements goes through both the slow control MUX

and the TestOut MUX. These measurements deviate from ~ 2 mV to 5 mV. This indicates that the voltages change as they pass through the MUX. Therefore, the TestOut measurements would be shifted in the first place. As the temperature calibration is calculated using the TestOut measurements, the whole calibration curve would be shifted by an offset. Therefore, the VTemp temperature calibrations would not apply for the digital measurements but shifted by an offset.

Lastly, the quality of the compensation for the temperature dependence of the ADC calibration (see subsection 3.3.2) is evaluated. The analogue measurements are therefore used as a reference.

The temperature difference ΔT of the analogue TestOut $T_{TestOut}$ and the digital ADC measurements T_{ADC} are calculated and compared using different ADC calibrations. For once, ADC calibration slopes a from the fit in Figure 3.13 are used. They take into account the temperature dependence as the VDDA voltage of each measurement is used to obtain the corresponding slope a. The corresponding temperatures are referred to as the 'T-calibrated' temperatures.

Secondly, an ADC calibration was used with a fixed calibration slope a_0. The slope from the fit at +30 °C chamber temperature is used so that the ADC is calibrated correctly at this temperature. This calibration does not take temperature changes into account. It is referred to as 'not T-calibrated'.

Figure 3.16 shows the difference between the temperatures of the analogue measurements and the digital ADC measurements for both ADC calibration methods. For these measurements, the chip is operated in 'default' settings with the comparators switched off (VComp2 DAC value = 0).

The difference between the measured temperatures of the TestOut and the 'not T-calibrated' digital values depends on the chamber temperature. At −10 °C it is −6 K and rises to −3 K at +70 °C for the thin chip 327-01-09. This behaviour is expected as a_0 does not take into account the temperature effect on the ADC. For ambient temperatures > +30 °C the slope a_0 overestimates the voltages corresponding to the digital ADC values, resulting in higher temperatures.

Although a_0 was chosen as the calibration slope from the ADC calibration curve at +30 °C ambient temperature, the data deviates by > 4.5 K. This constant offset is a systematic error which will be investigated below.

Chip 327-01-04 shows a similar linear behaviour for the 'not T-calibrated' values. The difference is 3 K at −10 °C and rises to >6 K at +70 °C chamber temperature. However, in this case the measurements at +30 °C agree with a deviation of < 0.2 K. No such systematic error is observed.

The 'T-calibrated' digital measurements are supposed to compensate for the linear dependence in the difference. The measurements of chip 327-01-09 suggest overcompensation, as the linear behaviour is reversed: the difference at −10 °C is −3 K and drops to −6 K at +70 °C.

However, the compensation of temperature dependence of ADC calibrating with the 327-01-04 chip works much better, as shown in Figure 3.16b and Figure 3.16d. The large differences are reduced to < 0.5 K at −10 °C to +30 °C and < 3 K at

+70 °C ambient temperature. The calibration that takes into account the effect of temperature ('T-calibrated') differs from ~ 5 K to 7 Kper80 K which corresponds to 6 % to 8 % from the values calibrated without consideration of temperature effects ('not T-calibrated').

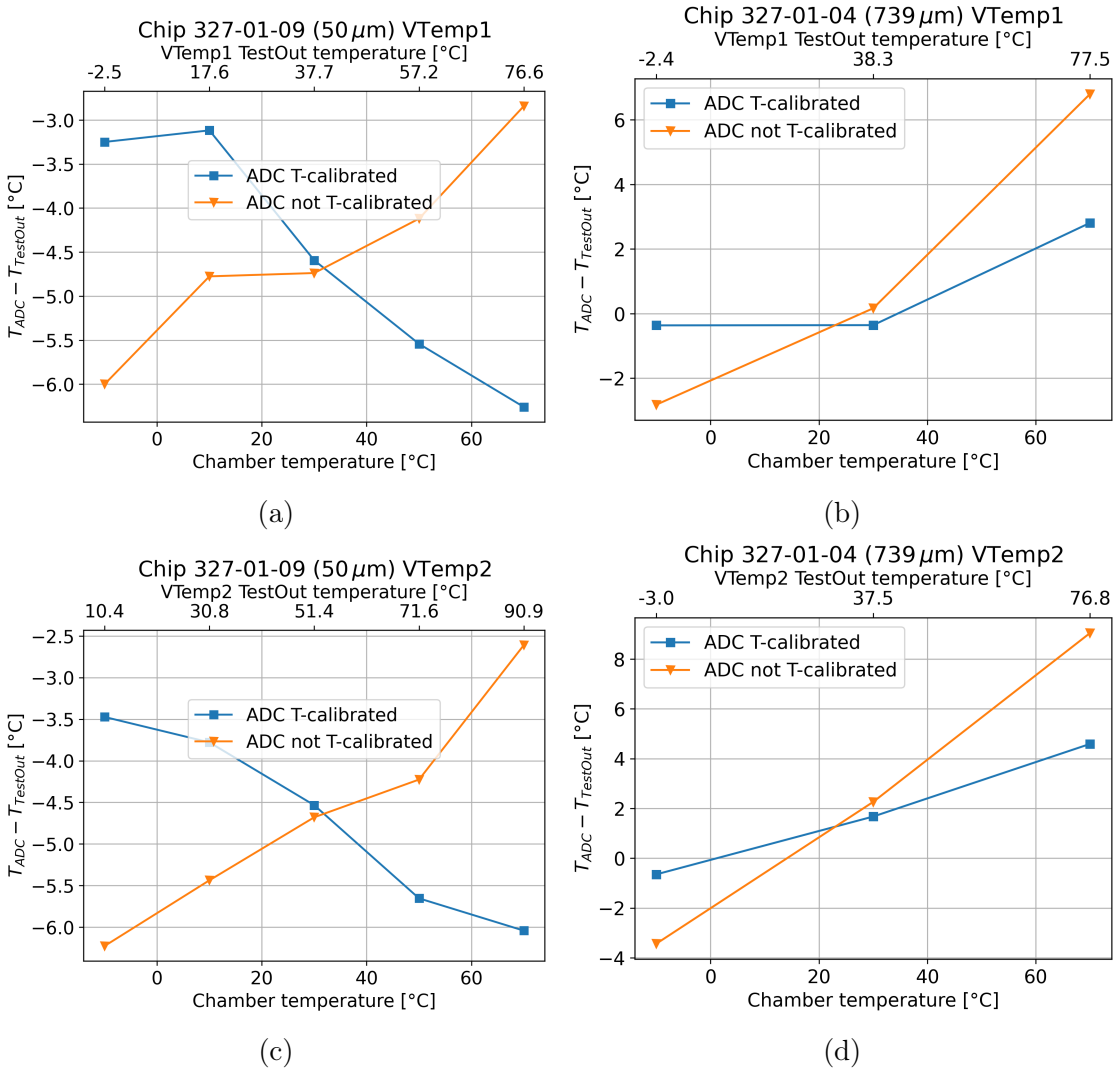


Figure 3.16: Comparison of two different ADC calibrations: The difference between the temperatures of the analogue measurements and the digital ADC measurements after two different ADC calibrations are plotted. The 'T-calibrated' values were obtained using an ADC calibration that takes into account the effect of temperature on the ADC. The 'not T-calibrated' values were obtained using a fixed ADC calibration curve. a): chip 327-01-09 (50 µm), b) chip 327-01-04 (739 µm).

This shows that the discrepancy between the digital ADC measurements and the analogue TestOut measurements is not related to the observed temperature effects

on the ADC due to VDDA voltage drops.

In conclusion, the digital VTemp measurements on the data stream were successful. It is possible to detect temperature changes and trends quite well as shown in Figure A.8, Figure A.9 and Figure 3.14. The bin size p is between 2.649 and 3.373 K. However, the VTemp measurements of the thin chip 327-01-09 show a discrepancy between the analogue measurements from the TestOut pad and the digital measurements from the ADC. This offset > 5 K is not yet fully understood. In addition, the calibration used to convert the digital values from the ADC into voltages is temperature dependent. Under laboratory conditions it is possible to compensate for this by tracking the VDDA voltage. In the Mu3e experimental setup, this is no longer possible. The implications for the Mu3e experiment are discussed in the next section.

3.4 Applications for the Mu3e experiment

Calibration and measurements of the temperature sensors in the lab not only confirmed their functionality, but also provided insight into the heat distribution of the chips. First conclusions can be drawn, despite some open questions regarding the ADC calibration for the digital readout of the VTemps via the data stream.

This chapter discusses the estimation of the chip temperature from the measurements of the integrated sensors. Secondly, it gives some ideas about the on-chip temperature calibration in the Mu3e experiment. Therefore, the focus is on the thin 50 µm sensors as they will be used in the experiment.

3.4.1 The MuPix11 Temperature Estimation

As seen in the previous chapter, the heat distribution in thinned 50 µm MuPix11 chips is uneven. There is a significant temperature gradient between the hot spot at the periphery and the active area. VTemp1 and VTemp2 are thermally connected to each other and to the rest of the chip by aluminium traces. There are power supply lines connected to all pixels in the chip matrix suggesting that the matrix has comparable thermal link to the periphery as VTemp1 has to VTemp2. This results in a temperature gradient between the chip matrix and the readout electronics similar to the gradient between VTemp2 and VTemp1 of 12 K to 14 K. How well this assumption fits the actual temperature distribution in the substrate on the chip needs further validation.

The infrared images in Figure 3.8 however support this conclusion, showing a fairly circular heat gradient around the hot spot. A large area of the chip matrix has the same temperature as the area in the periphery where the VTemp1 circuit is located.

Each of the VTemp temperatures therefore gives a good estimate of a different representative area of the active region. The VTemp2 temperatures correspond to

a small number of the hottest pixels immediately adjacent to the state machine in the periphery. VTemp1 provides an estimate of the average pixel temperature as it is at a similar distance from the hot spot as the central pixels.

Temperature diode measurements refer to parts of the silicon that are not able to distribute heat to the surrounding chip via aluminium traces. It is not a good estimate of the chip matrix temperature. However, it can indicate temperature peaks in the periphery.

In subsection 3.2.4, the marginal effect of matrix heating on the temperature of the periphery was discussed. Undesired matrix heating mechanisms at a single chip may be difficult to detect with any of the temperature sensors. These effects are not studied in this thesis but might be of interest for further investigation. However, all three temperature sensors are very capable of showing local and global temperature trends in the detector, which is what they are designed for.

3.4.2 Temperature Diode Implementation in the Mu3e experiment

In the Mu3e experiment, the temperature diode will be part of an interlock system that shuts down power when certain diode voltages indicating overheating are measured. Due to process variations, not all diodes will reach critical levels at the same temperatures. In order to extract chip temperatures and set interlock thresholds, temperature calibration must be performed on multiple sensors.

Temperature calibration of the sensors is required before they can be used in the experiment. The tracking detector will contain 2844 MuPix11 sensors on 174 ladders of different sizes. Two sensors on each ladder (one on each half-ladder) will be used to measure the temperature of the diode. Since the individual diode calibration in a climate chamber of 348 sensors would take too much time, it is not possible to calibrate the diode of each chip as was done in this thesis. Therefore, after introducing the measurement conditions, two possible calibration methods are presented and their limitations are discussed.

There are two setups in which the temperature diodes of the chips can be operated before the Mu3e experiment is initialised. Firstly, there is a quality control (QC) of each chip in the laboratory after production. This is to rule out sensors that don't work. In the testing station, the chip can be configured and operated, and temperature diode measurements can be taken. For both calibration methods, a test measurement of the diode should be carried out.

The diode reference measurement for further calibration should be conducted in the 'all zero' settings. In this setting, every power consuming unit is turned off and self heating with a the power consumption of 7.6 mW to 11.4 mW is assumed to be negligible (see subsection 3.1.1). It would also be possible to conduct temperature diode measurements with a completely unpowered chip. However, the 'all

zero' settings allow the LV to be applied to the diode which mimics the condition of operating chips.

In the first calibration method the calibration curves of each half-ladder diode is determined individually. This requires the possibility to measure each half-ladder diode in the experimental setup. Additionally, it must be possible to regulate the temperature of the entire tracking detectors in such a way that at least two uniformly distributed temperatures. One way to achieve this is to use the helium cooling system by supplying the detector with different gas temperatures. Another possibility is the use of heating units for the control of the ambient temperature of the whole setup. Finally, the comparators of the chips themselves can be used as a heat source. The consistent heat dissipation with respect to power consumption is demonstrated in section 3.2. Temperatures between 10 °C and 30 °C are realistic to control in the setup. Therefore, measurement points with 10 K difference could be aimed for.

However, the calibration measurements cannot be taken during this heating process as the periphery would be much hotter than the rest of the chip. The system needs time to distribute the heat evenly throughout the detector before the measurement can be taken. The timescales for this would need to be further investigated.

In the experimental setup, 'all zero' settings are applied all sensors. From here, calibration measurements can be made at different ambient temperatures of the detector. A minimum of three calibration points should be taken to calculate the linear calibration curve. One of them can be the measurement from the testing station.

The accuracy of the calibration is limited by the temperature range that can be controlled, how evenly the heat is distributed, the temperature difference between two measurements and the number of measurements at different temperatures. This is not studied in this thesis but should be subject of further investigation as it if of great importance for the applicability of this method in the Mu3e experiment.

The second calibration method does not require a controlled temperature regulation of the experimental setup. It uses a common calibration slope a_c for all diodes. Therefore, it requires only the single measurement of the testing station at room temperature to determine the offset parameter. The common calibration slope and it's error must be estimated from temperature calibrations in the laboratory climate chamber for a representative number of chips from different batches. Although the sample of two chips used for this thesis is not representative, their small standard deviation in calibration slopes of $< 1.5\,\%$ suggests little process variation. This is plausible given the simple diode architecture of the sensor which makes it less susceptible to process variation than the multi-transistor VTemp circuits.

The magnitude of the absolute temperature error for this method is calculated assuming different deviations δ in the calibration slopes. The common slope a_c is calculated from the average of the calibration slopes obtained from both chips. Calibration slopes differing by (10, 20 and 30)% from a_0 are calculated. An arbitrary voltage has been chosen to represent the +20 °C room temperature measurement in

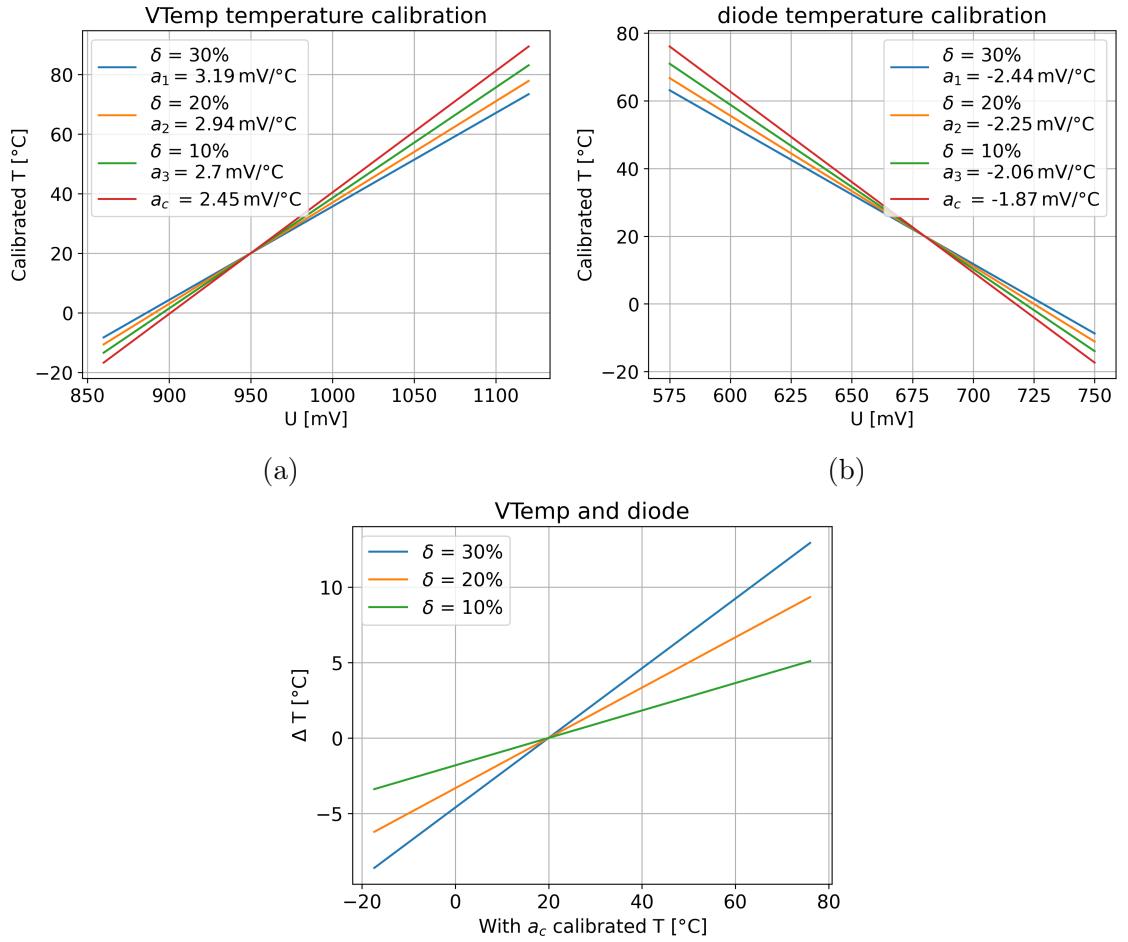
the test station.

The resulting calibration curves are shown in Figure 3.17b. Their absolute temperature deviations from the common slope calibration are shown in Figure 3.17c. In Table 3.2 these errors are listed for slope variations of (1.5, 5, 10, 20 and 30)% for different temperatures. The error increases with difference from the only calibration measurement in the testing station (in this calculation assumed to be +20 °C). The detector in the Mu3e experiment is planned to show maximum temperatures of +70 °C. For an expected slope variation of 20 % this would result in a deviation of 8.33 K

The standard deviation of the calibration slopes of chip 327-01-09 and 327-01-04 (see Equation 3.1) is < 1.5 %. This results in a deviation of < 0.15 K per 10 K difference from room temperature. Since both chips are from the same batch, larger variations must be expected for chips from different batches. To get a good estimate of the accuracy of this calibration method, more MuPix11 chips and their deviation in calibrating slopes have to be examined.

σ [%]	1.5	5	10	20	30
+25 °C	0.07 K	0.24 K	0.45 K	0.83 K	1.15 K
+30 °C	0.14 K	0.48 K	0.91 K	1.67 K	2.31 K
+40 °C	0.28 K	0.95 K	1.82 K	3.33 K	4.62 K
+50 °C	0.42 K	1.43 K	2.73 K	5.0 K	6.92 K
+60 °C	0.57 K	1.90 K	3.64 K	6.67 K	9.23 K
+70 °C	0.71 K	2.38 K	4.55 K	8.33 K	11.54 K

Table 3.2: Deviation from the common slope calibration for different slope variations σ from a_0. The room temperature calibration measurement is at +20 °C. Based on the calibrations in Figure 3.17



(a) (b)

(c)

Figure 3.17: Temperature sensor calibration errors when using a common calibration slope a_0. Different calibration slopes were calculated as deviating 10 %, 20 % and 30 % from a_0. A single calibration measurement at +20 °C is chosen representing a test station measurement. a) and b) show the calibration slopes. c) plots the deviation of each slope from the calibration using the common slope a_0

3.4.3 VTemp Implementation in the Mu3e experiment

The VTemp sensors are designed to monitor temperature changes throughout the experiment. This can be done with any of the over 2844 chips that make up the detector. As mentioned above, it is not possible to calibrate each chip individually as it would cost too much time. In the following the measurement conditions in the experimental setup and the QC are introduced. Then, two calibration methods are presented that are similar to the ones in the previous section. Finally, the impact of the temperature effects on the ADC calibration (see section 3.3) are discussed.

In the experiment, the VTemp sensor is only measured via the data stream. Un-

like the diode, the VTemp measurements in the experimental setup are only possible when the chip is providing a data stream. This requires the chip's readout electronics to operate, which generates a lot of heat in the periphery (see section 3.2). Therefore a few steps are necessary to get total temperature from the ADC values in the data stream. Firstly, a ADC calibration (see subsection 3.3.1) has to be performed that converts the ADC values into voltages. This calibration is the same for both temperature calibration methods and need to be done in the quality control. Secondly, a temperature calibration curve is needed to get absolute temperature from the voltages. In the following, measurements for both the ADC calibration and the temperature calibration that have to be performed during QC before detector assembly are described.

The ADC calibration should be performed using the otherwise unused 'ThPix' voltage as described in subsection 3.3.1. It was also shown there that the ADC calibration depends on the setting used. Therefore, two ADC calibrations must be performed: one for the 'low current' settings and one for the settings used in the experiment. The calibration for the 'low current' setting is necessary for the first temperature calibration method described below. With this, it is possible to convert the digital ADC values from the data stream to voltages. The ADC calibration in the settings used for the experiment is used when measuring the VTemp sensors in actual operation of the detector.

Since it is still possible to reach the VTemp circuits analogously in the testing station, VTemp measurement should be conducted via the TestOut bonds. A measurement can be made in 'all-zero' settings, which minimises the effects of self-heating. The absolute ambient temperature corresponds to the VTemp measurement. It is therefore used to determine the offset of the calibration curve. To complete the temperature calibration, the calibration slope is still needed. Both temperature calibration methods described below have different approaches obtaining it.

The first calibration method again determines the tempearture calibration slope of the VTemp sensors of all chips individually. It relies on the ability to control the ambient temperature of the entire detector. The chips of interest are configured to 'low current' settings. The 'low current' setting is introduced in section 3.2 and minimises the power consumption to $\sim 190\,\mathrm{mW}$ per chip. In this setting VTemp1 measures temperatures $< 5\,\mathrm{K}$ above ambient. This setting should be used for the calibration measurements with the experimental setup for two reasons. First, in this setting the ADC calibration is not temperature dependent, as the VDDA level does not change with temperature (see subsection 3.3.2). Therefore, the 'low current' ADC calibration hold for any chip temperature. Secondly, its comparatively low heat dissipation has the least effect on the temperature distribution in the detector. At different detector temperatures (at least three) VTemp measurements are taken. To minimise large heat distributions in the detector, a sequential approach could be considered where only a few chips are powered at a time. The digital values are then converted to voltages with the 'low current' ADC calibration and the temperature calibration slope is determined from a linear fit. This slope is combined with the

offset determining QC measurement in 'all zero' settings as this is the only measurement with negligible self heating. This way, a complete temperature calibration curve for the VTemp sensors of each chip is obtained.

The second calibration method is the same as that proposed for the diode: The test station measurement that determines the offset parameter of the temperature calibration curve is combined with a common calibration slope a_c. To estimate the absolute temperature variation, the same calculation as described in the previous section is performed. The common slope a_0 is the average of all four VTemp sensors, studied in this thesis (two on each chip). Figure 3.17a shows the resulting calibration curves and Equation 3.3 the corresponding errors.

The variation in the calibration curves for the VTemp sensors is much greater than for the diode. The standard deviation of the four sensors is $> 9\,\%$ even though they are from the same batch. This gives a deviation of $< 1\,\mathrm{K}$ per $10\,\mathrm{K}$ difference from room temperature. The size of the standard deviation of the slopes compared to the diode confirms that the VTemp calibration curves are susceptible to process variations as it consists of multiple transistors. As discussed earlier, more chips would need to be calibrated to get a representative estimate of the variation in the calibration slopes.

Even with of these temperature calibrations of the VTemp sensors is finished, the digital readout still presents some challenges. Firstly, the discrepancy between the analogue measurements from the TestOut pad and the digital ADC values obtained from the data stream is not yet fully understood (subsection 3.3.3). Even after taking into account the temperature dependencies of the ADC, the digital measurements differ from the analogue measurements due to a systematic error. The difference is $4\,\mathrm{K}$ to $6\,\mathrm{K}$ for the thin chip 327-01-09 and $0\,\mathrm{K}$ to $4\,\mathrm{K}$ for the thick chip 327-01-04, depending on the ambient temperature.

Secondly, the ADC is still temperature dependent for the settings used in the experiment, as shown in subsection 3.3.2. In subsection 3.3.3 this dependence was accounted for by tracking the VDDA voltage for each measurement and compensating for its changes with temperature. In the experimental setup this is no longer possible. In Figure 3.16 it was shown that the values of the calibration that compensated for the temperature influence ('T-calibrated') deviated $\sim 5\,\mathrm{K}$ to $7\,\mathrm{K}$ per $80\,\mathrm{K}$ which is $\approx 6\,\%$ to $8\,\%$ from the values calibrated without regard to temperature effects ('not T-calibrated').

A possible solution would be to select a fixed DAC value for the 'ThPix' voltage. The DAC will generate the voltage on the chip. This voltage can then be measured by the ADC, as was done to calibrate the ADC in subsection 3.3.1. Since the DAC provides the same 'ThPix' voltage, a change in the ADC values from the data stream would correspond to a temperature effect on the ADC. In this way the temperature effect can be ruled out, although the VDDA voltage is not measured.

This discussion shows that calibrating the temperature sensors on the MuPix11

chips for the Mu3e experiment is possible, but presents some challenges. The accuracy will be determined by the ability to take controlled temperature measurements in the experiment and the process variations of the temperature sensors themselves. Even with scatter in the calibration slopes of 25 %, the error in the returned absolute temperature is < 1.5 K per 10 K difference from room temperature. This is still sufficient to fulfil the purpose of the sensors. Rather than providing accurate absolute temperatures of each chip, they are designed to detect local and global temperature trends to monitor the performance of the cooling system. Their ability to detect temperature changes has been proven by the temperature measurements in section 3.2.

4 Temperature effects on the MuPix11 Performance

In the Mu3e experiment, the MuPix11 sensors will be exposed to a wide range of temperatures between +0 °C to + 70 °C depending on their location inside the detector. Even on-chip temperatures can exceed gradients > 10 K, as it was shown in chapter 3. Hence, a detailed study of the behaviour of the MuPix11 sensor under temperature changes is required. In this chapter its performance – in particular the signal shaping – over a range of −10 °C to +70 °C ambient temperature is presented.

Firstly, the temperature dependence of the current flow at constant operating voltage is discussed. Secondly, the effect of temperature on the signal measurement is investigated. To this end, a qualitative measurement is performed on a representative pixel to study the shape of the analogue amplifier output signal (AmpOut). Finally, the digitised signals of a group of 100 pixels are analysed for their Time-over-Threshold information. For all these measurements, the bandgap reference circuitry is tested. The temperature is recorded using the three integrated temperature sensors described in chapter 3.

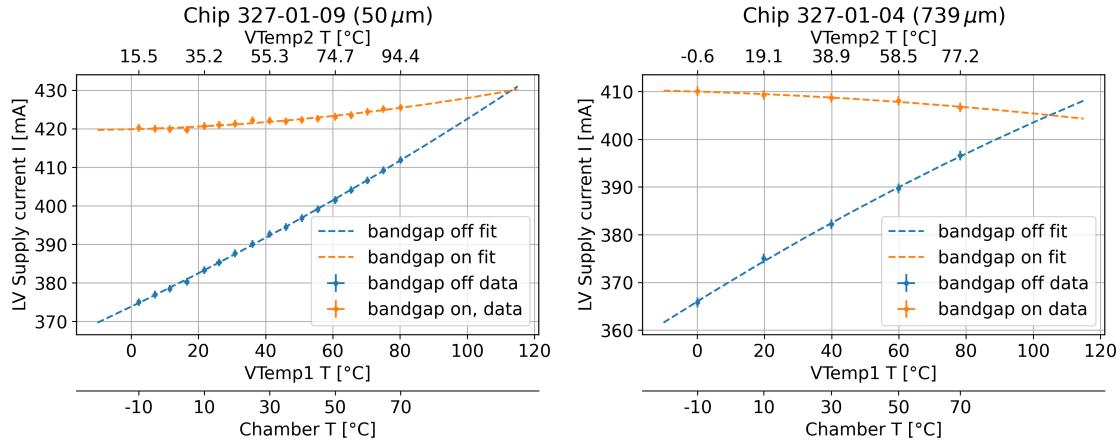
4.1 Temperature Dependence of Currents in the MuPix11

The operating point of a transistor shifts as the temperature changes. This results in a deviation in current flow and corresponding voltage drops. This section gives a qualitative overview of the temperature effect on the low voltage supply current and the threshold voltage of the chip's DACs. The bandgap circuit is tested in all measurements. It provides the current reference that is copied by almost all components on the chip and is designed to compensate for first-order temperature changes in the current as described in subsection 1.4.2.

4.1.1 Low Voltage Supply Current Change

The low voltage for this setup powers the whole chip at 1.9 V. As the supply current and internal currents change with temperature, the bandgap reference is introduced. It's performance is tested by measuring the current at constant supply voltage for ambient temperatures between −10 °C and + 70 °C. The results are shown in Figure 4.1.

With the bandgap disabled at 'default' settings, the current is 375 mA for chip 327-01-09 and 366 mA for chip 327-01-04 at −10 °C chamber temperature. As the ambi-



(a) (b)

Figure 4.1: Low voltage current versus temperature for the 327-01-04 and 327-01-09 chips in 'default' settings with and without the bandgap reference and quadratic fits. The x-axes include chamber temperature and VTemp measurements.

ent temperature increases to +70 °C, the current increases significantly by 38 mA and 31 mA. This is an increase of 9.8 % and 8.4 % respectively. Activating the bandgap significantly reduces this relative increase. At −10 °C the current is 420 mA for chip 327-01-09 (thickness: 50 µm) and 410 mA for chip 327-01-04 (thickness: 739 µm). While the current for chip 327-01-09 still increases slightly from 5.3 mA per 80 K it decreases for chip 327-01-04 from 3.4 mA per 80 K, which corresponds to changes of 0.8 % and 1.3 %. The data is fitted with a quadratic function representing a second order polynomial temperature dependence of the supply current. The linear part is significantly reduced when the bandgap is enabled. These results confirm that the bandgap circuit compensates for first order effects of temperature dependent current changes. The current change between enabling and disabling the bandgap is greatest at low temperatures. At high temperatures the currents approach each other. Extrapolating the curves with the fits, they meet at VTemp1 at temperatures > +100 °C.

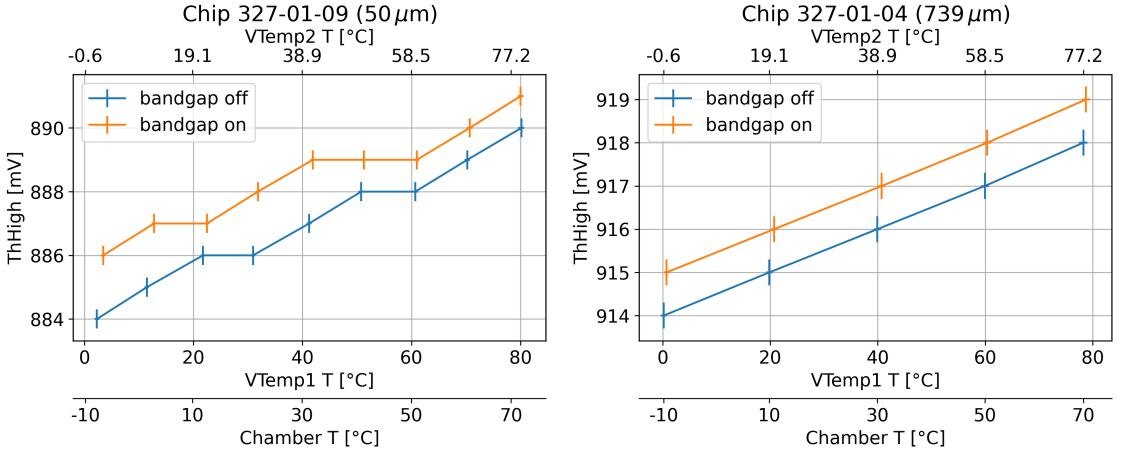
The opposite curvature of the LV current with temperature for both chips is not fully understood yet. It could be due to the different on-chip heat distribution which is much more uniform on the thick than on the thin chip as shown in subsection 3.2.5. However, more chips would need to be examined to validate this hypothesis.

4.1.2 Threshold and Baseline Voltage Change

Several voltage levels are generated on-chip. The two most important for signal processing are the threshold voltage and the digital baseline voltage. The analogue signal from the pixels is driven to the digital cell at the selectable baseline level. The threshold voltage defines the start and end of a hit. It must be greater than the

baseline and is referred to as 'ThHigh'. The resulting difference between the two is the actual threshold, which defines the voltage an incoming signal must exceed to produce a hit signal.

Therefore temperature effects influencing the baseline or the threshold voltages will affect the signal measurements. Both are measured for ambient temperatures of $-10\,^{\circ}\mathrm{C}$ to $+70\,^{\circ}\mathrm{C}$ to study their behaviour. Figure 4.2 shows the ThHigh voltage versus temperature at the lowest stable ThHigh DAC value for each chip. The measurements are taken with the bandgap enabled and disabled.



(a) (b)

Figure 4.2: Analogue measured ThHigh voltage versus temperature at 'default' settings. The ThHigh DAC value is 0x75 for the thin chip 327-01-09 and 0x79 for the thick chop 327-01-04.

A linear increase in voltage from 5 mV to 6 mV per 80 K for chip 327-01-09 and 4 mV per 80 K for chip 327-01-04 can be observed independent of the bandgap. Figure 4.3 displays the voltage difference over the range of $-10\,^{\circ}\mathrm{C}$ to $+70\,^{\circ}\mathrm{C}$ chamber temperature for several ThHigh DAC values. The plot shows that higher ThHigh voltages are less affected by temperature changes. The increase in voltage over the range of

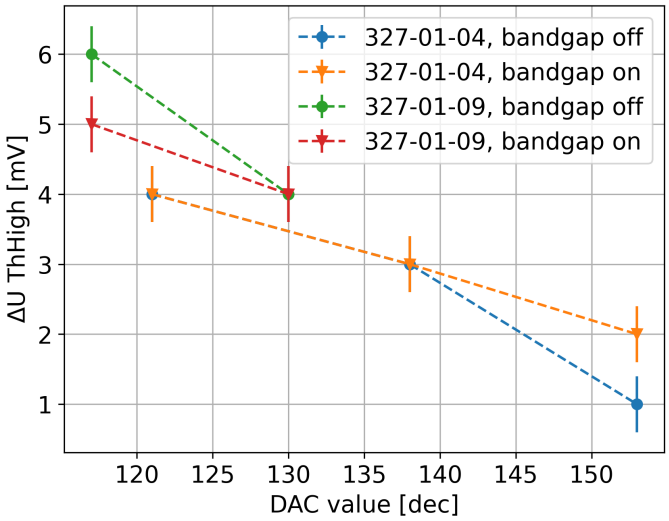
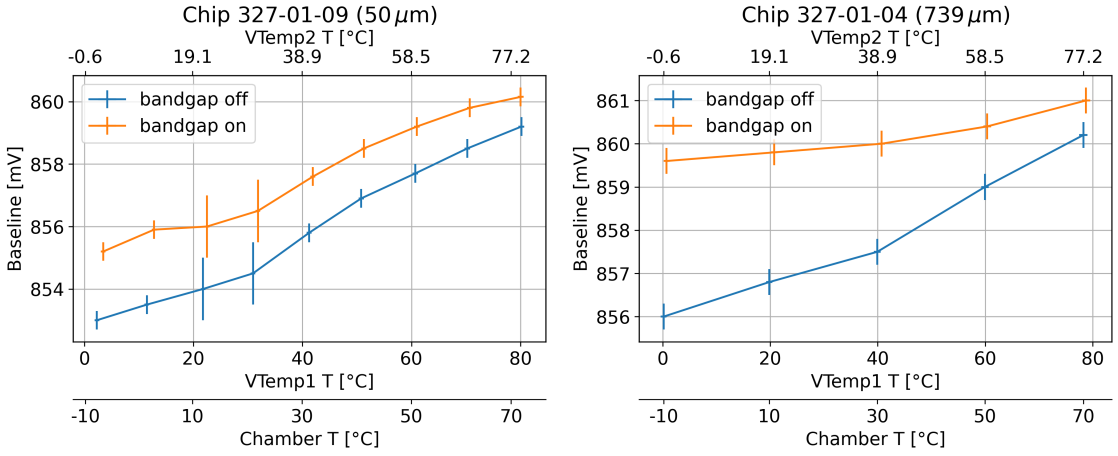


Figure 4.3: Analogue measured change of ThHigh voltage over the range from −10 °C to + 70 °C ambient temperature against different selected DAC values. For chip 327-01-04 three different ThHigh DAC values are selected, for chip 327-01-09 only two.

The baseline voltage is plotted against temperature in Figure 4.4. Over the considered range of 80 K, the baseline of chip 327-01-09 increases linearly by 5 mV to 6 mV. Chip 327-01-04 shows an increase of 4 mV with the bandgap disabled and only 1.5 mV with the bandgap reference enabled.

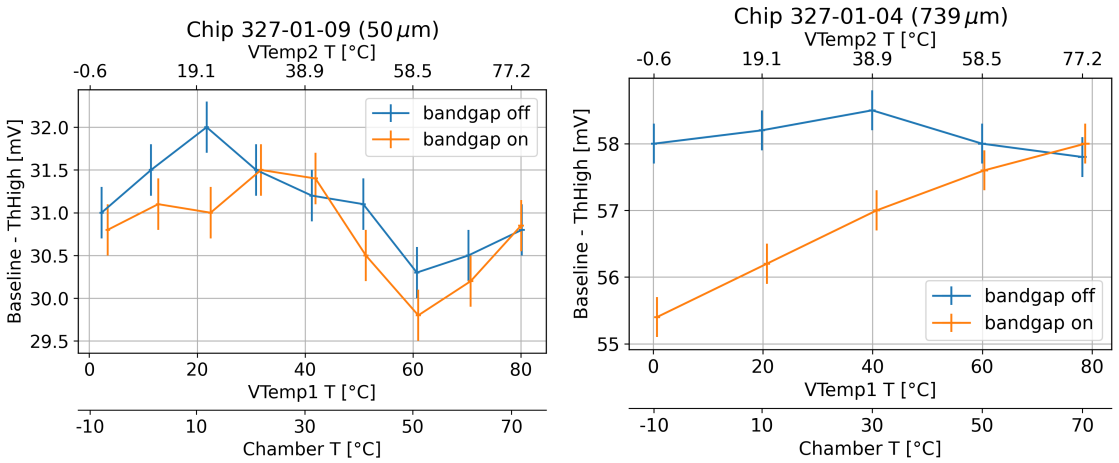


(a) (b)

Figure 4.4: Dgital baseline voltage measured at an ambient temperature of −10 °C to + 70 °C. The baseline DAC value is 0x70.

The resulting actual threshold, which is the voltage level difference between ThHigh and the baseline, is shown in Figure 4.5 for the lowest ThHigh DAC values. The

voltage differences over 80 K are < 3 mV for each measured ThHigh setting. Assuming a binning of 1.9 V/256 bins ≈ 7.4 mV/bin this corresponds to ~ 0.4 bins. This variation is of the order of the precision of the DAC itself, making it insignificant for measurements.



(a) (b)

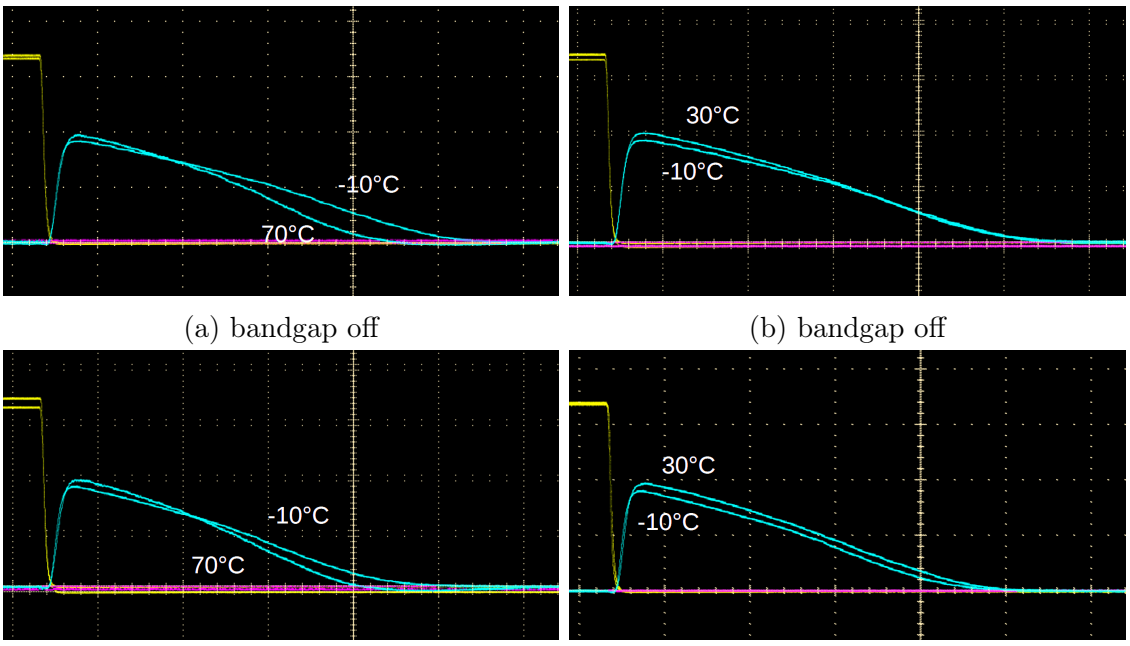
Figure 4.5: Threshold voltage (ThHigh - baseline) versus temperature. The baseline DAC value is 0x70. The ThHigh DAC value is 0x75 for chip 327-01-09 and 0x79 for chip 327-01-04.

As the ThHigh and baseline voltage DACs are voltage dividers the bandgap current reference has no influence on them. This can be seen in Figure 4.2 and Figure 4.4. The bandgap current reference shows no significant effect. This measurement is still performed to verify that the threshold voltage levels for operating the chip with the bandgap enabled and disabled are comparable. This ensures that any observed effects on the Hitbus signal are not due to changes in threshold levels when the bandgap is enabled and disabled. This result is important as the next sections also focus on Hitbus analysis and investigate the effects of the bandgap reference..

4.2 Single Pixel Measurement

The MuPix11 provides information about the amplitude of a detected signal by measuring the Time-over-Threshold for each hit. Its energy resolution therefore depends on the proportionality of the amplitude to the length of the signal. The feedback infrastructure ensures this relationship by producing linearly decreasing signal tails. To do this, it must handle currents of the order of pA.

Temperature changes affect this very sensitive circuit. Therefore, the signal shaping under temperature changes is investigated with an oscilloscope. For both chips 327-01-04 and 327-01-09 one pixel (3,0) is injected with a current corresponding to ~ 6990 e. The AmpOut signal generated on the pixel and the digital Hitbus signal



(a) bandgap off (b) bandgap off

(c) bandgap on (d) bandgap on

Figure 4.6: Chip 327-01-09 (50 µm: Overlapped images of the AmpOut signal for different chamber temperatures with the bandgap turned off and on.

generated by the periphery are analysed. The results for both signals are presented in this chapter.

4.2.1 Temperature Dependent Signal Shaping

The AmpOut and Hitbus signals for both chips are measured with a setting that was optimised for 50 µm thinned MuPix11 chips. It is the 'default_50um' setting in Table B.1. For each chip three ThHigh values are selected: the lowest possible for which the chip produced a stable signal, a very high value that just produced Hitbus signals and one moderate value in the middle. Measurements are taken for chamber temperatures of −10, +30 and +70 °C. The applied bias voltage is −5 V.

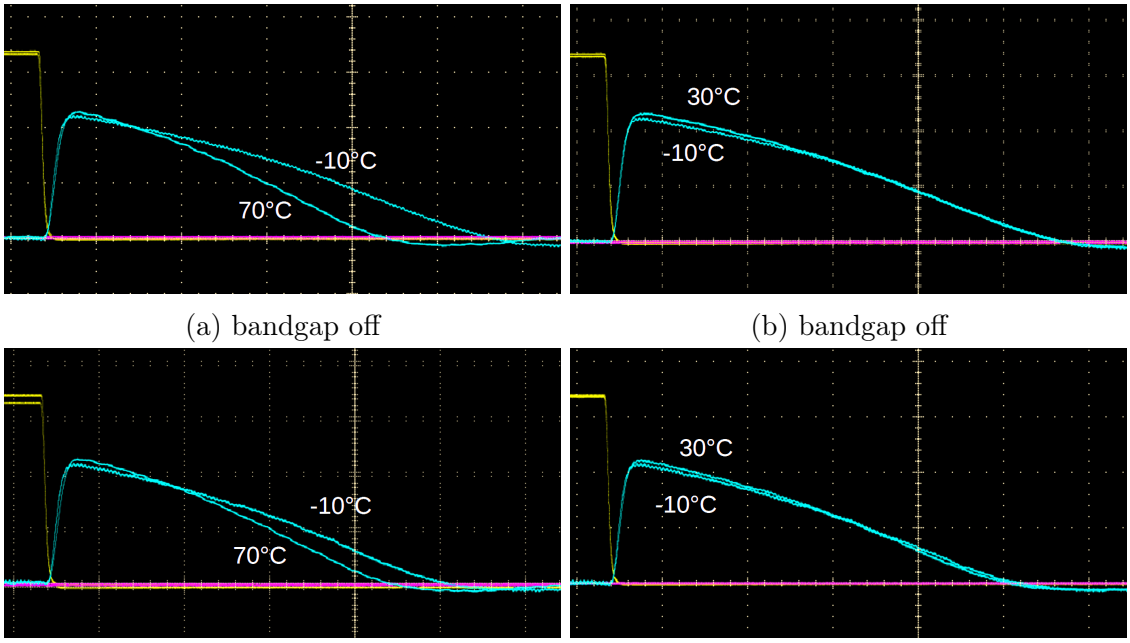
Figure 4.6 and Figure 4.7 show superimposed images of averaged AmpOut signals for different chamber temperatures. The offset is adjusted to align the baselines of the signals for better comparison. Various properties of the signal are measured with the oscilloscope in sample mode. The values are shown in Table 4.1 and Table 4.2.

Very similar observations are made for both chips. The low level is the baseline of the signal recognised by the oscilloscope. It grows linearly with increasing temperature. They show considerable differences of $\sim 30 mV$ per +30 °C. The bandgap reference reduces this effect slightly to ~ 25 mV per +30 °C. Since the amplifier is connected to the comparators in the periphery via a capacitance, this strongly temperature dependent low level change does not affect the Hitbus signal at all.

A small change in the delay between the injection pulse and the AmpOut signal

Bandgap	T [°C]	Delay [ns]	Width [µs]	Amplitude [mV]	Low level [mV]
off	−10	96.6 ± 3.8	3.5 ± 0.2	203.7 ± 3.6	414.7 ± 1.4
	+30	101.9 ± 5.0	3.4 ± 0.1	217.0 ± 4.3	448.3 ± 2.3
	+70	98.5 ± 5.4	2.8 ± 0.3	219.7 ± 6.2	478.7 ± 2.3
on	−10	91.3 ± 4.0	3.0 ± 0.2	200.0 ± 3.9	434.7 ± 1.5
	+30	96.3 ± 4.4	3.0 ± 0.1	215.0 ± 3.6	460.3 ± 0.9
	+70	96.6 ± 5.5	2.7 ± 0.2	222.7 ± 5.6	485.0 ± 2.2

Table 4.1: Characteristics of the AmpOut signals for chip 327-01-09 (50 µm) measured with the oscilloscope.



(a) bandgap off (b) bandgap off

(c) bandgap on (d) bandgap on

Figure 4.7: Chip 327-01-04 (739 µm: Overlapped images of the AmpOut signal for different chamber temperatures with the bandgap turned off and on.

Bandgap	T [°C]	Delay [ns]	Width [µs]	Amplitude [mV]	Low level [mV]
off	−10	74.6 ± 8.2	4.0 ± 0.2	258.0 ± 4.3	499.0 ± 2.7
	+30	82.1 ± 5.7	4.0 ± 0.1	268.3 ± 4.0	533.0 ± 2.3
	+70	86.2 ± 5.5	3.0 ± 0.1	262.7 ± 5.0	566.7 ± 2.5
on	−10	60.4 ± 8.6	3.5 ± 0.1	252.7 ± 4.6	524.7 ± 2.4
	+30	76.0 ± 7.3	3.6 ± 0.1	263.0 ± 5.0	546.3 ± 2.3
	+70	84.7 ± 5.8	3.0 ± 0.1	262.0 ± 5.2	573.0 ± 2.9

Table 4.2: Characteristics of the AmpOut signals for chip 327-01-04 (739 µm) measured with the oscilloscope.

was observed for chip 327-01-04. Higher temperatures caused either a shift of the whole signal or a flattening of the rising edge as the oscilloscope took the measurement at 30 % of the amplitude as reference level. Chip 327-01-09 showed no clear trend. Its uncertainties are in the order of the change over different temperatures. Due to the variations and the very small time scales, the oscilloscope may not be able to resolve the change in delay. With the bandgap enabled, the oscilloscope measured smaller delay times at low temperatures.

With increasing temperature the amplitude increases slightly for 327-01-09, while chip 327-01-04 shows the highest amplitudes for +30 °C. In both cases the difference is greatest between −10 °C and +30 °C. The bandgap does not change this tendency, but slightly reduces the amplitude for −10 °C and +30 °C, while the signal at +70 °C remains mostly unaffected.

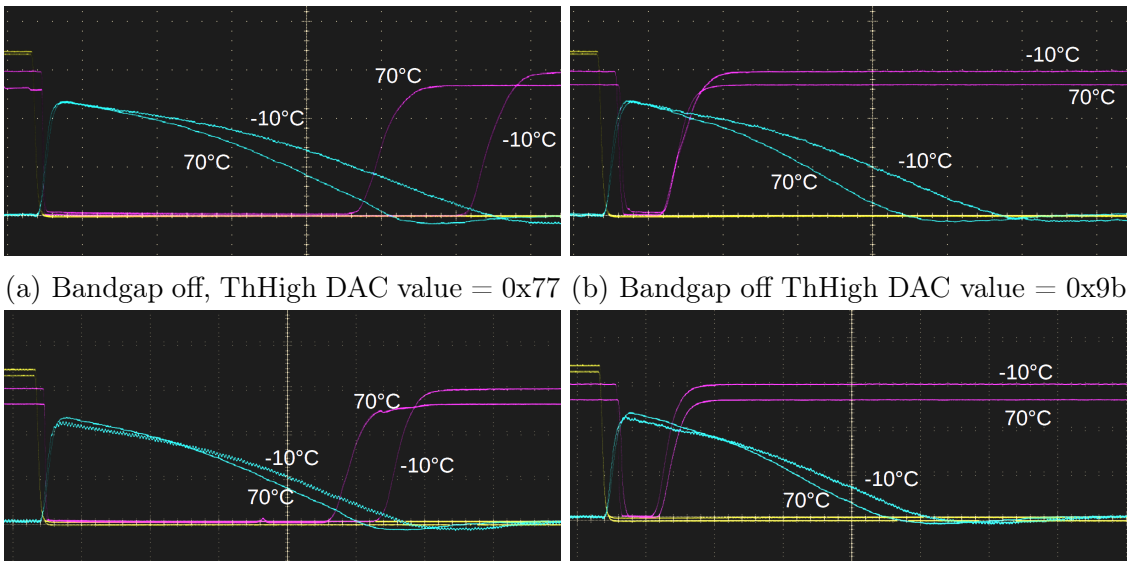
Most importantly, the signal width shows a significant dependence on temperature. The change in slope of the falling edge affects the relationship between signal width and amplitude. The width of the signal at +70 °C chamber temperature differs significantly from the other 2 signals. While it remains almost the same when comparing −10 °C and +30 °C, the +70 °C chamber temperature signals are shortened by 0.7 µs to 1 µs when the bandgap is off. With the bandgap enabled, this difference is reduced to 0.3 µs to 0.5 µs. Here the signals at −10 °C and +30 °C chamber temperature are significantly shortened, while the signal at +70 °C is unaffected.

This shows that temperature does indeed have a significant effect on the signal shape. The bandgap affects the signals at −10 °C and +30 °C chamber temperature much more than those at +70 °C. This can be motivated by considering the supply current measurements in Figure 4.1. The bandgap reference compensates for temperature dependent current changes by providing a current reference that is more stable over temperature. At low temperatures, the low voltage current with and without the bandgap are very different. The bandgap therefore has a significant effect. At higher temperatures, the two currents converge and the effect of the bandgap is reduced.

This behaviour can be transferred to the feedback infrastructure that controls the falling edge. The current flow in the feedback circuit determines the shape of the signal. If its supply current is changed, the feedback current will also change. However, a detailed analysis of the different operating points of individual pixels would be required to capture all the temperature effects on the signal shape. This is beyond the scope of this work, but could be the subject of further research.

4.2.2 Temperature Influence on the Hitbus Signal

The digital Hitbus signal is generated by the comparators which digitise the analogue signal sent by the pixels. Changes in the input signal are reflected in the digital output signal. Its length is determined by the time the signal is greater than the selected threshold voltage. It therefore depends on the width of the AmpOut signal itself and the value of ThHigh as shown in Figure 4.8. The temperature dependence of the Hitbus length can be observed at low thresholds, as the falling edge tail of



(a) Bandgap off, ThHigh DAC value = 0x77 (b) Bandgap off ThHigh DAC value = 0x9b

(c) Bandgap on, ThHigh DAC value = 0x77 (d) Bandgap on ThHigh DAC value = 0x9b

Figure 4.8: Chip 327-01-04 (739 µm): Overlapped images of the AmpOut and the digital Hitbus signal generated by the comparators for different chamber temperatures and thresholds.

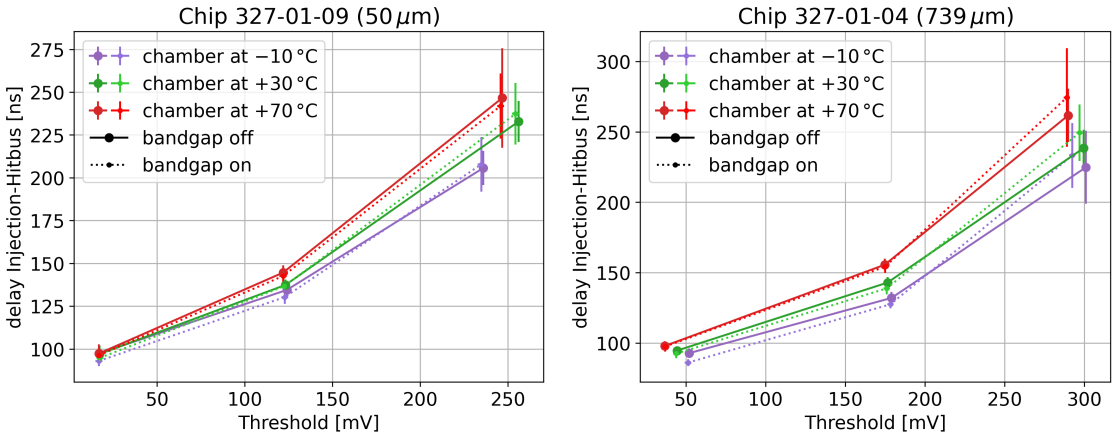
the AmpOut signal changes significantly.

The influence of the bandgap on the signal shaping is also clearly reflected in the Hitbus signal. At the high threshold setting, the temperature related difference in signal width is even reserved: With the bandgap disabled, the Hitbus at

Figure 4.9 shows the delay between the injection pulse and the Hitbus signal for three different ThHigh values. In the oscilloscope measurement, the threshold voltage defines both the beginning and the end of the Hitbus signal. The plot therefore represents the rising edge of the AmpOut signal as the threshold is scanned from low to high. The delay corresponds to the rise time and the threshold corresponds to the height of the signal when it reaches the threshold. Both chips show a temperature dependence, with steeper AmpOut signals at lower temperatures. This is more pronounced for chip 327-01-09, which reproduces the AmpOut measurements from the previous chapter. No bandgap effect is observed.

The width of both the AmpOut and Hitbus signals are plotted in Figure 4.10. As discussed in the previous chapter, the width of the AmpOut signal is significantly smaller at $+70\,^{\circ}$C chamber temperature and the bandgap mainly affects the signals at $-10\,^{\circ}$C and $+30\,^{\circ}$C. The Hitbus signal reproduces this result. Since the temperature-dependent deviation is most pronounced at the tail of the signal, measurements at low thresholds show pronounced changes in the width of the hitbus, as can be seen in Figure 4.8. In this case, the plot represents the falling edge of the AmpOut signal.

The temperature effect on the AmpOut and Hitbus signals are in very good agree-



(a) (b)

Figure 4.9: Delay between injection pulse and the Hitbus signal for pixel (0,3) measured with the oscilloscope. The bandgap is enabled and disabled for three selected thresholds at ambient temperatures of −10 °C, +30 °C and +70 °C.

ment. This suggests that temperature changes mostly affect the signal generation in the pixel cell rather than the digitisation. However, examining one pixel at a time only gives a qualitative picture. To gain insight into representative temperature effects on the sensor, a larger number of pixels must to be examined. This is done in the next chapter.

4.3 Digital ToT Measurement

Previous measurements have given a qualitative insight into the effect of temperature changes on signal shaping for a selected pixel, which lacks statistics to account for pixel-to-pixel variation. In order to overcome this problem, in this chapter, a 10×10 square of pixels in the lower right corner of the matrix is injected and analysed using the Time-over-Threshold information provided by the chip. An injection voltage of 0.7 V is used. The temperature of these 100 pixels is comparable to the temperatures measured by the VTemp1 sensor, as discussed in subsection 3.4.1. For all measurements, the temperature is also tracked with all three on-chip temperature sensors.

4.3.1 ToT Distribution for Multiple Pixels

The same settings as in the previous section are used for the thin and thick chip. A temperature scan with chamber temperatures from −10 °C to + 70 °C is performed with a step size of 10 K for the thin chip 327-01-09 and 20 K for the thick chip 327-01-04. Each pixel detected ~ 40 000 hits on each measurement to ensure sufficient

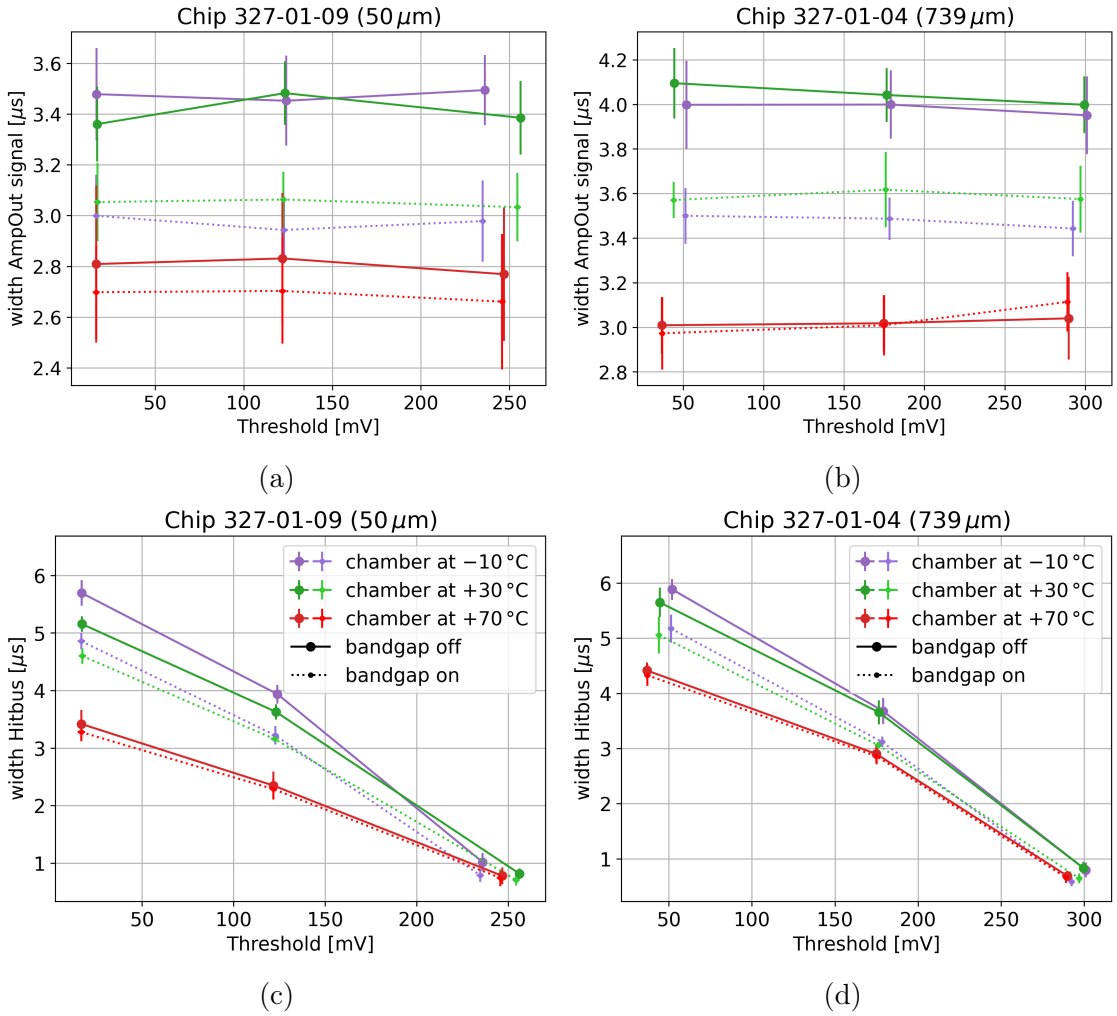


Figure 4.10: Width of the AmpOut signal (a,b) and the Hitbus signal (c,d) for pixel (0,3) measured with the oscilloscope. The bandgap was enabled and disabled for three selected thresholds at ambient temperatures of −10 °C, +30 °C and +70 °C.

statistics. Figure 4.11 shows the obtained ToT distributions for the low threshold settings with the bandgap reference enabled and disabled. The entries are normalised with respect to the total number of hits. One ToT bin corresponds to 512 ns. This is the largest possible bin size, chosen to ensure that there are no cut-offs for very large ToT values. The VTemp1 measurements are used as the temperature reference.

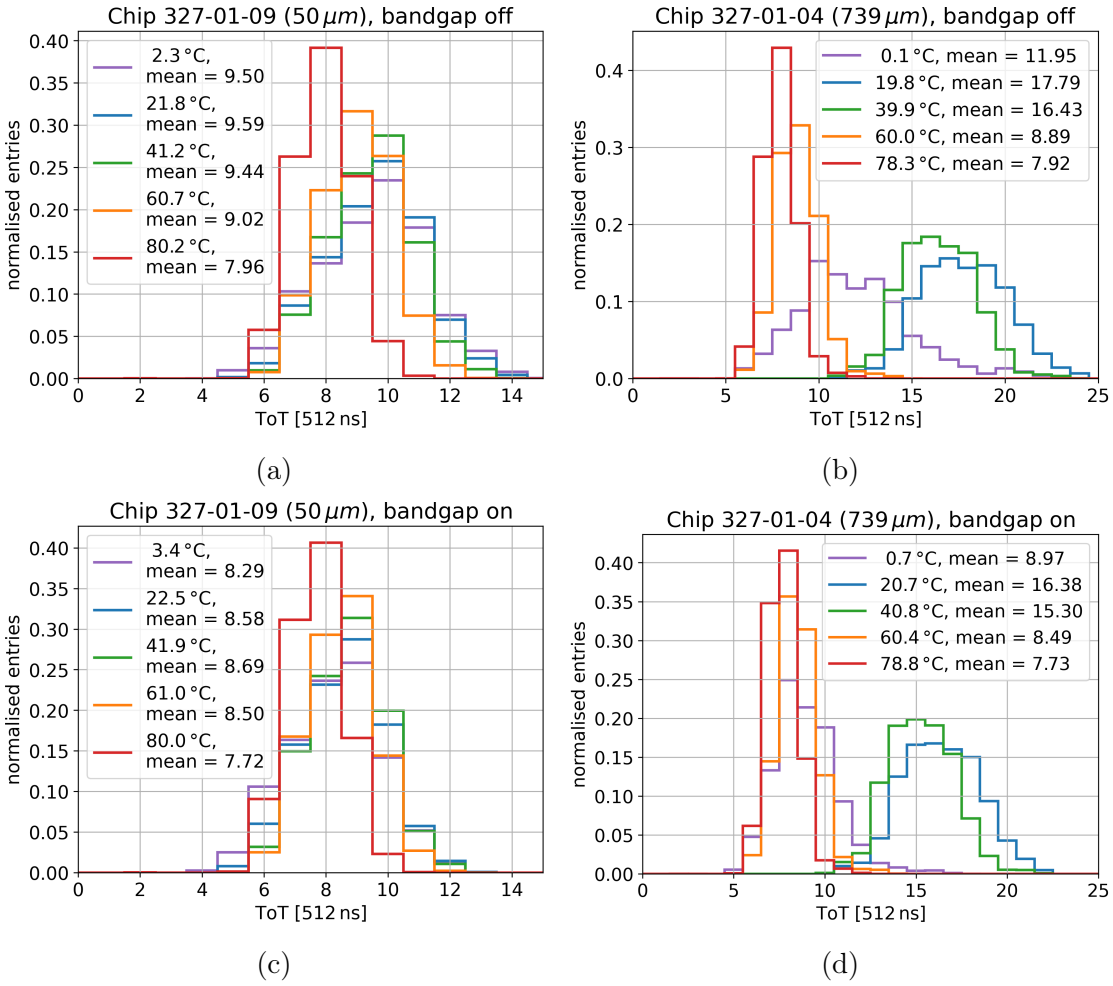


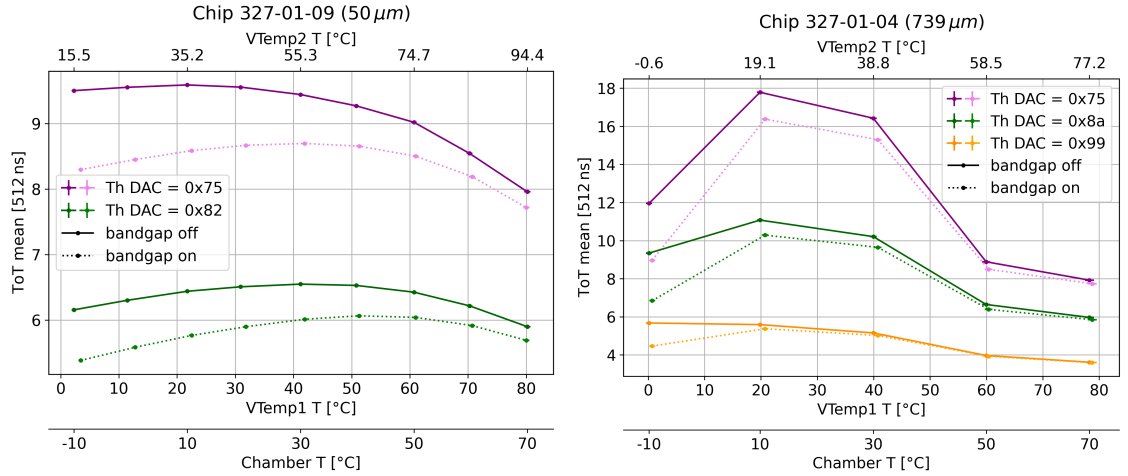
Figure 4.11: Time-over-Threshold distribution for 100 injected pixel at chamber temperatures of (−10, +10, +30, +50 and +70)°C. The low threshold DAC values (ThHigh) are 0x75 for chip 327-01-09 and 0x79 for chip 327-01-04. The histograms are normalised with respect to the number of entries.

In Figure 4.12 the ToT means of measurements at different temperatures are plotted. A peak can be observed for both chips, which varies with threshold and bandgap setting. In particular, no monotonically decreasing behaviour is observed as it is suggested in the previous section. Chip 327-01-04 has a significant peak at VTemp1 temperatures of ~ +20 °C of almost 18 bins. At 0 °C the ToT mean is 18 bins and at +80 °C it is 8 bins. At higher thresholds the ToT mean obviously

decreases. The peak also flattens at higher thresholds. Activating the band gap lowers the overall ToT mean for all temperatures. It has a greater effect on the ToT mean at lower temperatures than at higher temperatures, as observed with the single pixel measurements, with the greatest effect at 0 °C VTemp1.

The ToT means of chip 327-01-09 follow a much smoother quadratic curve. In contrast to the thick chip, the mean maximum is shifted to considerably higher values for higher thresholds or when enabling the bandgap. The maximum of the ToT means for low threshold settings (ThHigh DAC = 0x75) is at +20 °C VTemp1 temperature at 9.7 bins. Enabling the bandgap lowers the ToT mean by > 1 bin for VTemp1 temperatures.

This shift in the ToT maximum corresponds to the temperature dependent slope of the falling edge of the signal. At different temperatures the signal tails will cross at some point as shown in Figure 4.6. If the threshold is set higher than this crossing point, the digital signal at lower temperature may be the shorter one with less amplitude. For thresholds below this coursing point, it will now be longer than the signal at higher temperatures. The influence of the bandgap on the maximum of the curve shows that it shifts the crossing point to lower values, which agrees with the observations in the pictures in Figure 4.6.



(a) (b)

Figure 4.12: Mean values of ToT distributions for 100 injected pixel at chamber temperatures ranging from −10 °C to + 70 °C. Different threshold settings are shown for an enabled and disabled bandgap.

In section 4.2 it was concluded that the temperature dependence of ToT values is mainly due to the shaping of the analogue signal in the pixel itself. The amplifier and feedback system consists of a complex integrated circuit of multiple transistors. The falling edge of the signal is mainly determined by the feedback current that resets the accumulated charge. Its supply current reference is generated in the periphery.

As shown in subsection 4.1.1, the chip current consumption is strongly temperature dependent if the on-chip current reference is not generated by the bandgap circuit. Therefore, at higher temperatures, the on-chip currents are increased. More current in the feedback circuit will reset the accumulated charges faster and shorten the tail of the signal. This effect results in lower ToT values at higher temperatures.

The bandgap reference compensates for first order current changes as discussed in subsection 4.1.1. A small quadratic temperature dependence of inverted sign remains for both chips: Over the considered range of 80 °C, the LV current of the thin chip still increases by 0.8 %, while the current of the thick chip decreases by 1.3 %. Changes in the signal shaping due to the supply current would therefore show opposite behaviour for the two chips. This is not the case, the ToT mean versus temperature curves for both chips in Figure 4.12 are not inverted. Therefore, the remaining characteristics must be due to temperature dependencies of the amplifier and feedback infrastructure itself.

Overall, the trends and scales of the single pixel measurements in section 4.2 agree very well with the results shown in this section. However, the large decrease of the ToT mean for chamber temperatures of −10 °C compared to +30 °C for chip 327-01-04 is not observed in the single pixel measurement in Figure 4.10. However, the large jump from +30 °C to +70 °C chamber temperature suggested by the single pixel measurement (see Figure 4.10) turns out to be a smooth transition when considering more temperature steps.

The selection of the pixel may play a role in these discrepancies. The single pixel measurements are performed with a pixel in the lower left corner of the chip. This is closer to the hot state machine than the square in the matrix used in this chapter, which is at the bottom right corner. As discussed in section 3.2, this results in a temperature difference, assumable of the order of 10 K, between these two areas. This would shift the single pixel measurement to hotter temperatures in Figure 4.12a and could explain why no increase in ToT is visible at low temperatures. Considering the even heat distribution of the thick chip 327-01-04 (see subsection 3.2.5), comparable temperatures can be assumed for both areas.

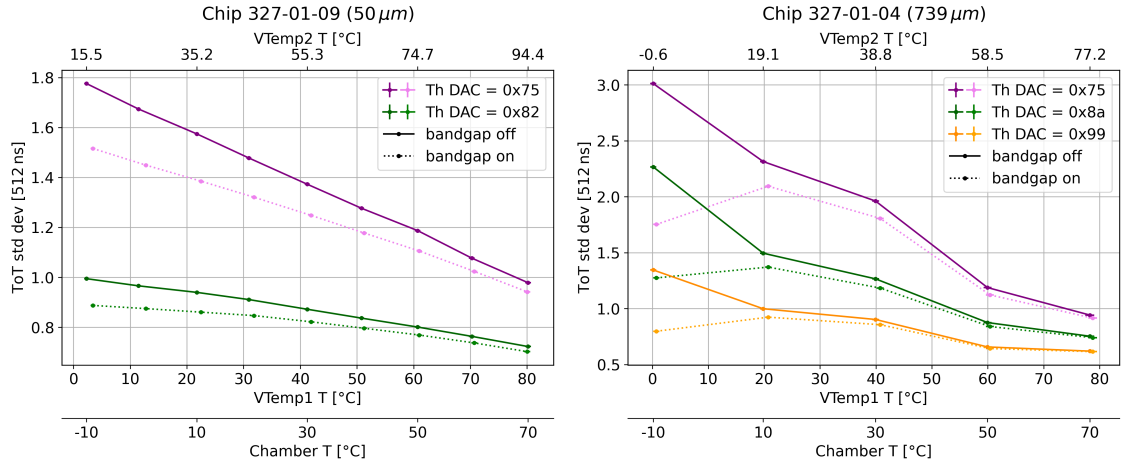
As mentioned above, the single pixel measurements lack statistics and are not intended to give a complete picture. It is most likely that pixel-to-pixel variations cause the small discrepancies between both single and multi-pixel measurements. The extent and temperature dependence of such variations is discussed in the next chapter.

4.3.2 Temperature Effect on the Deviation of the ToT Spectrum

The plots in Figure 4.11 shows not only a shift in the mean of the ToT spectra for different ambient temperatures but also a change of their spread. The spectra at −10 °C chamber temperature show a much larger deviations than the +70 °C meas-

urements. The standard deviation of all distributions is plotted against temperature in Figure 4.13.

It decreases linearly with increasing temperature, indicating less deviation at higher temperatures. Chip 327-01-04 shows a significant standard deviation of $\sim 3\,\text{bins} \triangleq 3 \times 512\,\text{ns} = 1536\,\text{ns}$ for $-10\,^{\circ}\text{C}$ chamber temperature which falls below 512 ns over a range of 80 K heating for the lowest threshold. Higher thresholds produce less steep curves but show the same tendencies. The bandgap has the greatest effect at low temperatures, flattening the curves slightly. As before, chip 327-01-09 shows much smoother linear curves. The low threshold just reaches $3\,\text{bins} \triangleq 921.6\,\text{ns}$ for $-10\,^{\circ}\text{C}$ chamber temperature and drops to below 512 ns in the 80 K range. For the second threshold the change over 80 K is reduced to $< 0.4\,\text{bins} \triangleq 204.8\,\text{ns}$. Again, the bandgap flattens the curves, affecting the lower temperatures more than the higher ones.



(a) (b)

Figure 4.13: Standard variation of ToT distributions for 100 injected pixels at chamber temperatures of $-10\,^{\circ}\text{C}$ to $+70\,^{\circ}\text{C}$. Different threshold settings are shown for an enabled and disabled bandgap.

Deviation in the ToT distribution comes from both pixel-to-pixel variation and variation in ToT within individual pixels. To investigate the extent of both, the mean and standard deviation are calculated separately for each of the 100 injected pixels. The resulting histograms are shown in Figure 4.14b and Figure 4.12a for the means and in Figure 4.15a, Figure 4.15b for the standard deviations. Each entry represents the ToT mean and standard deviation of one of the injected pixels.

The standard deviation of the pixel ToT mean histogram in Figure 4.14b and Figure 4.14a is a measure of the ToT pixel-to-pixel variation. A spread would indicate that the average ToT size varies greatly from pixel to pixel. The standard deviation was calculated for each histogram and the results are plotted against temperature in Figure 4.14c and Figure 4.14d.

The mean of the pixel ToT standard deviation distribution in is a measure of the variation of ToT within a single pixel. A large standard deviation mean indicates a large spread in the ToT distribution of the pixel in question. The mean is also calculated for each histogram and the results are shown in Figure 4.15c and Figure 4.15d. Comparing these two distributions with the combined ToT distribution dispersion gives an indication of whether the pixel-to-pixel variation or the single pixel variation dominates the overall distribution.

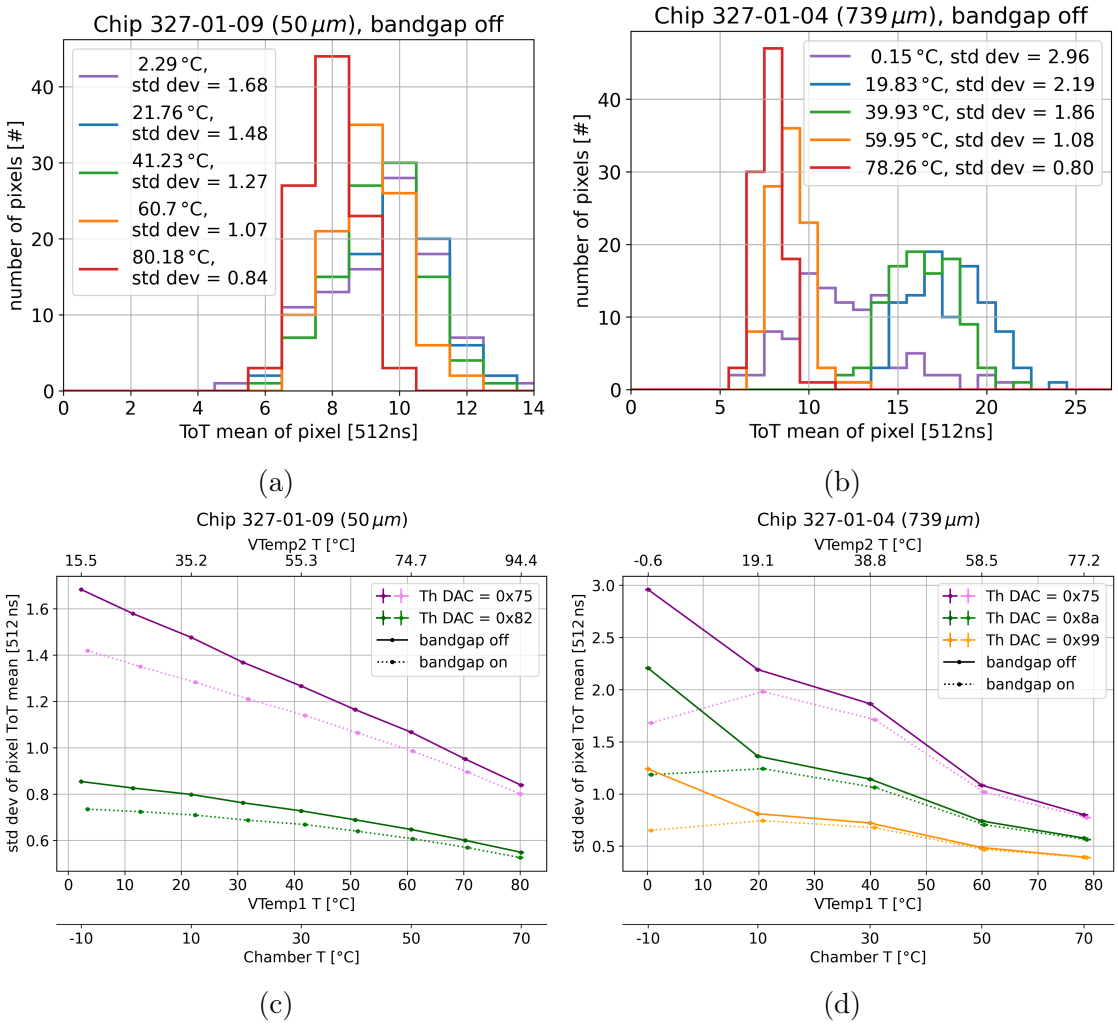


Figure 4.14: a) and b) show the mean ToT values for each of the 100 injected pixels at chamber temperatures of $(-10, +10, +30, +50$ and $+70)^{\circ}$C. The low threshold DAC values are 0x75 for chip 327-01-09 and 0x79 for chip 327-01-04. The histograms are normalised with respect to the entries. In c) and d) the standard deviation of the mean pixel ToT values is plotted against temperature.

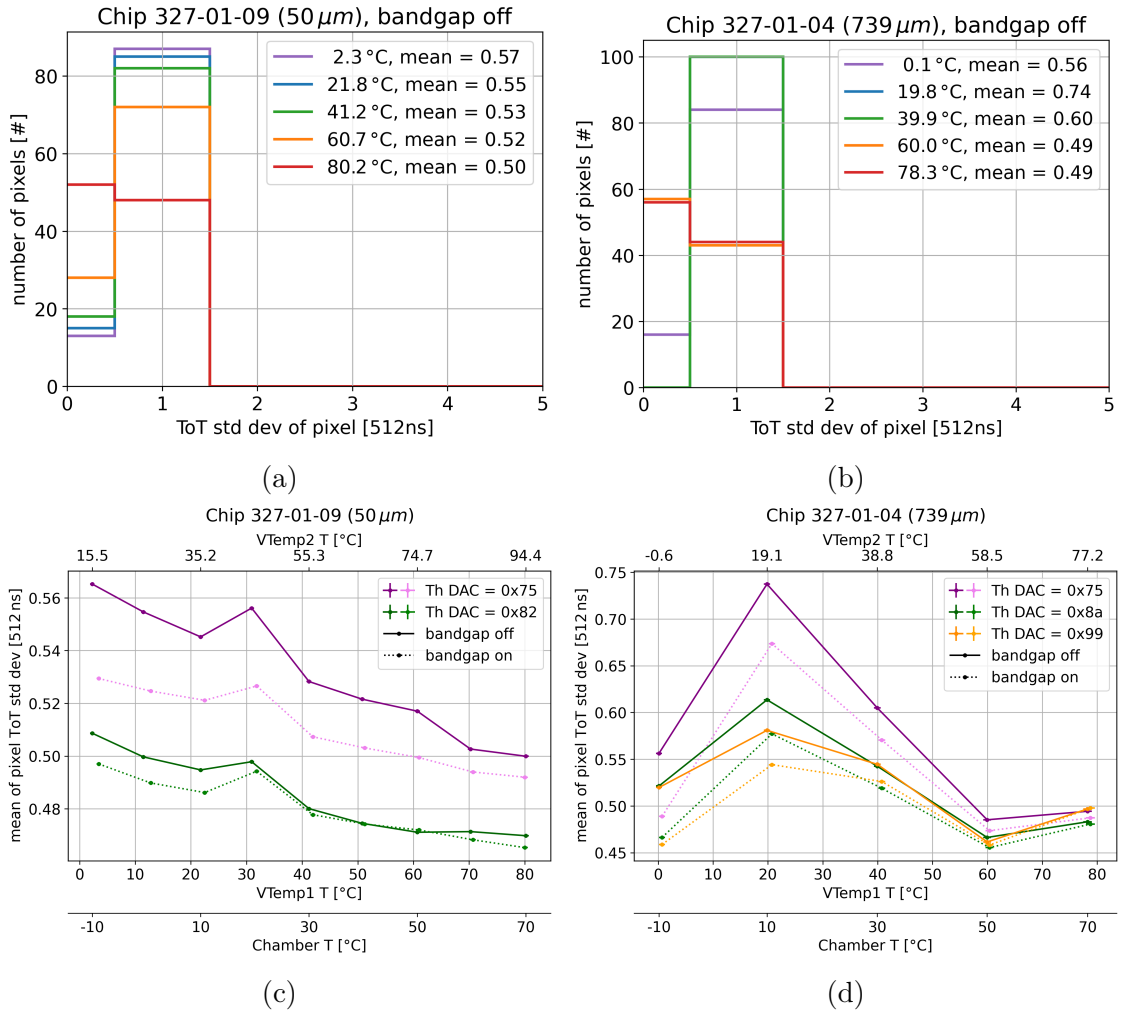


Figure 4.15

Figure 4.16: Standard deviation of the ToT mean distribution for each of the 100 injected pixels at chamber temperatures of (−10, +10, +30, +50 and +70)°C. The low threshold DAC values are 0x75 for chip 327-01-09 and 0x79 for chip 327-01-04. The histograms are normalised with respect to the entries. In c) and d) the mean of the pixel ToT standard deviation distribution are plotted against temperature.

The standard deviation of the pixel ToT means over temperature in Figure 4.14c and Figure 4.14d mirrors the standard deviation of the combined ToT values in Figure 4.13. The linear decrease of the values with temperature and the influence of enabling the bandgap are reproduced for both chips. The curves are slightly shifted to lower values of ~ 0.1 bins to 0.2 bins ≙ 50 ns to 100 ns compared to the standard deviation of the combined ToT values. Therefore, the magnitudes agree very well.

This shows that a pixel-to-pixel variation is primarily responsible for the temperature dependence of the dispersion of the total ToT distribution. The pixel-to-

pixel variation is large at low temperatures and decreases with increasing temperature. The magnitude of the temperature dependence is correlated with the selected threshold, as it increases significantly at low thresholds.

This indicates that the feedback system in the pixel has difficulty in making the last part of the falling edge linear where very small currents are handled. In this regime, even small operating point differences between pixels due to process variations of the transistors result in large ToT spreads.

Changing the temperature will also change the operating point. As discussed above, higher temperatures show smaller ToT values and steeper falling edges of the signal. The charge reset of the feedback system is faster as the same amount of current flows in less time. The feedback current and signal drop faster, making the falling edge less susceptible to variation.

The results show that at lower temperatures the working points of several pixels are spread out, resulting in a standard deviation of ~ 1.7 bins $\triangleq 820$ ns with respect to chip 327-01-09 at $0\,^{\circ}$C ambient temperature and low thresholds. At the same time, the temperature dependence of ToT is smallest at ambient temperatures of $+0\,^{\circ}$C to $+30\,^{\circ}$C (see Figure 4.12). Considering the whole chip and not only the 10×10 square used for the measurements, a temperature gradient of > 10 K in the pixel matrix must be assumed, as shown in section 3.2. If the matrix temperature varies in a range from $+0\,^{\circ}$C to $+30\,^{\circ}$C due to its temperature gradient, they will perceive the smallest possible ToT variations caused by on-chip temperature gradients of < 0.2 bin $\triangleq 100$ ns as observed with chip 327-01-09.

The temperature gradient on the chip has a greater effect on the pixel ToT distribution of 1 bin when operated at higher ambient temperatures of $+50\,^{\circ}$C to $+70\,^{\circ}$C $\triangleq$ 512 ns. At the same time, the working points of the pixels are pushed closer together. The deviation of the ToT distribution observed in Figure 4.13 is reduced to 1.2 bins to 1.0 bins $\triangleq$ 614 ns to 512 ns.

This discussion for the thin chip 327-01-09 at low thresholds shows that each temperature range in which the chip is operated brings its own temperature related variations in ToT. At low ambient temperatures of $+0\,^{\circ}$C to $+30\,^{\circ}$C the temperature related pixel-to-pixel spread dominates. At temperatures of $+50\,^{\circ}$C to $+70\,^{\circ}$C this effect diminishes while the temperature gradient on the chip affects the pixel ToT values based on their temperature. Within this study, no optimal operating temperature can be determined

Tuning is a promising tool that accounts for pixel-to-pixel process variations by slightly varying the threshold levels for individual pixels. This could also be used to compensate for temperature-related pixel variations. However, it is necessary that the chips have the same temperature and heat distribution when operating as they had when they were tuned. Therefore, tuning must be done in the same setup as the chips will ultimately be operated.

5 Discussion

5.1 Summary & Conclusion

For the Mu3e experiment, monitoring the temperature distribution within the tracking detector is essential to prevent damages from overheating. Furthermore, the understanding of temperature effect on the detector performance is crucial to reach the sensitivity goal of a SES of 2×10^{15}.

Within the scope of this thesis, the temperature sensors of the Mupix11 are successfully calibrated using a climate chamber. This enables on-chip temperature measurements to be performed, providing valuable insight into the temperature distribution across the chip. The 50 µm thinned sensors show large temperature gradients of 11 K to 13 K over thermally connected parts of the periphery alone.

It is examined how the integrated temperature diode and the two VTemp sensors reflected the temperature distribution on the chip. The VTemp1 circuit is found to represent the temperature of the majority of pixels in a central area of the matrix, while VTemp2 provides the temperature of the hottest pixels near the state machine. Both sensors show similar thermal link as the pixel electronics within the matrix. The temperature diode is identified as a thermally isolated component providing temperature measurements of the substrate in the hottest region of the periphery near the state machine.

Furthermore, digital VTemp sensor measurements via the data stream are successfully conducted for the first time in MuPix11, with a bin size from p_{min} = 2.649 K to p_{max} = 3.373 K. The bin size depends on the temperature calibration curve of each VTemp circuit and the calibration of the analogue-to-digital converter on each chip. The calibration of the analogue-to-digital converter yielded satisfactory results, with a residuals of less than 1 bin for a linear fit. The digital readout allows for measurement of temperature changes and trends. However, temperature effects are observed as the ADC supply voltage (VDDA) exhibited temperature dependent voltage drops during chip operation. In addition, for one of the two chips considered, the digital measurements via the data stream consistently deviated from the analogue measurements to lower temperatures by more than 5 K, indicating a not understood for systematic error.

Taking into account the conditions in the Mu3e experiment and quality control measurements during the testing phase of the chips, two possible methods for calibrating the temperature sensors in the detectors have been proposed. Both methods involve temperature measurements at the testing station under verifiable ambient temperature (room temperature) to obtain a linear calibration curve. The first method requires temperature control of the entire tracking detector after all chips

have been mounted. By taking temperature measurements at different ambient temperatures, a the slope of the calibration curve can be determined. Combining this with the room temperature measurement from the testing station allows individual absolute temperature calibration with a linear calibration curve for each chip.

The second method uses a common slope (one for the diodes and one for all VTemp sensors) for the temperature calibration for all chips in the detector. The offset is determined by the measurements from the QC testing station. The accuracy of temperature measurements using this calibration method is discussed, considering variations in the calibration slope caused by process variation. In Mu3e chip temperatures are assumed reach +70 °C at maximum. If the calibrating curve of a temperature sensor showed a deviation of 20 % (or 30 %) from the common calibration slope, this would result in an error of 8.33 K or (11.54 K) in its temperature measurements respectively.

In chapter 4 of the study, the performance of the MuPix11 under temperature influences and the functionality of the bandgap is investigated. The linear part of the temperature dependence of the low voltage is successfully compensated using the bandgap. The > 8 % increase in LV current from −10 °C to + 70 °C ambient temperature is reduced to a deviation of < 1.4 %. The influence on the baseline and threshold is found to be insignificant, as their deviations from −10 °C to + 70 °C are within the range of the binary bin error of the DAC.

Furthermore, the impact of temperature on signal shaping is examined for a single pixel. It is observed that higher temperatures led to shorter signals due to increased feedback current from the pixel. The Hitbus signal is shown to correspond to the shaping of the amplifier signal. Therefore, the temperature dependence is found to be mainly rooted in the pixel feedback circuits.

Finally, temperature effects on the Time-over-Threshold of a group of 100 pixels is investigated. The mean of the ToT show a quadratic dependency of the temperature with a maximum at +20 °C pixel temperature for a 50 µm thinned chip at low threshold settings (ThHigh DAC = 0x75). For pixel temperatures of 80 °C, the ToT mean falls to < 82 % of the maximum value. Enabling the bandgap reduces this to > 89 %. The temperature at which the ToT mean has its maximum varies with the threshold value and from chip to chip. For low threshold values the ToT maximum remains within the range of approximately +10 °C to + 30 °C ambient temperature for both regarded MuPix11 sensors.

The standard deviation of ToT distribution shows a linear temperature dependence with steeper slopes at low thresholds (ThHigh DAC = 0x75). ToT spectra at pixel temperatures of 80 °C have < 60 % the standard deviation of ToT spectra at 0 °C. This effect can be attributed to pixel to pixel variations, whereas variations within a single pixel have a smaller impact.

5.2 Outlook

In order to apply the proposed temperature sensor calibration presented in this thesis to the Mu3e experiment, several aspects have to be evaluated. Firstly, the conditions regarding ambient temperature regulation in the experimental setup is required to be discussed as they play a crucial role in enabling individual temperature calibration for each chip. Additionally, an investigation on chip to chip variations of the temperature calibration curves in the laboratory is necessary. This increases the accuracy and allows to estimate the uncertainties of the calibration when using a common temperature calibration slope for all chip.

The studies on temperature distribution throughout the chips in the laboratory are limited to single chip setups with PCBs. Therefore, a comprehensive investigation of temperature distribution on multi-chip ladders, as used in the Mu3e experiment, is still pending.

The potential of the VTemp sensor measurements have been demonstrated in this thesis. However, the digital readout via the data stream still presents a challenge. Firstly, a temperature dependence of the ADC is observed that has impact on the accuracy of the VTemp measurements. The proposed approach of compensating for this by logging the 'ThPix' voltage needs to be evaluated. Secondly, the systematic discrepancy between the digital and the analogue VTemp measurements requires further investigation, as it is not yet fully understood.

Regarding the temperature effect on the performance of the MuPix11, the qualitative research of this work needs to be quantified. In this thesis, the pixel-to-pixel variations of the Time-over-Threshold measurements due to ambient temperature change are studied for a group of 100 pixels. However, it is shown that temperature gradients on the chip are unavoidable. Consequently, further investigation on pixel-to-pixel variations due to temperature gradients between pixels on the chip are required. Therefore, pixels close to the state machine hot spot in the periphery can be grouped and compared to pixel groups in colder areas.

Furthermore, it is important to note that only one setting is used to investigate the temperature dependence of the ToT measurements. Therefore, it is necessary to evaluate the resilience to temperature effects of different configuration settings and consider the results in the search of the optimal settings in the Mu3e experiment.

By addressing these research areas, a more comprehensive understanding of temperature effects on the performance of the MuPix11 in the tracking detector can be achieved. This knowledge will contribute to the optimisation and successful implementation of the MuPix11 in the Mu3e experiment.

A Additional Plots

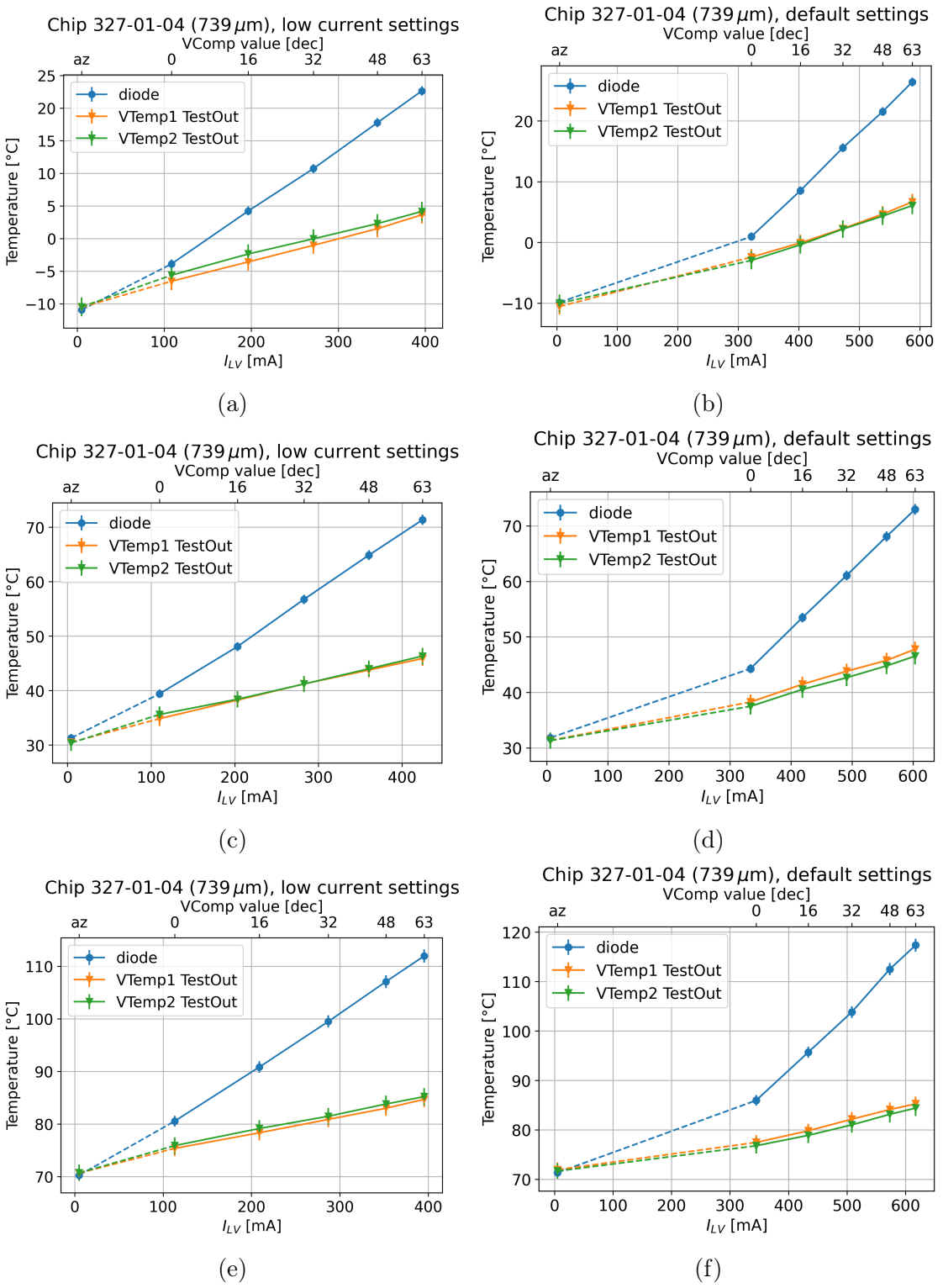


Figure A.1: Chip 327-01-04 (739 µm: Comparator scan (VComp2) temperature measurements. The diode and VTemp measurements are plotted against the low voltage supply current at −10 °C, 30 °C and 70 °C.

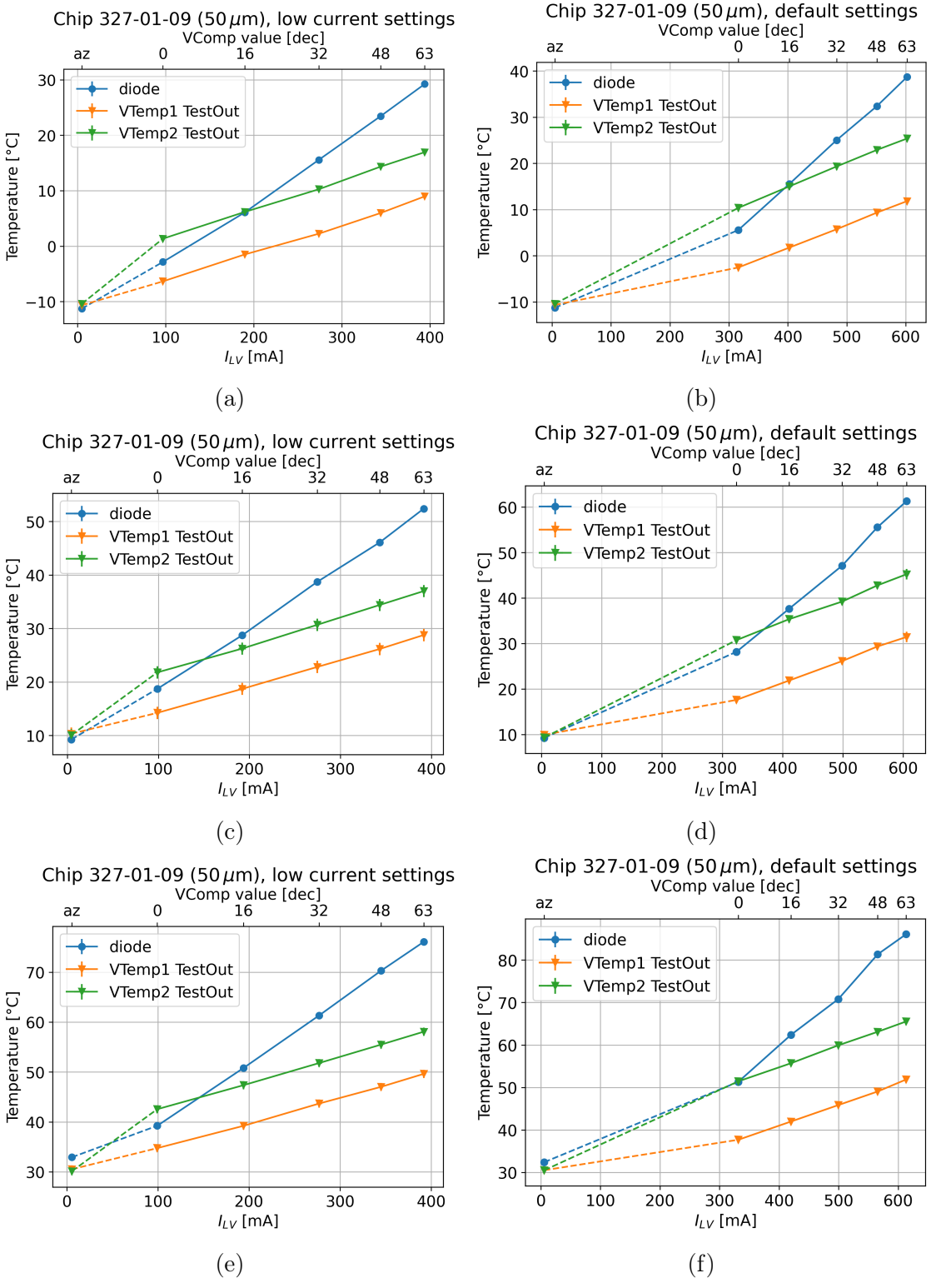


Figure A.2: Chip 327-01-09 (50 µm: Comparator scan (VComp2) temperature measurements. The diode and VTemp measurements are plotted against the low voltage supply current at −10 °C, 10 °C and 30 °C.

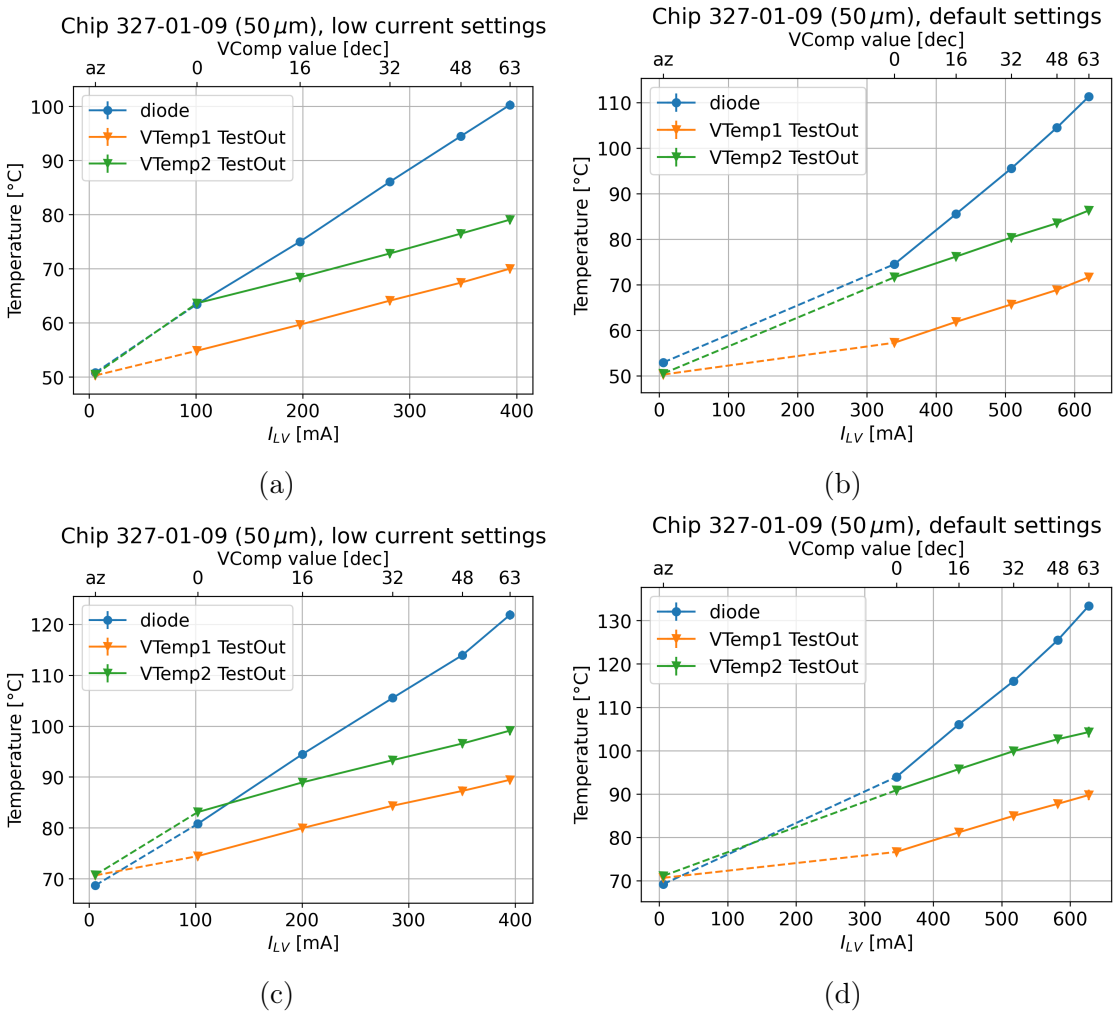


Figure A.3: Chip 327-01-09 (50 µm: Comparator scan (VComp2) temperature measurements. The diode and VTemp measurements are plotted against the low voltage supply current at 50 °C and 70 °C.

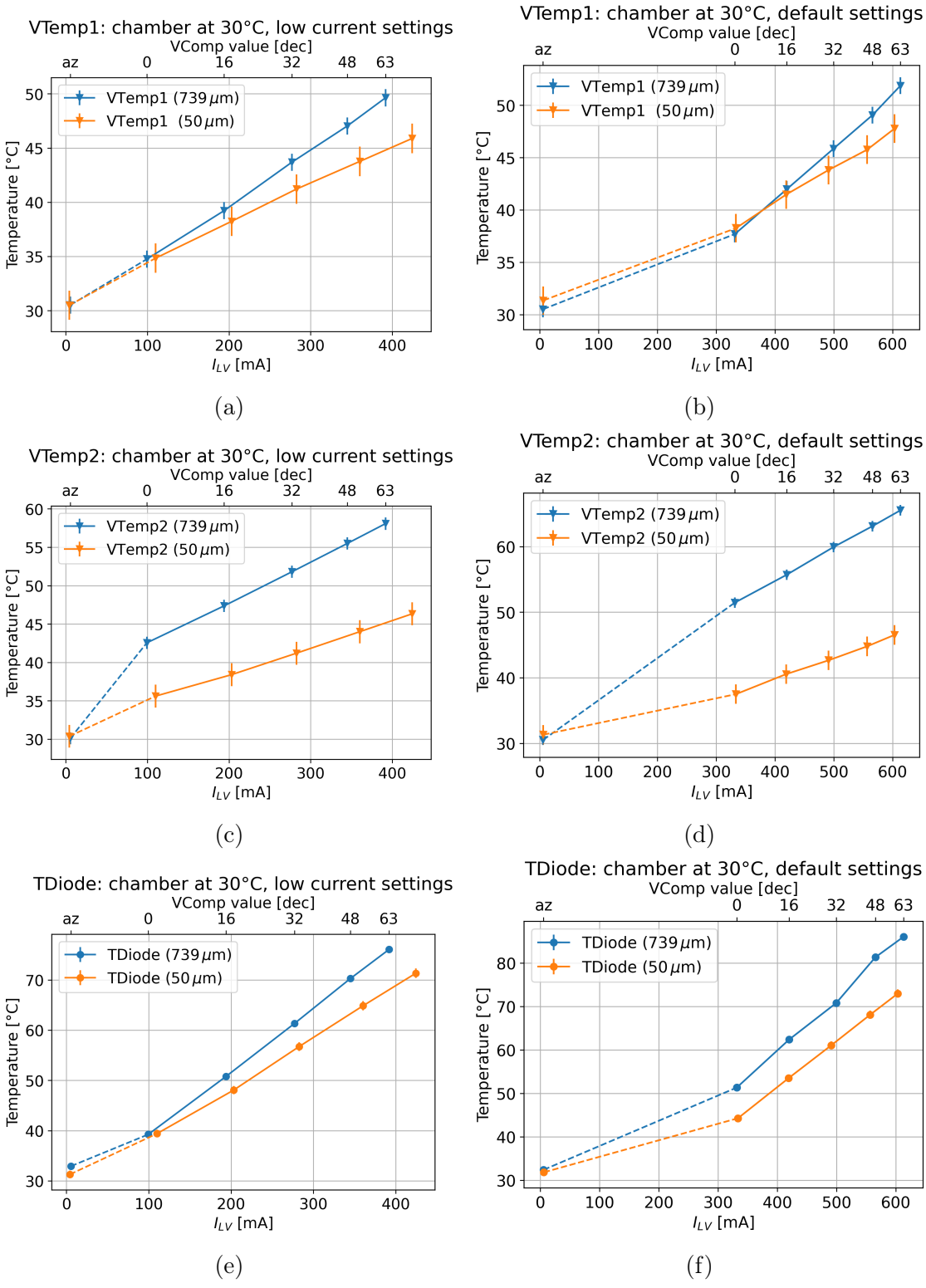


Figure A.4: Comparison of temperature measurements between the 327-01-04 (739 µm) and the 327-01-09 (50 µm) chip at +30 °C chamber temperature. For each temperature sensor a low current and a default measurement is compared.

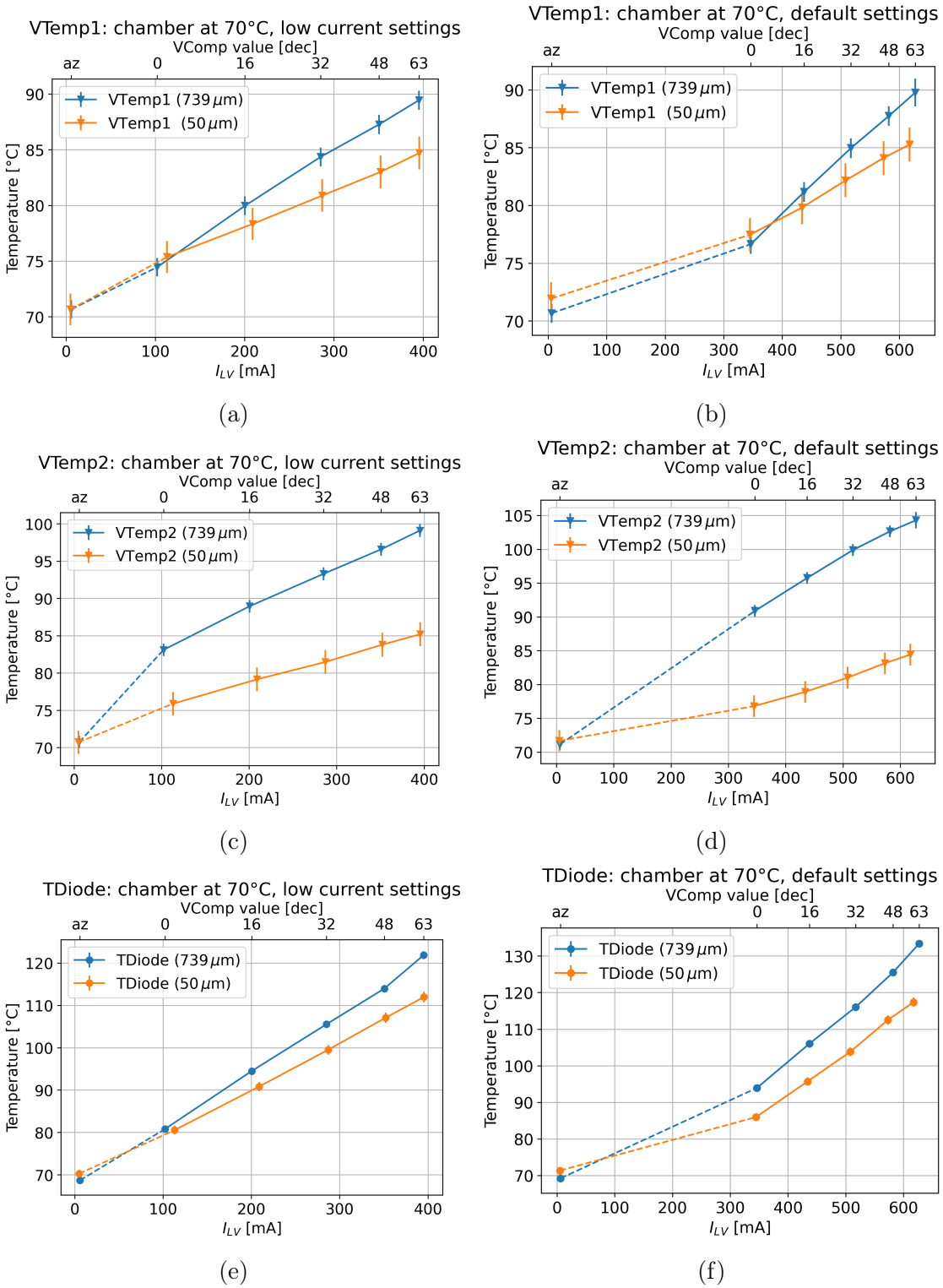


Figure A.5: Comparison of temperature measurements between the 327-01-04 (739 µm) and the 327-01-09 (50 µm) chip at +70 °C chamber temperature. For each temperature sensor a low current and a default measurement is compared.

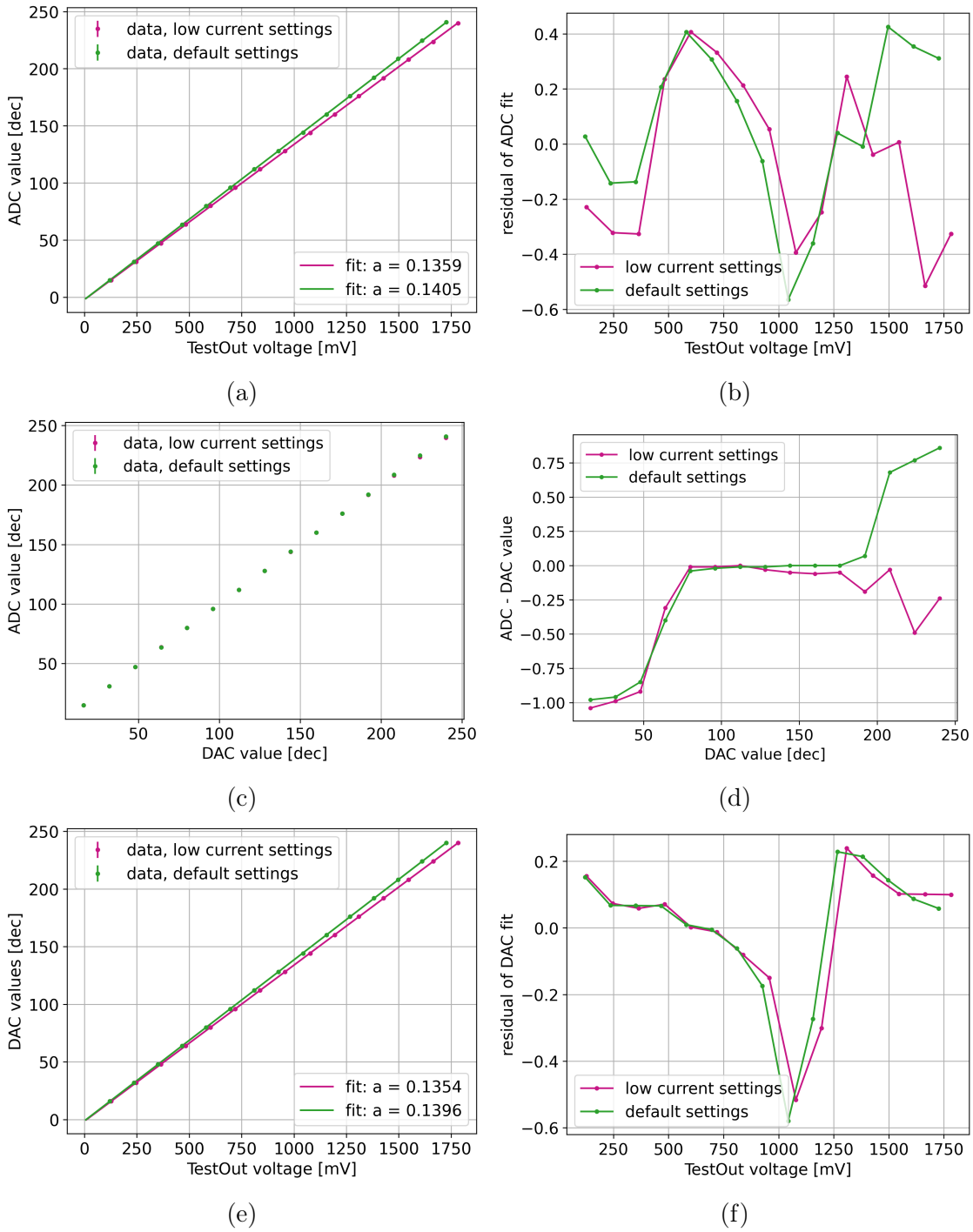


Figure A.6: ThPix scans of chip 327-01-04 (739 µm) at +30 °C chamber temperature for 'low current' and 'default' settings. The digital ADC values are calculated as the mean of > 70 measured values. Different relations are plotted. In a): the data of the digital ADC values versus the analogue TestOut voltages and their linear fit. Its residuals are shown in b). In c): the selected DAC input values against the digital ADC values. Their deviation is shown in d). In e): the selected DAC input values versus the analogue TestOut voltages and its linear fit. Its residuals are shown in f).

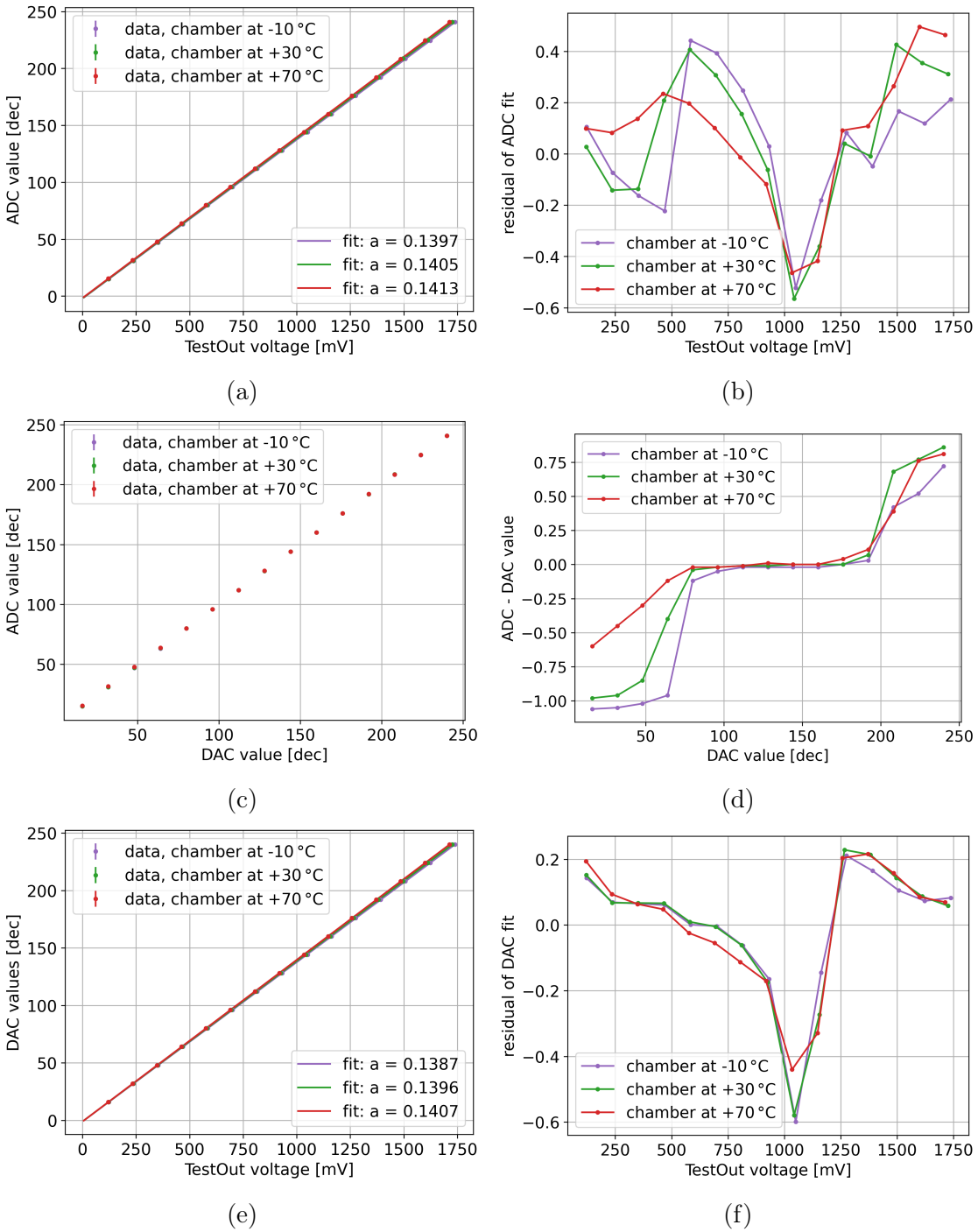


Figure A.7: ThPix scans of chip 327-01-04 739 µm at 'default' settings for chamber temperatures of −10 °C, +30 °C and +70 °C. The digital ADC values are calculated as the mean of > 70 measured values. Different relations are plotted. In a): the data of the digital ADC values versus the analogue TestOut voltages and their linear fit. Its residuals are shown in b). In c): the selected DAC input values against the digital ADC values. Their deviation is shown in d). In e): the selected DAC input values versus the analogue TestOut voltages and its linear fit. Its residuals are shown in f).

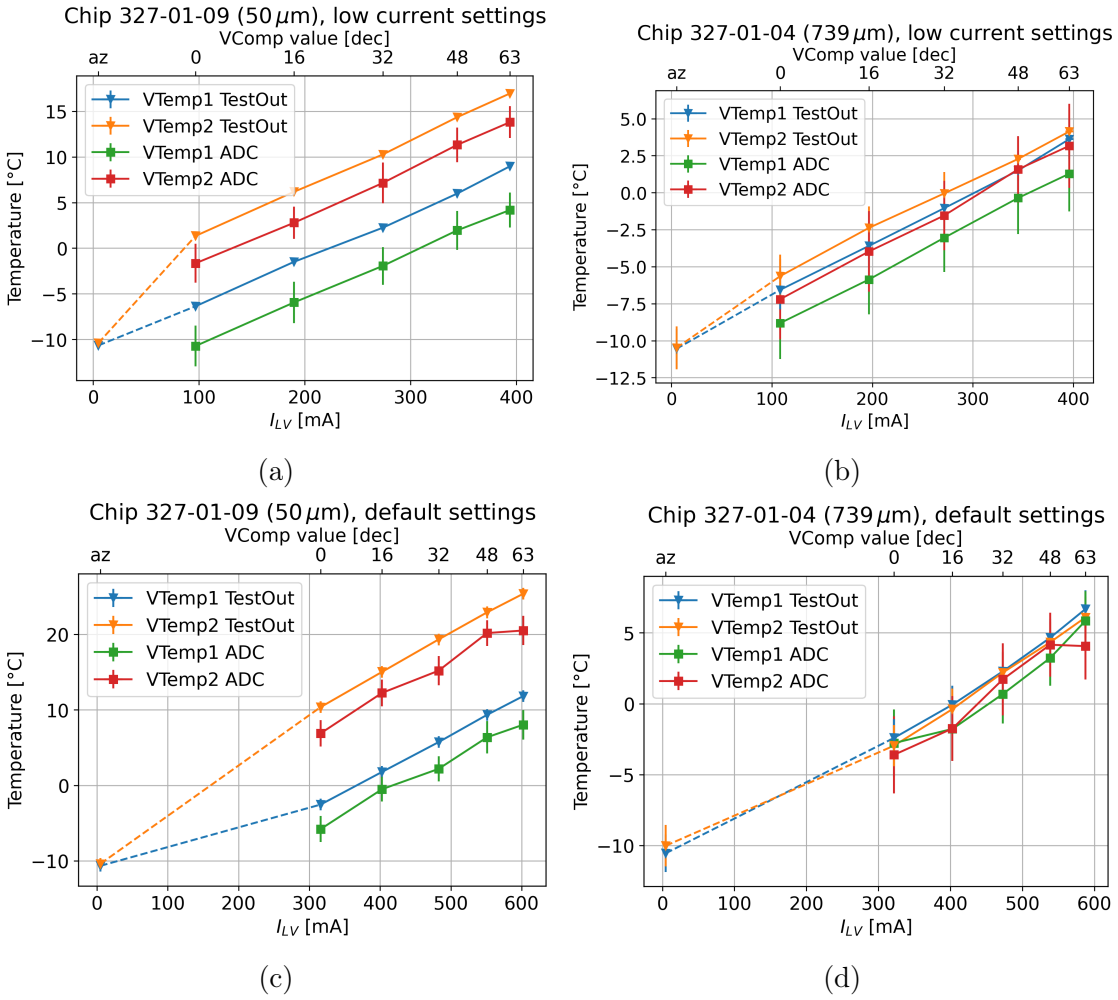


Figure A.8: Comparator scan (VComp2) temperature measurement comparison of VTemp measurements: analogue via the TestOut and digital via data stream after ADC calibration for different settings at $-10\,^{\circ}$C chamber temperature.

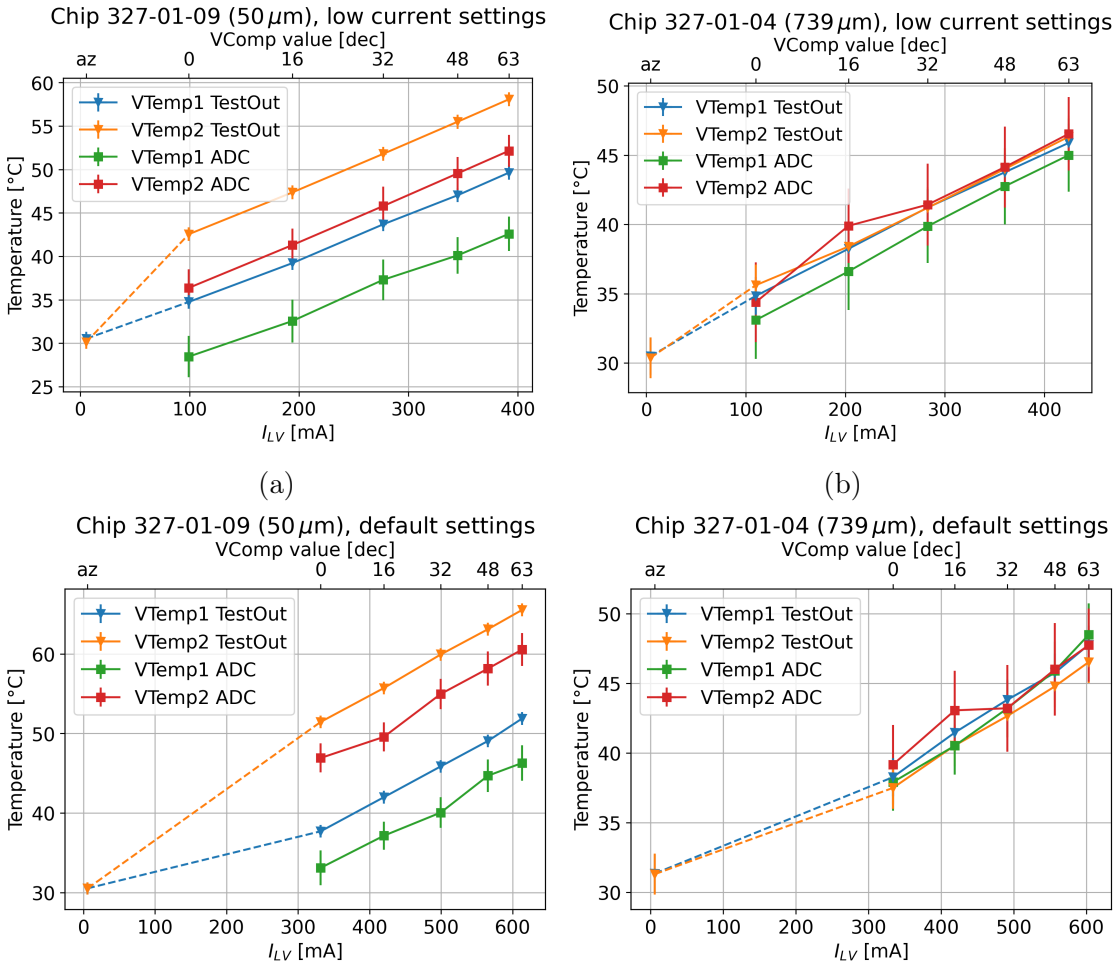


Figure A.9: Comparator scan (VComp2) temperature measurement comparison of VTemp measurements: analogue via the TestOut and digital via data stream after ADC calibration for different settings at +30 °C chamber temperature.

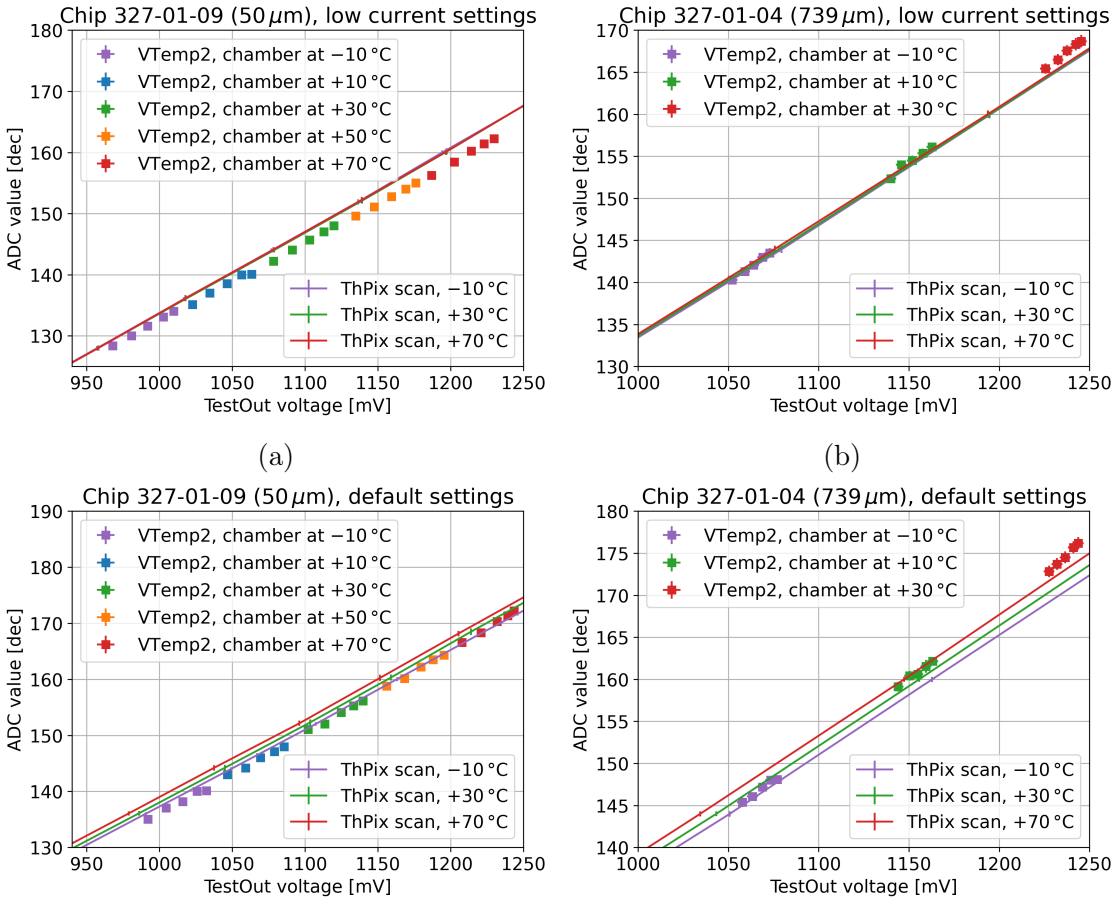


Figure A.10: Comparison of the ThPix scans used for ADC calibration and the VTemp2 measurements for different settings. The analogue TestOut voltage is plotted against the digital ADC value. For the ADC value the mean of > 70 measurements is used.

B DAC settings

DAC name	default_50um	default	matrix off	low current	all zero
Bandgap_on	0x0	0x0	0x0	0x0	0x0
BiasBlock_on	0x5	0x5	0x5	0x5	0x0
BLResPix	0x6	0x1e	0x0	0x0	0x0
ThRes	0x0	0x0	0x0	0x0	0x0
VNPix	0xa	0xa	0x0	0x0	0x0
VNFBPix	0x3	0x1e	0x0	0x0	0x0
VNFollPix	0x5	0x5	0x0	0x0	0x0
VNRegC	0x0	0x0	0x0	0x0	0x0
VNDel	0xa	0xa	0x0	0x0	0x0
VPComp1	0x5	0x5	0x0	0x0	0x0
VPDAC	0x0	0x0	0x0	0x0	0x0
VNPix2	0x0	0x0	0x0	0x0	0x0
BLResDig	0x5	0x5	0x0	0x0	0x0
VNBiasPix	0x0	0x0	0x0	0x0	0x0
VPLoadPix	0x5	0x5	0x0	0x0	0x0
VNOutPix	0x8	0x1	0x0	0x0	0x0
VPVCO	0x16	0x16	0x16	0x16	0x0
VNVCO	0x17	0x17	0x17	0x17	0x0
VPDelDclMux	0xa	0xa	0xa	0xa	0x0
VNDelDclMux	0xa	0xa	0xa	0xa	0x0
VPDelDcl	0xa	0xa	0xa	0xa	0x0
VNDelDcl	0xa	0xa	0xa	0xa	0x0
VPDelPreEmp	0xa	0xa	0xa	0xa	0x0
VNDelPreEmp	0xa	0xa	0xa	0xa	0x0
VPDcl	0x1e	0x1e	0x1e	0xa	0x0
VNDcl	0xf	0xf	0xf	0x6	0x0
VNLVDS	0xf	0xf	0xf	0x6	0x0
VNLVDSDel	0x0	0x0	0x0	0x0	0x0
VPPump	0x3f	0x3f	0x3f	0x3f	0x0
VPComp2	0x5	0x5	0x0	0x0	0x0
VNHB	0x0	0x0	0x0	0x0	0x0
VNComp	0x0	0x0	0x0	0x0	0x0
VPFoll	0x0	0x0	0x0	0x0	0x0
VNDAC	0x0	0x0	0x0	0x0	0x0
VPTimerDel	0x9	0x8	0x0	0x8	0x0

DAC name	default_50um	default	matrix off	low current	all zero
VNTimerDel	0xa	0xa	0x0	0xa	0x0
ckdivend	0x0	0x0	0x0	0x0	0x0
ckdivend2	0xf	0xf	0xf	0xf	0x0
timerend	0x0	0x0	0x0	0x0	0x0
slowdownend	0x0	0x0	0x0	0x0	0x0
maxcycend	0x3f	0x3f	0x3f	0x3f	0x0
resetckdivend	0x0	0x0	0x0	0x0	0x0
sendcounter	0x0	0x0	0x0	0x0	0x0
tsphase	0x0	0x0	0x0	0x0	0x0
linksel	0x0	0x0	0x0	0x0	0x0
EnSync_SC	0x0	0x0	0x1	0x0	0x0
slowdownlDColEnd	0x7	0x7	0x7	0x7	0x0
invert	0x1	0x1	0x1	0x1	0x0
SelEx	0x0	0x0	0x0	0x0	0x0
SelSlow	0x0	0x0	0x0	0x0	0x0
EnPLL	0x1	0x1	0x1	0x1	0x0
En2thre	0x1	0x1	0x1	0x1	0x0
AlwaysEnable	0x0	0x0	0x0	0x0	0x0
Tune_Reg_R	0x0	0x0	0x0	0x0	0x0
Tune_Reg_L	0x0	0x0	0x0	0x0	0x0
Aur_res_n	0x1	0x1	0x1	0x1	0x0
Ser_res_n	0x1	0x1	0x1	0x1	0x0
RO_res_n	0x1	0x1	0x1	0x1	0x0
disable_HB	0x1	0x1	0x1	0x1	0x0
TestOut	0x0	0x0	0xc	0xb	0xb
count_sheep	0x0	0x0	0x0	0x0	0x0
SelFast	0x0	0x0	0x0	0x0	0x0
ref_Vss	0xa9	0xa9	0x0	0x0	0x0
VDAC1	0x0	0x0	0x0	0x0	0x0
Baseline	0x70	0x70	0x0	0x70	0x0
ThLow2	0x0	0x0	0x0	0x0	0x0
ThHigh2	0x0	0x0	0x0	0x0	0x0
ThLow	0x75	0x72	0xff	0x90	0xff
ThHigh	0x76	0x80	0xff	0x90	0xff
ThPix	0x77	0x0	0x0	0x0	0x0
BLPix	0x50	0x90	0x0	0x90	0x0
VCAL	0x0	0x0	0x0	0x0	0x0
Bandgap_on	0x0	0x0	0x0	0x0	0x0
BiasBlock_on	0x5	0x5	0x5	0x5	0x0
BLResPix	0x6	0x1e	0x0	0x0	0x0
ThRes	0x0	0x0	0x0	0x0	0x0
VNPix	0xa	0xa	0x0	0x0	0x0
VNFBPix	0x3	0x1e	0x0	0x0	0x0

DAC name	default_50um	default	matrix off	low current	all zero
VNFollPix	0x5	0x5	0x0	0x0	0x0
VNRegC	0x0	0x0	0x0	0x0	0x0
VNDel	0xa	0xa	0x0	0x0	0x0
VPComp1	0x5	0x5	0x0	0x0	0x0
VPDAC	0x0	0x0	0x0	0x0	0x0
VNPix2	0x0	0x0	0x0	0x0	0x0
BLResDig	0x5	0x5	0x0	0x0	0x0
VNBiasPix	0x0	0x0	0x0	0x0	0x0
VPLoadPix	0x5	0x5	0x0	0x0	0x0
VNOutPix	0x8	0x1	0x0	0x0	0x0
VPVCO	0x16	0x16	0x16	0x16	0x0
VNVCO	0x17	0x17	0x17	0x17	0x0
VPDelDclMux	0xa	0xa	0xa	0xa	0x0
VNDelDclMux	0xa	0xa	0xa	0xa	0x0
VPDelDcl	0xa	0xa	0xa	0xa	0x0
VNDelDcl	0xa	0xa	0xa	0xa	0x0
VPDelPreEmp	0xa	0xa	0xa	0xa	0x0
VNDelPreEmp	0xa	0xa	0xa	0xa	0x0
VPDcl	0x1e	0x1e	0x1e	0xa	0x0
VNDcl	0xf	0xf	0xf	0x6	0x0
VNLVDS	0xf	0xf	0xf	0x6	0x0
VNLVDSDel	0x0	0x0	0x0	0x0	0x0
VPPump	0x3f	0x3f	0x3f	0x3f	0x0
VPComp2	0x5	0x5	0x0	0x0	0x0
VNHB	0x0	0x0	0x0	0x0	0x0
VNComp	0x0	0x0	0x0	0x0	0x0
VPFoll	0x0	0x0	0x0	0x0	0x0
VNDAC	0x0	0x0	0x0	0x0	0x0
VPTimerDel	0x9	0x8	0x0	0x8	0x0
VNTimerDel	0xa	0xa	0x0	0xa	0x0
ckdivend	0x0	0x0	0x0	0x0	0x0
ckdivend2	0xf	0xf	0xf	0xf	0x0
timerend	0x0	0x0	0x0	0x0	0x0
slowdownend	0x0	0x0	0x0	0x0	0x0
maxcycend	0x3f	0x3f	0x3f	0x3f	0x0
resetckdivend	0x0	0x0	0x0	0x0	0x0
sendcounter	0x0	0x0	0x0	0x0	0x0
tsphase	0x0	0x0	0x0	0x0	0x0
linksel	0x0	0x0	0x0	0x0	0x0
EnSync_SC	0x0	0x0	0x1	0x0	0x0
slowdownlDColEnd	0x7	0x7	0x7	0x7	0x0
invert	0x1	0x1	0x1	0x1	0x0
SelEx	0x0	0x0	0x0	0x0	0x0

DAC name	default_50um	default	matrix off	low current	all zero
SelSlow	0x0	0x0	0x0	0x0	0x0
EnPLL	0x1	0x1	0x1	0x1	0x0
En2thre	0x1	0x1	0x1	0x1	0x0
AlwaysEnable	0x0	0x0	0x0	0x0	0x0
Tune_Reg_R	0x0	0x0	0x0	0x0	0x0
Tune_Reg_L	0x0	0x0	0x0	0x0	0x0
Aur_res_n	0x1	0x1	0x1	0x1	0x0
Ser_res_n	0x1	0x1	0x1	0x1	0x0
RO_res_n	0x1	0x1	0x1	0x1	0x0
disable_HB	0x1	0x1	0x1	0x1	0x0
TestOut	0x0	0x0	0xc	0xb	0xb
count_sheep	0x0	0x0	0x0	0x0	0x0
SelFast	0x0	0x0	0x0	0x0	0x0
ref_Vss	0xa9	0xa9	0x0	0x0	0x0
VDAC1	0x0	0x0	0x0	0x0	0x0
Baseline	0x70	0x70	0x0	0x70	0x0
ThLow2	0x0	0x0	0x0	0x0	0x0
ThHigh2	0x0	0x0	0x0	0x0	0x0
ThLow	0x75	0x72	0xff	0x90	0xff
ThHigh	0x76	0x80	0xff	0x90	0xff
ThPix	0x77	0x0	0x0	0x0	0x0
BLPix	0x50	0x90	0x0	0x90	0x0
VCAL	0x0	0x0	0x0	0x0	0x0
Bandgap_on	0x0	0x0	0x0	0x0	0x0
BiasBlock_on	0x5	0x5	0x5	0x5	0x0
BLResPix	0x6	0x1e	0x0	0x0	0x0
ThRes	0x0	0x0	0x0	0x0	0x0
VNPix	0xa	0xa	0x0	0x0	0x0
VNFBPix	0x3	0x1e	0x0	0x0	0x0
VNFollPix	0x5	0x5	0x0	0x0	0x0
VNRegC	0x0	0x0	0x0	0x0	0x0
VNDel	0xa	0xa	0x0	0x0	0x0
VPComp1	0x5	0x5	0x0	0x0	0x0
VPDAC	0x0	0x0	0x0	0x0	0x0
VNPix2	0x0	0x0	0x0	0x0	0x0
BLResDig	0x5	0x5	0x0	0x0	0x0
VNBiasPix	0x0	0x0	0x0	0x0	0x0
VPLoadPix	0x5	0x5	0x0	0x0	0x0
VNOutPix	0x8	0x1	0x0	0x0	0x0
VPVCO	0x16	0x16	0x16	0x16	0x0
VNVCO	0x17	0x17	0x17	0x17	0x0
VPDelDclMux	0xa	0xa	0xa	0xa	0x0
VNDelDclMux	0xa	0xa	0xa	0xa	0x0

DAC name	default_50um	default	matrix off	low current	all zero
VPDelDcl	0xa	0xa	0xa	0xa	0x0
VNDelDcl	0xa	0xa	0xa	0xa	0x0
VPDelPreEmp	0xa	0xa	0xa	0xa	0x0
VNDelPreEmp	0xa	0xa	0xa	0xa	0x0
VPDcl	0x1e	0x1e	0x1e	0xa	0x0
VNDcl	0xf	0xf	0xf	0x6	0x0
VNLVDS	0xf	0xf	0xf	0x6	0x0
VNLVDSDel	0x0	0x0	0x0	0x0	0x0
VPPump	0x3f	0x3f	0x3f	0x3f	0x0
VPComp2	0x5	0x5	0x0	0x0	0x0
VNHB	0x0	0x0	0x0	0x0	0x0
VNComp	0x0	0x0	0x0	0x0	0x0
VPFoll	0x0	0x0	0x0	0x0	0x0
VNDAC	0x0	0x0	0x0	0x0	0x0
VPTimerDel	0x9	0x8	0x0	0x8	0x0
VNTimerDel	0xa	0xa	0x0	0xa	0x0
ckdivend	0x0	0x0	0x0	0x0	0x0
ckdivend2	0xf	0xf	0xf	0xf	0x0
timerend	0x0	0x0	0x0	0x0	0x0
slowdownend	0x0	0x0	0x0	0x0	0x0
maxcycend	0x3f	0x3f	0x3f	0x3f	0x0
resetckdivend	0x0	0x0	0x0	0x0	0x0
sendcounter	0x0	0x0	0x0	0x0	0x0
tsphase	0x0	0x0	0x0	0x0	0x0
linksel	0x0	0x0	0x0	0x0	0x0
EnSync_SC	0x0	0x0	0x1	0x0	0x0
slowdownlDColEnd	0x7	0x7	0x7	0x7	0x0
invert	0x1	0x1	0x1	0x1	0x0
SelEx	0x0	0x0	0x0	0x0	0x0
SelSlow	0x0	0x0	0x0	0x0	0x0
EnPLL	0x1	0x1	0x1	0x1	0x0
En2thre	0x1	0x1	0x1	0x1	0x0
AlwaysEnable	0x0	0x0	0x0	0x0	0x0
Tune_Reg_R	0x0	0x0	0x0	0x0	0x0
Tune_Reg_L	0x0	0x0	0x0	0x0	0x0
Aur_res_n	0x1	0x1	0x1	0x1	0x0
Ser_res_n	0x1	0x1	0x1	0x1	0x0
RO_res_n	0x1	0x1	0x1	0x1	0x0
disable_HB	0x1	0x1	0x1	0x1	0x0
TestOut	0x0	0x0	0xc	0xb	0xb
count_sheep	0x0	0x0	0x0	0x0	0x0
SelFast	0x0	0x0	0x0	0x0	0x0
ref_Vss	0xa9	0xa9	0x0	0x0	0x0

DAC name	default_50um	default	matrix off	low current	all zero
VDAC1	0x0	0x0	0x0	0x0	0x0
Baseline	0x70	0x70	0x0	0x70	0x0
ThLow2	0x0	0x0	0x0	0x0	0x0
ThHigh2	0x0	0x0	0x0	0x0	0x0
ThLow	0x75	0x72	0xff	0x90	0xff
ThHigh	0x76	0x80	0xff	0x90	0xff
ThPix	0x77	0x0	0x0	0x0	0x0
BLPix	0x50	0x90	0x0	0x90	0x0
VCAL	0x0	0x0	0x0	0x0	0x0
Bandgap_on	0x0	0x0	0x0	0x0	0x0
BiasBlock_on	0x5	0x5	0x5	0x5	0x0
BLResPix	0x6	0x1e	0x0	0x0	0x0
ThRes	0x0	0x0	0x0	0x0	0x0
VNPix	0xa	0xa	0x0	0x0	0x0
VNFBPix	0x3	0x1e	0x0	0x0	0x0
VNFollPix	0x5	0x5	0x0	0x0	0x0
VNRegC	0x0	0x0	0x0	0x0	0x0
VNDel	0xa	0xa	0x0	0x0	0x0
VPComp1	0x5	0x5	0x0	0x0	0x0
VPDAC	0x0	0x0	0x0	0x0	0x0
VNPix2	0x0	0x0	0x0	0x0	0x0
BLResDig	0x5	0x5	0x0	0x0	0x0
VNBiasPix	0x0	0x0	0x0	0x0	0x0
VPLoadPix	0x5	0x5	0x0	0x0	0x0
VNOutPix	0x8	0x1	0x0	0x0	0x0
VPVCO	0x16	0x16	0x16	0x16	0x0
VNVCO	0x17	0x17	0x17	0x17	0x0
VPDelDclMux	0xa	0xa	0xa	0xa	0x0
VNDelDclMux	0xa	0xa	0xa	0xa	0x0
VPDelDcl	0xa	0xa	0xa	0xa	0x0
VNDelDcl	0xa	0xa	0xa	0xa	0x0
VPDelPreEmp	0xa	0xa	0xa	0xa	0x0
VNDelPreEmp	0xa	0xa	0xa	0xa	0x0
VPDcl	0x1e	0x1e	0x1e	0xa	0x0
VNDcl	0xf	0xf	0xf	0x6	0x0
VNLVDS	0xf	0xf	0xf	0x6	0x0
VNLVDSDel	0x0	0x0	0x0	0x0	0x0
VPPump	0x3f	0x3f	0x3f	0x3f	0x0
VPComp2	0x5	0x5	0x0	0x0	0x0
VNHB	0x0	0x0	0x0	0x0	0x0
VNComp	0x0	0x0	0x0	0x0	0x0
VPFoll	0x0	0x0	0x0	0x0	0x0
VNDAC	0x0	0x0	0x0	0x0	0x0

DAC name	default_50um	default	matrix off	low current	all zero
VPTimerDel	0x9	0x8	0x0	0x8	0x0
VNTimerDel	0xa	0xa	0x0	0xa	0x0
ckdivend	0x0	0x0	0x0	0x0	0x0
ckdivend2	0xf	0xf	0xf	0xf	0x0
timerend	0x0	0x0	0x0	0x0	0x0
slowdownend	0x0	0x0	0x0	0x0	0x0
maxcycend	0x3f	0x3f	0x3f	0x3f	0x0
resetckdivend	0x0	0x0	0x0	0x0	0x0
sendcounter	0x0	0x0	0x0	0x0	0x0
tsphase	0x0	0x0	0x0	0x0	0x0
linksel	0x0	0x0	0x0	0x0	0x0
EnSync_SC	0x0	0x0	0x1	0x0	0x0
slowdownlDColEnd	0x7	0x7	0x7	0x7	0x0
invert	0x1	0x1	0x1	0x1	0x0
SelEx	0x0	0x0	0x0	0x0	0x0
SelSlow	0x0	0x0	0x0	0x0	0x0
EnPLL	0x1	0x1	0x1	0x1	0x0
En2thre	0x1	0x1	0x1	0x1	0x0
AlwaysEnable	0x0	0x0	0x0	0x0	0x0
Tune_Reg_R	0x0	0x0	0x0	0x0	0x0
Tune_Reg_L	0x0	0x0	0x0	0x0	0x0
Aur_res_n	0x1	0x1	0x1	0x1	0x0
Ser_res_n	0x1	0x1	0x1	0x1	0x0
RO_res_n	0x1	0x1	0x1	0x1	0x0
disable_HB	0x1	0x1	0x1	0x1	0x0
TestOut	0x0	0x0	0xc	0xb	0xb
count_sheep	0x0	0x0	0x0	0x0	0x0
SelFast	0x0	0x0	0x0	0x0	0x0
ref_Vss	0xa9	0xa9	0x0	0x0	0x0
VDAC1	0x0	0x0	0x0	0x0	0x0
Baseline	0x70	0x70	0x0	0x70	0x0
ThLow2	0x0	0x0	0x0	0x0	0x0
ThHigh2	0x0	0x0	0x0	0x0	0x0
ThLow	0x75	0x72	0xff	0x90	0xff
ThHigh	0x76	0x80	0xff	0x90	0xff
ThPix	0x77	0x0	0x0	0x0	0x0
BLPix	0x50	0x90	0x0	0x90	0x0
VCAL	0x0	0x0	0x0	0x0	0x0
Bandgap_on	0x0	0x0	0x0	0x0	0x0
BiasBlock_on	0x5	0x5	0x5	0x5	0x0
BLResPix	0x6	0x1e	0x0	0x0	0x0
ThRes	0x0	0x0	0x0	0x0	0x0
VNPix	0xa	0xa	0x0	0x0	0x0

DAC name	default_50um	default	matrix off	low current	all zero
VNFBPix	0x3	0x1e	0x0	0x0	0x0
VNFollPix	0x5	0x5	0x0	0x0	0x0
VNRegC	0x0	0x0	0x0	0x0	0x0
VNDel	0xa	0xa	0x0	0x0	0x0
VPComp1	0x5	0x5	0x0	0x0	0x0
VPDAC	0x0	0x0	0x0	0x0	0x0
VNPix2	0x0	0x0	0x0	0x0	0x0
BLResDig	0x5	0x5	0x0	0x0	0x0
VNBiasPix	0x0	0x0	0x0	0x0	0x0
VPLoadPix	0x5	0x5	0x0	0x0	0x0
VNOutPix	0x8	0x1	0x0	0x0	0x0
VPVCO	0x16	0x16	0x16	0x16	0x0
VNVCO	0x17	0x17	0x17	0x17	0x0
VPDelDclMux	0xa	0xa	0xa	0xa	0x0
VNDelDclMux	0xa	0xa	0xa	0xa	0x0
VPDelDcl	0xa	0xa	0xa	0xa	0x0
VNDelDcl	0xa	0xa	0xa	0xa	0x0
VPDelPreEmp	0xa	0xa	0xa	0xa	0x0
VNDelPreEmp	0xa	0xa	0xa	0xa	0x0
VPDcl	0x1e	0x1e	0x1e	0xa	0x0
VNDcl	0xf	0xf	0xf	0x6	0x0
VNLVDS	0xf	0xf	0xf	0x6	0x0
VNLVDSDel	0x0	0x0	0x0	0x0	0x0
VPPump	0x3f	0x3f	0x3f	0x3f	0x0
VPComp2	0x5	0x5	0x0	0x0	0x0
VNHB	0x0	0x0	0x0	0x0	0x0
VNComp	0x0	0x0	0x0	0x0	0x0
VPFoll	0x0	0x0	0x0	0x0	0x0
VNDAC	0x0	0x0	0x0	0x0	0x0
VPTimerDel	0x9	0x8	0x0	0x8	0x0
VNTimerDel	0xa	0xa	0x0	0xa	0x0
ckdivend	0x0	0x0	0x0	0x0	0x0
ckdivend2	0xf	0xf	0xf	0xf	0x0
timerend	0x0	0x0	0x0	0x0	0x0
slowdownend	0x0	0x0	0x0	0x0	0x0
maxcycend	0x3f	0x3f	0x3f	0x3f	0x0
resetckdivend	0x0	0x0	0x0	0x0	0x0
sendcounter	0x0	0x0	0x0	0x0	0x0
tsphase	0x0	0x0	0x0	0x0	0x0
linksel	0x0	0x0	0x0	0x0	0x0
EnSync_SC	0x1	0x1	0x1	0x1	0x1
slowdownlDColEnd	0x7	0x7	0x7	0x7	0x0
invert	0x1	0x1	0x1	0x1	0x0

DAC name	default_50um	default	matrix off	low current	all zero
SelEx	0x0	0x0	0x0	0x0	0x0
SelSlow	0x0	0x0	0x0	0x0	0x0
EnPLL	0x1	0x1	0x1	0x1	0x0
En2thre	0x1	0x1	0x1	0x1	0x0
AlwaysEnable	0x0	0x0	0x0	0x0	0x0
Tune_Reg_R	0x0	0x0	0x0	0x0	0x0
Tune_Reg_L	0x0	0x0	0x0	0x0	0x0
Aur_res_n	0x1	0x1	0x1	0x1	0x0
Ser_res_n	0x1	0x1	0x1	0x1	0x0
RO_res_n	0x1	0x1	0x1	0x1	0x0
disable_HB	0x1	0x1	0x1	0x1	0x0
TestOut	0x0	0x0	0xc	0xb	0xb
count_sheep	0x0	0x0	0x0	0x0	0x0
SelFast	0x0	0x0	0x0	0x0	0x0
ref_Vss	0xa9	0xa9	0x0	0x0	0x0
VDAC1	0x0	0x0	0x0	0x0	0x0
Baseline	0x70	0x70	0x0	0x70	0x0
ThLow2	0x0	0x0	0x0	0x0	0x0
ThHigh2	0x0	0x0	0x0	0x0	0x0
ThLow	0x80	0x80	0xff	0x90	0xff
ThHigh	0x80	0x80	0xff	0x90	0xff
ThPix	0x77	0x0	0x0	0x0	0x0
BLPix	0x50	0x90	0x0	0x90	0x0
VCAL	0x0	0x0	0x0	0x0	0x0

Table B.1: DAC values of the used settings. The 'default_50um' setting is used for 4. It is a setting optimised in test beam sessions for 50 µm MuPix11 chips. The 'default' setting is a common setting optimised for the MuPix11. The 'matrix off' setting is a copy of the 'default' settings with all entities on the chip matrix turned off. The 'low current' setting as well disables the chip matrix and additionally reduces power consumption in the periphery to a minimum. At 'all zero' settings, every power consuming entity is switched off to minimise self-heating effects.

C Bibliography

[1] G. Aad et al. "Observation of a new particle in the search for the Standard Model Higgs boson with the ATLAS detector at the LHC". In: *Physics Letters B* 716.1 (2012), pp. 1–29. ISSN: 0370-2693. DOI: https://doi.org/10.1016/j.physletb.2012.08.020. URL: https://www.sciencedirect.com/science/article/pii/S037026931200857X.

[2] S. Chatrchyan et al. "Observation of a new boson at a mass of 125 GeV with the CMS experiment at the LHC". In: *Physics Letters B* 716.1 (2012), pp. 30–61. ISSN: 0370-2693. DOI: https://doi.org/10.1016/j.physletb.2012.08.021. URL: https://www.sciencedirect.com/science/article/pii/S0370269312008581.

[3] M. Thomson. "Modern Particle Physics". In: *Cambridge University Press, New York* (2013). DOI: 10.1017/CBO9781139525367.

[4] Q. R. et al Ahmad. "Measurement of the Rate of $\nu_e + d \rightarrow p + p + e^-$ Interactions Produced by ^8B Solar Neutrinos at the Sudbury Neutrino Observatory". In: *Phys. Rev. Lett.* 87 (7 July 2001), p. 071301. DOI: 10.1103/PhysRevLett.87.071301. URL: https://link.aps.org/doi/10.1103/PhysRevLett.87.071301.

[5] F. P. et al An. "Observation of Electron-Antineutrino Disappearance at Daya Bay". In: *Phys. Rev. Lett.* 108 (17 Apr. 2012), p. 171803. DOI: 10.1103/PhysRevLett.108.171803. URL: https://link.aps.org/doi/10.1103/PhysRevLett.108.171803.

[6] Y. et all Fukuda. "Evidence for Oscillation of Atmospheric Neutrinos". In: *Phys. Rev. Lett.* 81 (8 Aug. 1998), pp. 1562–1567. DOI: 10.1103/PhysRevLett.81.1562. URL: https://link.aps.org/doi/10.1103/PhysRevLett.81.1562.

[7] G. et al Apollinari. "High-Luminosity Large Hadron Collider (HL-LHC). Technical Design Report V. 0.1". In: (Jan. 2017). DOI: 10.23731/CYRM-2017-004. URL: https://www.osti.gov/biblio/1767028.

[8] Michelangelo et all Mangano. *FCC Physics Opportunities: Future Circular Collider Conceptual Design Report Volume 1. Future Circular Collider*. Tech. rep. 6. Geneva: CERN, 2019. DOI: 10.1140/epjc/s10052-019-6904-3. URL: https://cds.cern.ch/record/2651294.

[9] A. Blondel et al. *Research Proposal for an Experiment to Search for the Decay μ -> eee*. 2013. arXiv: 1301.6113 [physics.ins-det].

[10] K. Arndt et al. "Technical design of the phase I Mu3e experiment". In: *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment* 1014 (2021), p. 165679. ISSN: 0168-9002. DOI: https://doi.org/10.1016/j.nima.2021.165679. URL: https://www.sciencedirect.com/science/article/pii/S0168900221006641.

[11] D. Galbraith and C. Burgard. "Standard Model of Physics". In: *CERN Webfest 2012* (). URL: http://davidgalbraith.org/portfolio/ux-standard-model-of-%20the-standard-model/.

[12] F. Englert and R. Brout. "Broken Symmetry and the Mass of Gauge Vector Mesons". In: *Phys. Rev. Lett.* 13 (9 Aug. 1964), pp. 321–323. DOI: 10.1103/PhysRevLett.13.321. URL: https://link.aps.org/doi/10.1103/PhysRevLett.13.321.

[13] Peter W. Higgs. "Broken Symmetries and the Masses of Gauge Bosons". In: *Phys. Rev. Lett.* 13 (16 Oct. 1964), pp. 508–509. DOI: 10.1103/PhysRevLett.13.508. URL: https://link.aps.org/doi/10.1103/PhysRevLett.13.508.

[14] Takehiko Asaka and Mikhail Shaposhnikov. "The nuMSM, dark matter and baryon asymmetry of the universe". In: *Physics Letters B* 620 (2005), pp. 17–26. DOI: https://doi.org/10.1016/j.physletb.2005.06.020. URL: http://infoscience.epfl.ch/record/151084.

[15] Yoshitaka Kuno and Yasuhiro Okada. "Muon decay and physics beyond the standard model". In: *Reviews of Modern Physics* 73.1 (Jan. 2001), pp. 151–202. DOI: 10.1103/revmodphys.73.151. URL: https://doi.org/10.1103/RevModPhys.73.151.

[16] U. Bellgardt et al. "Search for the Decay mu+ —> e+ e+ e-". In: *Nucl. Phys. B* 299 (1988), pp. 1–6. DOI: 10.1016/0550-3213(88)90462-2.

[17] "Search for the lepton flavour violating decay μ+ → e+ with the full dataset of the MEG experiment". In: *European Physical Journal* C, Particles and Fields 76.8 (2016). DOI: 10.1140/epjc/s10052-016-4271-x.193.

[18] A. M. Baldini et al. "The design of the MEG II experiment". In: *The European Physical Journal C* 78.5 (May 2018). DOI: 10.1140/epjc/s10052-018-5845-6. URL: https://doi.org/10.1140/epjc/s10052-018-5845-6.

[19] W. Bertl et al. "A Search for muon to electron conversion in muonic gold". In: *Eur. Phys. J. C* 47 (2006), pp. 337–346. DOI: 10.1140/epjc/s2006-02582-x.

[20] R Abramishvili et al. "COMET Phase-I technical design report". In: *Progress of Theoretical and Experimental Physics* 2020.3 (Mar. 2020). DOI: 10.1093/ptep/ptz125. URL: https://doi.org/10.1093/ptep/ptz125.

[21] Robert H. Bernstein. "The Mu2e Experiment". In: *Frontiers in Physics* 7 (Jan. 2019). DOI: 10.3389/fphy.2019.00001. URL: https://doi.org/10.3389/fphy.2019.00001.

[22] Thomas T. Rudzki. "The Mu3e vertex detector - construction, cooling, and first prototype operation". PhD Thesis. Heidelberg University, Germany, 2022.

[23] M. Aiba et all. *Science Case for the new High-Intensity Muon Beams HIMB at PSI*. 2021. arXiv: 2111.05788 [hep-ex].

[24] G. Hernández-Tomé, G. Castro and P. Roig. "Flavor violating leptonic decays of τ and μ leptons in the Standard Model with massive neutrinos". In: *The European Physical Journal C* 79 (Jan. 2019). DOI: 10.1140/epjc/s10052-019-6563-4.

[25] H. Kolanoski N. Wermes. *Teilchendetektoren, Grundlagen und Anwendungen*. Springer-Verlag Berlin Heidelberg, 2016.

[26] Thomas Theodor Rudzki, Frank Meier Aeschbacher, Marin Deflorin and Niculin Flucher. "Successful cooling of a pixel tracker using gaseous helium: Studies with a mock-up and a detector prototype". In: *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment* 1054 (2023), p. 168405. ISSN: 0168-9002. DOI: https://doi.org/10.1016/j.nima.2023.168405. URL: https://www.sciencedirect.com/science/article/pii/S0168900223003959.

[27] S. Hunklinger. *Festkörperphysik*. 5th ed. Walter de Gruyter GmbH, Berlin/Bosten, 2018.

[28] Behazad Razavi. *Fundamentals of Microelectronics*. 2nd ed. Wiley, 2014.

[29] Heiko Augustin. "Development of a novel slow control interface and suppression of signal line crosstalk enabling HV-MAPS as sensor technology for Mu3e". PhD Thesis. Heidelberg University, Germany, 2021.

[30] *MK53*. URL: https://www.binder-world.com/de-de/produkt/asset/16171?cHash=c307168ec523a262cffe01dee42c2c94.

[31] Dostmann Electronics. *Precision Measuring Instrument - P600 series*. URL: http://www.dostmann-electronic.de/docs/48.pdf.

[32] FLIR Systems. *User's manual: ThermaCAM™ Researcher Professional*. 2009. URL: https://manualzz.com/doc/6786377/user-s-manual-thermacam%E2%84%A2-researcher-professional.

[33] D. Dannheim et al. "Corryvreckan: a modular 4D track reconstruction and analysis software for test beam data". In: *Journal of Instrumentation* 16.03 (Mar. 2021), P03008. DOI: 10.1088/1748-0221/16/03/p03008. URL: https://iopscience.iop.org/article/10.1088/1748-0221/16/03/P03008.

[34] Rene Brun and Fons Rademakers. "ROOT — An object oriented data analysis framework". In: *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment* 389.1 (1997). New Computing Techniques in Physics Research V, pp. 81–86. ISSN: 0168-9002. DOI: https://doi.org/10.1016/S0168-9002(97)00048-X. URL: https://www.sciencedirect.com/science/article/pii/S016890029700048X.

Acknowledgements

I would like to acknowledge the following individuals for their contributions to this thesis. Firstly, I express my sincere gratitude to Prof. Dr. André Schöning for providing me with the opportunity to be part of his research group and for allowing me to undertake this thesis. I extend my special thanks to Dr. Heiko Augustin for his invaluable guidance, expertise, and continuous availability for answering my questions and providing support throughout this project.
I am grateful to all the members of the HV-MAPS research group, particularly David Immig, Dr. Thomas Rudzki, Ruben Kolb, and Benjamin Weinlaeder, for their generous assistance in the laboratory and their careful proofreading of this thesis.
Furthermore, I would like to acknowledge my father, Michael, for sharing his inspiring passion for physics with me, as well as my mother and sister for their unwavering support throughout my journey.
Finally, I want to express my heartfelt appreciation to my dear friends Felix, Lasse, Leoni, Line, Paula, and Pauline, whose companionship and inspiration have been invaluable to me during my years of study.

Declaration of Authorship

Ich versichere, dass ich diese Arbeit selbstständig verfasst habe und keine anderen als die angegebenen Quellen und Hilfsmittel benutzt habe.

Heidelberg den 05.07.2023