Special - LMX Seminar

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Ferroelectric Synaptic Weights with Hafnia Superlattices

Expanding beyond traditional silicon, the integration of innovative materials into the back-end-of-line (BEOL) of CMOS circuits is essential for the advancement of Artificial Neural Networks accelerators. The hardware realization of synaptic weights necessitates the utilization of linear and reprogrammable resistive elements. Within ferroelectric tunnel junctions, resistance can be tailored by manipulating the arrangement of ferroelectric domains through electrical pulses. By partitioning ferroelectric $HfZrO_4$ into HfO_2–ZrO_2 superlattices, the crystallization temperature falls below the 400 °C threshold required for BEOL integration. A reduction in device footprint is accompanied by a notable increase in the maximum-to-minimum conductance ratio from 7 to 32. Operating from ultra-fast (20 ns) to biological (500 µs) timescales, the synaptic plasticity is extensively characterized. Dynamic hysteresis mode, spanning up to 10^{11} switching cycles, reveals the coexistence of ferroelectric and non-ferroelectric phenomena, such as defect rearrangement. Temperature-dependent transport measurements conducted under the linear (Ohmic) regime corroborate these findings. Additionally, the integration of superlattices into CMOS BEOL facilitates multi-level resistive switching. Demonstrating 1T-1R operation, this advancement lays the groundwork for the hardware realization of synaptic weights, enabling in-memory neuromorphic computing.