# The Mu3e pixel detector: Ultra-light, helium cooled, HV-MAPS based

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### **Physics motivation of Mu3e**

• Search for **charged lepton flavor** violation in the decay:

 $\mu^+ \rightarrow e^+ e^- e^+$ 

In the Standard Model including neutrino mixing, this process is **highly** suppressed with a branching fraction of  $\mathcal{B} < 10^{-54}$  (Figure below).

#### **Detector building blocks**

Area:

20.66 x 23.18

 $mm^2$ 

- MuPix11, 50/70 µm thin, High-voltage monolithic pixel sensor (HV-MAPS)
- High-density interconnects Al-polyimide laminates, electrical serives + mechanical support

#### **Vertex detector & Outer pixel layers**

#### Pixel detector

- $\diamond$  2,844 pixel chips  $\rightarrow$  182,016,000 channels
- ♦ cooled by gaseous helium
- Vertex detector
  - 2x inner tracking layers
- Radii: 1) 23.3 mm, 2) 29.8 mm
- Sensor thickness: 50 µm
- $\diamond$  8 + 10 ladders, 6 chips each,

#### Outer layers

- 2x outer tracking layers

with sensor chips





Thus, an observed signal would indicate the presence of new physics.



Radii: 3) 73.9 mm, 4) 86.3 mm Sensor thickness: 70 µm  $\diamond$  24 +28 ladders, 17/18 chips each Closing the helium volum  $\diamond$  3 stations: flex PCB nnecting 4 la o one module 1x central: around target 2x recurl: upstream & downstream Long tracks curl back  $\rightarrow$  6 pixel hits per track Recurl Central Recurl

#### Helium as coolant for the pixel detectors

- Signal decay has to be distinguished from:  $\mu^+ \rightarrow e^+ e^- e^+ \nu \bar{\nu}$
- Only possible for sufficient momentum resolution.
- Resolution is multiple-Coulomb scattering dominated



little material budget:  $\sim 0.1 \% X_0$  per tracking layer negligible scattering in passive part of detector gaseous cooling adds least material

#### Thermal studies of the Mu3e vertex detector

- Thermal-mechanical mock-up using silicon heater chips instead of MuPix11
- Vertex detector: **2 g/s helium** are provided in two flow channels for cooling
- Outer pixel layers: **16 g/s helium** in two flow channels per each station
- **Measured** temperature difference to gas inlet temperature on each heater chip of the vertex detector **♦** All temperature below 70°C







for 350 mW/cm<sup>2</sup> (mechanical limit)

**Characterity** of temperature to power as well as temperature to mass flow

> Temperature to mass flow and temperature to power relation for all chips of a heater ladder in Layer 2



#### **Detector production and QC**

Module/detector production verified with silicon heater chips



DFG

- Vertex detector produced manually by Heidelberg at Paul Scherrer Institut (PSI)
- Outer layers produced highly automatized in Oxford & Liverpool





Chip alignment and ladder production tool for the vertex detector



spTAB bonding of an outer pixel ladder in Oxford;

- Working on single chip QC in Heidelberg
- Ladder QC algorithms under development, same building blocks as chip QC
- Testing vertical slice with Ladder QC, all final electrical components in hand
- Finish vertex detector construction in 2023

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