Test Measurements with the Technical Prototype for the Mu3e Tile Detector

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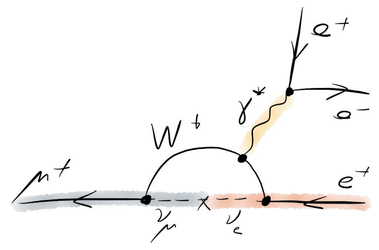
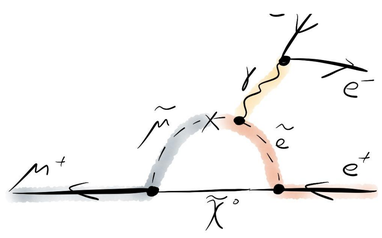
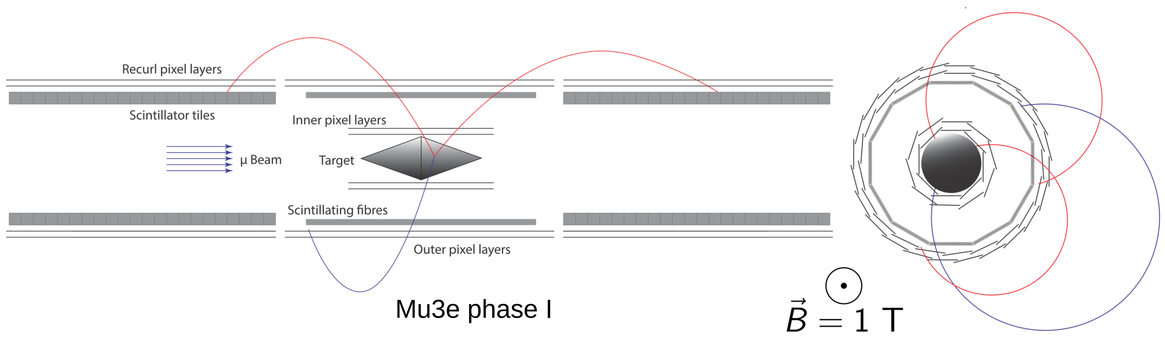
The Mu3e Experiment

- searching for the **lepton-flavour violating (LFV) decay μ → eee**
  - → suppressed in extended SM by O(10^{-54})
  - → enhanced LFV predicted by **new physics**



- aimed sensitivity of **BR < 10^{-16}**
  - → precise spatial and timing measurements for background suppression needed
  - → tracking: pixel detector (HV-MAPS)
  - → **timing: scintillating tiles**/fibres

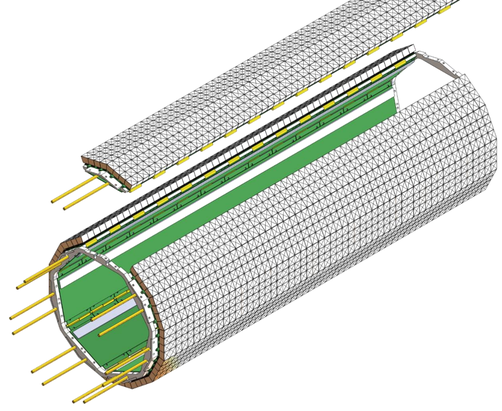


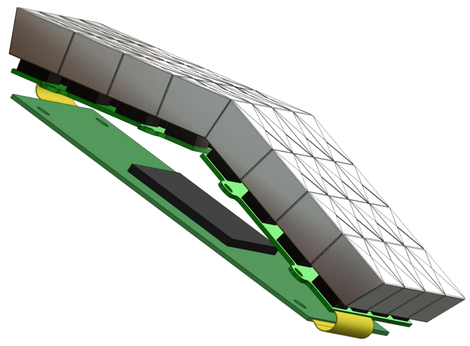


Mu3e phase I

The Tile Detector

- to be installed on recurl stations (up- and downstream of target)
- **scintillator tiles** (≈ 6x6x5 mm^3)
- signals read out by silicon photomultipliers (**SiPMs**)
- dedicated read-out ASIC **MuTRiG**
- targeted timing resolution **< 100 ps**





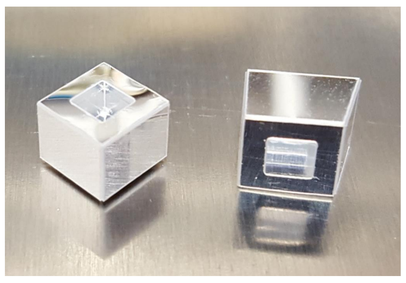
structure:

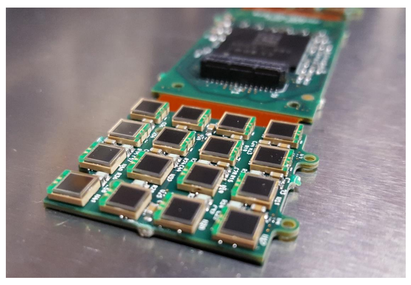
- 2 x 16 tiles per **submodule**
- 14 submodules per module
- 7 modules per full recurl station
- 2 recurl stations (Mu3e phase I)
  - → more than **6.000 channels** in total

Development of a Technical Prototype

assembly:

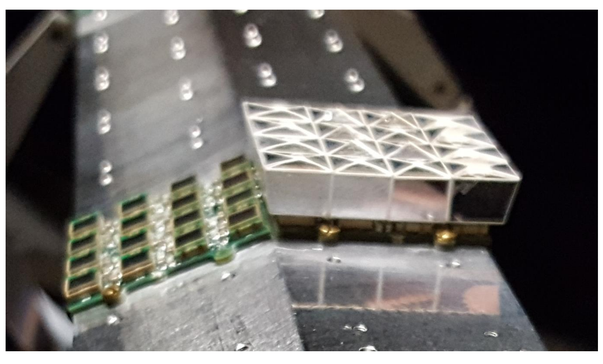
- design and equipping of dedicated front end-boards (FEBs)
  - → chip bonding
  - → soldering of SiPMs and components
- individual tile wrapping with reflective foils
  - → reduce optical cross-talk
- gluing of tiles to SiPMs
- assembly of submodules to cooling structure
  - → cooling support structure produced in local mechanics workshop





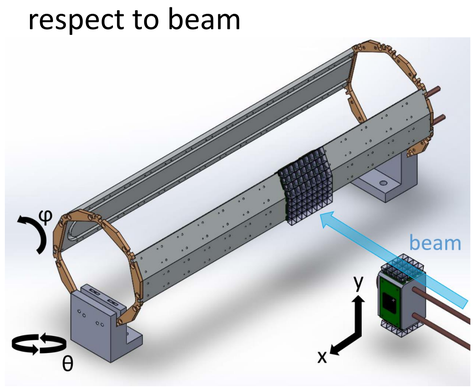
in progress:

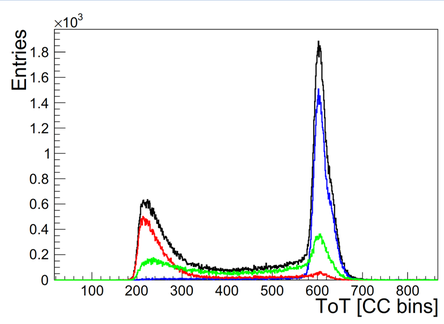
- development of production and assembly line for full detector
  - → FEB equipping in local electronics workshop
  - → dedicated tooling for wrapping and gluing procedures
    - finished prototyping stage
  - → simplified assembly to cooling structure to reduce risks of damage
- development of testing and QA scheme in the laboratory
  - → gluing and assembly within tolerance limits
  - → ASIC functionality
  - → SiPM characteristics

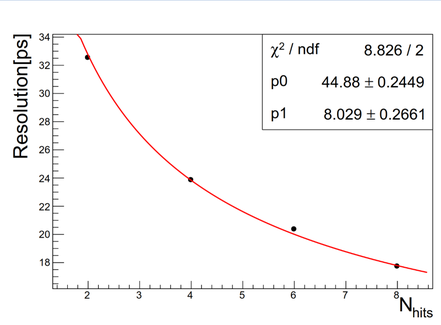


Prototype Measurements at DESY

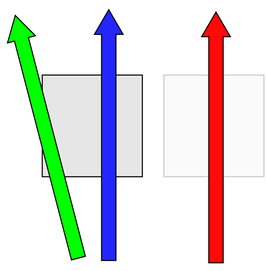
- two testbeam campaigns in February and June 2018 at DESY
- prototype consisting of **three submodules**
  - → one serving as trigger
  - → two devices under test (DUTs)
- moveable in height and angle with respect to beam



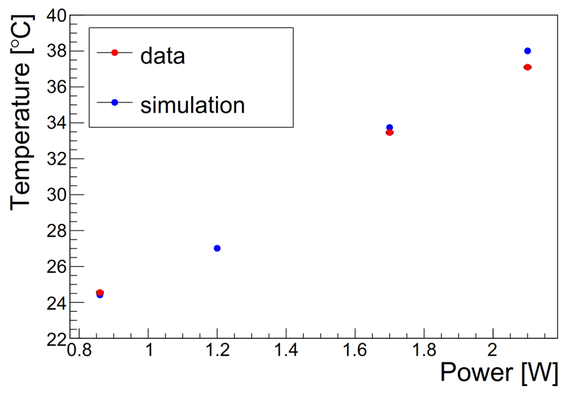




- different contributions to ToT spectrum
  - → blue: particle fully traversing the tile
  - → red: crosstalk
  - → green: particle grazing tile
- excellent timing measurements achieved
  - → single channel resolution at **45 ps**
  - → down to ≈ 18 ps possible for 8 hits per track



Thermal Simulation Studies of the Tile Detector



- implementation of prototype design in CAD software
- finite-element simulation of heat flux to investigate cooling system
  - → ASIC and SiPMs implemented as heat source
  - → water-cooled aluminium support structure
- excellent agreement of simulation with measured data

enhanced simulation:

- 14 ASICs implemented as heat sources (14 x 1.2 W)
- stress test: T_{water} = 1°C, T_{air} = 50°C
  - → chip temperature below 42°C
  - → SiPM PCBs sufficiently cooled