MuTRiG: A Mixed-Mode Silicon Photomultiplier Readout ASIC for Ultra-Fast Timing and Ultra-High Event Rate Applications

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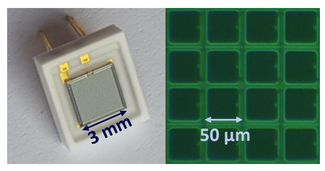
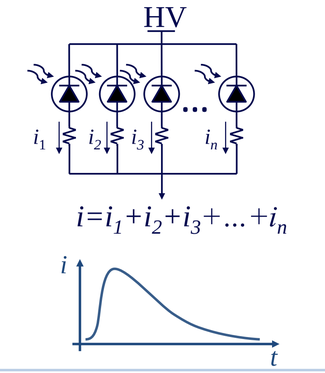
Silicon Photomultiplier





Array of Avalanche Photodiodes in Geiger mode allows for photon counting measurements.

Pros:

- Low timing jitter
- High Gain (~ 10^6)
- Low operating voltage (20 ~ 100 V)
- Compact design
- Insensitive to external magnetic field

Cons:

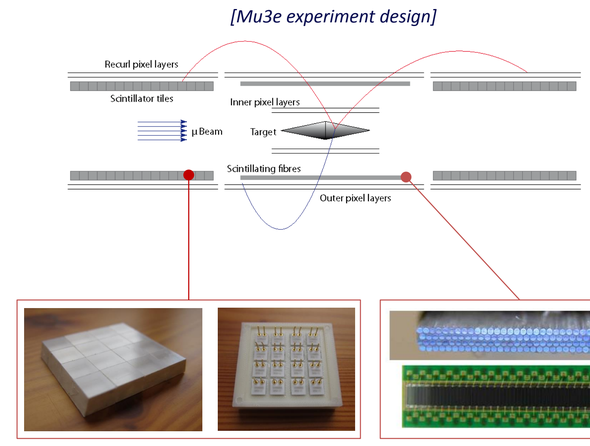
- Temperature dependent
- High Dark Count Rate (DCR)

Motivation

Mu3e experiment

Looking for new physics by searching for $\mu^+ \rightarrow e^+e^+e^-$, which is forbidden in standard model (BR < 10^{-52}).

[Mu3e experiment design]



Challenges on readout electronics:

High timing resolution to reduce the combinatorial background and to facilitate event reconstruction:

- Mu3e Tile detector: 100 ps
- Mu3e Fiber detector: 500 ps

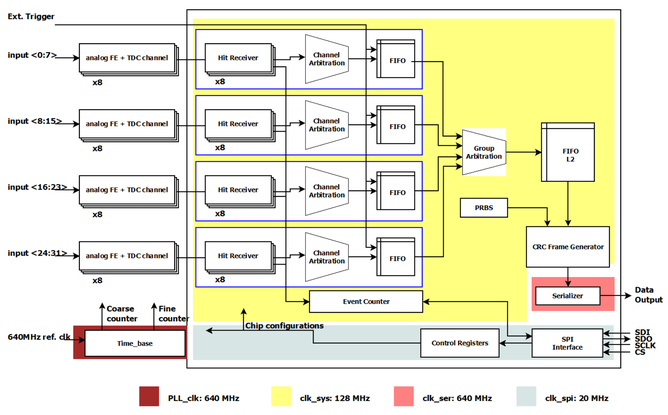
High event rate to collect enough data in reasonable experiment run time:

- Mu3e Fiber detector: 1.3 MHz/channel

[Mu3e tile detectors]

[Mu3e fiber detectors]

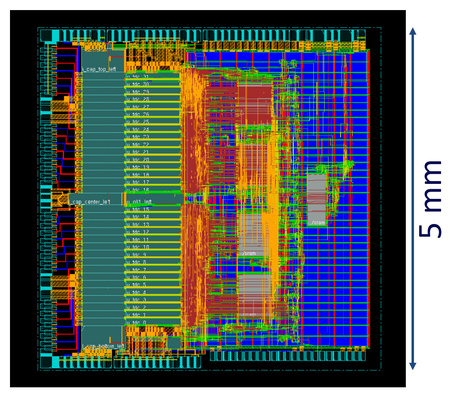
MuTRiG Introduction



[MuTRiG block diagram]

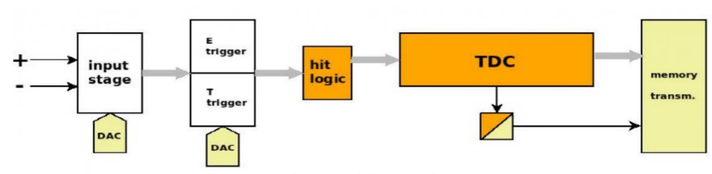
- 32-channel Mixed-Mode ASIC
- UMC 180 nm CMOS technology
- SiPM readout chip with high timing resolution and high data rate
- System On Chip:
  - analog frontend + TDC channel
  - digital part

- External validation in L1_FIFO
- High speed LVDS data link (1.28 Gbps)
- Configurable output event data structure
- CRC for data transmission error detection
- Event counter for event rate monitoring
- SPI slow control for chip configuration
- Prototype submitted in Sep. 2016

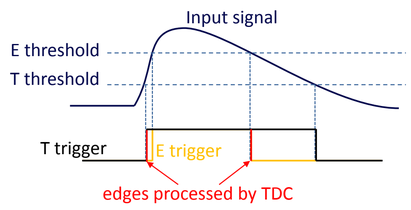


[MuTRiG prototype ASIC]

Analog Frontend and TDC



[Channel diagram]



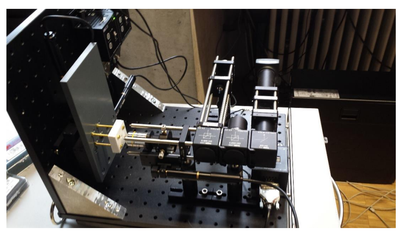
[Threshold principle]

Analog frontend:

- Fully differential structure
- Single-ended or differential connection scheme with SiPM
- Timing threshold and energy threshold triggering
- Linearized Time-over-threshold method for energy measurement
- SiPM bias tuning within ~500 mV
- Jitter < 20 ps for input charge > 300 fC
- Silicon proven in STiCv3[1] submissions

TDC[2]:

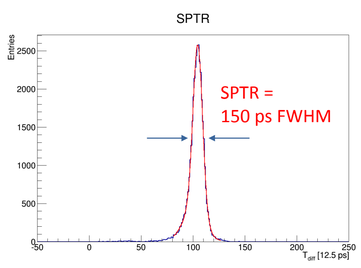
- 16-stage VCO ring locked by PLL to 640 MHz external clock
- 50 ps time binning
- Jitter < 40 ps
- < 0.1 LSB with DNL correction
- Silicon proven[1]



[SPTR measurement setup]

Single Photon Timing Resolution Measurements with STiCv3:

- SiPM: HAMAMATSU MPPC S13360-1350CS
- Picosecond pulse laser with wavelength of 460 nm
- Focused Laser spot on single pixel: < 3 µm
- Single Photon Timing Resolution: ~150 ps FWHM

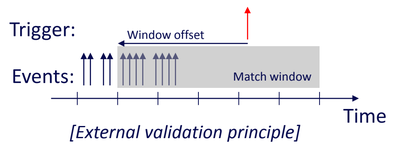


[SPTR measurement result]

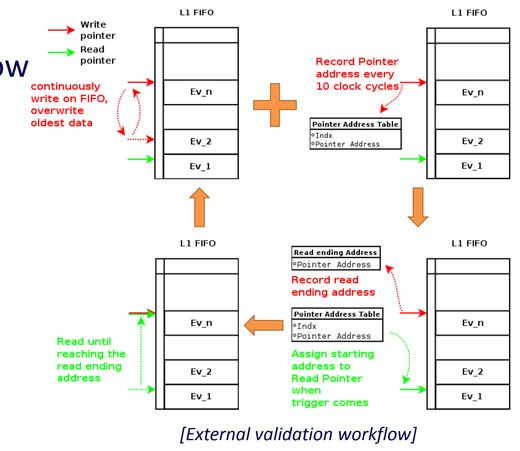
External Validation in L1_FIFO

Reduced load of output data link by only sending event data within matching window of the trigger signal:

- Configurable matching window
- Matching window resolution: 78 ns
- Max. matching window offset: 1.25 µs
- Max. matching window width: 2.5 µs



[External validation principle]

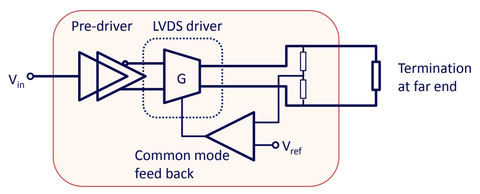


[External validation workflow]

Gigabit LVDS Serial Data Link

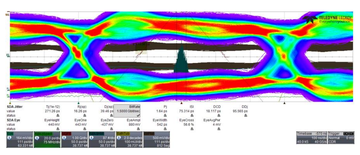
Boosted output data rate with gigabit LVDS transmitter and double data rate serializer:

- Bridge-Switched Current Source LVDS driver
- Common-mode feedback
- Double data rate
- Designed for 1.28 Gpbs



[LVDS transmitter]

- LVDS serial link test chip fabricated in 2015
- Eye diagram of PRBS data with 8b/10b encoding



[Eye diagram @ 1.5Gbps]

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Reference:

1. H. Chen *et al.*, A dedicated readout ASIC for Time-of-Flight Positron Emission Tomography using Silicon Photomultiplier (SiPM), *2014 IEEE Nuclear Science Symposium and Medical Imaging Conference (NSS/MIC)*, Seattle, WA, 2014, pp. 1-5.
2. Peter Fischer et al., Fast self triggered multi channel readout ASIC for time and energy measurement. *IEEE Transaction on Nuclear Science*, 56:1153 1158, 2009. 97.

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DFG Deutsche Forschungsgemeinschaft