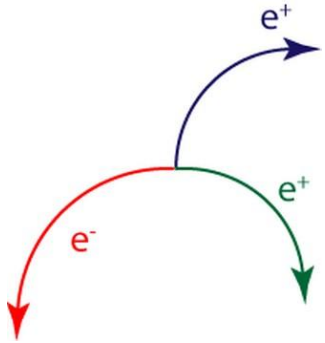
HVMAPS for Mu3e and beyond

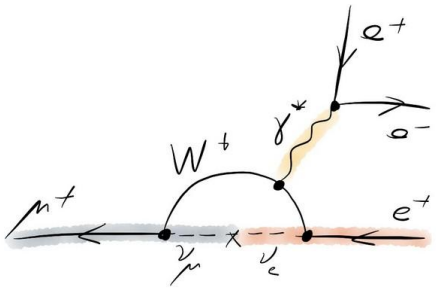
Heiko Augustinfor the Mu3e Collaboration
Physikalisches Institut Heidelberg

Vienna Conference on Instrumentation 2025

19.02.2025

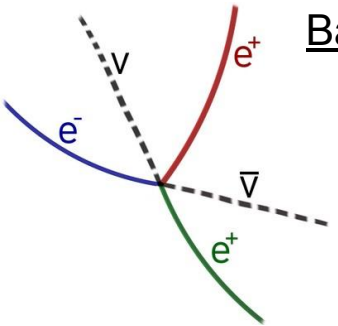
Mu3e: Physics Motivation



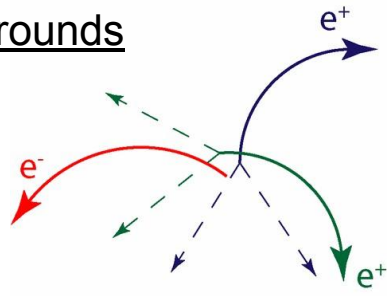


- Search for the cLFV decay **$\mu^+ \rightarrow e^+e^-e^+$** (vSM: BR < 10^{-54})
- Current limit (SINDRUM) BR < 10^{-12} @ 90% CL
- Sensitivity goal (Phase1): 1 in 10^{15} decays
- Up to 10^8 decays per second
- Suppress background below sensitivity level

Backgrounds



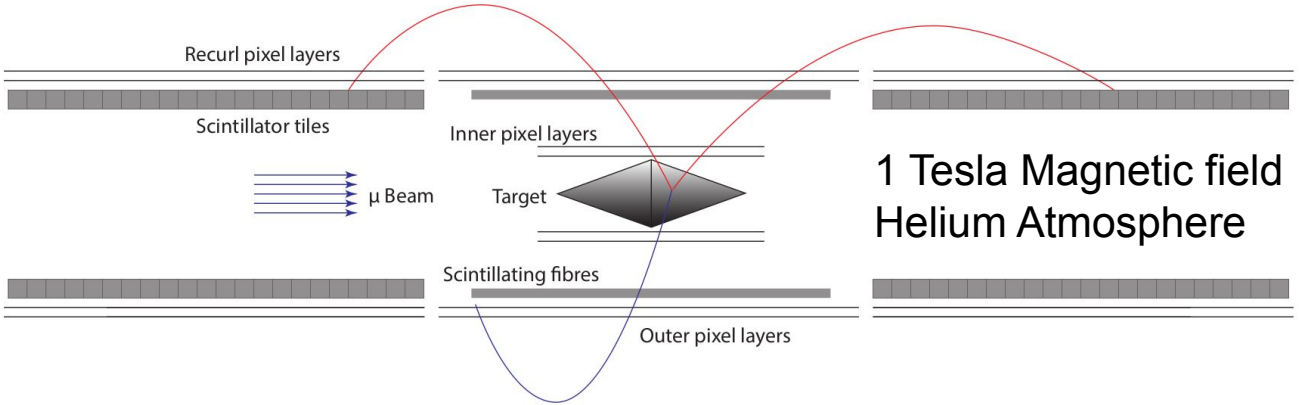
Internal Conversion

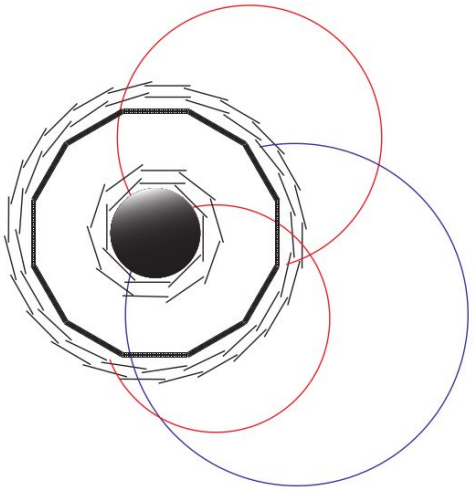


Accidental

More on Mu3e!
Elizaveta Nazarova →Tuesday 18.2.
Sandro Bravar →Thursday 20.2.

The Mu3e Detector





- 10^8 decays per second
- $p_{max} = m_\mu/2 = 53$ MeV
  - ➡ Multiple Coulomb Scattering
  - ➡ Triplet Track Fit
    [arXiv:1606.04990v2]
    [arXiv:2406.05240v2]

- Good vertex and time resolution (100 μm & 500 ps)
- Excellent momentum resolution (0.5 MeV)
- Continuous Beam! No trigger!
  - ➡ Online reconstruction and selection

Helium Gas Cooling
[arXiv:2301.13813], [arXiv:2307.14803]

The Mu3e Detector

Pixel detector requirements:

Pixel Size	Time Resolution	Material Budget	Efficiency
80 x 80 μm^2	< 20 ns	0.1% X_0/layer	> 99 %

Mu3e TDR **[arXiv:2009.11690v3]**

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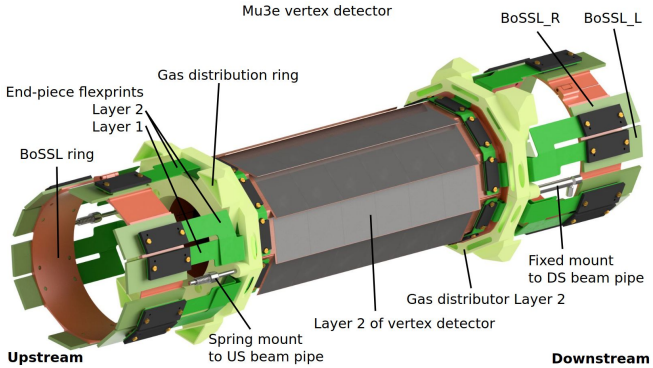
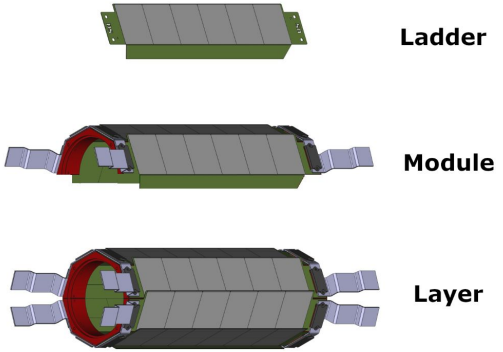
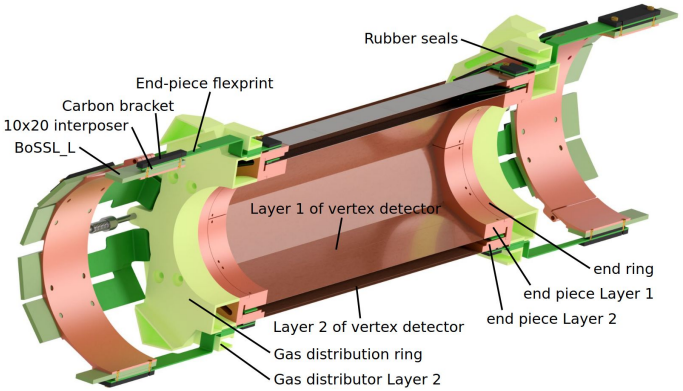
Tracking System - Vertex Detector

Layer 0+1





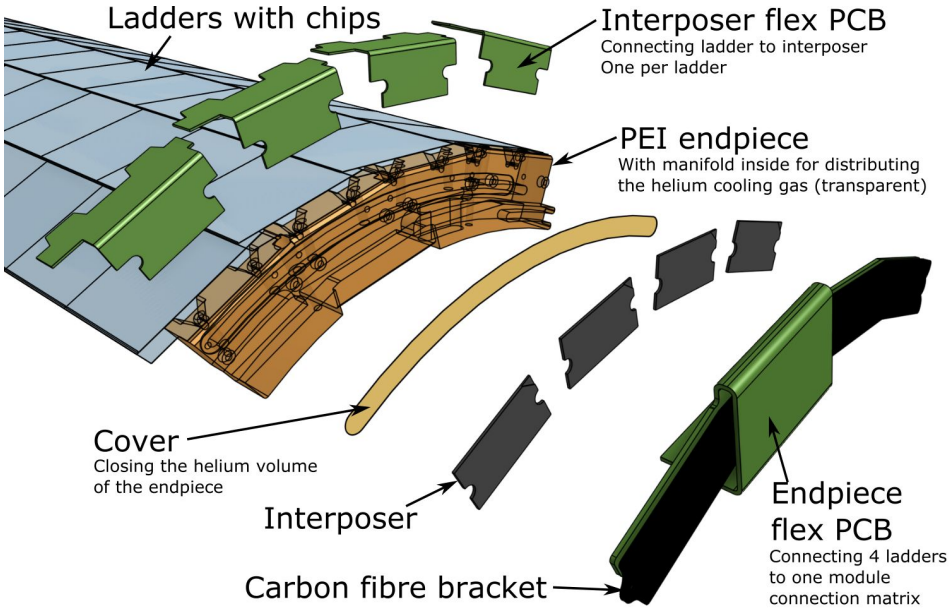


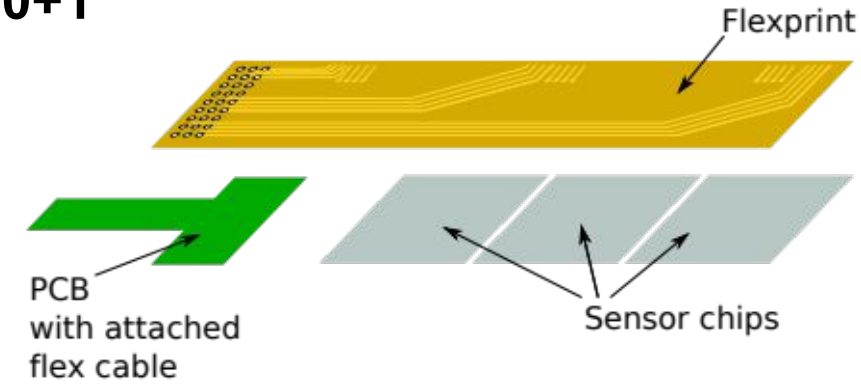
Chips glued and bonded High Density Interconnects (HDIs)

- 6 for layer 0 and 1
- 17/18 for layer 2 and 3
- 50 µm thin
- Connection via interposers (pressed against RO flexes)

Tracking System - Vertex Detector

Layer 0+1





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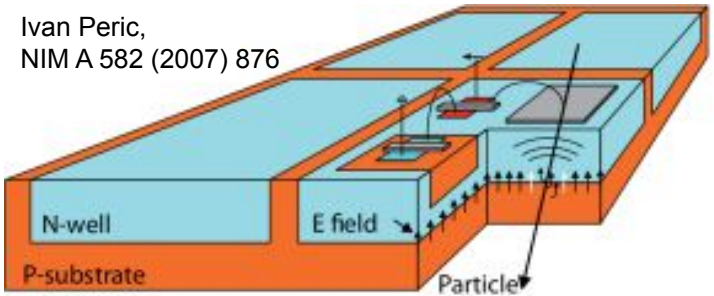
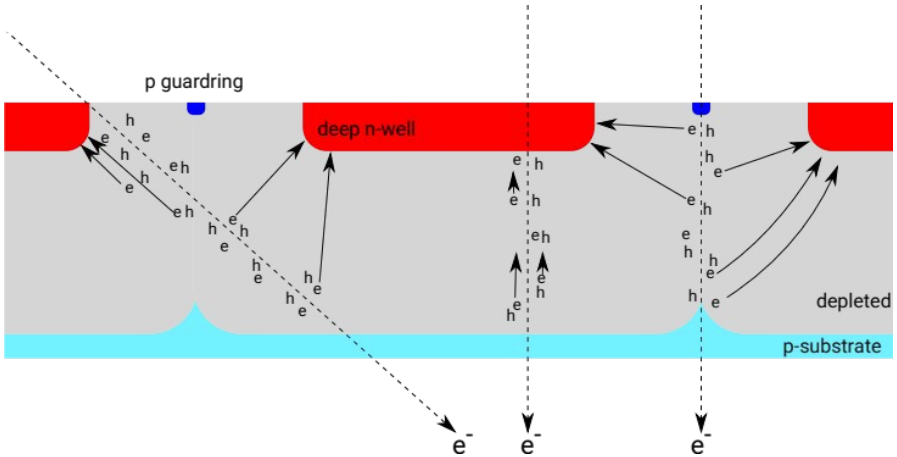
High Voltage - Monolithic Active Pixel Sensors

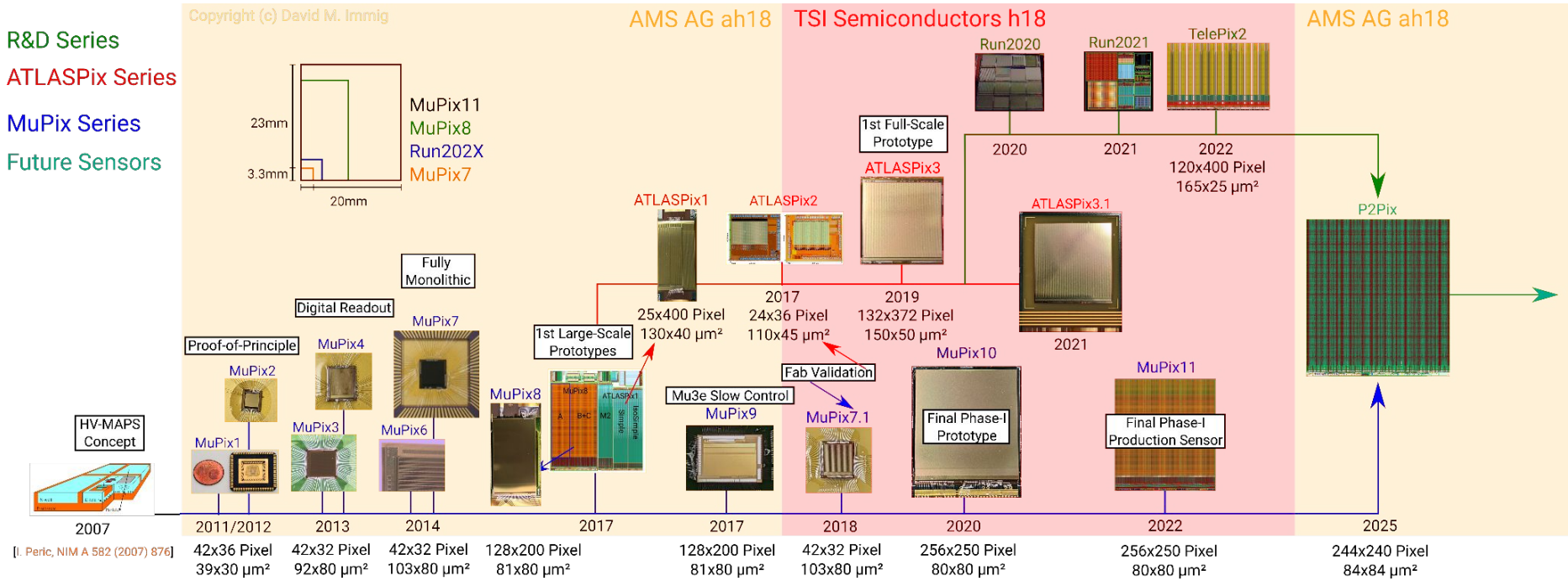


- In-pixel electronics
- Monolithic design: Detection and Readout combined in one chip
- Chips are thinned to 50 µm

- Commercial HV-CMOS processes: TSI 180nm (h18)
- Deep N-well diode (large fill factor)
- Low Ohmic substrates (10-400 Ωcm)
- High voltages up to 100V
- Charge collection via drift

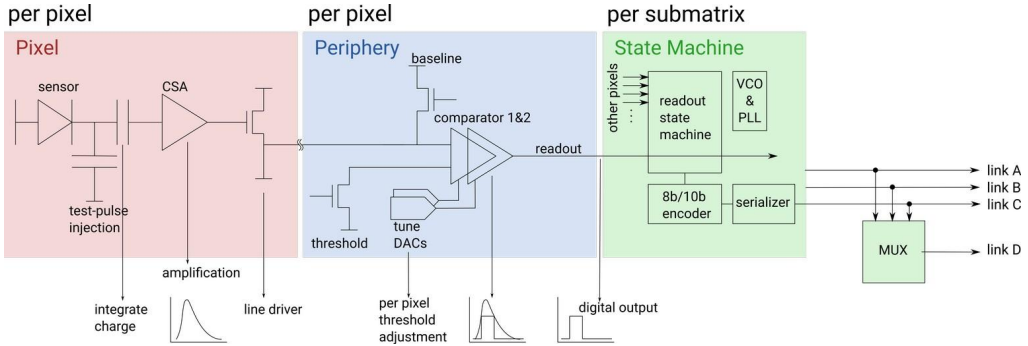


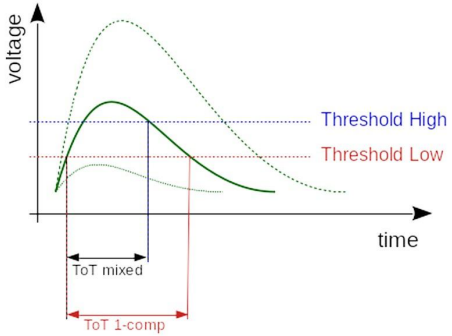
MuPix/HV-MAPS R&D process



The MuPix Sensor

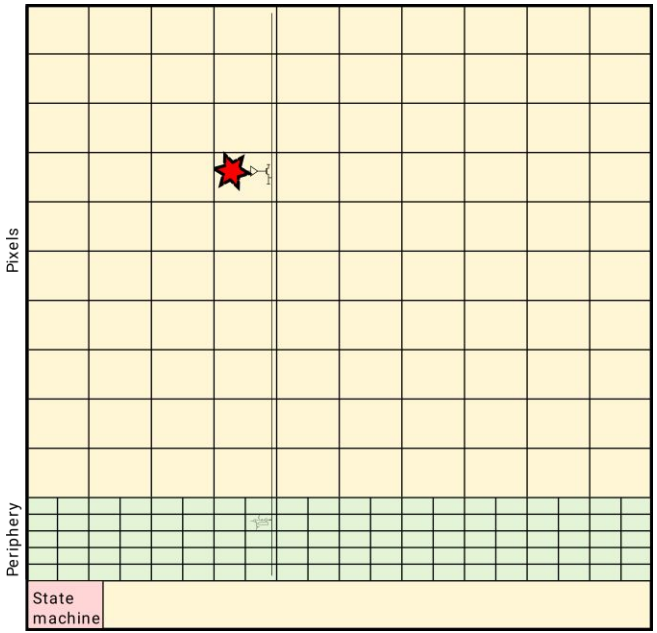
MuPix Architecture





- Clear separation of analog and digital electronics
- 2 comparator design
- Tuning/Trimming and masking available
- Priority encoder / column-drain readout
- Chip sub-divided into 3 matrices → 1 Data link each + 1 multiplexed link

The MuPix Principle



Courtesy: Frank Meier

- Deposited charge amplified by in-pixel amplifier
- Source follower drives the signal to the periphery
- Digitisation in periphery
- Timestamp sampling
- Readout statemachine manages column-drain readout
- Data is send out via a 1.25 Gbit/s differential link

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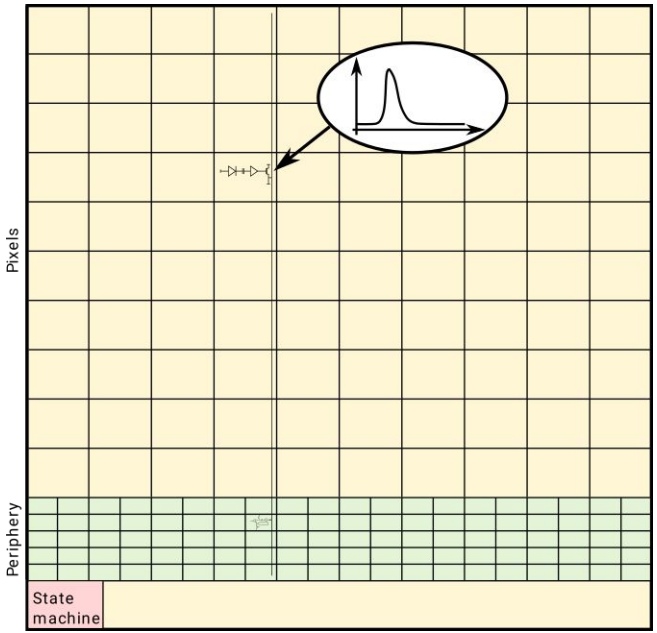

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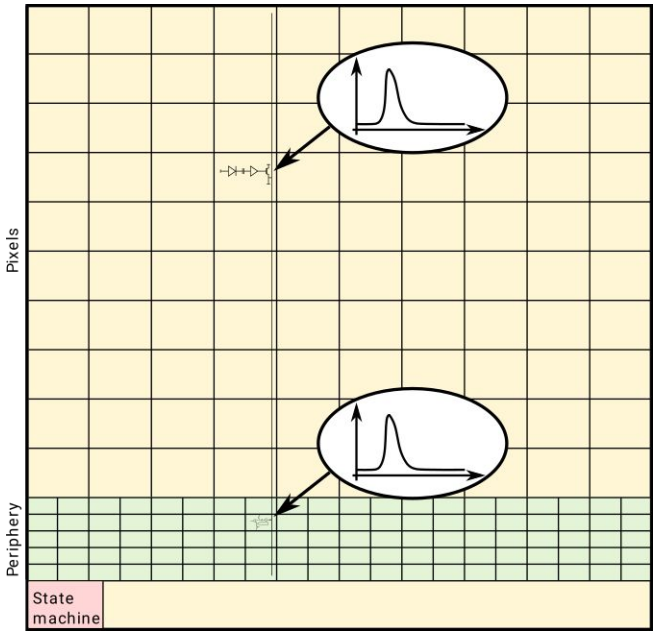

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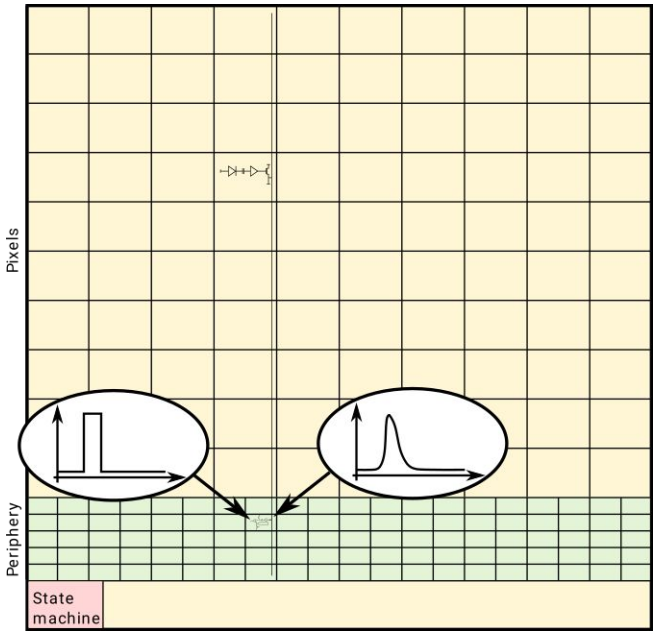

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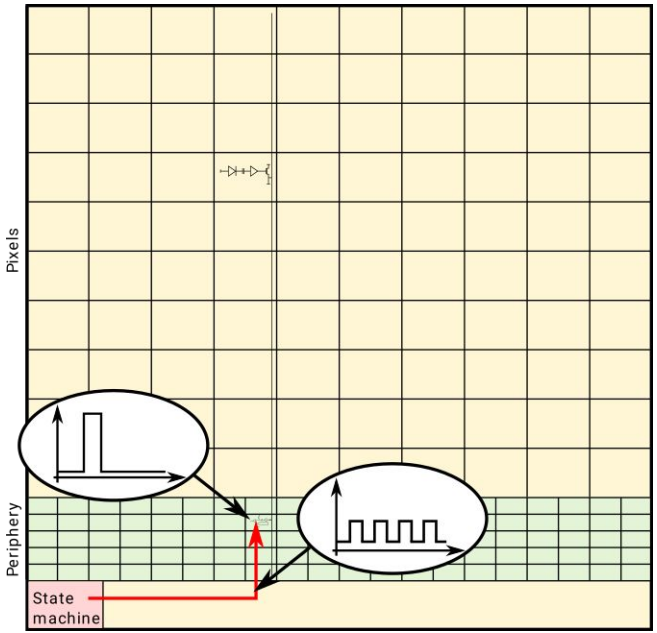

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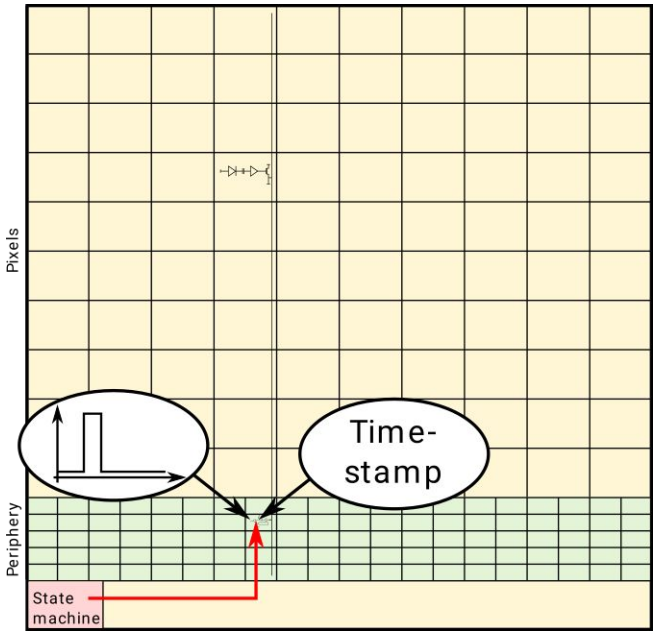

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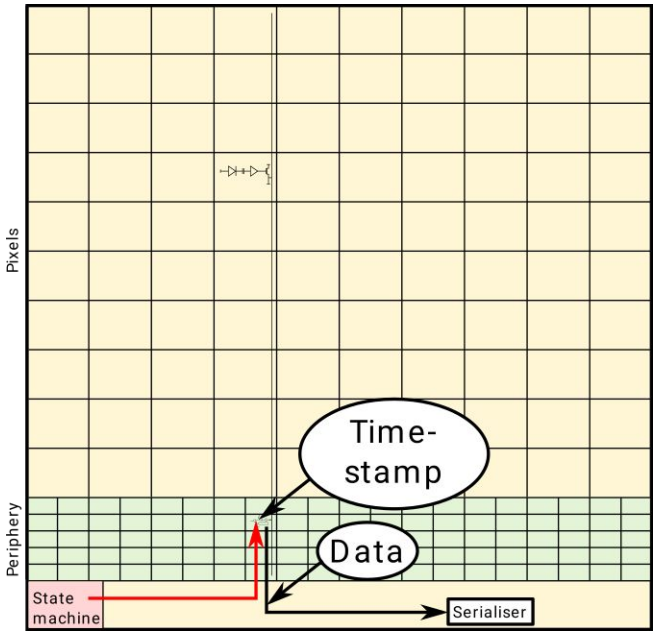

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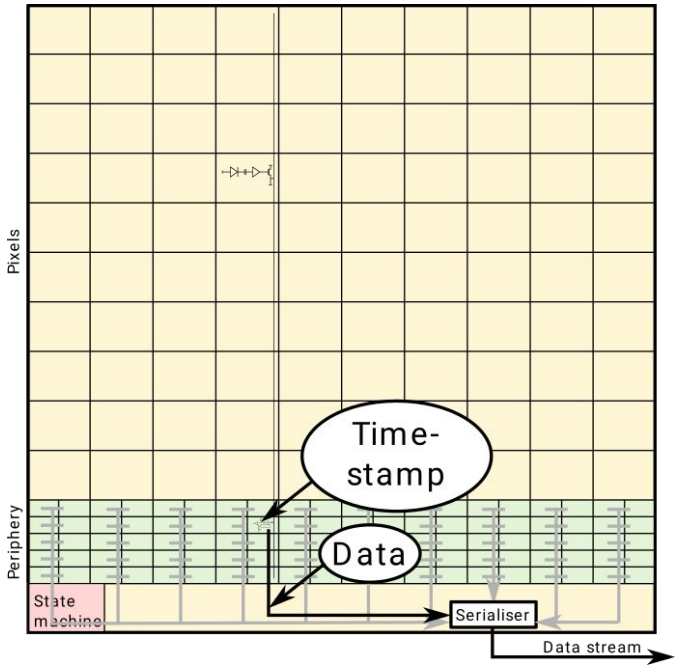

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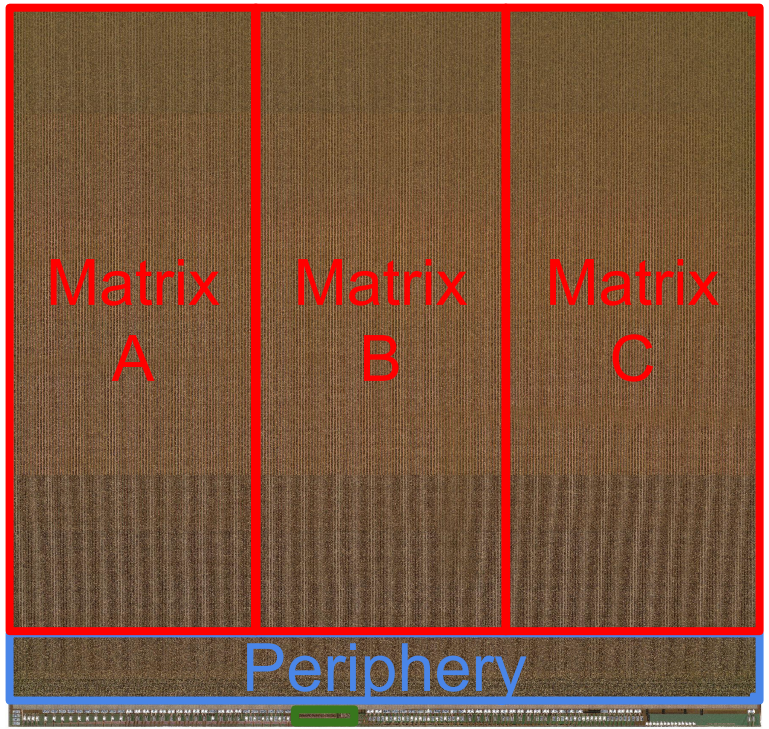
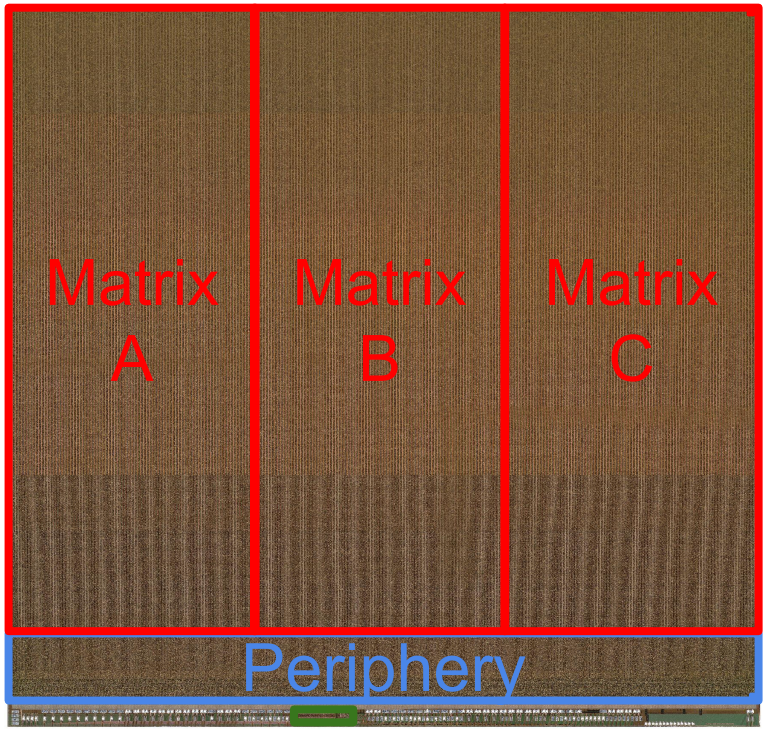
MuPix10 & MuPix11



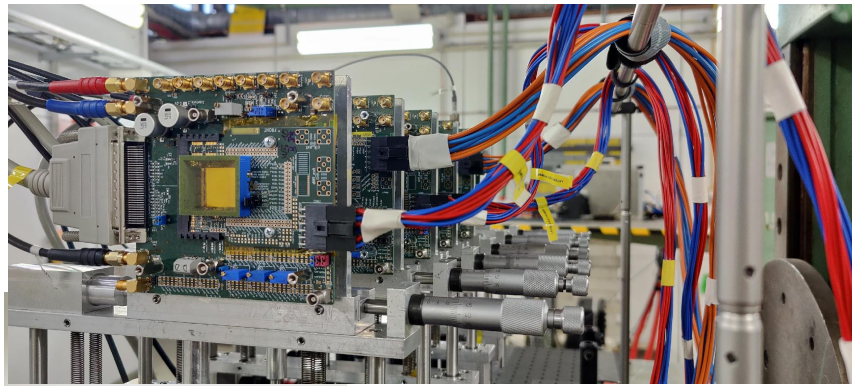
Pixel size [µm²]	80 x 80
Sensor size [mm²]	20.66 x 23.18
Active size [mm²]	20.48 x 20.0
Pixel matrix	256 x 250
Thickness [µm]	**50, 70**
Substrate [Ωcm]	80, 370
Data links	**3+1**
Data speed [Gbit/s]	1.25
Time-of-arrival [bits]	11
ToT [bits]	5
TS binning [ns]	8 (option for 1.6)

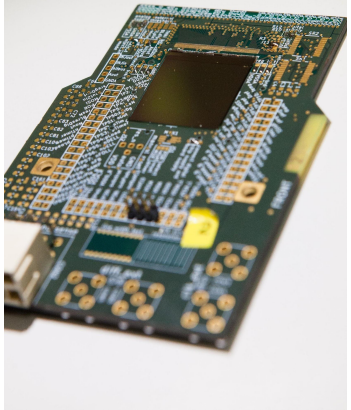
From MuPix10 to MuPix11



- Removal of R&D features
  - ➡ More pads for powering
- Improvement of powering grid
  - ➡ Less on-chip voltage drop
- Buffering of data lines
  - ➡ Full speed readout
    30 MHits/s per sub-matrix
- Re-synthesis of State machine
  - ➡ Fast configuration interface available
- Re-done pixel point-to-point connection
  - ➡ Reduced delays and parasitic couplings

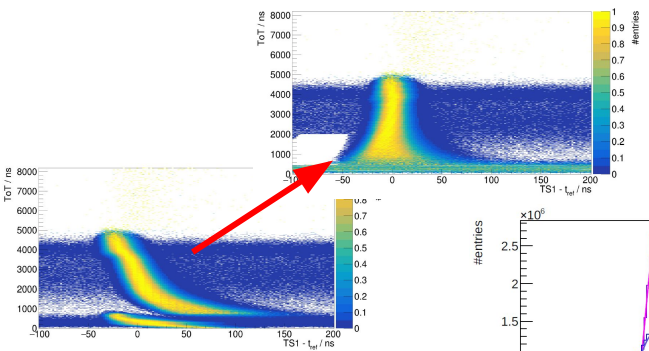
Sensor Characterisation



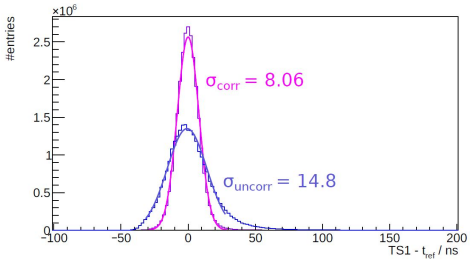


- Lab commissioning
- Lab optimisation:
  Radioactive sources: ^{55}Fe, ^{90}Sr
  Time coincidence
- Testbeam Campaigns:
  DESYII (Hamburg, GER)
  MAMI (Mainz, GER)
  PSI piM1 (Villigen, CH)
- MuPix-Telescope
- Mimosa/Alpide-Telescopes

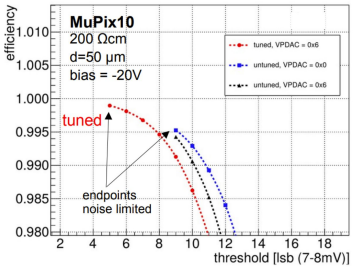
Summary - Results MuPix10

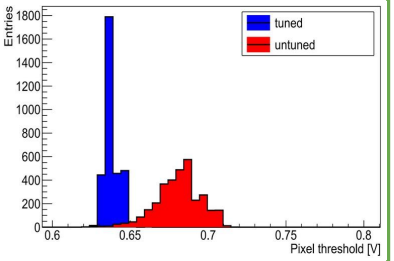


MuPix10
100µm 370Ωcm

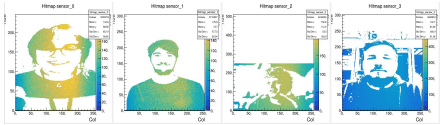


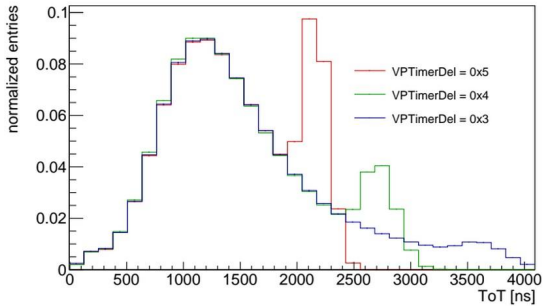
Timing Correction





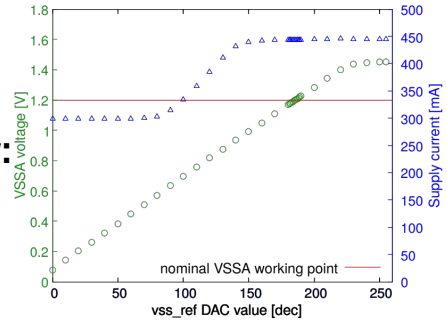
Tuning/Trimming Masking





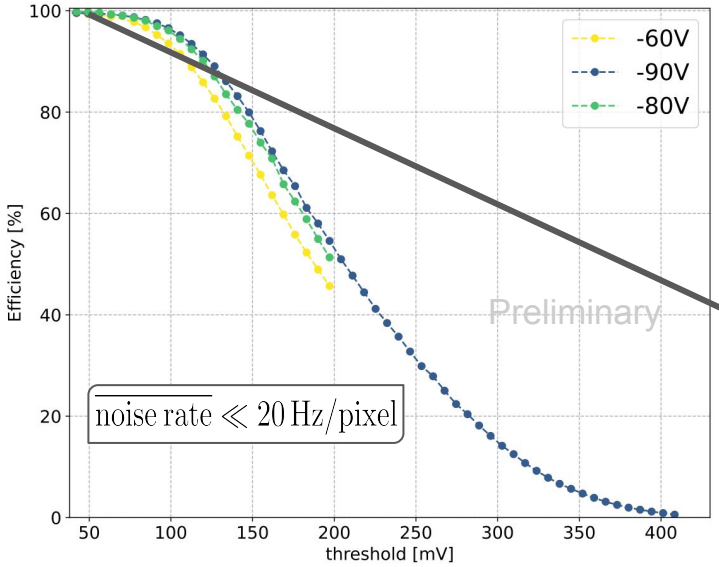
Hit readout delay: Hit Chronology

Voltage Regulator: Single Supply

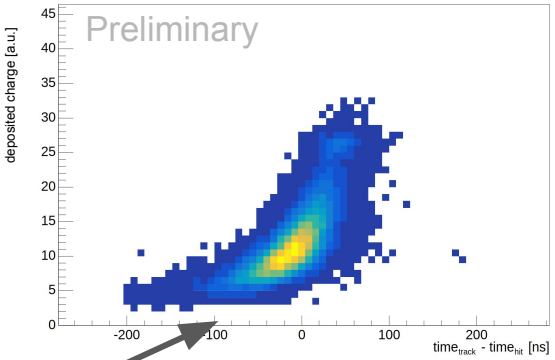


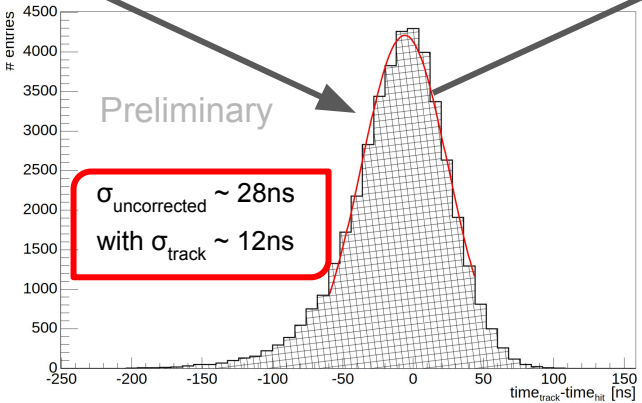
[arXiv:2012.05868] & 10.7566/JPSCP.42.011020

MuPix11 - 50 µm - 80Ωcm (Vertex detector)



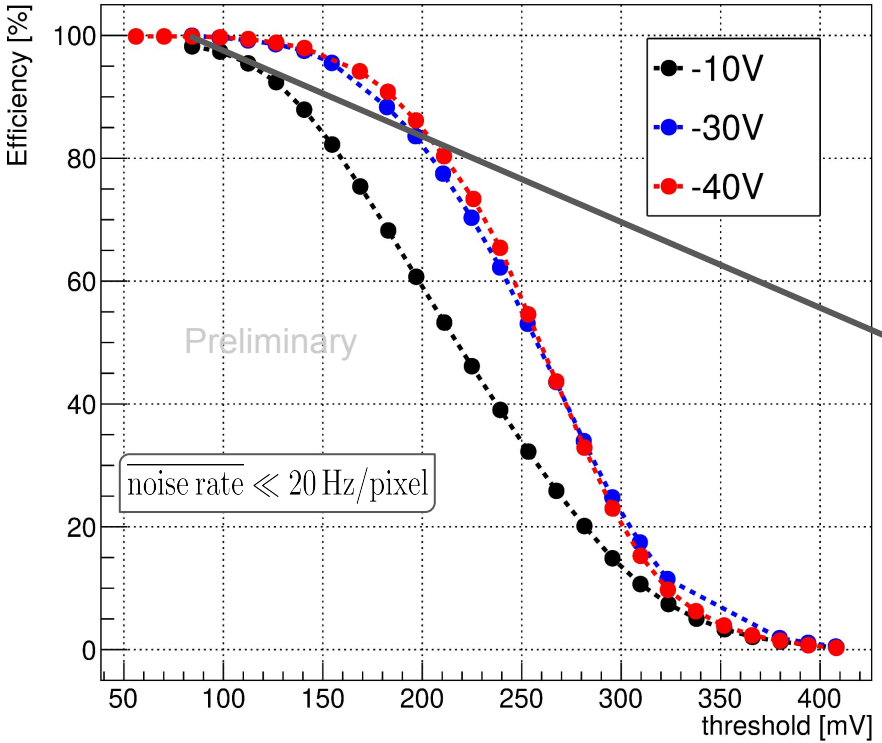
Raw time resolution
for 50µm @ -80V



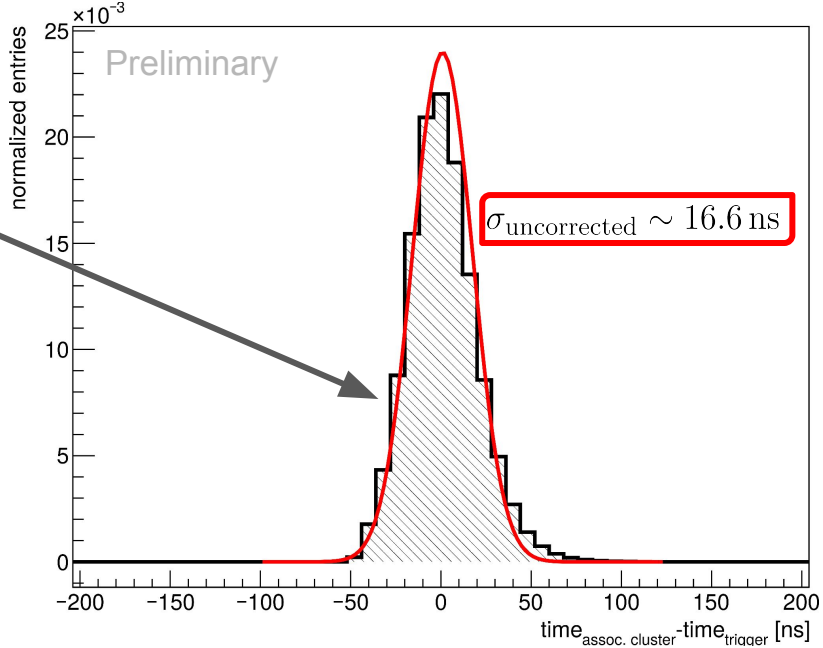


Time walk correction will enable
substantial improvement!

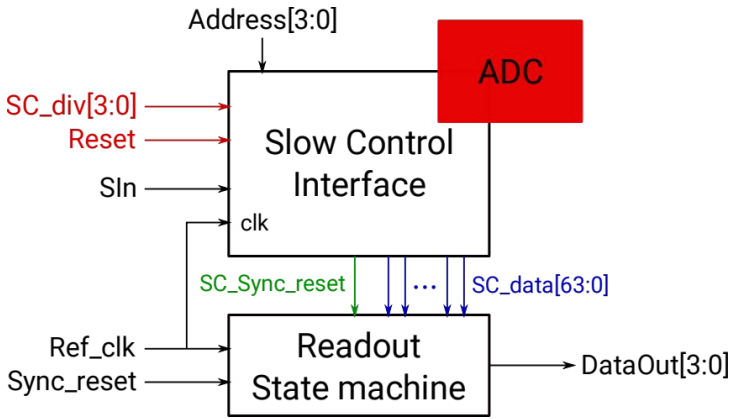
MuPix11 - 70 µm - 370Ωcm (Outerlayers)



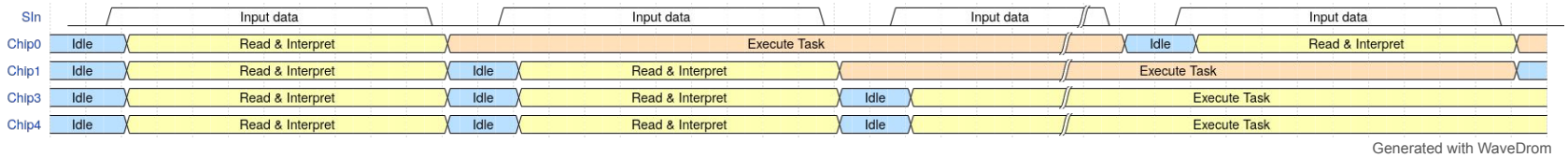
Raw time resolution for 70µm @ -30V



MuPix Fast Configuration Interface



- Chips of a ladder share a bus of clock, synchronous reset and configuration input
- Custom configuration protocol
- Commands interleavable
- **~400ms configuration time** for 9 chip ladder
  ⇒ Configuring the ladder is not a bottleneck
- On-going development for future use



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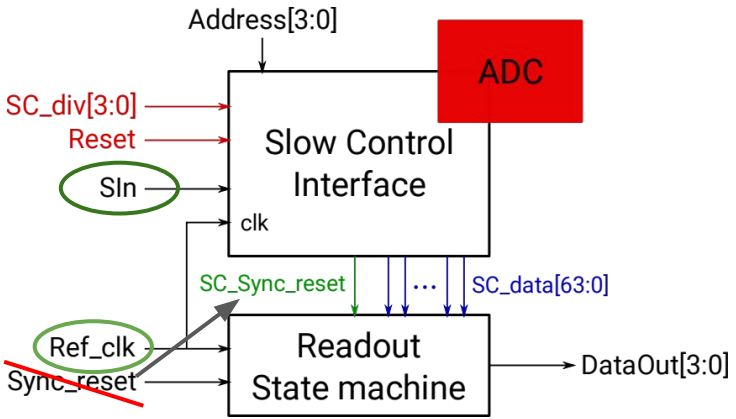

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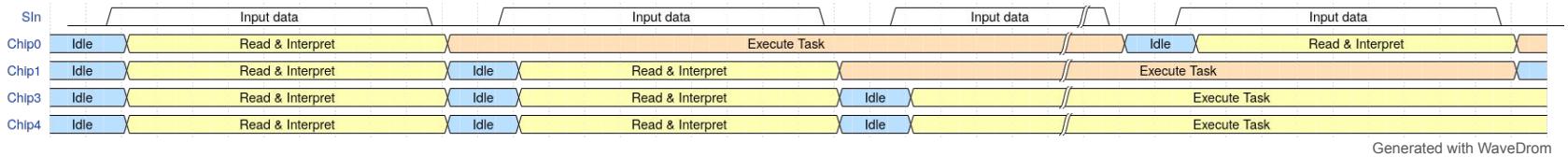

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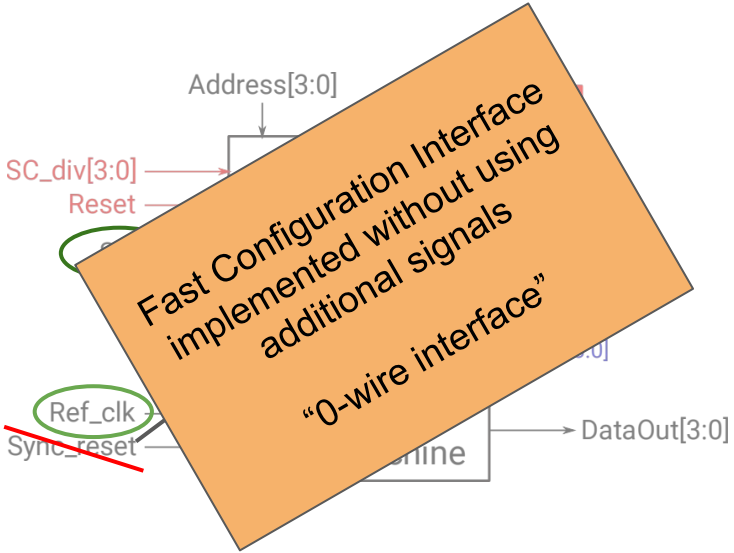

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  ⇒ Configuring the ladder is not a bottleneck
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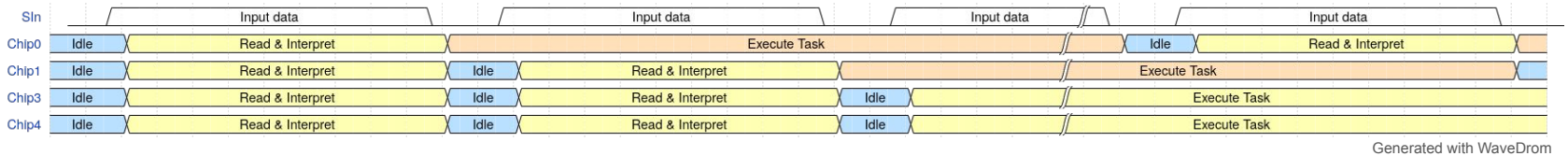
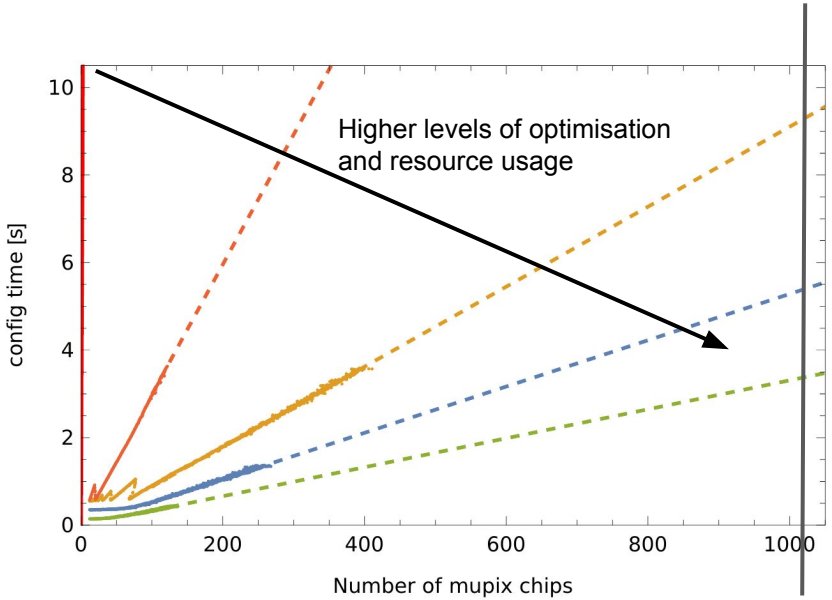
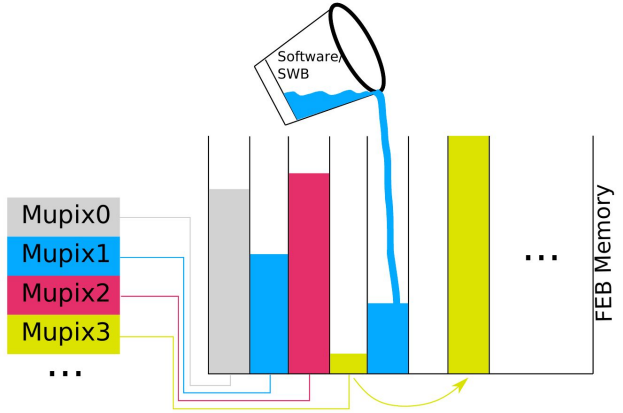


Configuring the Mu3e Central Pixel detector

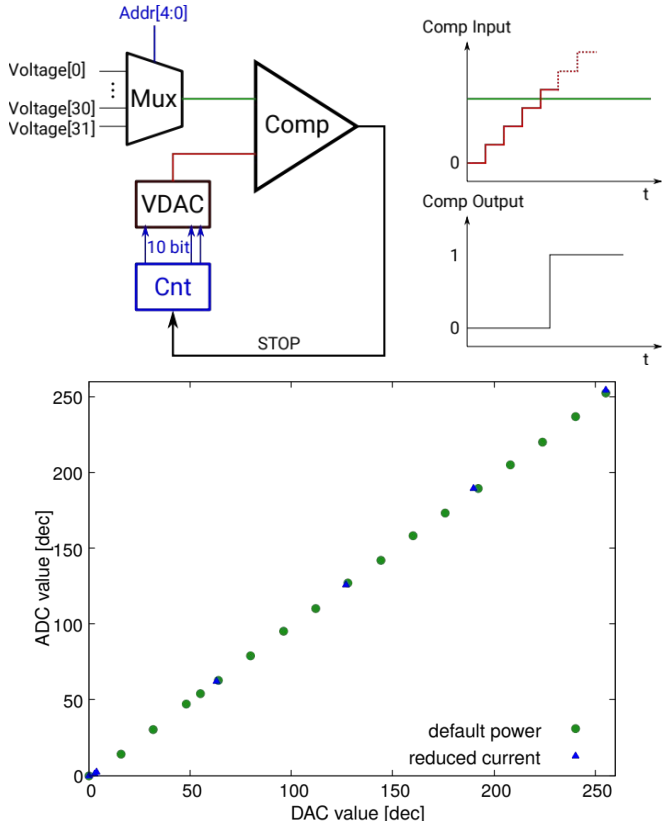


[Martin Müller, PhD Thesis, KPH Mainz]

- The bottleneck is to get the data to the chip
- Firmware optimisation towards data preparation
- **Detector** currently configurable **< 4s** (emulated detector)

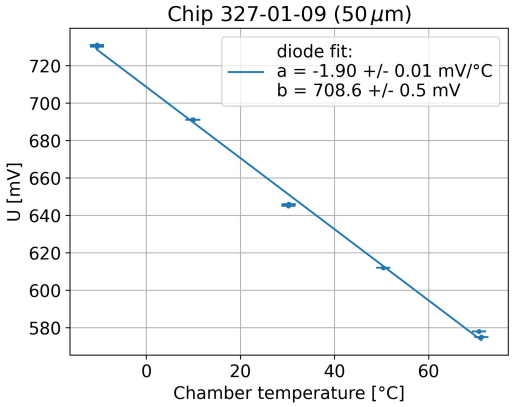


On-chip ADC

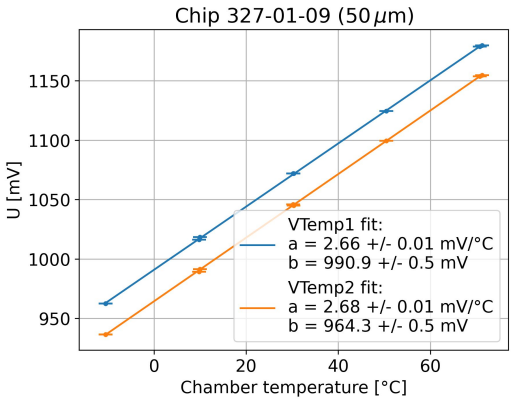


- ADC programmable through Mu3e configuration interface
- Allows measurement of on-chip voltages
- Data send out via 1.25 Gbit/s data links
- ADC shows a good linearity

On-Chip Temperature Measurement

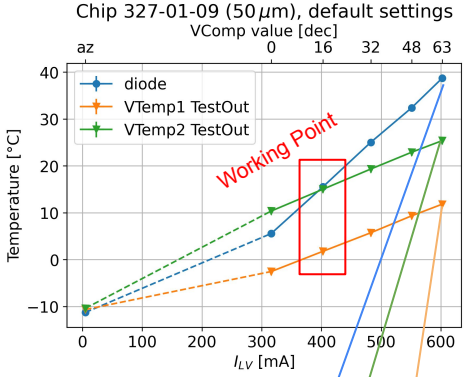


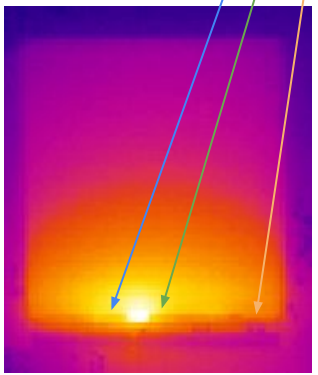
Simple PN-**Diode**
(Shockley)

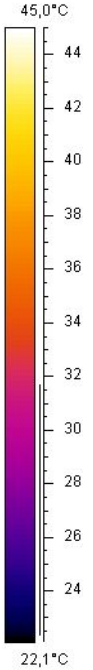


Temperature sensitive circuit
(Read out via ADC)

Gauging

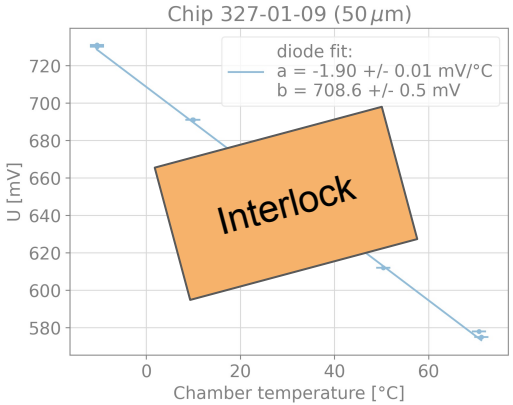


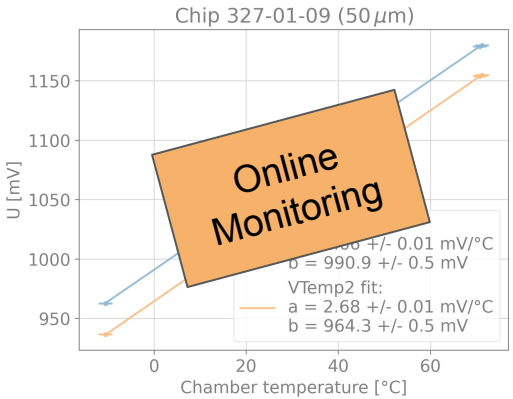




➡ Full detector temperature monitoring

On-Chip Temperature Measurement





Simple PN-**Diode**
(Shockley)

Temperature sensitive circuit
(Read out via ADC)

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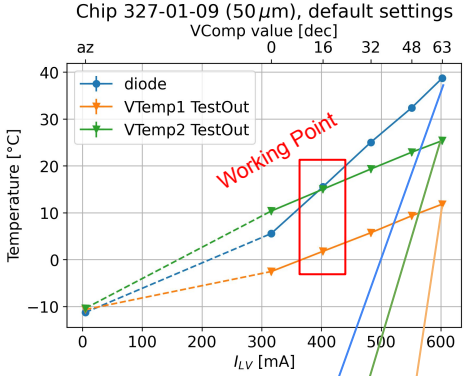
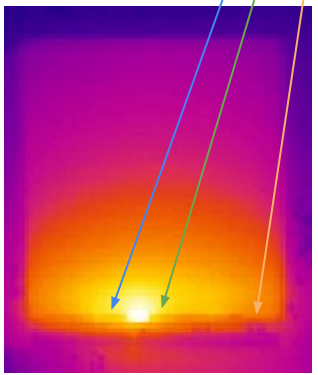
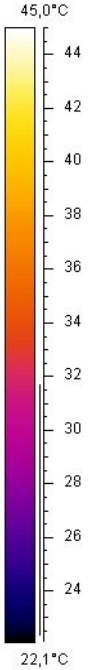






➡ Full detector temperature monitoring

Vertex Detector Status

Photos from Thomas

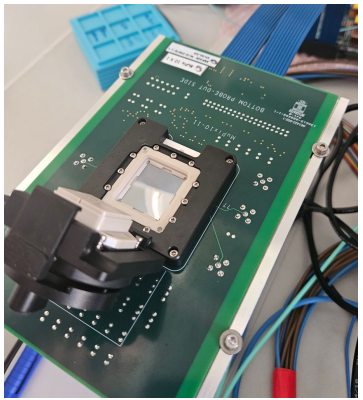
Outlook - Future of HVMAPS

TelePix2, P2Pix, explore new foundries, Conditions Mu3e Phase

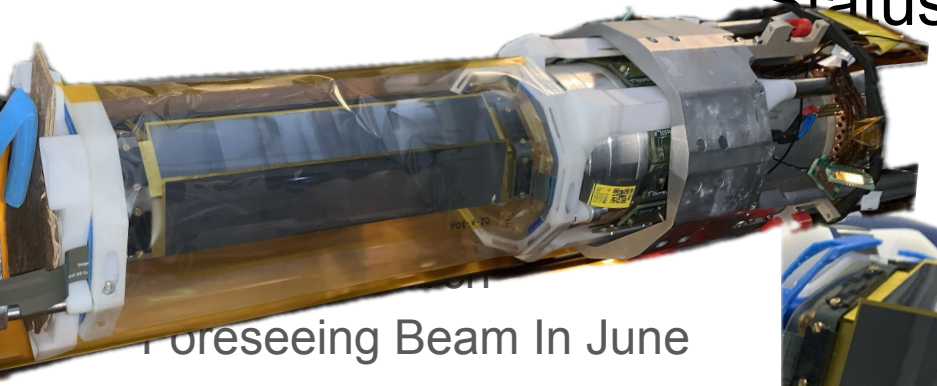
MuPix11 a sensor of

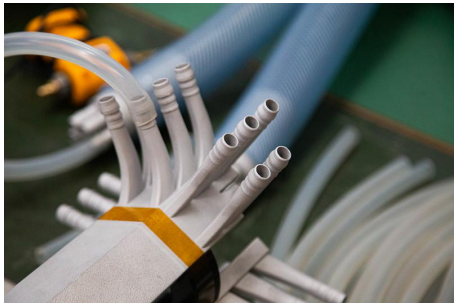
Stuff from luigis review poster

Mu3e ~ 150 Wafers

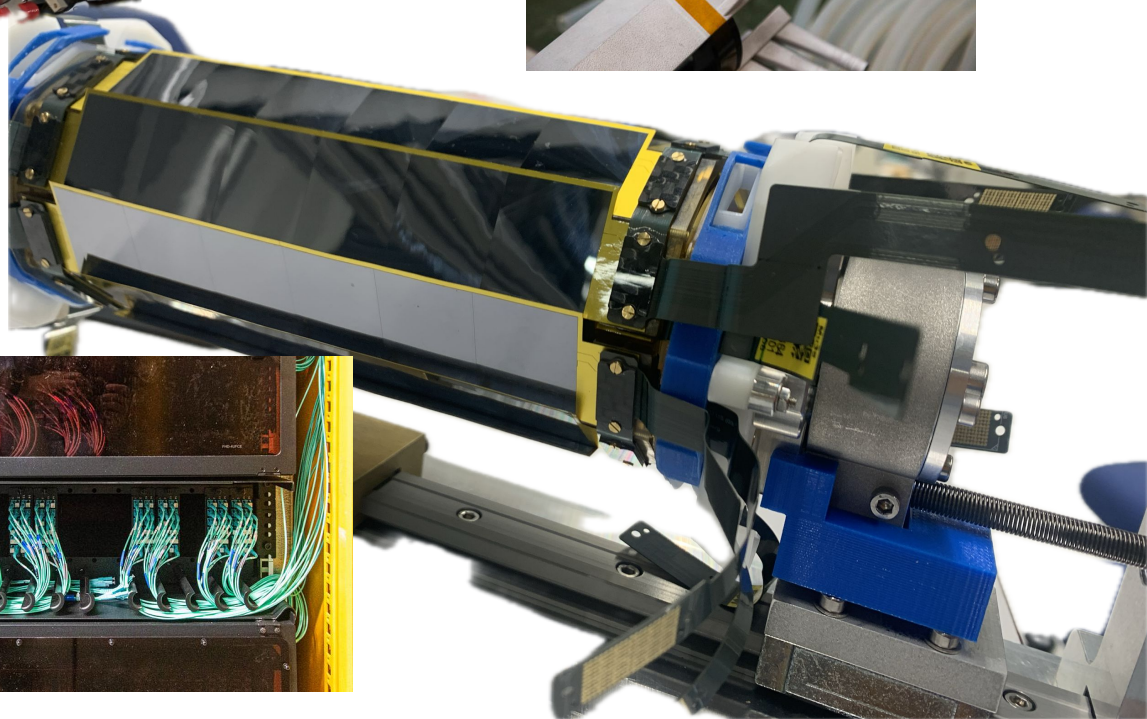


Status Vertex

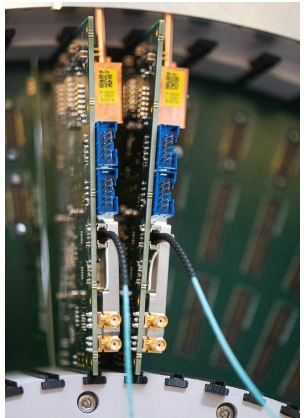


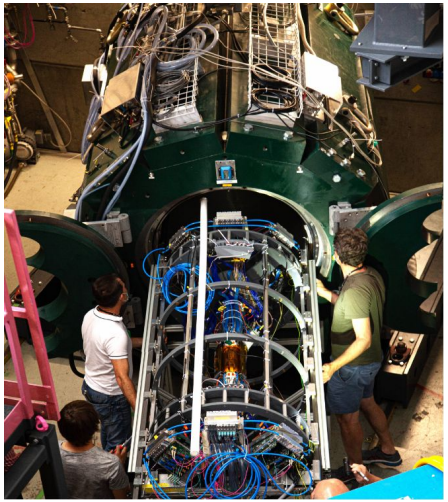


Foreseeing Beam In June

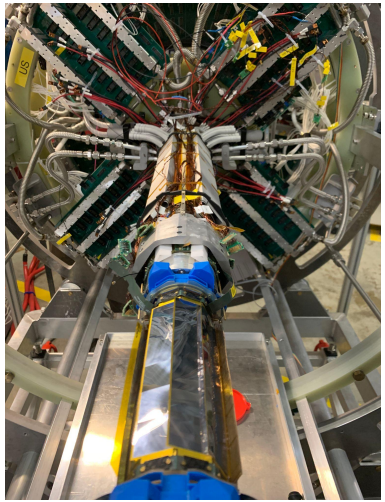


Ladders in beam plot?





Experiment-Insertion
into the Mu3e Magnet



First Installation of the Mu3e Vertex Detector (December 2024)

Re-Roadmap

Moeller, P2, Panda, MuSR [MKref], Telescope-Maintenance

→ P2Pix

→ MightyPix

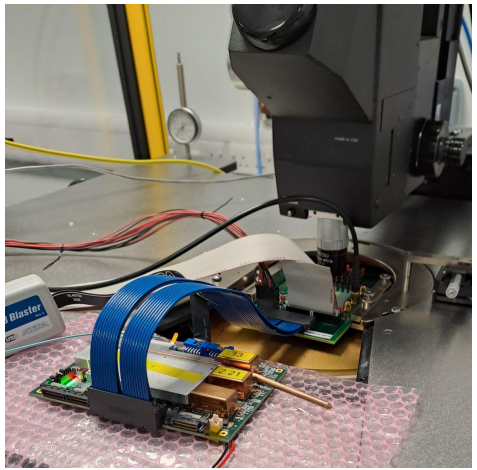
→ Mu3e Phase 2

Types

Xfab

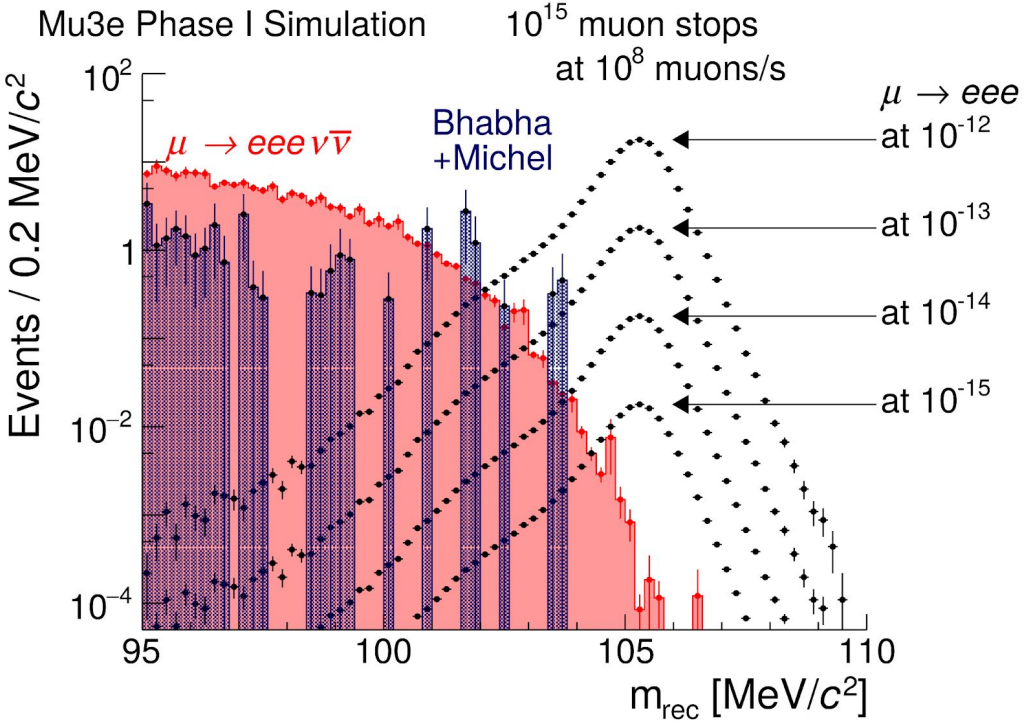
Summary & Outlook

- Successful transition from MuPix10 to MuPix11
  - Everything functional, expected to fulfill Mu3e requirements
- QC procedures have been developed and implemented
  - First successful test of needle card for large volume testing
- Production of Vertex ladders started
  - First in-beam test still this week
  - Full vertex detector expected in Spring
- First ladders of outer pixel layers expected in Spring
- Start with detector commissioning next year



Backup

Experimental sensitivity



Invariant mass of signal decay, radiative decay and accidental background (Bhabha+Michel)

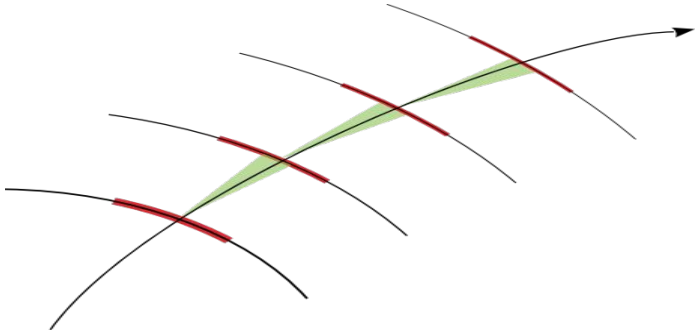
Momentum resolution crucial for detecting the peak at muon mass…

Material budget is key factor!

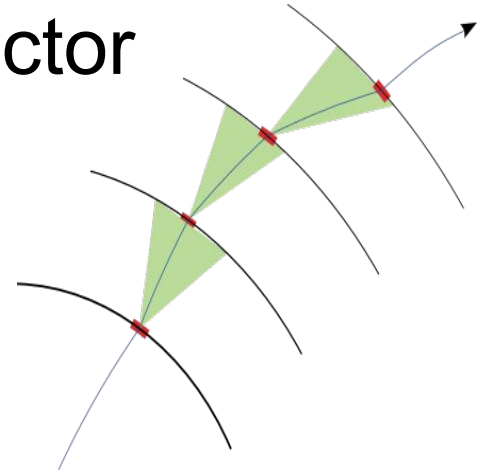
1 MeV resolution with 0.1% * X/X_0 per layer

Mu3e TDR at *Nucl.Instrum.Meth.A* 1014, 165679

The Mu3e Detector



Spatial resolution dominates

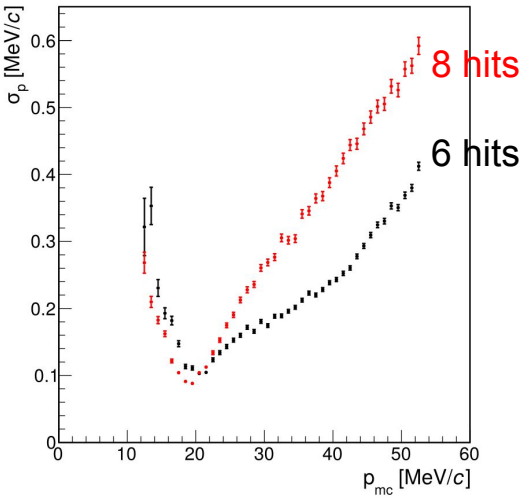


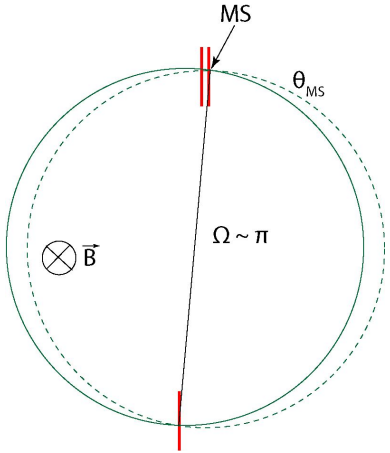
Scattering dominates

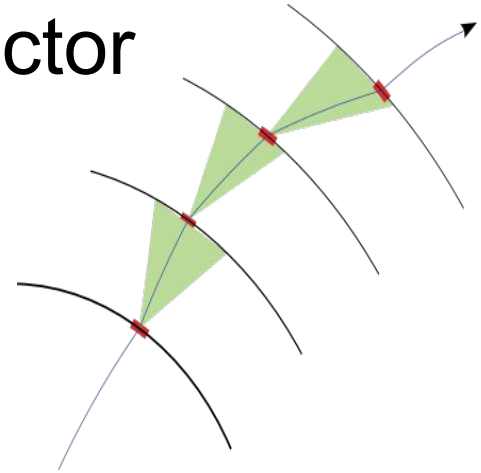
- 10^8 decays per second
- $p_{max} = m_\mu/2 = 53$ MeV
  - ➡ Multiple Coulomb Scattering
  - ➡ Triplet Fit **[arXiv:1606.04990v2]**

- Good vertex and time resolution (100 µm & 500 ps)
- Good momentum resolution (0.5 MeV)
- Continuous Beam! No trigger!
  - ➡ Online reconstruction and selection

The Mu3e Detector







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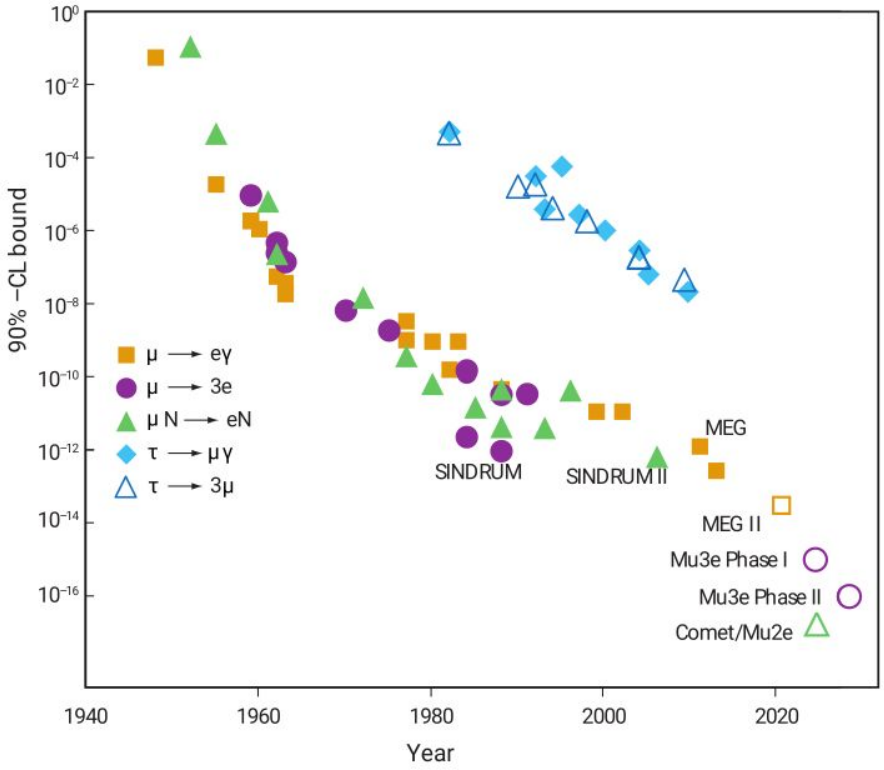
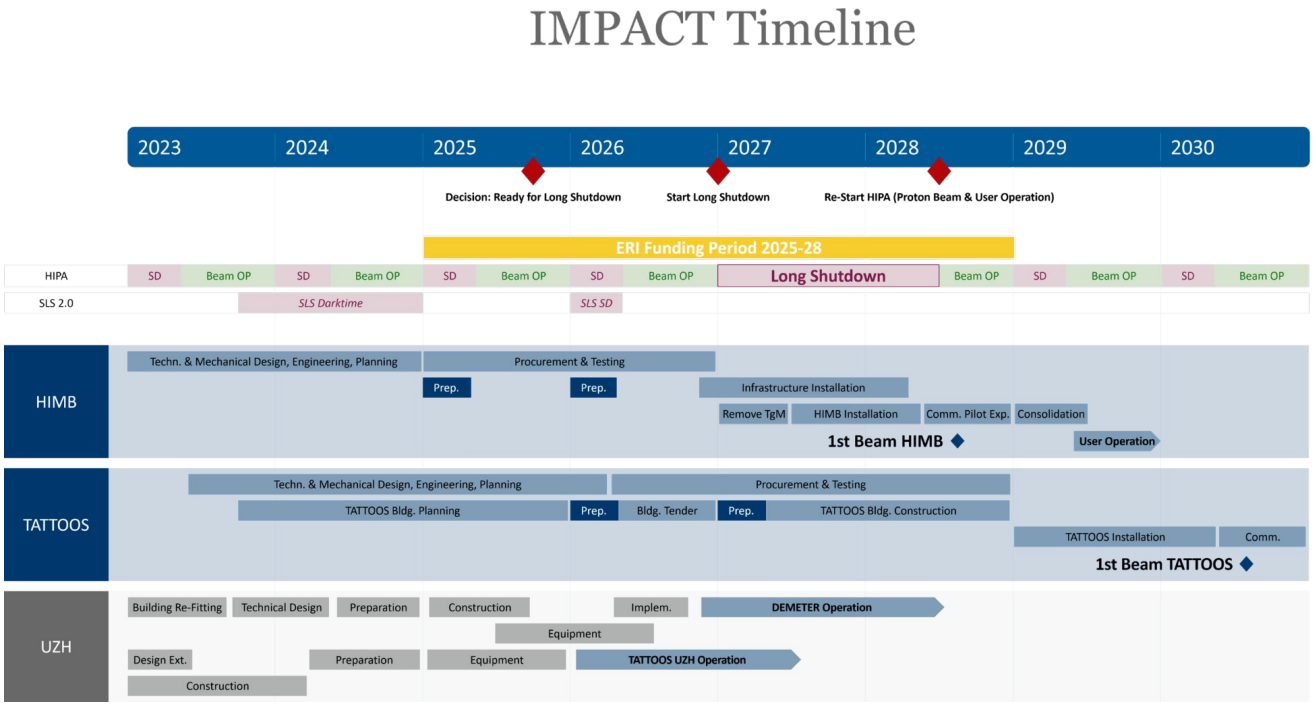
cLFV - Landscape

updated?

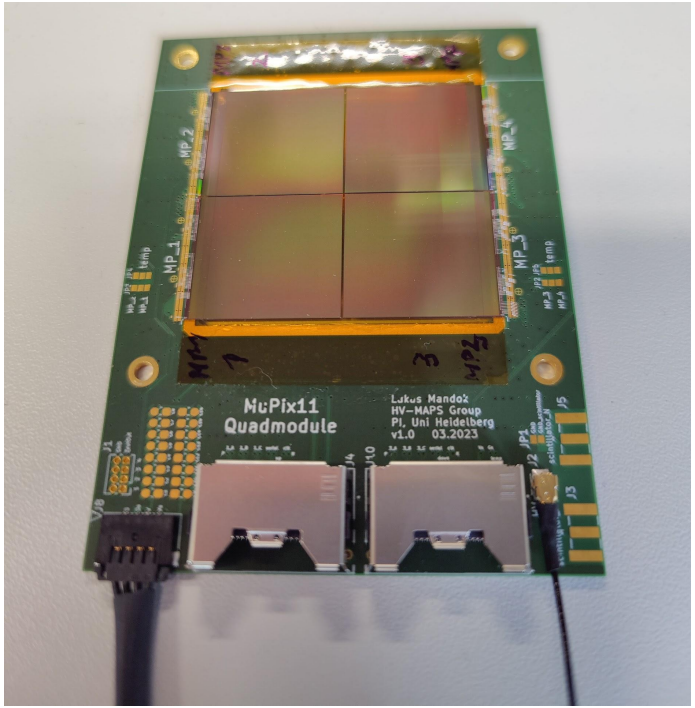


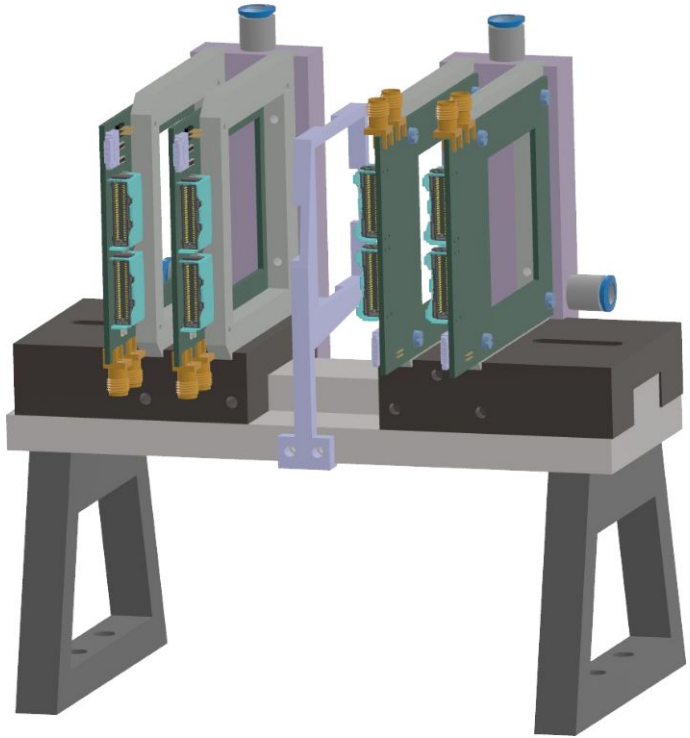
PSI - Beamline Upgrades

updated



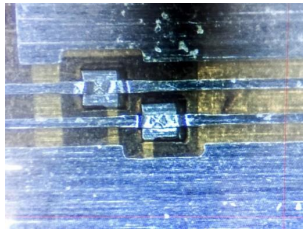
Quad - Module Telescope





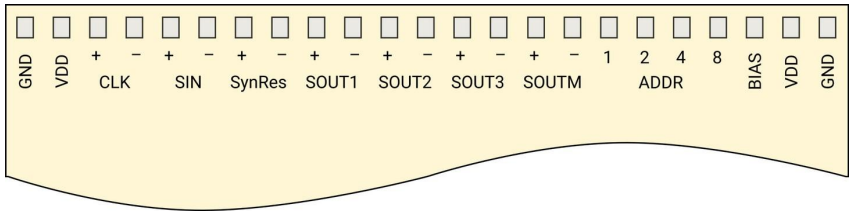
A MuPix Module

- Chips glued and SpTAB-bonded to flexprint
- No additional components!
- 1.15‰ X_0 per layer
- Minimize dead space between the chips
- Only 11 µm dead silicon outside the guardring
- Power consumption limited to 400 mW/cm² (Sensors+Flex)

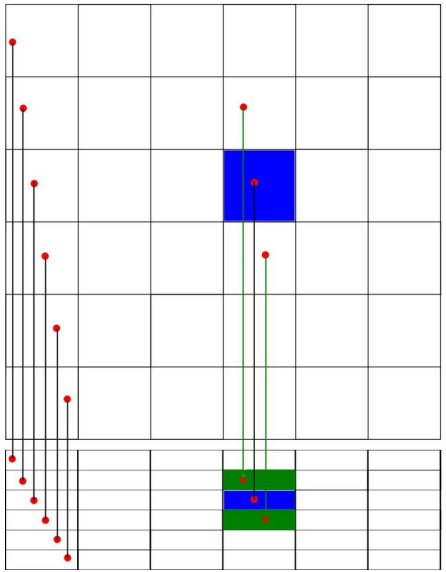


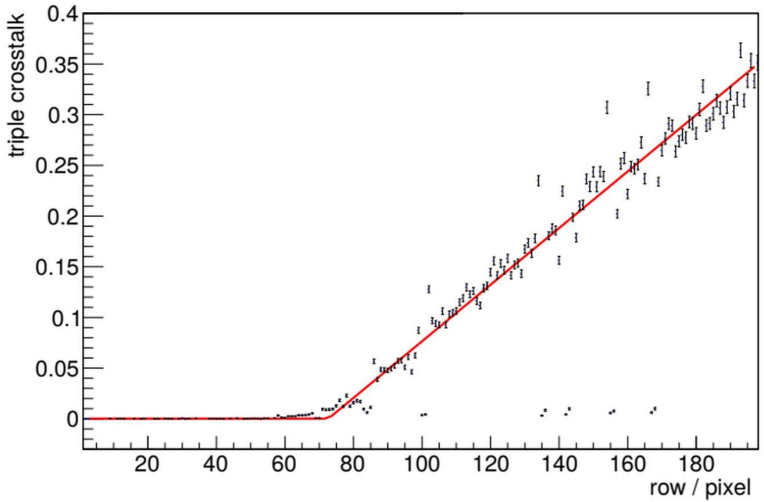
The Flexprint Environment

- 2 layer aluminum polyimide flexprint (LTU)
- Provides:
  Power & HV (parallel)
  Differential Signal I/O
- Only 1 supply voltage, but no LDO-regulators!
- Minimise I/O
- Flex design rules define PadOut



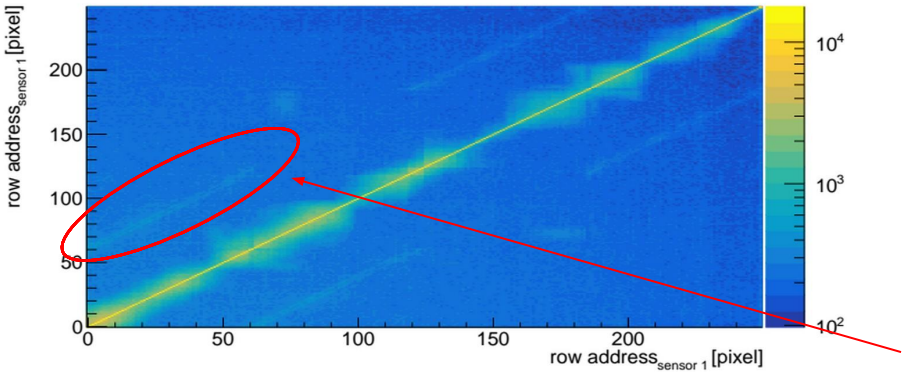
Signal Line Crosstalk - MuPix8





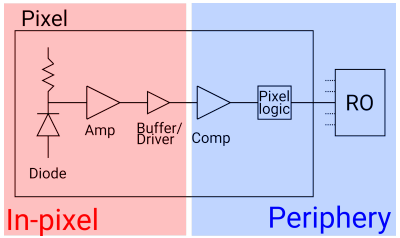
Triple Crosstalk:
hit induced in both neighbouring lines

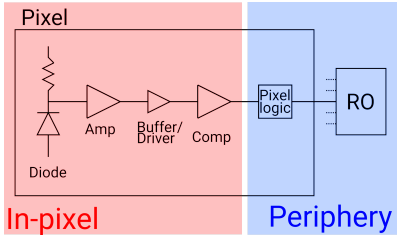
Routing Optimisation - MuPix10

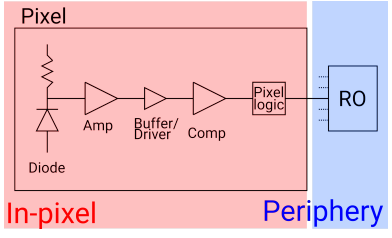


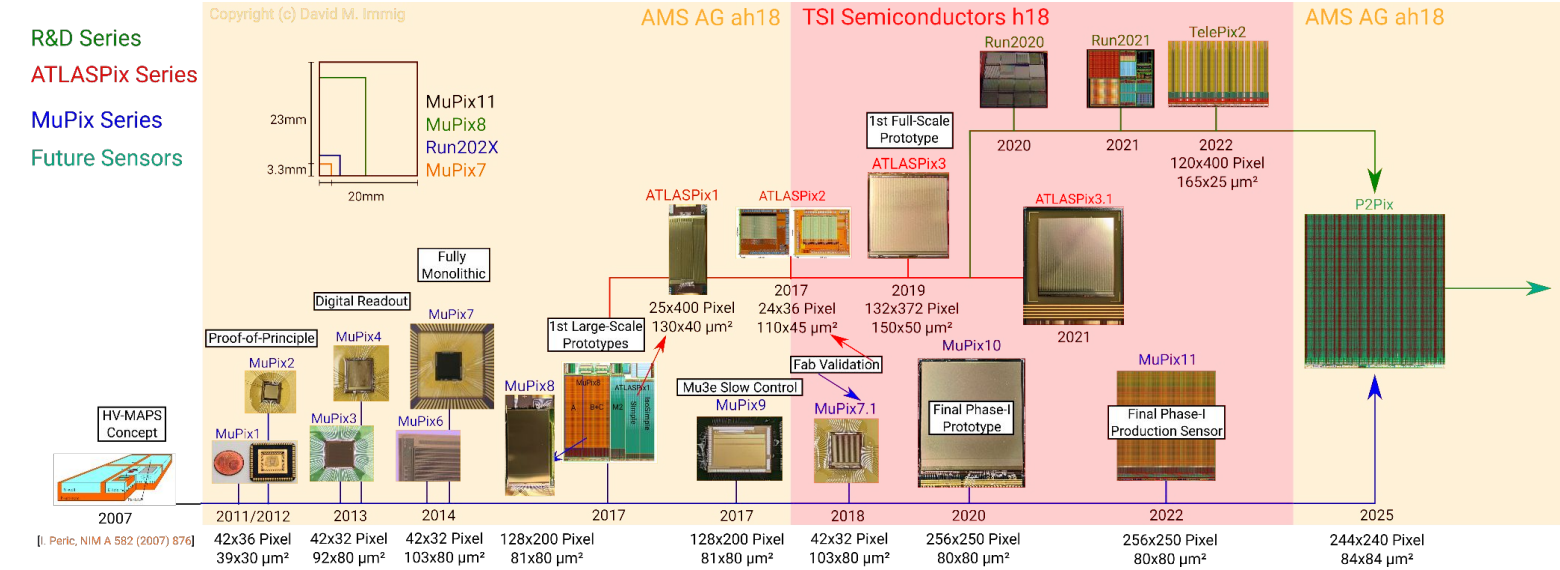
- Equalize but reduce crosstalk
  →miminise the length that two line are neighbouring
  (¼ of total length, 2cm)
- ~12% triple crosstalk expected
- Make Crosstalk easily detectable
  → neigbouring signal lines are not neigbouring pixels
- Crosstalk can be removed, possibly already during the data taking
- Even more improvement expected for MuPix11

Beyond MuPix11 – Roadmap -- Architectures

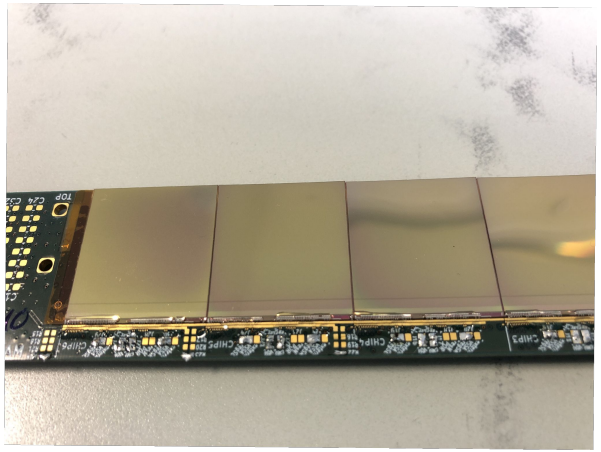




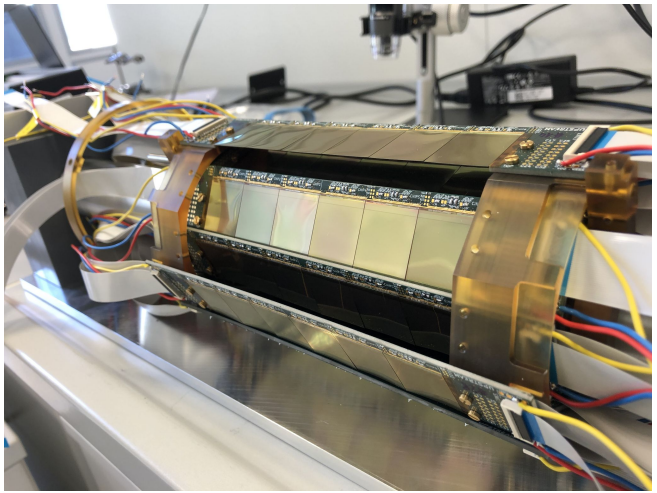




Proto Vertex Detector



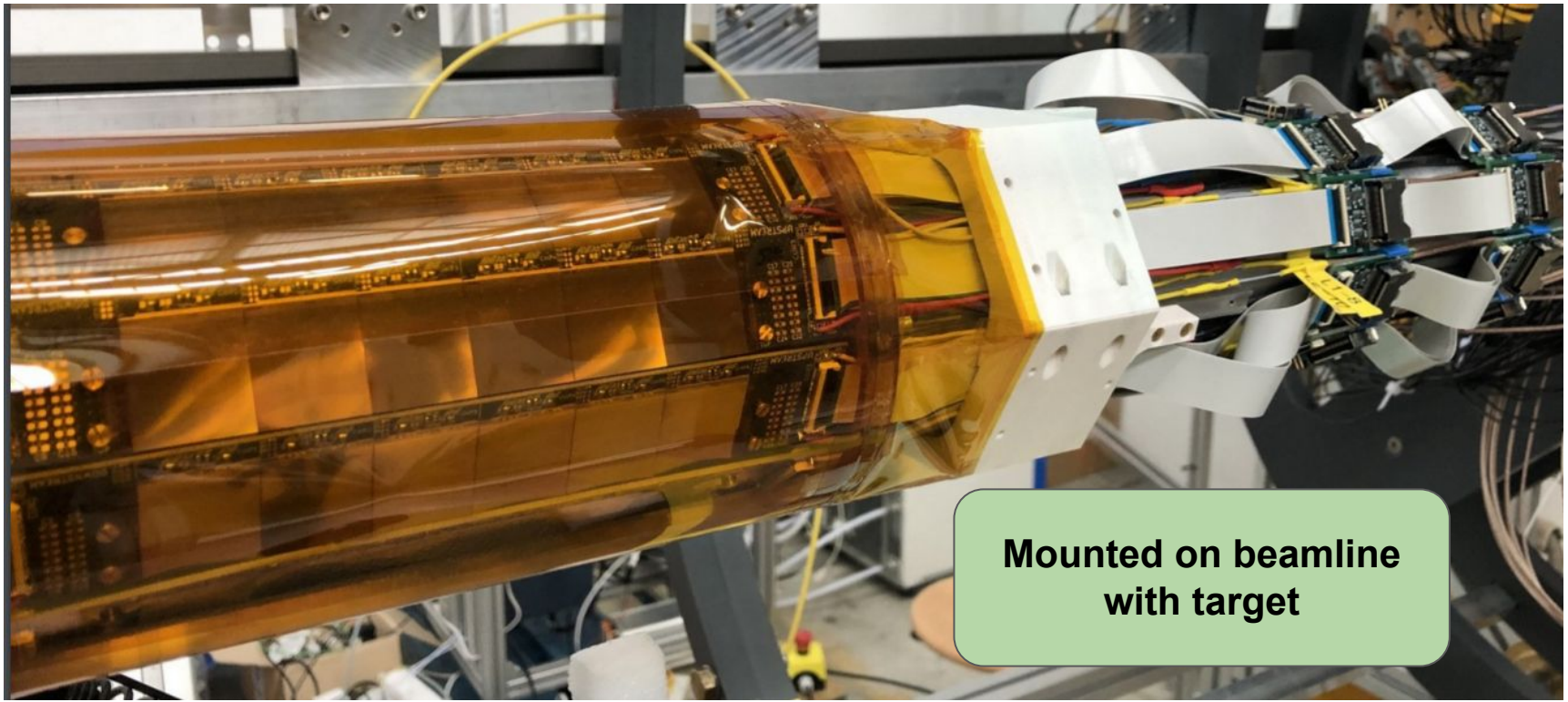
- First proto-detector with 6 chips modules
  - Still PCB based!!!



- Two layer vertex detector (MuPix10)
  - Gain operational experience
  - Test Mu3e readout chain

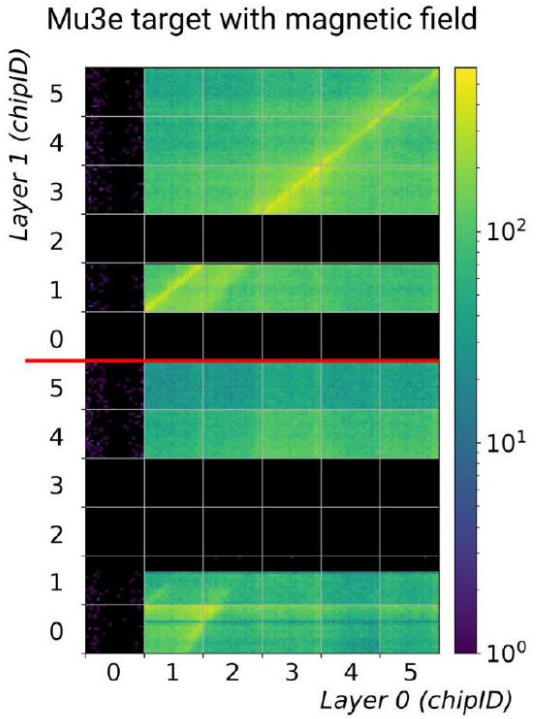
Operation in experimental conditions

DAQ and experimental concept



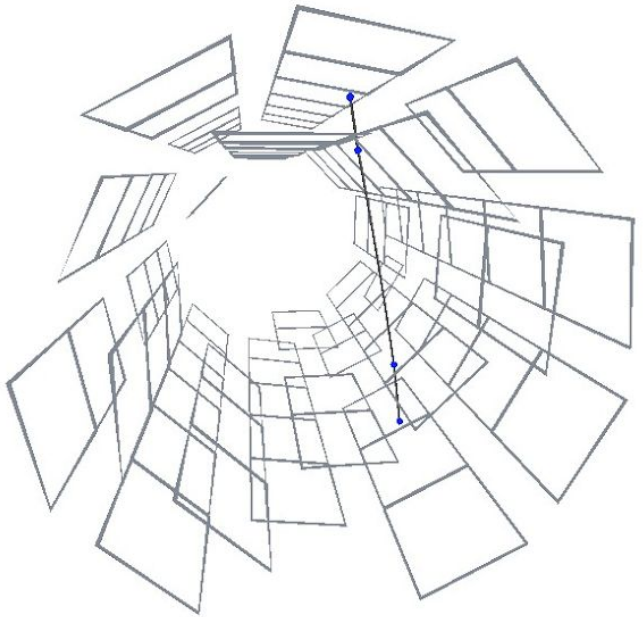
Operation in experimental conditions

With beam (2021)



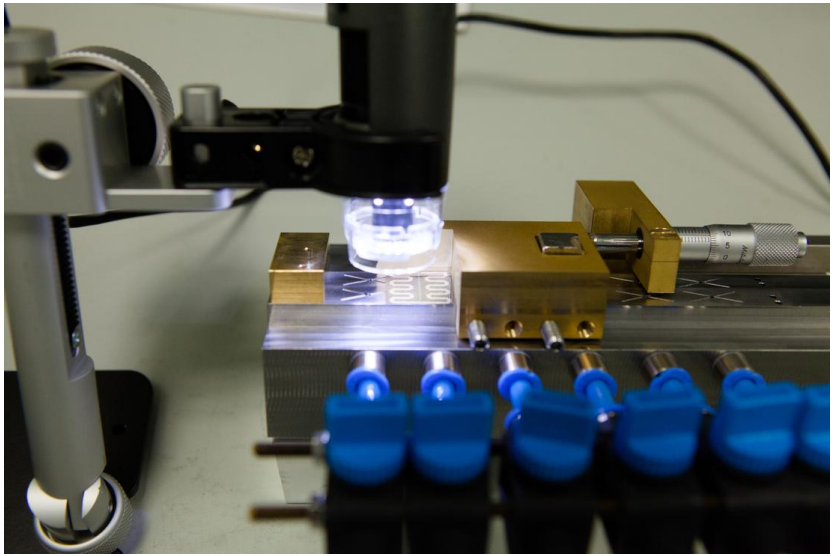
Layer 0-1 correlation!

With cosmics (2022)



More analysis ongoing

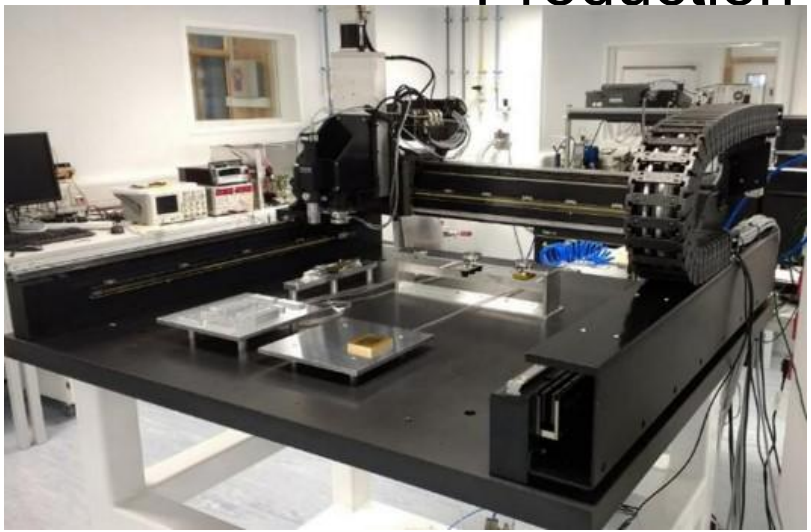
Production of inner layers



Heidelberg/PSI

Quick demo: https://youtu.be/0SYqHSbH3U4

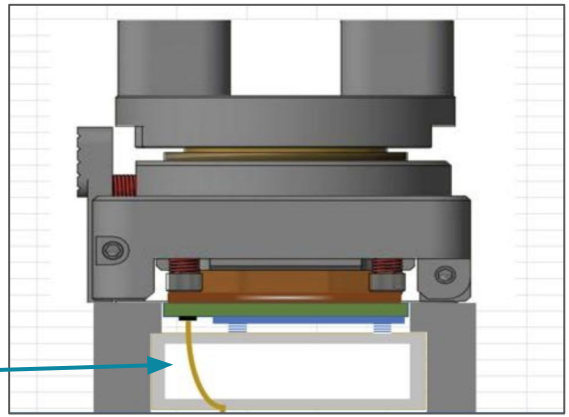
Production of outer layers

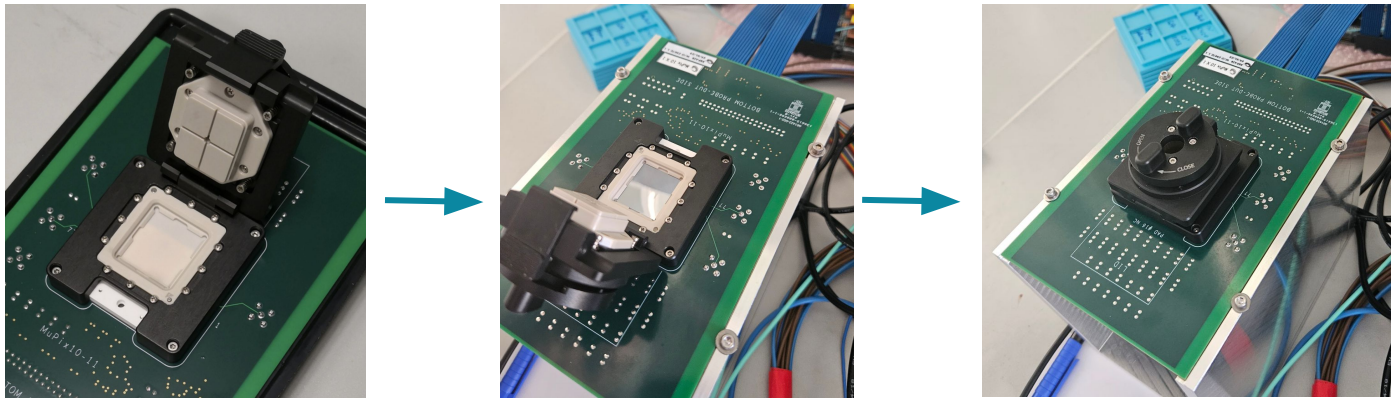


Oxford/Bristol/Liverpool

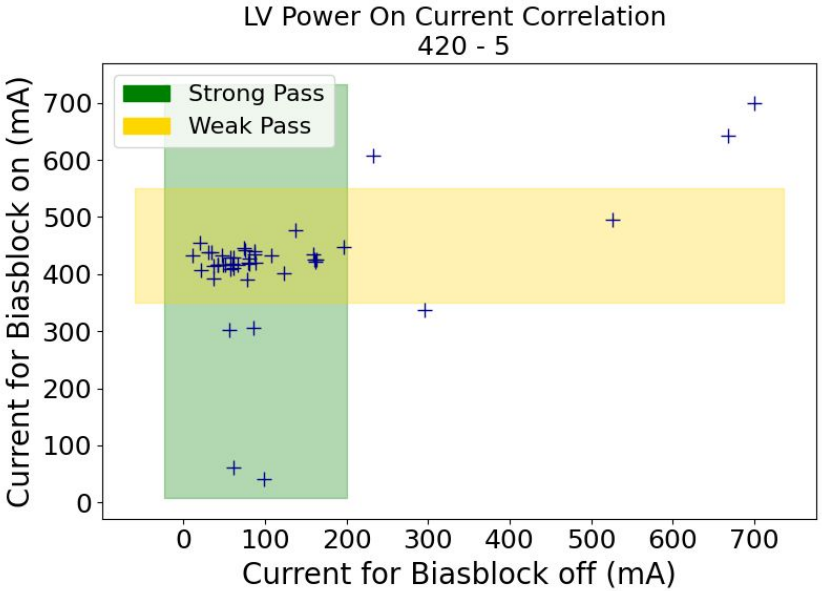
Quality Control (QC)

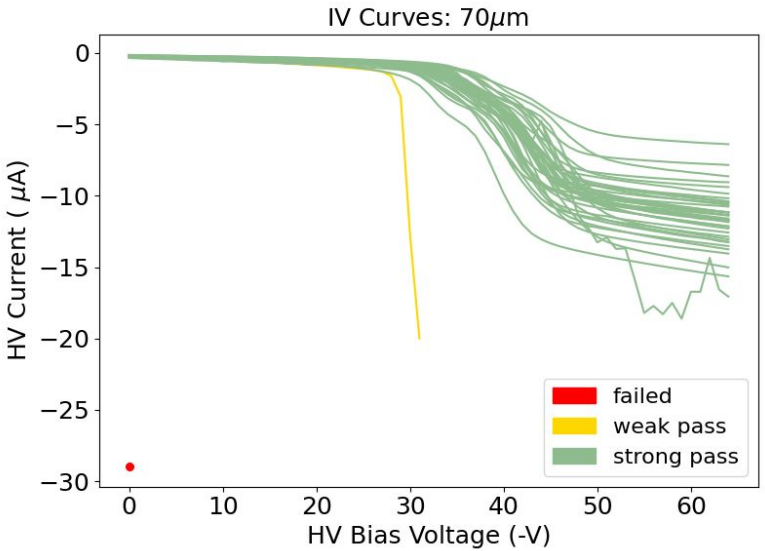
- Quality assurance is key before a large scale detector assembly
- Testing after assembly is too risky and costly, since dismantling is impossible
- Press down mechanism with contact needles for prior testing





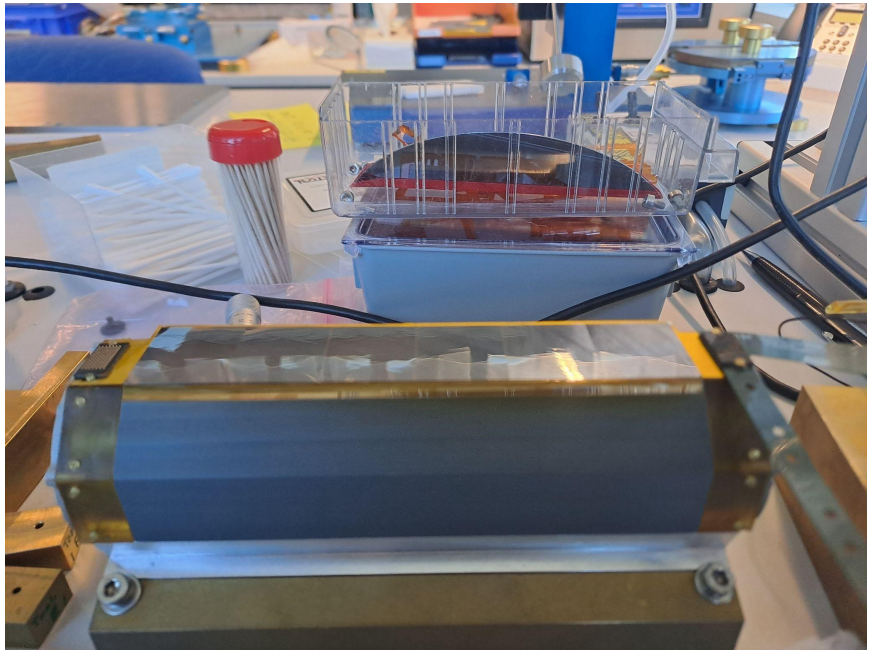
QC - Test procedures



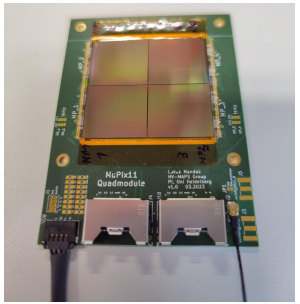


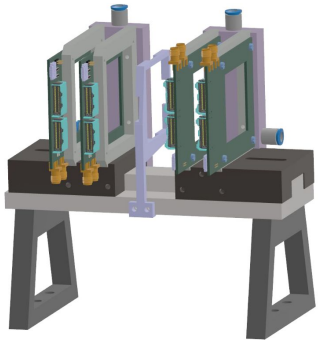
- 2 Single Chip test sites
- First needle card test station being setup in Oxford
- QC procedure still being refined, but almost final
- Grading scheme still adjusting (pre-production)

The Vertex Detector



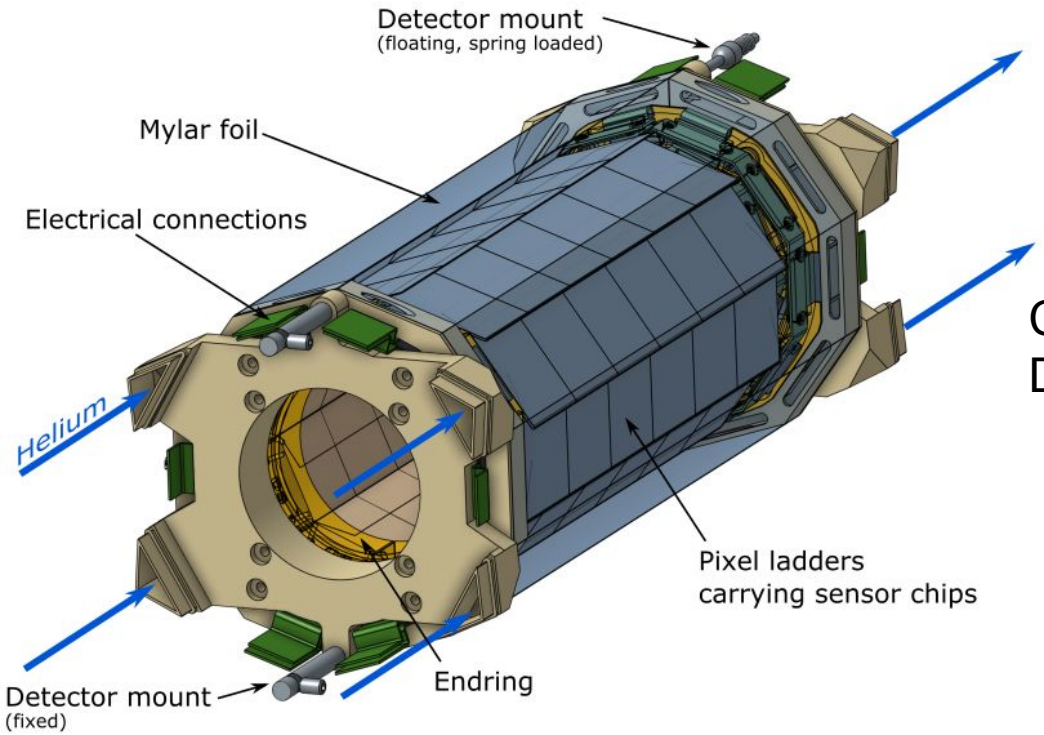
- First Vertex ladders have been produced
- Ladder QC under development in parallel to single chip QC
- Fully functional 50µm ladder in Hand
- Currently running beam time at PSI:
  First time in-beam commissioning of final ladder





Tracking System - Vertex Detector

Layer 0+1



Chips glued and bonded High Density Interconnects (HDIs)

- 6 for layer 0 and 1
- 17/18 for layer 2 and 3
- 50 μm thin
- Connection via interposers (pressed against RO flexes)

In-House Wafer Handling

- Diced and thinned wafers delivered on tape
- Equipement:
  - Vacuum chuck
  - Pick-up tools (tweezer & suction pen)
  - A lot of patience & time
- Pending on use case thickness vary between 50µm to 100µm + 750µm

Mu3e ~ 150 Wafers