Data Flow in the Mu3e Filter Farm

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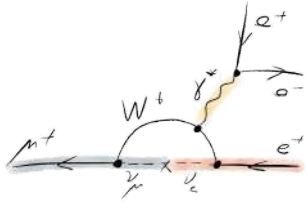
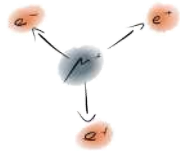
Mu3e Motivation



SM with ν oscillation Br: $< 10^{-54}$



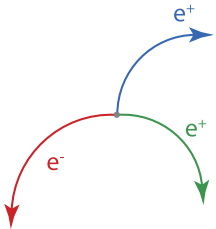
decay at rest

- Search for Lepton Flavor Violation $\mu^+ \to e^+e^-e^+$
- Current limit (Br < 10^{-12}) set by SINDRUM (1988)

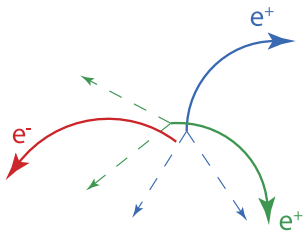
- Muon beam of 1×10^8 μ/s
- One year of data taking
- Sensitivity up to one in 10^{15}

$\to$ High data rate of 80 Gbit/s

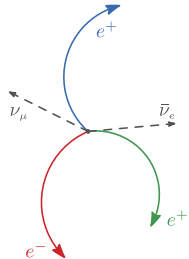
Mu3e Experiment



signal



random combinations

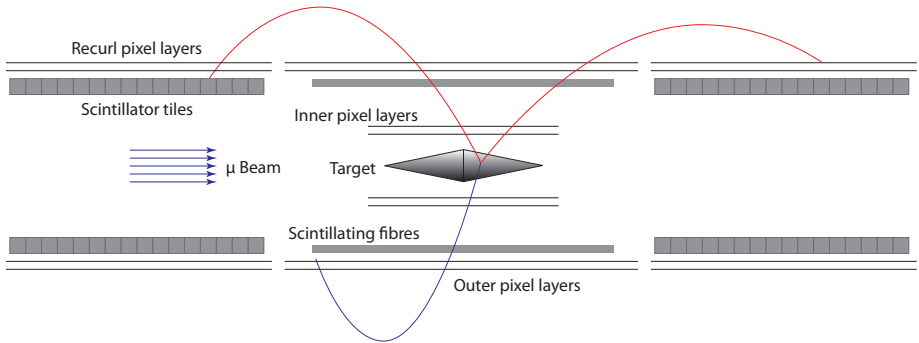


internal conversion

- $\sum p_e = 0$
- $\sum E_e = m_\mu$
- Good vertex and time resolution

$\rightarrow$ Need of online reconstruction

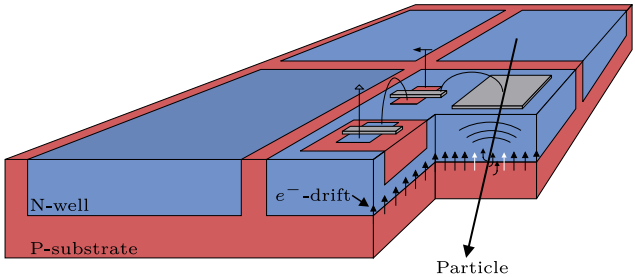
Mu3e Detector Concept



size around 1m

- Magnetic fild of $1\,\mathrm{T}$
- Target stops μ^+

High Voltage Monolithic Active Pixel Sensors



[1]

- Thinned down to $50\,\mu\text{m}$
- Fast charge collection
- Time resoluton of a few ns
- Digitalization and zero suppression on the chip

$\rightarrow 1.25\,\text{Gbit/s}$ unsorted hit data

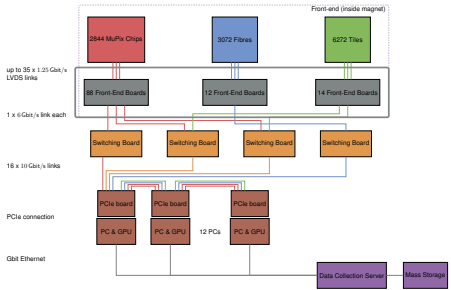
[1] Ivan Perić et al., NIM A582 (2007) 876-885

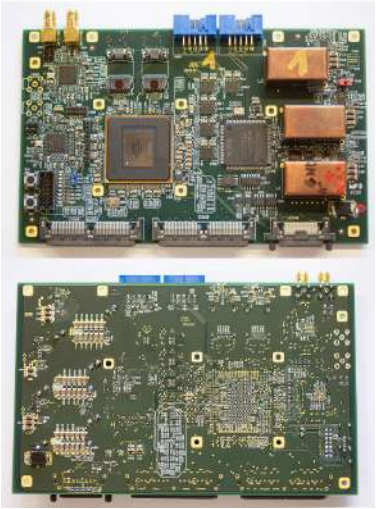
Timing Detectors

- Fibre < 500 ps time resolution
- Tiles < 70 ps time resolution

$\rightarrow$ Readout via MuTrig chip, 1.25 Gbit/s unsorted hit data

Front-end FPGA Board

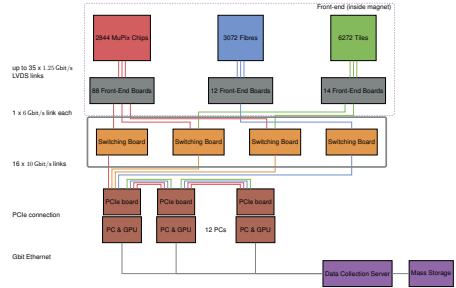




- Located inside the magnet
- Receives data from the detectors
- Sorts the data in time
- From electrical to optical

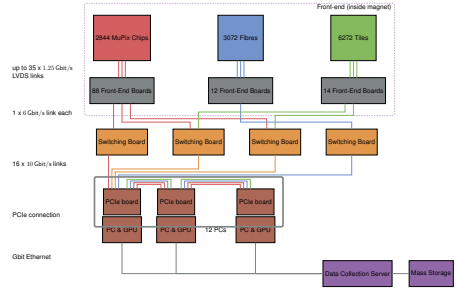
Switching FPGA Board

- Located outside the magnet, connected via PCIe to PC
- PCIe40 board from LHCb & ALICE Upgrade
- Hit synchronisation from multiple FEBs

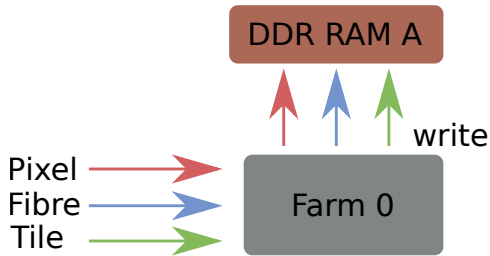


PC Interface FPGA Board

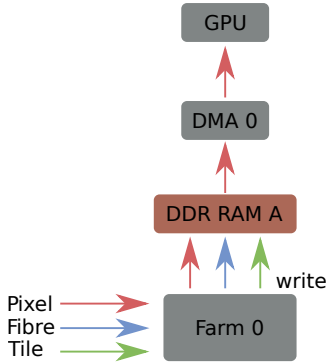
- Located outside the magnet, connected via PCIe to PC & GPU
- Synchronisation data of different detector types
- Terasic DE5e-Net board
- Buffers the data for online tracking on the GPU



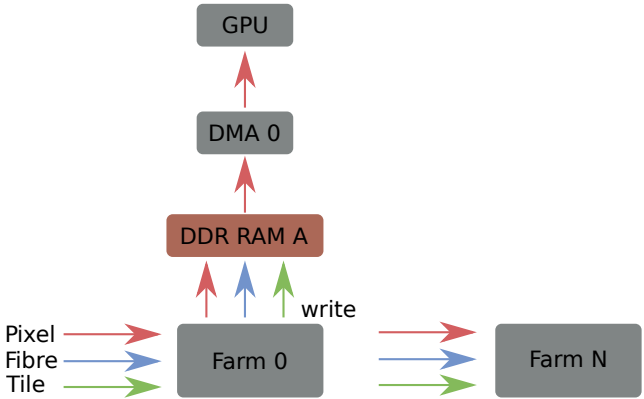
PC Interface FPGA Board Firmware



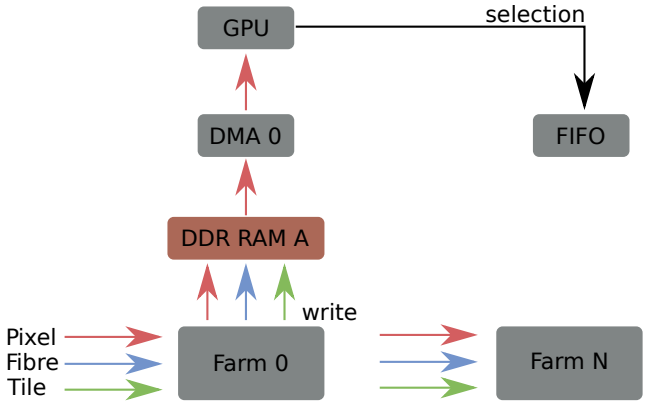
PC Interface FPGA Board Firmware



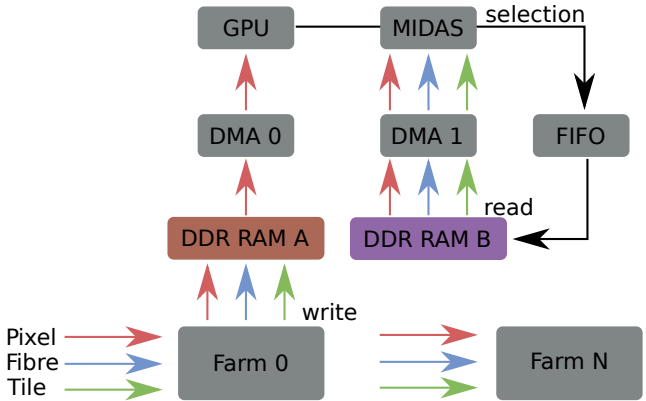
PC Interface FPGA Board Firmware



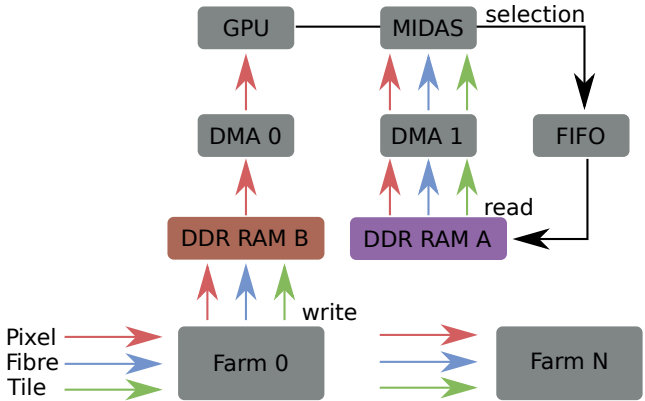
PC Interface FPGA Board Firmware



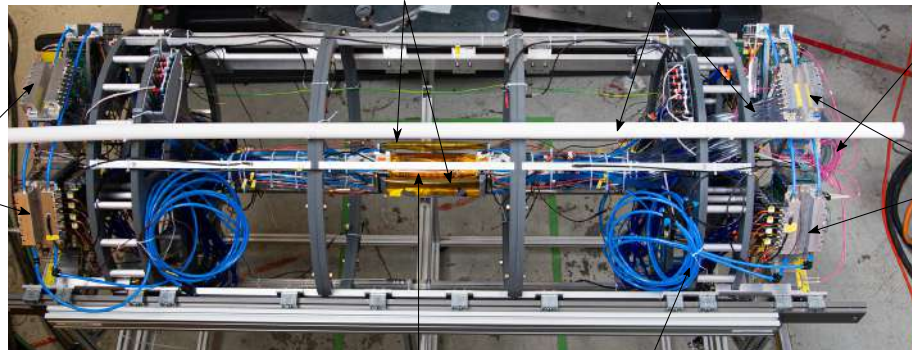
PC Interface FPGA Board Firmware



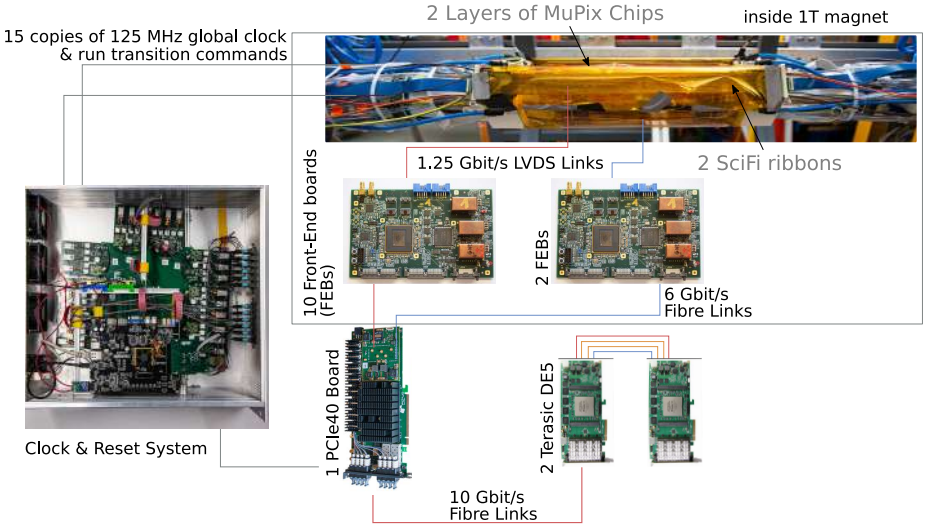
PC Interface FPGA Board Firmware



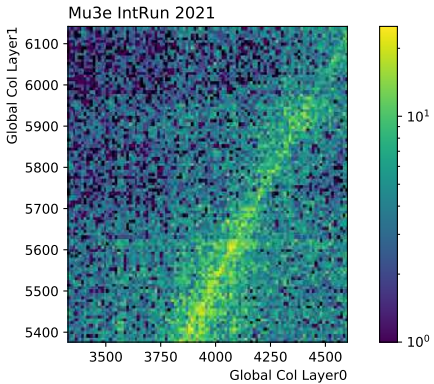
Mu3e Integration Run



Mu3e Integration Run DAQ

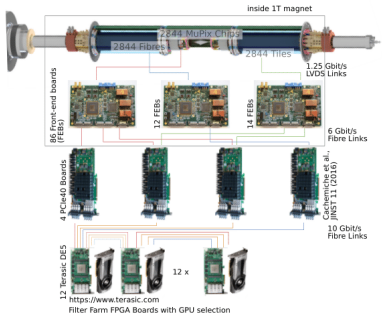


Mu3e Integration Results



- Space correlation of decay particle in the two vertex layers
- Analysis is still ongoing
- Very preliminary results

Conclusion & Outlook



- Testing of PC Interface FPGA Board firmware with detector data
- Integration of the GPU selection
- Currently at another integration run with cosmics