Hit Synchronisation in the Mu3e DAQ

Marius Köppel on behalf of the Mu3e collaboration

Institute for Nuclear Physics, JGU Mainz

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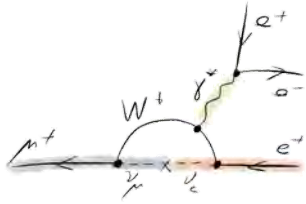
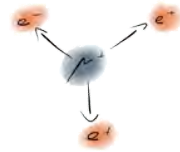
Mu3e Motivation



SM with ν oscillation Br: $< 10^{-54}$



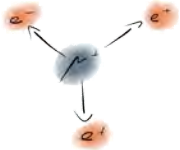
decay at rest

- Search for Lepton Flavor Violation $\mu^+ \to e^+e^-e^+$
- Current limit (Br < 10^{-12}) set by SINDRUM (1988)

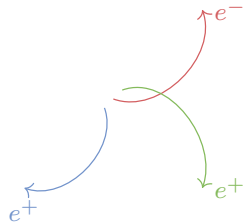
- Muon beam of 10^8 μ/s
- One year of data taking
- Sensitivity up to one in 10^{15}

→ High data rate of 80 Gbit/s

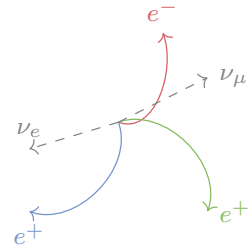
Mu3e Experiment



signal



random combinations

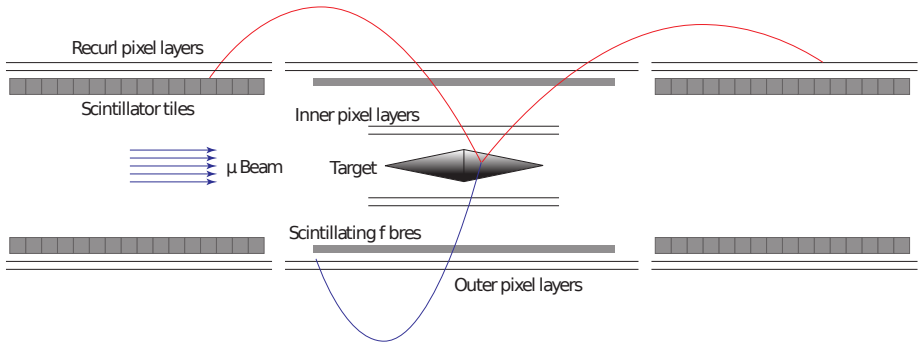


internal conversion

- $\sum p_e = 0$
- $\sum E_e = m_\mu$
- Good vertex and time resolution

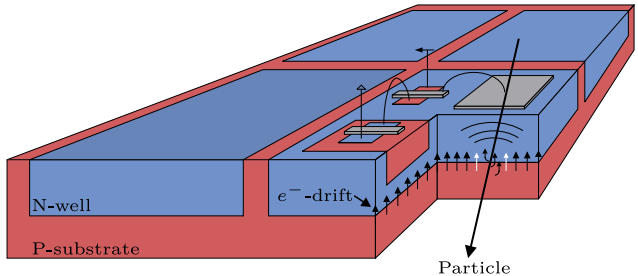
$\rightarrow$ Need of online reconstruction

Mu3e Detector Concept



- Magnetic fild of 1 T
- Target stops μ^+

High Voltage Monolithic Active Pixel Sensors



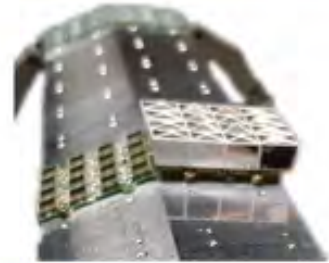
[1]

- Thinned down to 50 µm
- Fast charge collection
- Time resoluton of a few ns
- Readout on the chip

→ 1.25 Gbit/s zero suppressed, unsorted hit data

[1] Ivan Perić et al., NIM A582 (2007) 876-885

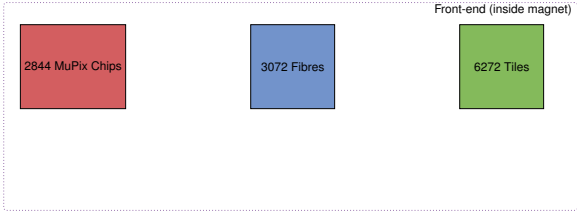
Timing Detectors



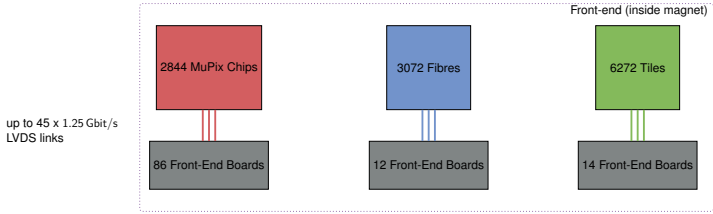
- Fibre < 500 ps time resolution
- Tiles < 70 ps time resolution

→ Readout via MuTrig chip, 1.25 Gbit/s unsorted hit data

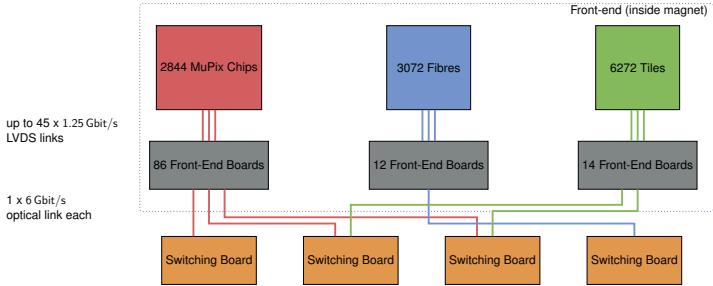
Mu3e DAQ


Front-end (inside magnet)
2844 MuPix Chips
3072 Fibres
6272 Tiles

Mu3e DAQ


Front-end (inside magnet)
2844 MuPix Chips
3072 Fibres
6272 Tiles
up to 45 x 1.25 Gbit/s
LVDS links
86 Front-End Boards
12 Front-End Boards
14 Front-End Boards

Mu3e DAQ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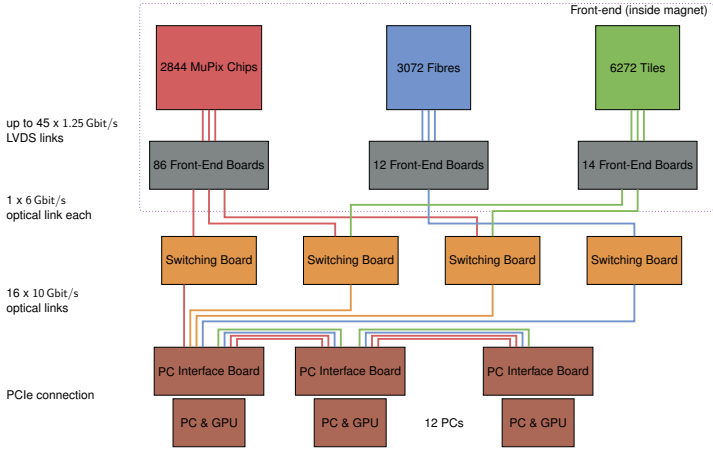
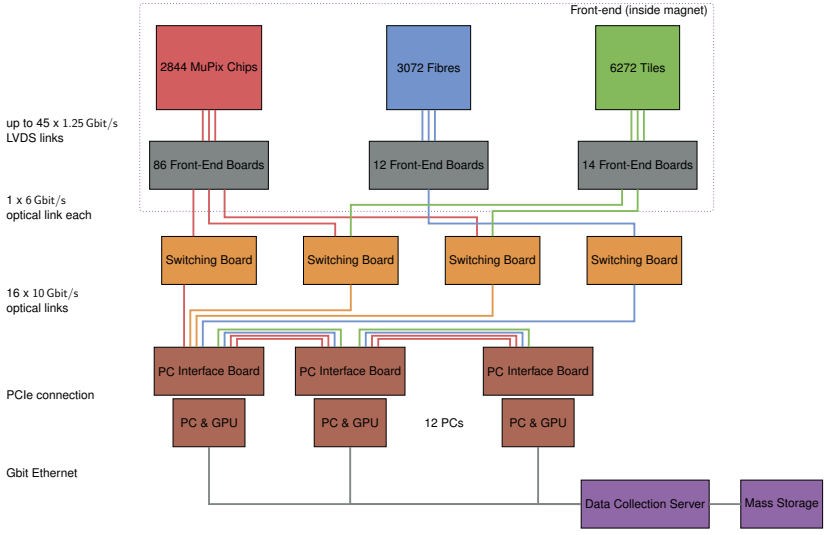
2844 MuPix Chips
3072 Fibres
6272 Tiles
up to 45 x 1.25 Gbit/s
LVDS links
86 Front-End Boards
12 Front-End Boards
14 Front-End Boards
1 x 6 Gbit/s
optical link each
Switching Board
Switching Board
Switching Board
Switching Board

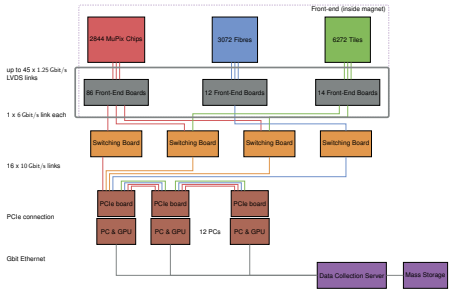
Mu3e DAQ


Front-end (inside magnet)
2844 MuPix Chips
3072 Fibres
6272 Tiles
up to 45 x 1.25 Gbit/s
LVDS links
86 Front-End Boards
12 Front-End Boards
14 Front-End Boards
1 x 6 Gbit/s
optical link each
Switching Board
Switching Board
Switching Board
Switching Board
16 x 10 Gbit/s
optical links
PC Interface Board
PC Interface Board
PC Interface Board
PCIe connection
PC & GPU
PC & GPU
12 PCs
PC & GPU

Mu3e DAQ


Front-end (inside magnet)
2844 MuPix Chips
3072 Fibres
6272 Tiles
up to 45 x 1.25 Gbit/s
LVDS links
86 Front-End Boards
12 Front-End Boards
14 Front-End Boards
1 x 6 Gbit/s
optical link each
Switching Board
Switching Board
Switching Board
Switching Board
16 x 10 Gbit/s
optical links
PC Interface Board
PC Interface Board
PC Interface Board
PCIe connection
PC & GPU
PC & GPU
12 PCs
PC & GPU
Gbit Ethernet
Data Collection Server
Mass Storage

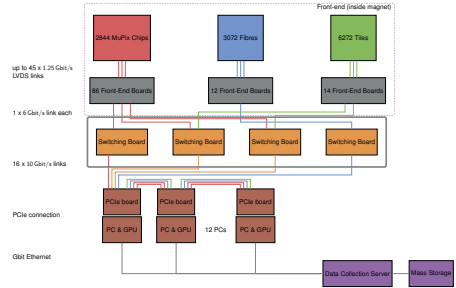
Front-end FPGA Board

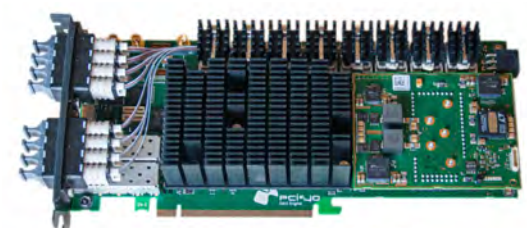


- Located inside the magnet
- Receives data from the detectors
- Sorts the data in time
- From electrical to optical

Switching FPGA Board

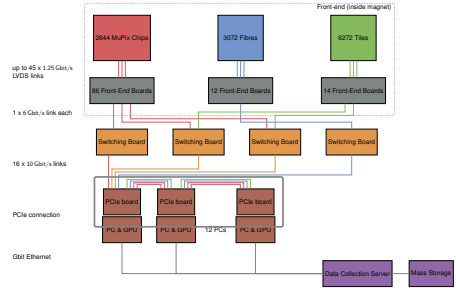
- Located outside the magnet, connected via PCIe to PC
- PCIe40 board from LHCb & ALICE Upgrade
- Hit synchronisation from multiple FEBs



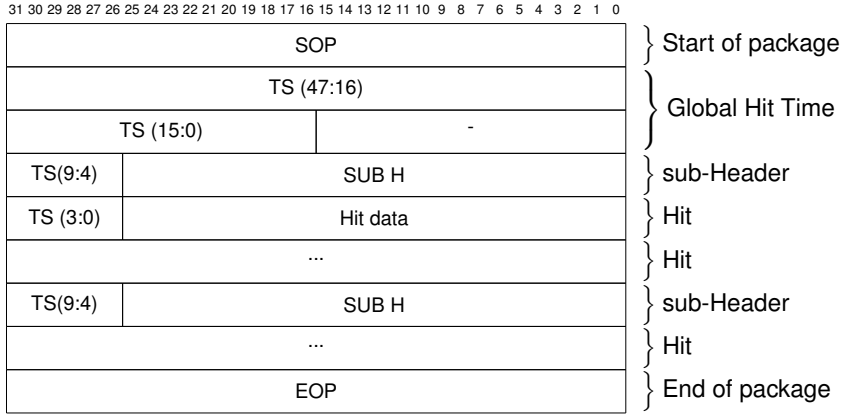


PC Interface FPGA Board

- Located outside the magnet, connected via PCIe to PC & GPU
- Synchronisation data of different detector types
- Buffers the data for online tracking on the GPU
- Terasic DE5e-Net board

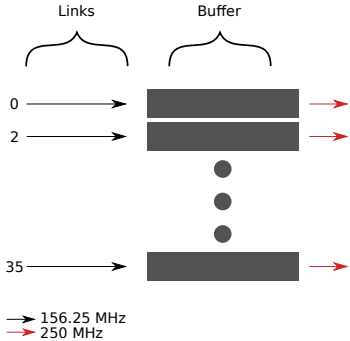


Protocol - MuPix Data

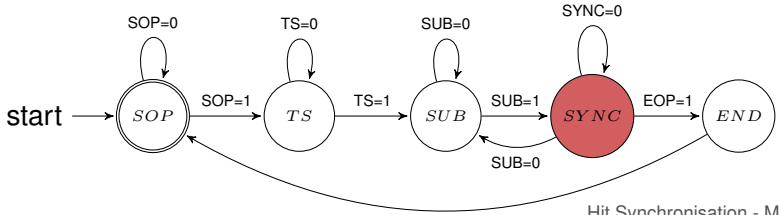


- Front-end FPGAs send every 16 timestamps one sub-header
- All hits from the Front-end FPGAs are sorted in time

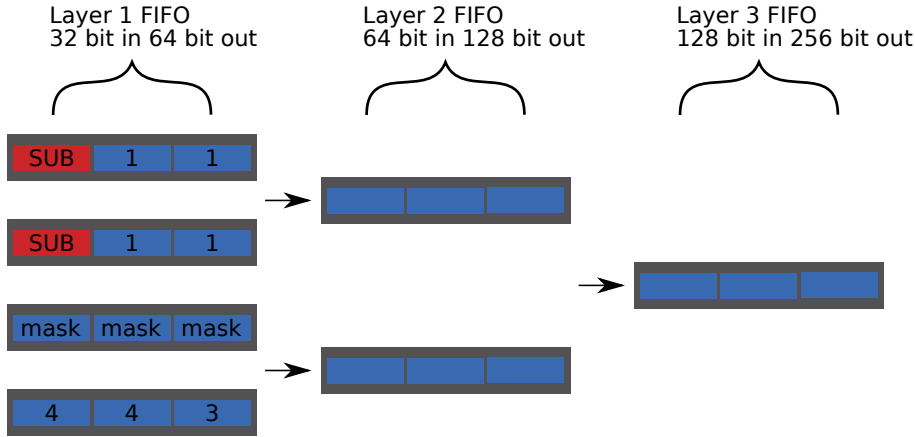
Synchronisation



- Input 32 bit x 156.25 MHz
- Output 256 bit x 250 MHz



Sketch 4 to 1 Synchronisation Tree



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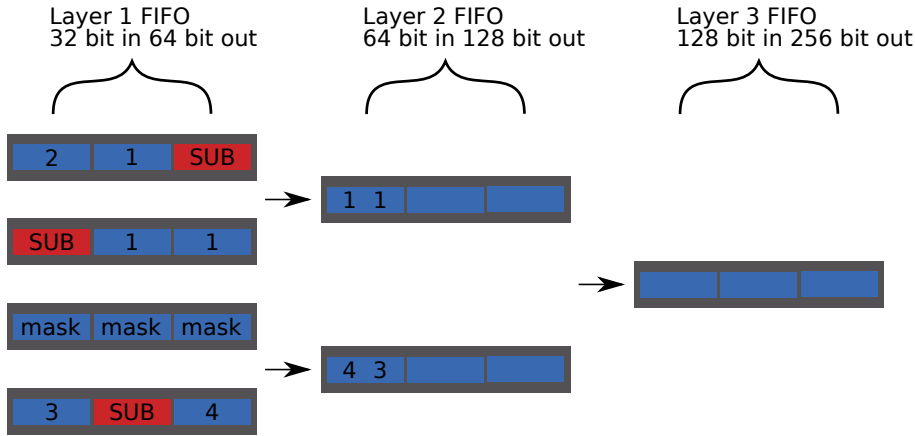

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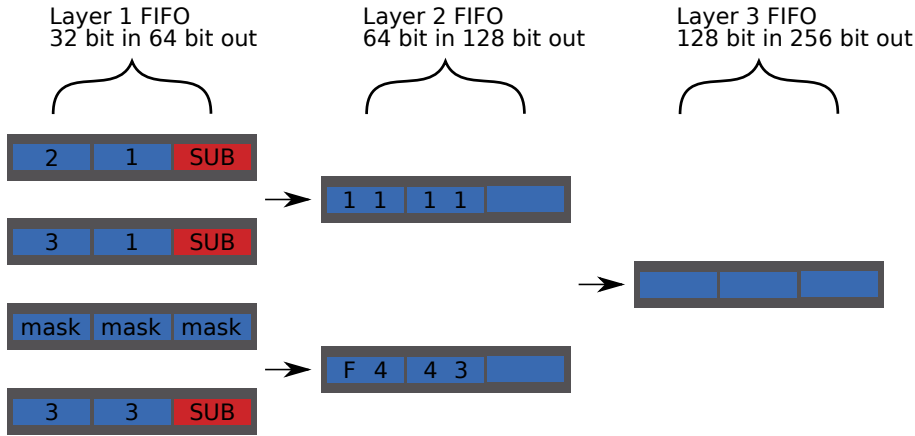
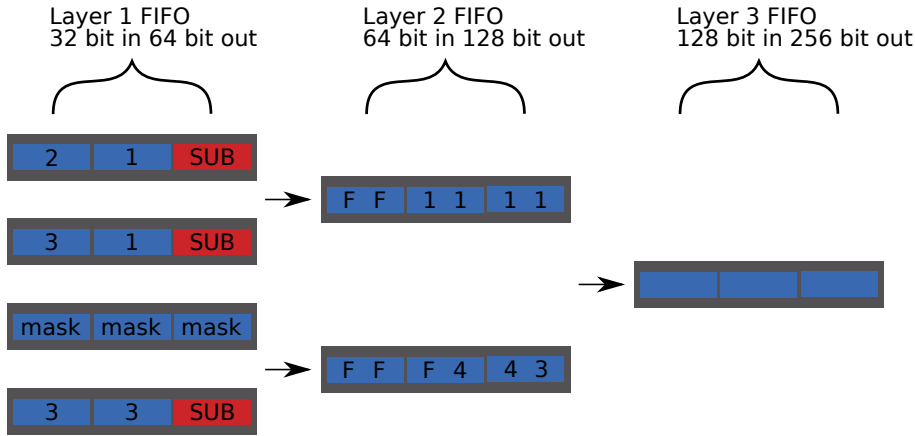


Sketch 4 to 1 Synchronisation Tree



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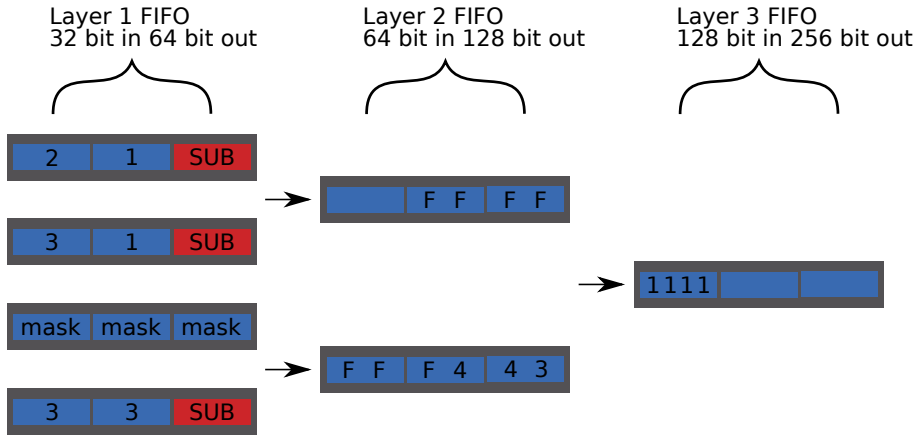

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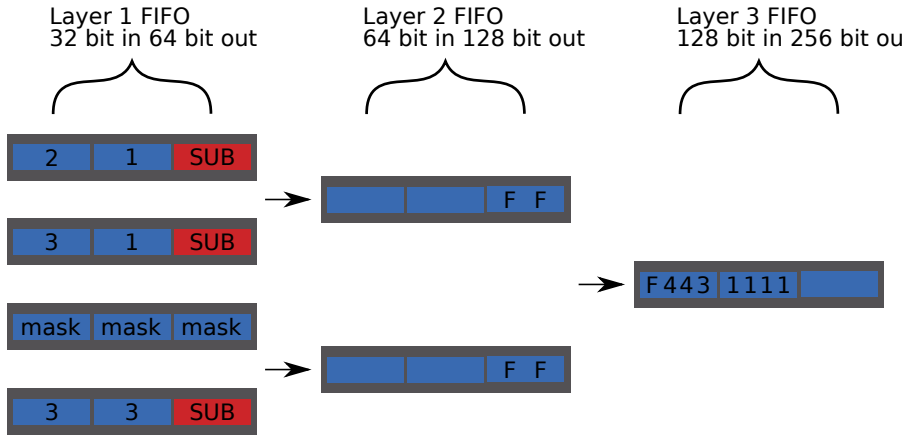

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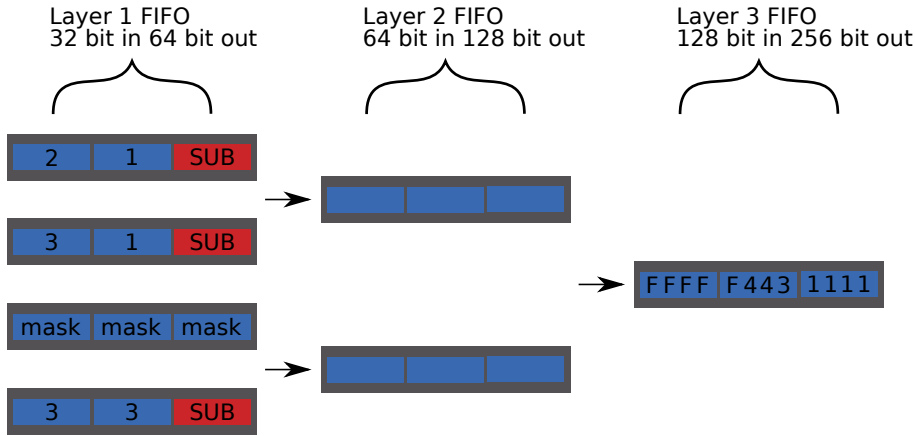

Conclusion & Outlook

- Alignment of 64 links worked in hardware - Mu3e needs 36 links
- Currently working PC Interface FPGA Board firmware
- Planed integration / commissioning run in spring