The DRS2 Chip: a 4.5 GHz Waveform Digitizing Chip for the MEG Experiment

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***Abstract*--A switched-capacitor array (SCA) chip is currently under development for fast waveform digitizing of PMT and drift chamber signals for the MEG Experiment at PSI, Switzerland. This experiment searches for the lepton-flavor violating decay $\mu^+ \to e^+\gamma$ with a sensitivity down to 10^{-13}. After a first prototype (DRS1), the second prototype chip (DRS2) has been fabricated in a 0.25 μm CMOS process and successfully been tested. It contains 10 channels, each with 1024 capacitive sampling cells. Waveform digitizing takes place with an on-chip generated frequency ranging from 0.5 GHz to 4.5 GHz. The cells are read out at 40 MHz with an external 12 bit flash ADC. A phase-locked-loop circuit (PLL) ensures high stability, making the chip suitable to replace both ADCs and TDCs in an experiment with a timing resolution below 100ps and an ADC resolution equivalent of 14 bit. The design of the chip is described and results from performance measurements are reported. Ideas of fast online waveform processing are discussed.**

I. Introduction

THE MEG experiment [1] utilizes a high resolution liquid xenon calorimeter and a drift chamber system to detect the decay positron and gamma from a potential $\mu^+ \to e^+\gamma$ decay, respectively. A muon beam with ~10^8 *m/sec* is stopped in a thin target. Since the calorimeter is unsegmented, a high pile-up rate is expected, making waveform digitizing on all PMT channels mandatory. Instead of using commercial flash analog-to-digital converters (FADC), an analog waveform digitizer in the GHz range will be used, which follows an earlier development at PSI [2]. This solution is not only cheaper and requires less power than a FADC, it also delivers high timing resolution, which makes the usage of discriminators and TDCs unnecessary.

II. Principle of Operation

Since it is very hard to generate and distribute clock signals in the GHz range, the sampling frequency is generated with a series of inverters. A sampling signal propagates through these inverters freely (domino principle). Transmission gates between the inverters make the sampling frequency controllable in a wide range by an analog voltage supplied to the chip. A special "tail-biting" circuitry ensures that the width of the sampling signal is always four cells wide. Additional AND-gates allow to stop the domino wave in any cell by an external trigger signal. The domino wave runs continuously in a circular fashion, hence the name Domino Ring Sampling chip (DRS). Since the storage depth is larger than a typical PMT signal width, the storage chain acts like an analog pipeline and makes delay cables unnecessary for first level trigger latencies up to several hundred nanoseconds. Figure 1 shows the simplified schematic of the chip.

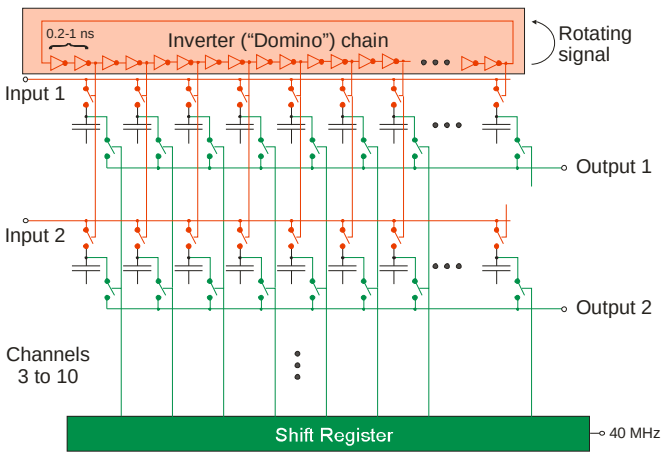

Fig. 1: Simplified schematic of the DRS2 chip.

Since the speed of the domino wave depends on many factors like the temperature and the supply voltage, an external phase-locked loop (PLL) is used to lock the frequency and phase to a high precision quartz oscillator. By distributing this reference signal to all DRS2 chips in an experiment, it is assured that all domino waves in all modules run at the same phase and frequency with a timing jitter better than 200 ps.

A trigger signal stops the domino wave, freezing the contents of the sampling capacitors. They are then read out by a shift

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register at a clock speed of 40 MHz and digitized externally by a multiplexed 12 bit flash ADC. Since the sampling capacitors are much smaller (200fF) than the parasitic capacitance of the readout line, the analog performance is very poor as observed in the DRS1 chip. The DRS2 chip however uses a "current mode" readout, where the sampling capacitances are connected to the gate of individual NFET transistors for readout, which produce a current proportional to the voltage in the sampling cell. This leads to a much more robust readout and improves the signal-to-noise ratio significantly. For high accuracy applications, a 20 MHz master clock signal and a voltage reference signal can be applied to channels 9 and 10, respectively, offering the possibility for an additional offline calibration. Using this technique, the required timing accuracy of 100 ps for the MEG experiment can be achieved.

TABLE I
BASIC CHIP PARAMETERS FOR DRS1 AND DRS2

	DRS1	DRS2
Number of channels/chip	1	10
Number of cells/channel	768	1024
Maximum sampling speed [GHz]	2.5	4.5
Minimum sampling speed [GHz]	0.7	0.5
Readout speed [MHz]	20	40
Readout dead time [µs]	40	256 (10 chn.)
Signal-to-noise ratio [bit]	8	13*)
Timing accuracy at 2.5 GHz [ps]	80	40

*) *see text*

III. TEST RESULTS

The DRS2 chip was manufactured in the UMC 0.25 µm 1P5M MMC process in spring 2004 (Fig. 2).

Since the design is based on a gate library derived from the CMS pixel chip, the DRS2 chip is radiation hard. The domino wave runs stably up to 4.5 GHz. A timing jitter between consecutive turns of the domino wave of 40 ps has been measured. The power consumption for the complete chip is 50mW at 2.5V.

Fig. 3 shows the readout of a square wave pulse digitized at 2.5 GHz, which had a width of 12 ns and a rise time of ~1 ns.

The lower track represents the 40MHz readout clock, the upper track the signal directly coming from the DRS2 analog output. The signal edge is contained in three adjacent sampling cells, indicating an analog bandwidth well above 500 MHz.

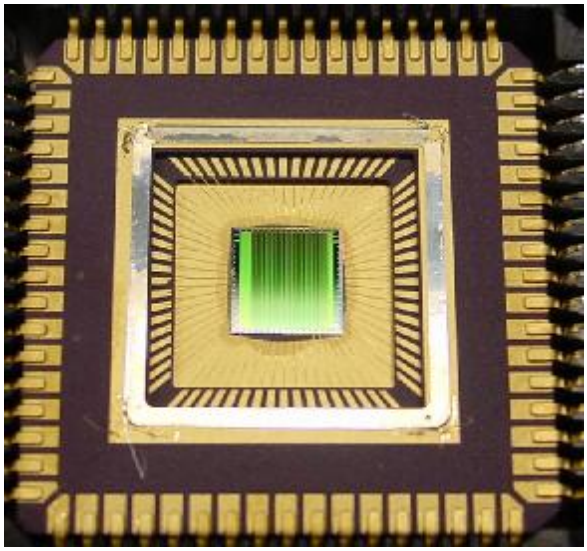

Fig. 2: The packaged DRS2 chip

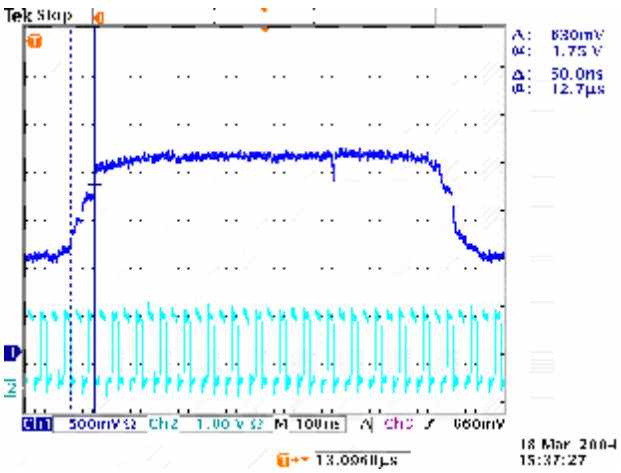

Fig. 3: Readout of a single square wave pulse at 40 MHz

IV. CHIP READOUT

The DRS chip is read out with a commercial 12-bit 40 MHz flash ADC. The ADC is housed together with two DRS chips on a single Mezzanine board. The readout of all 20 channels from both chips takes 512 µs. It is planned to reduce this readout time for short input pulses by only digitizing the relevant part of the 1024 storage cells and thus reducing the readout time by some factor. Two Mezzanine boards are contained on a 6HE VME board, resulting in 32 effective channels per VME board. The VME board contains FPGAs for generating the readout sequence and the storage of the digitized data. FPGA algorithms for

baseline subtraction signal integration and timing analysis are under development. It is planned to process all waveforms in the FPGA and only ship ADC and TDC data to the front-end computers. Only in case of a pile-up event the full waveform has to be stored for later offline analysis and peak fitting. The VME board contains two Virtex-II Pro FPGAs, each having two PowerPC cores, which can be used to assist in waveform analysis. The cost per channel in small quantities is about 30$ (chip) and 70$ (VME board).

The full system was first tested in October 2004 in a test beam at PSI. A first quick tests shows a random noise of 2 mV at a full scale of 1.5 V indicating a resolution of 9-10 bits. If the digitized signals are integrated over several bins, the signal-to-noise ratio (SNR) can be improved. Summing over a 100 ns wide PMT signal from the MEG xenon calorimeter (250 bins) results in a resolution of 13 bits, which does not yet meet the required 14 bits. A redesign of the Mezzanine board with an better analog layout is planned and should reduce the noise by a factor of two.

V. Outlook

The DAQ system of the MEG experiment will use exclusively the DRS chip on all 1000 PMT channels running at 2.5 GHz and on all 3000 drift chamber channels (cathodes and anodes) at a speed of 500 MHz, delivering an excellent pile-up rejection. A timing calibration signal will be distributed and sampled in all DRS chips, in order to meet the experiment requirement of 100 ps timing accuracy.

An online cluster of about ten PC's is foreseen for online waveform processing, resulting in a data rate below 2 MB/sec for an event rate of 100 Hz. A last prototype chip is planned for spring 2005, and the bulk production in fall 2005. The MEG experiment will start taking data in 2006. In meantime, several other experiments as well as commercial companies expressed their interest in this system, so it is hoped that this work will be to the benefit of many others.

VI. References

[1] T. Mori *et al.*, PSI R-99-05 Experiment Proposal, Paul Scherrer Institute, Villigen, 1999

[2] C. Brönnimann *et al.*, NIM **A 420**, 264 (1999)