12 channel, 5 GSPS Switched Capacitor Array

DRS3

FEATURES
Single 2.5 V Power Supply
Sampling speed 10 MSPS to 5 GSPS
12 Channels with 1024 Storage Cells,
Cascading of channels allows deeper sampling depth
Differential Inputs with 450 MHz Bandwidth
Readout speed: 33 MHz
Region-Of-Interest readout mode for shorter dead time
Multiplexed or parallel analog outputs
Low Power: 50 mW at 2 GSPS
Low Integral Nonlinearity: $0.5x10^{-3}$ at 0.1 V to 1.1 V Range
High SNR: 69 dB after Offset Correction
Low Noise: 0.35 mV after Offset Correction

APPLICATIONS
Instrumentation and Measurement
Photomultiplier, Drift Chamber and APD Readout
Low Cost Digital Oscilloscopes
Ultrasound Equipment
Handheld Oscilloscopes

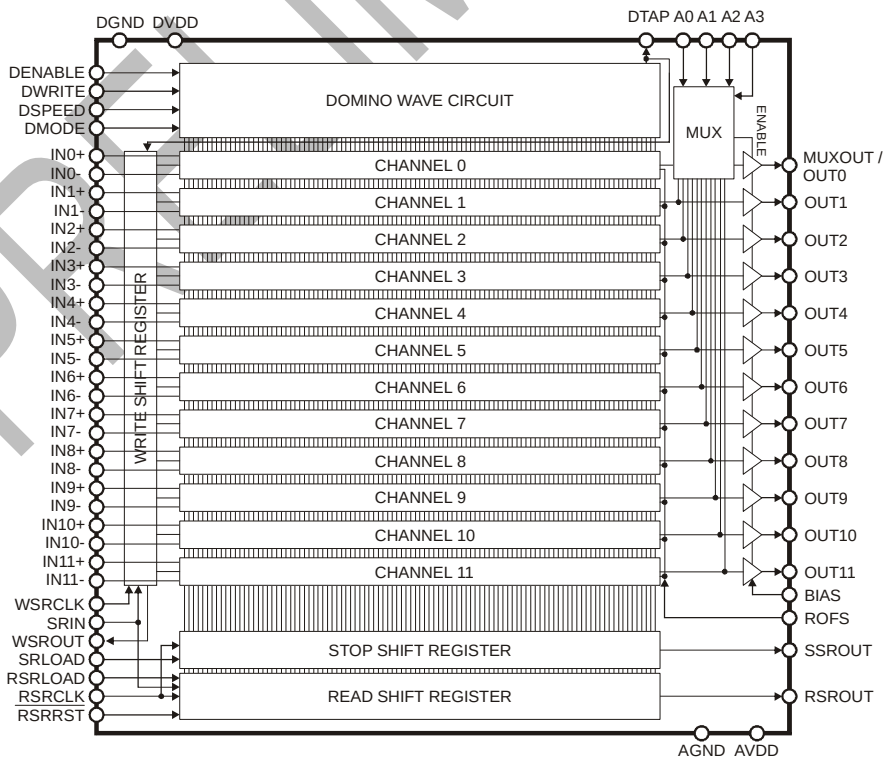
PRODUCT DESCRIPTION

The DRS3 is a switched capacitor array (SCA) capable of sampling 12 differential input channels at a sampling speed of 10 MSPS to 5 GSPS. The analog waveform is stored in 1024 sampling cells per channel, and can be read out after sampling via a shift register clocked at 33 MHz for external digitization.

The write signal for the sampling cells is generated by a chain of inverters (domino principle) generated on the chip. The domino wave is running continuously until stopped by a trigger. A read shift register clocks the contents of the sampling cells either to a multiplexed or to individual outputs, where it can be digitized with an external ADC. It is possible to read out only a part of the waveform for reducing the digitization time.

The high channel density, high analog bandwidth of 450 MHz and low noise of 0.35 mV (after offset calibration) makes this chip ideally suited for low power, high speed, high precision waveform digitizing. Fabricated on an advanced CMOS process in a radiation hard design, the DRS3 is available in a 64-lead low profile quad flat pack (LQFP) and a 64-pin quad flat non-leaded package (QFN).

FUNCTIONAL BLOCK DIAGRAM



REV. 1

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SPECIFICATIONS

(AVDD = 2.5 V, DVDD = 2.5 V, Temp. = 25°C, unless otherwise noted)

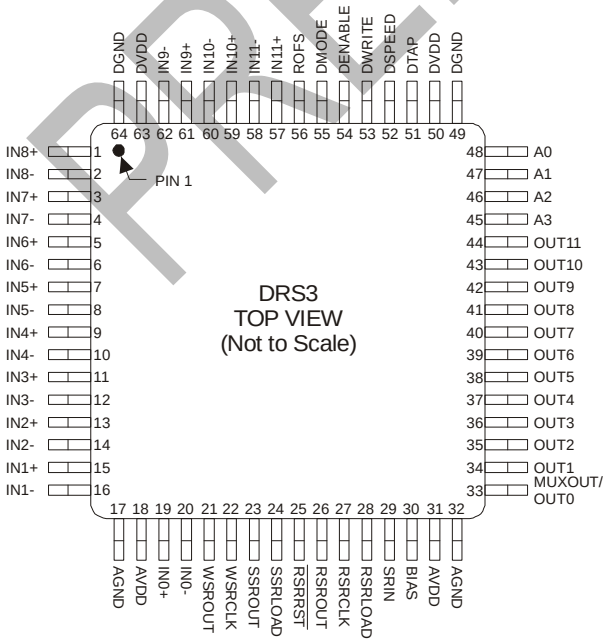
Parameter	Typ.	Unit	Comment
DRS3			
Sampling speed f_{SAMP}	0.01	GSPS min	
	5	GSPS max	
Readout speed	10	MHz min	Optimal Performance at 33 MHz
	40	MHz max	
Fixed pattern offset error	5	mV rms	
Random noise	0.35	mV rms	After offset correction
Signal-to-Noise Ratio (SNR)	69.1	dB	After offset correction
Effective number of bits	11.5	Bits	After offset correction
Gain	0.982	V/V min	
	0.988	V/V max	
Integral Nonlinearity	0.5	mV	Input Range 0.1 V – 1.1 V, BIAS = 0.70 V
	10	mV	Input Range 0 V – 1 V, BIAS = 0.70 V
Fixed pattern timing jitter	TBD	ps	f_{SAMP} = 0.5 GHz
	TBD	ps	f_{SAMP} = 2 GHz
	TBD	ps	f_{SAMP} = 5 GHz
Random pattern timing jitter	TBD	ps	f_{SAMP} = 0.5 GHz
	TBD	ps	f_{SAMP} = 2 GHz
	TBD	ps	f_{SAMP} = 5 GHz
TEMPERATURE DRIFT			
Offset Error	75	µV/°C	Tested between 25° C and 50° C
Gain Error	25	ppm/°C	Tested between 25° C and 50° C
ANALOG INPUTS			
Input Span	1	V p-p	
Absolute Voltage Limits	AGND – 300 mV	V min	
	AVDD + 300 mV	V max	
Linear Range	0.1 – 1.1	V	Optimal Performance, ROFS = 0.85 V
	0 – 1	V	Reduced Linearity, ROFS = 0.95 V
Input Capacitance	TBD		
Input Current	TBD		
Bandwidth (-3dB)	450	MHz	
Crosstalk	< -46	dB	1 ns rise-time pulse driven differentially
	-40	dB	1 ns rise-time pulse driven non-differentially
TIMING CHARACTERISTICS			
t_{DTAP}	$2048 \times 1/f_{SAMP}$	s	
t_{CLK}	1	µs max	Clock speed for all shift registers
	2	ns min	
t_O	10	ns	RSRCLK Rising Edge to Analog Output
t_{SAMP}	t_O+t_{CLK}		For optimal performance, use t_{CLK}=30 ns and sample analog signal 38 ns after RSRCLK
t_{RST}	10	ns min	$\overline{\text{RSRRST}}$ Pulsewidth
POWER REQUIREMENTS			
AV_{DD}	2.5	V	
DV_{DD}	2.5	V	
DI_{DD}	0.5	mA	Domino wave stopped (Standby)
	4.4	mA	Running at 0.5 GSPS
	6.7	mA	Running at 1 GSPS
	11.2	mA	Running at 2 GSPS
	24.9	mA	Running at 5 GSPS
AI_{DD}	1.6	mA	A0-A3=1 (Standby)
	14.9	mA	Running at 2 GSPS, 10 Hz trigger rate, single channel readout
	38	mA	Running at 2 GSPS, 10 Hz trigger rate, parallel channel readout

PIN FUNCTION DESCRIPTIONS

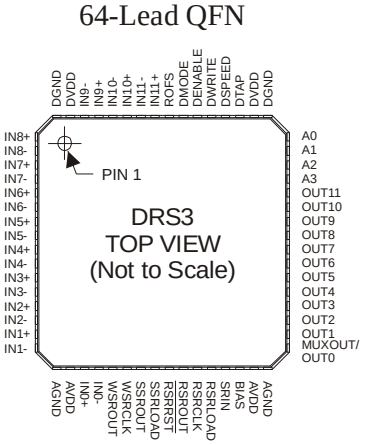
Pin Number	Mnemonic	Description
1	IN8+	Analog Input Channel 8 (+)
2	IN8-	Analog Input Channel 8 (-)
3,5,7,9,11,13,15	IN7+ – IN1+	Analog Input Channels 7 – 1 (+)
4,6,8,10,12,14,16	IN7- – IN1-	Analog Input Channel 7 – 1(-)
17,32	AGND	Analog Ground
18,31	AVDD	Analog Power Supply, 2.5 V Nominal
19	IN0+	Analog Input Channel 0 (+)
20	IN0-	Analog Input Channel 0 (-1)
21	WSROUT	Write Shift Register Output
22	WSRCLK	Write Shift Register Clock
23	SSROUT	Stop Shift Register Output
24	SSRLOAD	Stop Shift Register Load
25	$\overline{\text{RSRRST}}$	Read Shift Register Reset
26	RSROUT	Read Shift Register Output
27	RSRCLK	Read Shift Register Clock
28	RSRLOAD	Read Shift Register Load
29	SRIN	Common Shift Register Input
30	BIAS	Bias voltage for internal buffers. Use internal voltage of 0.68 V if left open. If connected to a low impedance voltage source overwrites the internal bias voltage.
33	MUXOUT/OUT0	Multiplexed Analog Output/Analog Output Channel 0
34 – 44	OUTx	Analog Output Channel 1 – 11
45,46,47,48	A3,A2,A1,A0	Address bits, see *Table 1*
49,64	DGND	Digital Ground
50,63	DVDD	Digital Power Supply, 2.5 V Nominal
51	DTAP	Domino tap signal toggling on each domino revolution
52	DSPEED	Analog Setting Voltage for Domino Speed
53	DWRITE	Domino Write Input. Connect the Domino Wave Circuit to the write switches if high. Also used to initialize the write shift register.
54	DENABLE	Domino Enable Input. A low-to-high transition starts the Domino Wave. Setting this input low stops the Domino Wave.
55	DMODE	Domino Mode Input. Low for a single revolution, high for continuously running Domino Wave.
56	ROFS	Read Offset Voltage Input. Used to shift the contents of the sampling capacitors into the linear range of the output buffers.
57,59,61	IN11+ – IN9+	Analog Input Channels 11 – 9 (+)
58,60,62	IN11- – IN9-	Analog Input Channels 11 – 9 (-)

PIN CONFIGURATION

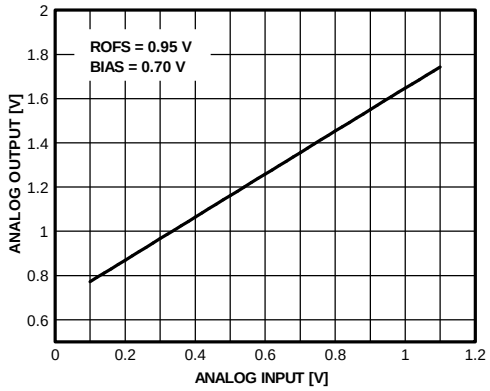
64-Lead LQFP



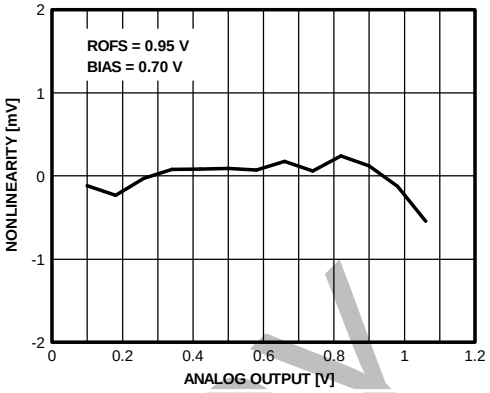
64-Lead QFN



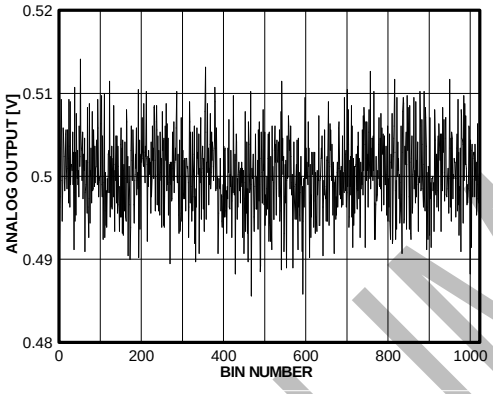
Typical Performance Characteristics



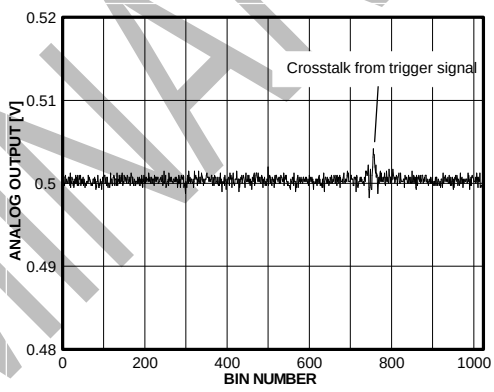
Plot 1. Analog Output vs. Analog Input



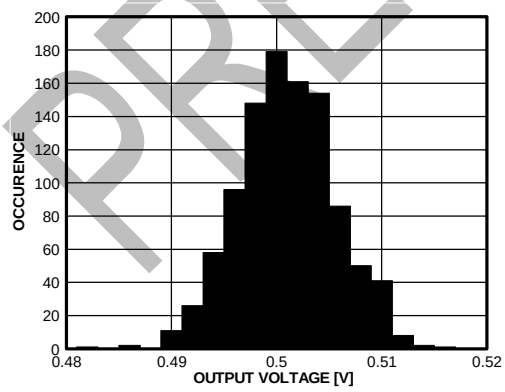
Plot 2. Nonlinearity



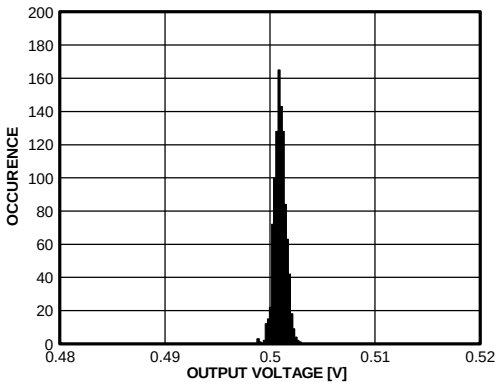
Plot 3. 0.5 V DC signal sampled at 5 GSPS before offset correction



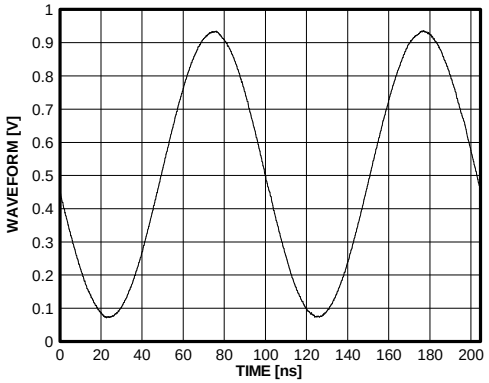
Plot 4. 0.5 V DC signal sampled at 5 GSPS after offset correction



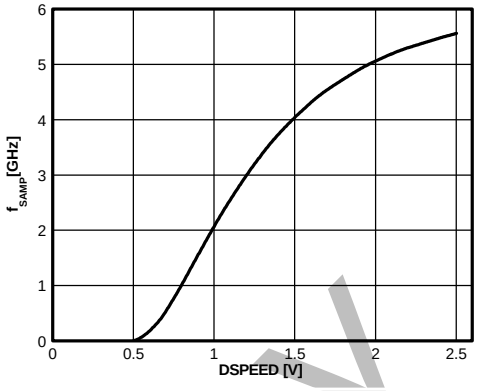
Plot 5. Noise Histogram before offset correction



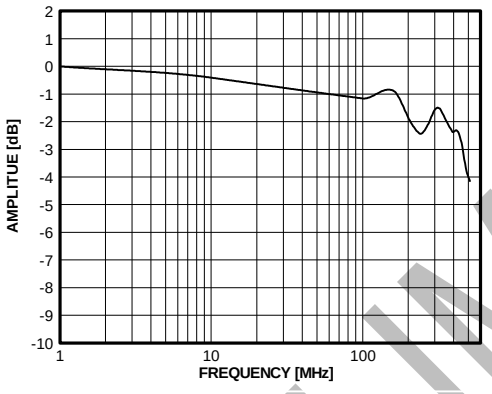
Plot 6. Noise Histogram after offset correction. The distribution is a convolution of the DRS3 noise and the AD9238 ADC noise.



Plot 7. 5 MHz sine wave sampled at 5 GSPS



Plot 8. Sampling Speed vs. DSPEED Voltage



Plot 9. Signal Frequency Response

THEORY OF OPERATION

The DRS3 consists of an on-chip inverter chain generating a sampling frequency up to 5.5 GHz (domino wave circuit), eliminating the need to feed an external sampling clock in the GHz range into the chip. This signal opens write switches in all 12 sampling channels, where the differential input signal is sampled in small (200 fF) capacitors. After being started, the domino wave runs continuously in a circular fashion until stopped by a trigger signal, which freezes the currently stored signal in the sampling capacitors. The signal is then read out via a read shift register for external digitization.

DOMINO WAVE CIRCUIT

The domino wave circuit is basically a series of 1024 double inverters. After raising the DENABLE signal high, a wave traverses through these inverters producing the write signal for the sampling cells. *Figure 1* shows a simplified schematics of two double inverter blocks.

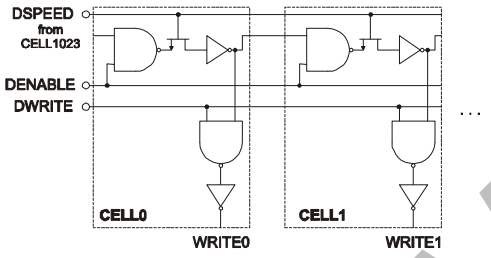


Figure 1. Simplified schematics of two out of 1024 double inverter blocks forming the domino wave circuit

The first inverter is actually an AND gate. This allows to enable and to stop the domino wave at any time via the DENABLE signal. The AND gate is connected to the following inverter via an NMOS transistor operating as a voltage controlled resistor. This resistor forms with the parasitic input capacitance of the inverter a RC-circuit, imposing a variable delay for the propagation of the domino wave, which can be controlled by the analog voltage DSPEED. Since the actual domino wave speed depends on the power supply voltage and the temperature, some stabilization is necessary to ensure steady operation. For this purpose the DTAP signal is available, which toggles its state each time the domino wave reaches cell #512. If operating the chip at f_{DMONIO}, the DTAP outputs a rectangular signal with 50% duty cycle with a frequency according to following formula:

$$f_{DTAP} = 2 \times 1024 \times f_{DOMINO}$$

This signal can be used by an external PLL circuit to lock the domino frequency and phase to a quartz generated frequency. An alternative approach is to feed this signal into a frequency counter implemented in a FPGA, and to correct the DSPEED signal via a 16-bit DAC in case of a deviation.

The domino wave gets started by raising the DENABLE signal high. An internal circuit ensures that the write signal is always 16 cells wide. If DMODE is high, the domino wave runs infinitely until being stopped by setting DENABLE low. If DMODE is low, the domino wave only propagates once through each cell and stops after cell 1023. In this case only a signal low-to-high transition at cell 512 is seen at the DTAP output. The DWRITE signal determines if the write signal is sent to the sampling cells. If using an external PLL circuit, it might be advantageous to keep the domino wave running during the readout phase. This can be achieved by keeping DENABLE high and only lowering DWRITE to stop the sampling process. In this case, the DTAP signal is also produced by the revolving domino wave during readout. Care has however be taken that the DTAP signal does not interfere with the analog output of the DRS3 chip and therefore degrading the signal quality.

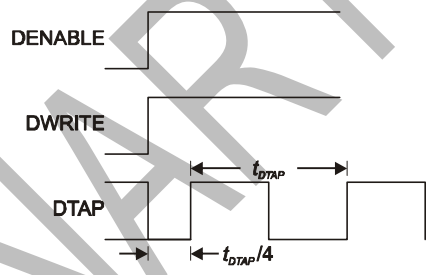


Figure 2. Timing of the Domino Wave Circuit

Domino Wave Jitter

A small timing jitter is present between the double inverter blocks. This jitter is composed of a constant deviation for each cell (the so-called "fixed pattern jitter") arising from the mismatch of the transistors in each cell, and a variable term for each domino revolution. While the overall jitter can be minimized by using an external PLL, a cell-to-cell variation will still be present. If applications require high timing accuracy, the fixed pattern jitter can be calibrated and corrected for. Since one domino wave circuit controls all 12 channels inside the DRS3, only one channel for each DRS3 chip needs to be calibrated. One possibility to do this is to sample a high accurate sine wave with the DRS3 chip, and look for deviations between the sampled waveform and the ideal one obtained from a sine fit of all samples. Averaging over many waveforms at different phases of the sine wave, the fixed pattern jitter can be measured and stored for calibration in a database for example.

An additional complication might arise from the fact that the domino wave can only be stopped between cells. This gives a timing accuracy of $1/f_{DOMINO}$. If higher accuracy is needed, it is recommended to sample a highly stable clock signal in one of the 12 channels of each DRS3 chip. By fitting the edges of this clock signal, the actually sampling frequency and phase for each waveform can be measured preciselsy, and a timing accuracy below 100 ps can be achieved.

ANALOG INPUTS

Each sampling cell consists of a sampling capacitor with C_s = 200 fF connected to the IN+ and IN- inputs via two NMOS transistors (*Figure 3*). This allows a quasi differential input, given than both input signals do not exceed

the rails of the power supply. After the sampling cycle, the capacitor stores the voltage

$$U_s = U_{IN+} - U_{IN-}$$

Since the NMOS transistors show a nonlinear behavior when approaching the rails, it is recommended to operate them 100 mV away from the lower rail. The full range is limited by the linearity of the buffer in each cell, which shows a non-linearity better than 0.5 mV for an input voltage between 1.05 V and 2.05 V. If signals smaller than 1.05 V should be sampled, it is possible to shift U_s up by applying an external voltage ROFS during the readout phase. This works similar like a charge pump, lifting the bottom plate of the capacitor from IN- to ROFS. The voltage seen by the buffer during readout is therefore

$$U'_S = U_{IN+} - U_{IN-} + U_{ROFS}$$

An input range of 0.1 V to 1.1 V can therefore be obtained for example by applying 0.95 V to the ROFS input. This shifts the input signal into the linear range of 1.05 V to 2.05 V of the cell buffer. The DRS3 has an additional buffer at each analog output, which then shifts this output to a range from approximately 0.8 V to 1.8 V. The overall gain of the analog chain is 0.985.

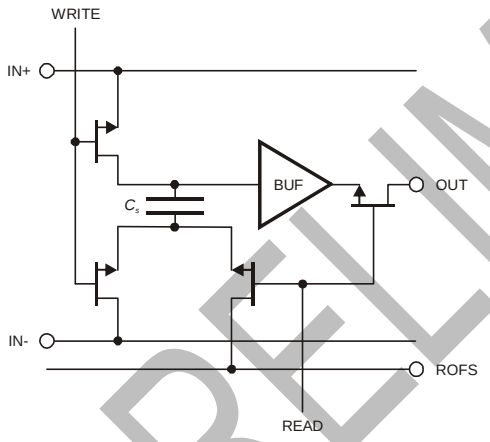


Figure 3. Simplified Schematics of one Sampling Cell

It should be noted that the charge stored in the sampling capacitor is lost over time due to charge leakage, and the readout of a cell should be done quickly (< 1 ms) after the sampling phase.

CASCADING OF CHANNELS

It is possible to cascade two or more channels to obtain deeper sampling depth with the cost of fewer channels. The sampling cells on DRS3 can be cascaded according to *Table 1*.

A write shift register containing 12 bits is used to activate each channel. The bits are rotated by one position on each revolution of the domino wave. If this register is loaded with 1's, all channels are active all the time, and the DRS3 works like having 12 independent channels. The other extreme is a single 1 loaded into the register. This 1 is clocked through all 12 positions consecutively. This means that on the first domino revolution the first channel is active, on the second domino revolution the second channel is active and so on. If the input signal gets fanned out into each of the 12 channels, the DRS3 chip works like having a single channel with 12 times the sampling depth.

Table 1. Cascading of Channels

Number of channels	Number of sampling cells per channel	Initial write shift register bit pattern
12	1024	111111111111_b
6	2048	101010101010_b
4	3072	100100100100_b
3	4096	100010001000_b
2	6144	100000100000_b
1	10288	100000000000_b

To bring the write shift register in one of the above states, the bit pattern according to *Table 1* has to be written into the register initially according to the timing diagram given in *Figure 4*.

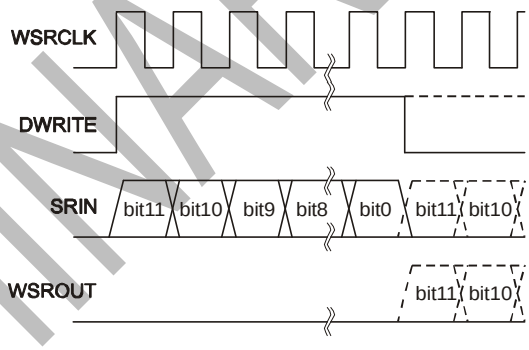


Figure 4. Write Shift Register Timing Diagram

Writing to the shift register is enabled by setting DWRITE high. Twelve bits are then clocked into the shift register, MSB first. Bits are latched into the shift register on the falling edge of WSRCLK. To ensure proper working of the shift register, the DWRITE signal can be kept high for more than 12 clock cycles, in which case the bits are clocked out of the chip via the WSROUT signal (dashed lines). In this case the bits must be reapplied at the SRIN input again for proper operation.

After the domino wave has been started via the DENABLE signal, the bit pattern is rotated one position on each revolution of the domino wave. If the domino wave gets stopped by setting DENABLE low, it can happen at any state of the shift register. To test in which state the shift register has been stopped, a timing diagram similar to *Figure 4* must be used to clock out the last state of the shift register. Twelve clock cycles reveal the 12 current bits at WSROUT when DWRITE is kept high.

WAVEFORM READOUT

After sampling has been stopped by either setting DENABLE or DWRITE low, the waveform can be read out via the read shift register. To do so, a single "1" is clocked into the shift register, followed by 1024 clock cycles at 33 MHz. Care has to be taken in the PCB design that the DENABLE, DWRITE and DTAP signals are far away from the analog inputs. Otherwise some crosstalk between these signals and the analog input channels may occur, as can be seen in *Plot 4*.

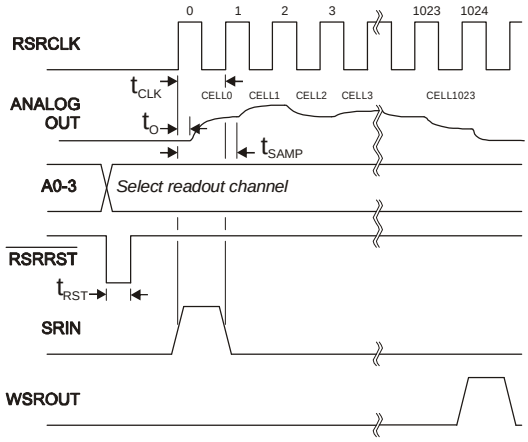


Figure 5. Readout Shift Register Timing Diagram

Pulling $\overline{\text{RSRRST}}$ low for at least 10 ns while RSRCLK and SRIN are low erases the contents of the read shift register. A "1" is clocked into the first cell of the register at the falling edge of RSRCLK. This "read bit" is then shifted down on each consecutive clock cycle, until it appears at the 1024th cycle at WSROUT indicating successful operation of the shift register. On the rising edge of RSRCLK at each clock cycle the contents of the next sampling cell appears at the analog output MUXOUT after a delay of t_O = 10 ns if the multiplexer is used. When operated at 33 MHz clock speed (t_{CLK} = 30 ns), the analog signal has 30 ns to settle at the output. Care must be taken to sample it with an external flash ADC at the end of this 30 ns period, but just before the beginning of the next cycle. So with $t_{SAMP} = t_O + t_{CLK}$ = 40 ns the sampling should occur about 38 ns after the rising edge of RSRCLK. Sampling the signal after 35 ns already degrades the DRS3 linearity.

Since each sampling cell contains a buffer at the output, an offset error from that buffer is seen due to the mismatch of the transistors inside the buffer, which is typically 5 mV rms (*Plot 3*, *Plot 5*). Since this offset error is constant over time ("fixed pattern noise"), it can be measured and corrected for during the readout. One example to do this is to put an offset correction table into the FPGA which does the readout of the ADC connected to the DRS3. This way the noise can be reduced by more than one order of magnitude. Care has to be taken to choose an ADC which matches the performance of the DRS3. Many 12-bit ADCs have a SNR which is lower than 70 dB and would therefore not give optimal performance.

CHANNEL MULTIPLEXER

Four address bits A0-A3 are used to configure the analog output. In multiplexed mode, each channel's analog output can be routed to one single output MUXOUT, making it possible to use only a single external ADC to digitize all 12 channels. If digitization time however is important, all 12 channels can be digitized in parallel using 12 external ADCs, thus reducing the digitization time by a factor of 12.

TABLE 2. Address Bit Settings

A0	A1	A2	A3	Output
0	0	0	0	Channel 0 at MUXOUT
1	0	0	0	Channel 1 at MUXOUT
0	1	0	0	Channel 2 at MUXOUT
1	1	0	0	Channel 3 at MUXOUT
0	0	1	0	Channel 4 at MUXOUT
1	0	1	0	Channel 5 at MUXOUT
0	1	1	0	Channel 6 at MUXOUT
1	1	1	0	Channel 7 at MUXOUT
0	0	0	1	Channel 8 at MUXOUT
1	0	0	1	Channel 9 at MUXOUT
0	1	0	1	Channel 10 at MUXOUT
1	1	0	1	Channel 11 at MUXOUT
0	0	1	1	Don't use (internal test purpose only)
1	0	1	1	Don't use (internal test purpose only)
0	1	1	1	Enable OUT0-OUT11
1	1	1	1	Disable all outputs (standby)

Setting all address bits to one disables all analog output drivers, reducing the power consumption to 2 mA for the complete chip.

REGION-OF-INTEREST READOUT MODE

The digitization of all 1024 samples at 33 MHz takes 30 µs, even if the 12 channels are digitized in parallel. During this time the sampling of the DRS3 is stopped and no new waveforms can be acquired. If this dead time is not acceptable, two or more DRS3 systems can be run in parallel connected to the same signal channel. If one DRS3 is stopped for readout, the others are still active. The overall dead time can therefore be reduced. Another approach is to read only a subset of all sampling cells, for applications where one is interested only in short pulses like illustrated in *Figure 6*.

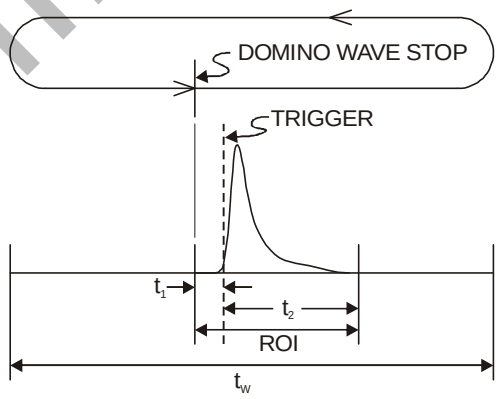


Figure 6. Region-of-Interest (ROI) Readout Mode

Assume that the domino wave is running with a window size $t_W = 1/f_{SAMP} \times 1024$, and a short signal occurs, like a hit from a photomultiplier. This signal triggers an external trigger circuit, similar like in an oscilloscope. The interesting part of the waveform is now in a region t_1 before and t_2 after that trigger point. If only this ROI is read out, the dead time will be reduced by the fraction $(t_1+t_2)/t_W$. To achieve this with DRS3, the domino wave has to be stopped t_W-t_1 after the trigger by means of an external delay. The stop position of the domino wave is then transferred into the readout shift register via a pulse on the RSRLOAD pin. The readout starts at this position and can be stopped after *n* samples when the complete ROI is covered. *Figure 7* shows the timing for this readout mode.

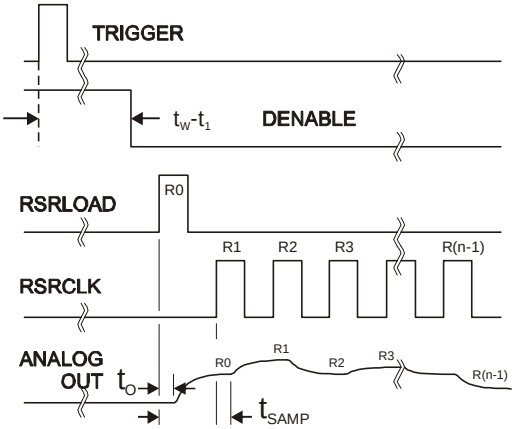


Figure 7. Timing Diagram for ROI Readout

The rising edge of the RSLOAD pin transfers the first sample R0 of the ROI to the analog output, where it can be digitized after (t_{SAMP}.- 2ns). Consecutive pulses on RSRCL transfer following samples R_i, until all *n* samples are digitized. This sequence can be repeated 12 times to digitize all channels if multiplexing is used. Each pulse on RSLOAD re-transfers the domino wave stop position into the read shift register, so the same ROI can be digitized on all channels. If the read bit arrives at cell #1023, it is seen at the RSROUT output, and then wraps around automatically into cell #0.

If offset correction is applied during readout, one must know which cell is currently visible at the analog output, since each cell has a different offset error. If the domino wave stop happens close to the end of the cell array, the ROI might overlap with cell #1023 and the read bit can be detected during the normal ROI readout. If the read bit appears after n clock cycles, the domino stop happed at cell #(1023-n), and the offset correct for that cell should be applied to the first readout value. If the domino stop however happens at the beginning of the cell array, the read bit will never be visible at RSROUT, since for each channel it is re-set via the RSLOAD pulse. One possibility to solve this problem is to apply more read pulses after the last ROI readout if multiplexed readout is used. Assuming the domino stop happens at cell #700 and the ROI is 100 cells wide, the read bit will be shifted from cell #700 to #800 for each individual channel readout. After the last ROI readout, it will sit at cell #800, and additional 223 clock cycles will shift it to cell #1023, where it can be detected via the RSROUT output. The total time of the readout will therefore take 12×100+223 clock cycles or 43.1 µs at 33 MHz readout speed. If the domino wave stop position is randomly scattered around all cells, the average amount of clock cycles will be 12×100+512 or 51.9 µs.

One possibility to reduce this time is to increase the shift register clock speed from 33 MHz to higher values up to several hundred MHz. This can however make the FPGA readout design more complicated. Another approach is to use the dedicated "stop shift register" which has been implemented in DRS3. This register is loaded similar to the read shift register via SSRLOAD pulse, and has a dedicated output SSROUT at cell #1023. It is now possible to load this register *only* on the first channel readout. Taken the example from above, the read bit will be shifted from cell #700 to #800 during the first ROI readout. If the SSRLOAD is omitted between individual channels, the read bit will be shifted from cell #800 to #900 on the second channel and to cell #1000 on the third channel. After the 23 more clock cycles it will appear at SSROUT. One can now calculate the domino stop position as 1023-3×100+23=700. This readout mode requires no additional clock cycles after the last channel, so the total readout time is 12×100 clock cycles or 36.4 µs at 33 MHz. The timing for this example is shown in *Figure 8*.

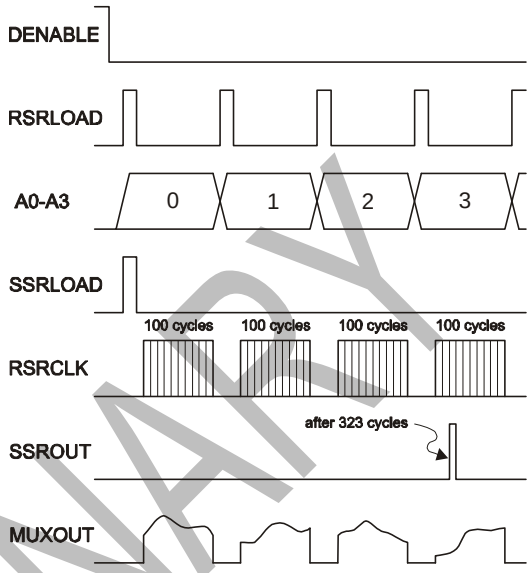
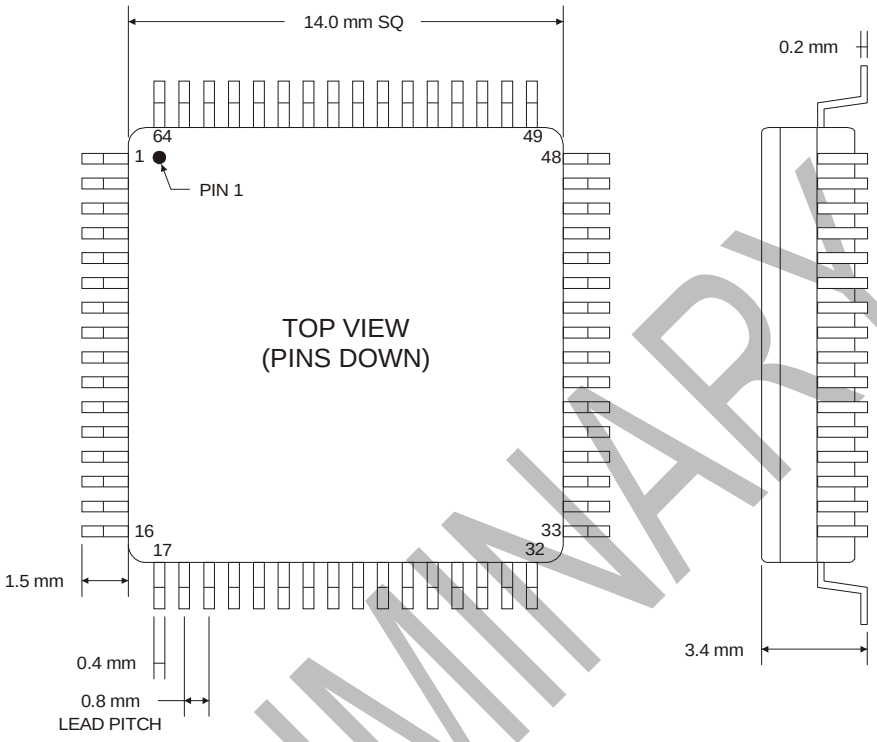


Figure 8. Timing Diagram using the Stop Shift Register

This method reduces the average readout time by about 30% for a ROI of 100 cells.

OUTLINE DIMENSIONS

64-Lead Low Profile Quad Flat Pack (LQFP)



64-lead quad flat non-leaded package (QFN)