Quality Control Development for MuPix11 for the Mu3e Detector

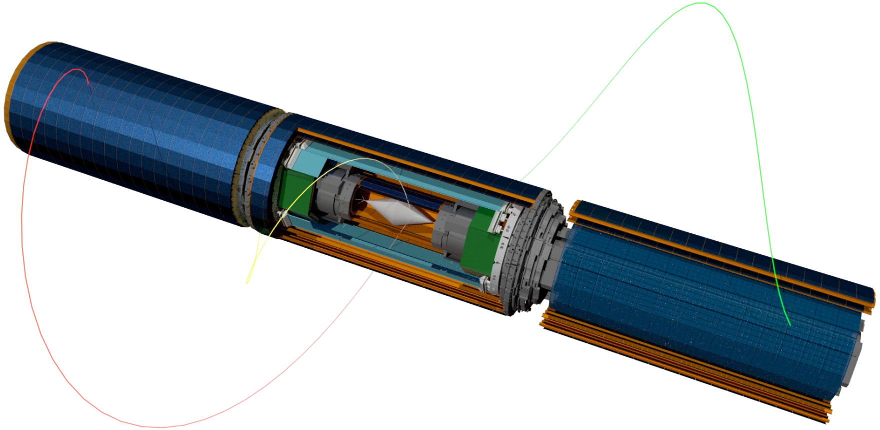
Anna Lelia Fuchs | PI Uni Heidelberg

On behalf of the Mu3e collaboration

Deutsche Forschungsgemeinschaft

The Mu3e Experiment

- Search for the cLFV $\mu^+ \rightarrow e^+e^-e^+$ decay
- SM Branching fraction $< 1 \times 10^{-54}$
- Evidence of physics *beyond the standard model.*
- Tracking detector requirements:
  - Momentum resolution < 0.5 MeV
  - Low material budget



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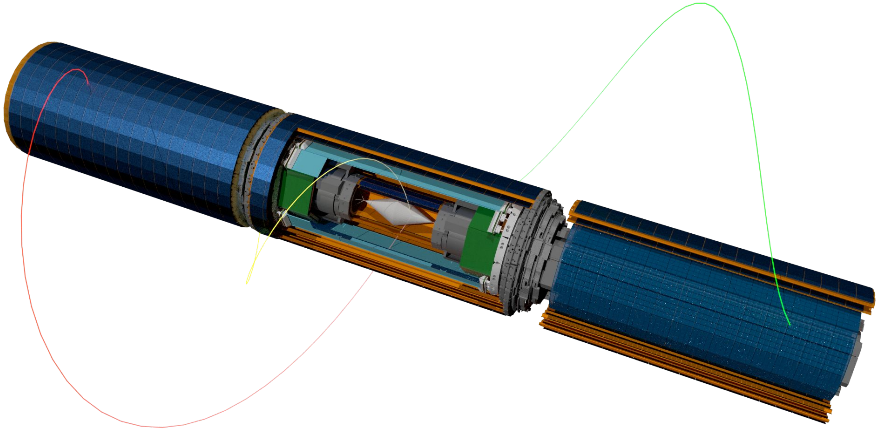

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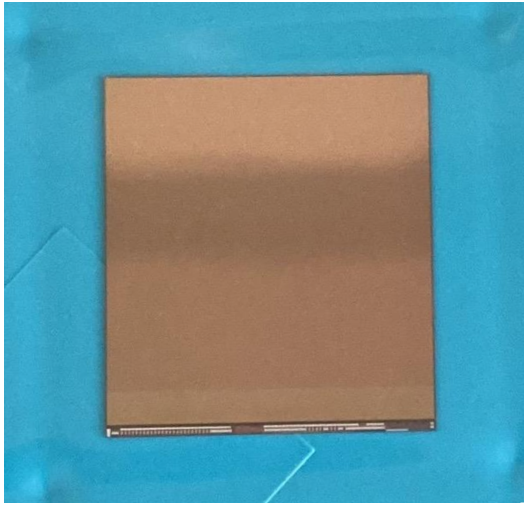
This will be achieved using 2844 MuPix11 pixel sensors.

The MuPix11 Sensor

A pixel sensor with High-Voltage Monolithic Active Pixel Sensor (HV-MAPS) technology at 50 µm / 70 µm.



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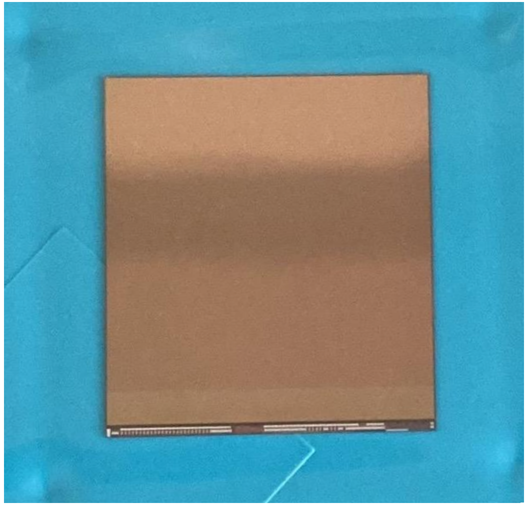

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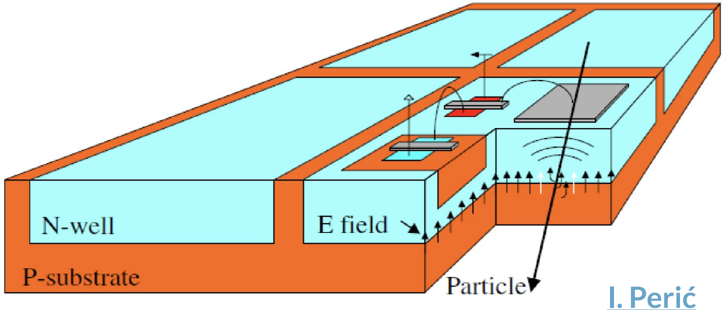

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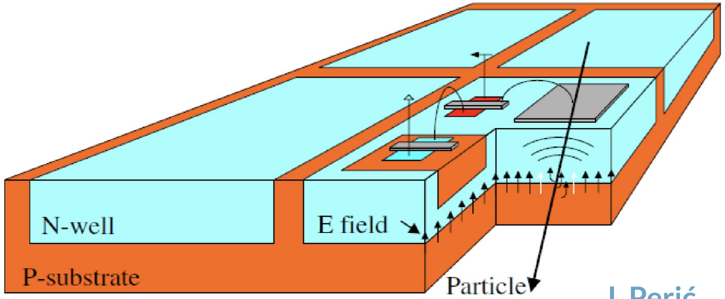

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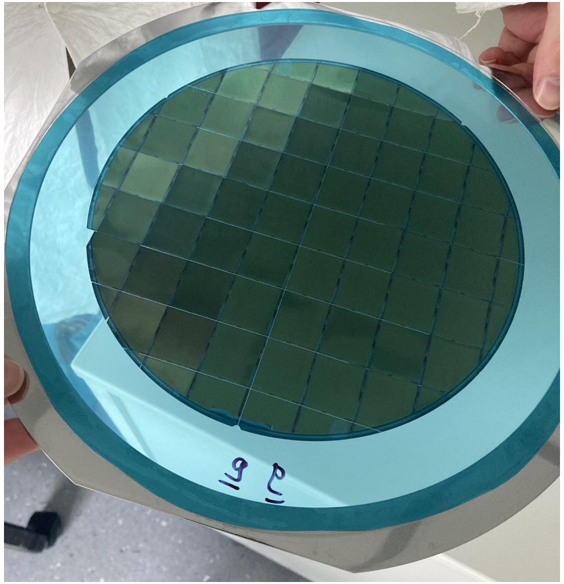
The functionality of each sensor must be verified before installation.

The MuPix 11 Quality Control Strategy

Aim: To evaluate if a sensor can perform the functions necessary for operation in the Mu3e detector.



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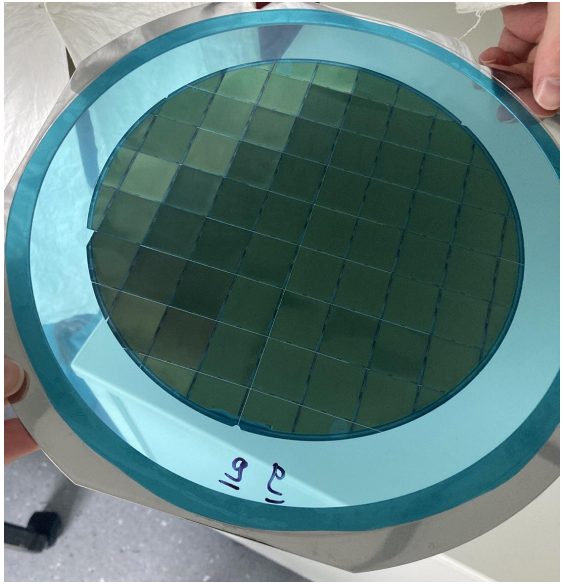

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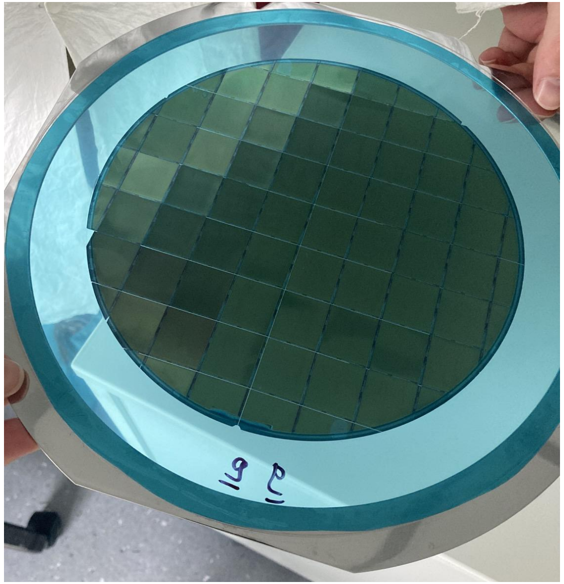

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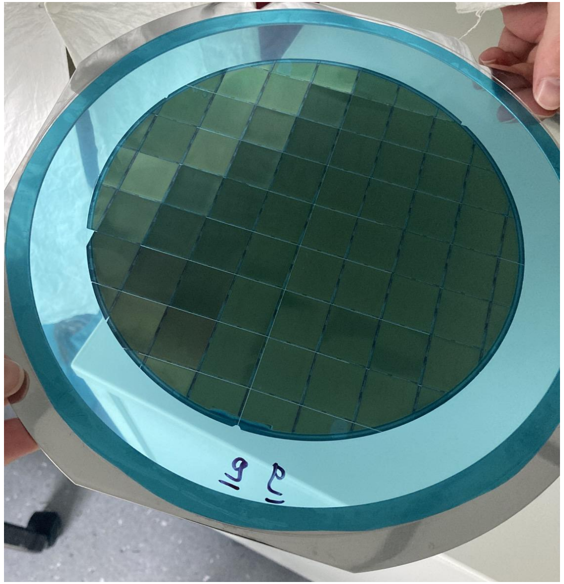
- A sensor which passes all tests passes the quality control.



The Experimental Setup

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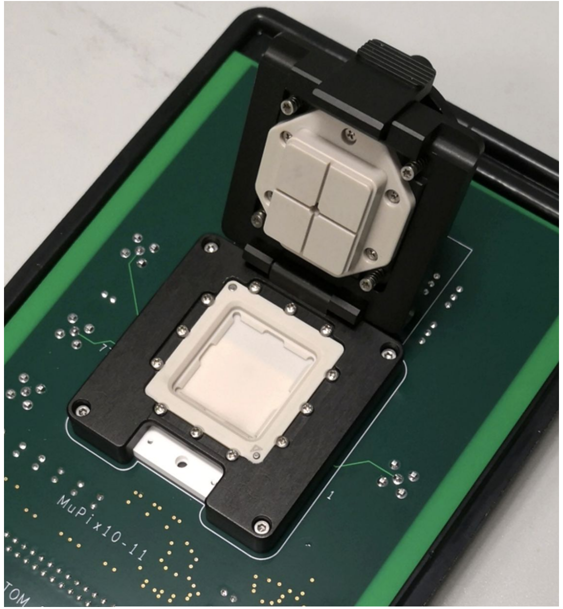

Probe card for MuPix11 QC

L. Vigani

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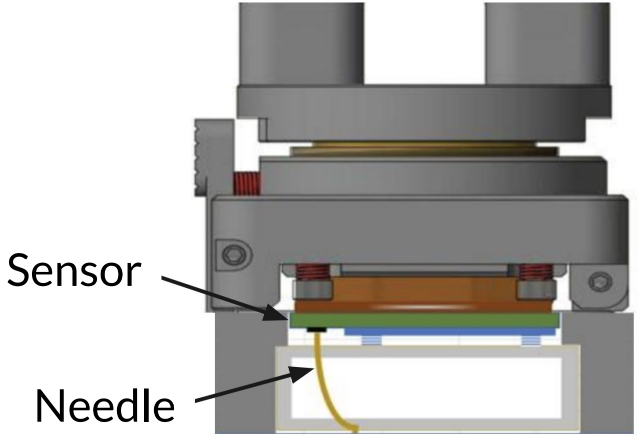
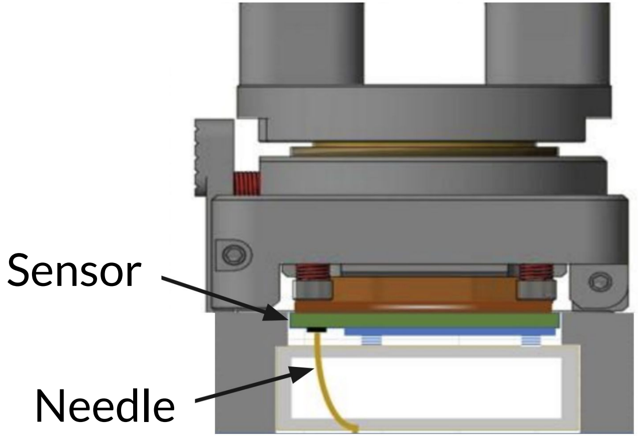


Probecard: side view

Source: PTSL

The Experimental Setup

- Temporary, non-invasive connection
- Probe card with a needle mechanism
- Quick testing of multiple chips



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Development of the Quality Control

Developing evaluation strategies → Improving for accuracy → Optimisation for speed

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- Identify key functions
- Identify functionality indicators
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- Reduction of errors in testing
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Developing evaluation strategies

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- Identify functionality indicators
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Improving for accuracy

- Investigation of failure modes
- Reduction of errors in testing
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Optimisation for speed

- Target functionality indicators
- Remove excess measurements

Developing Evaluation: The IV Scan

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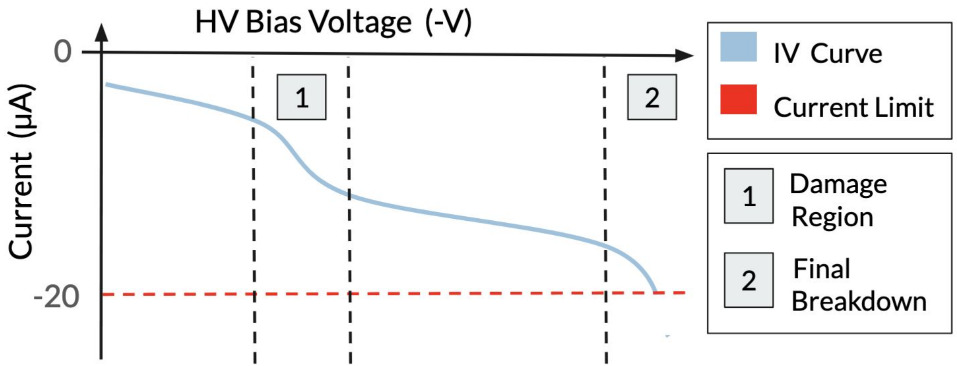

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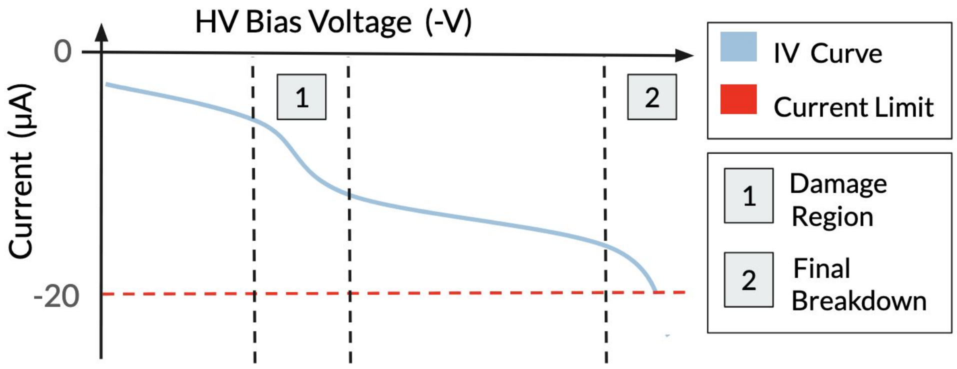

Evaluation:

- Is a suitable bias voltage reached?
- What is the necessary bias voltage?

Improving for Accuracy: The Contact Strategy

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Fixed contact strategy

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- Contact is a frequent failure mode.

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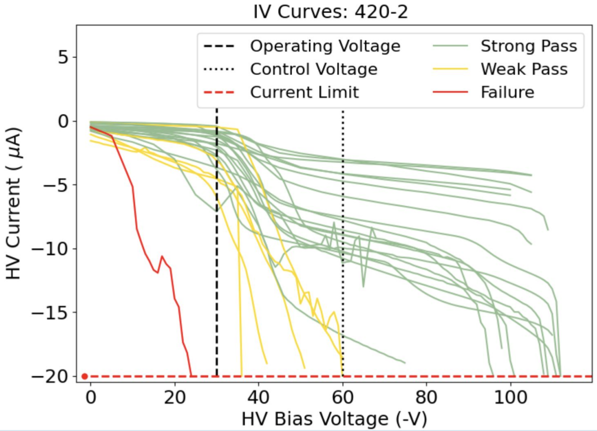

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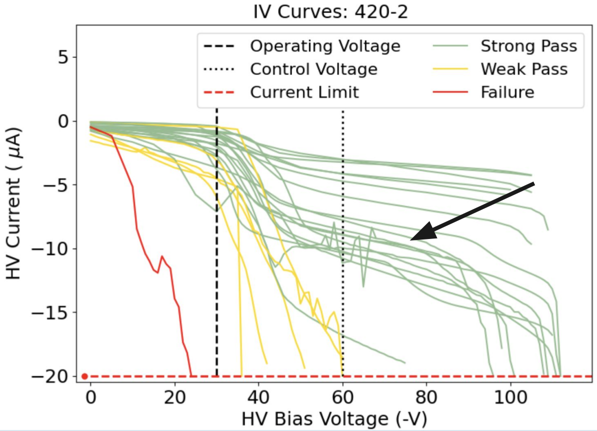

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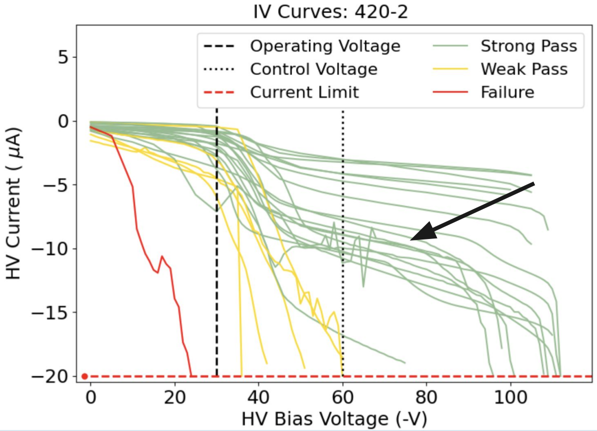

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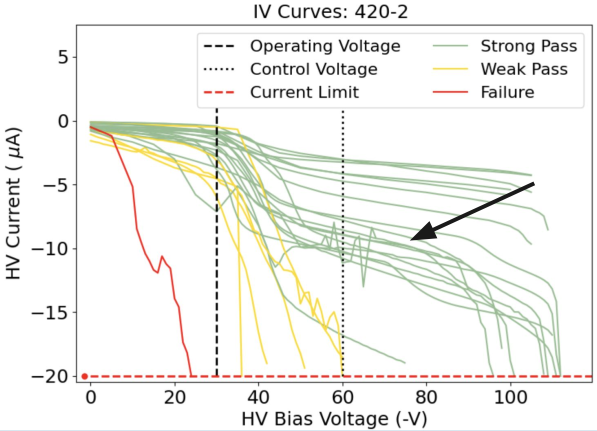

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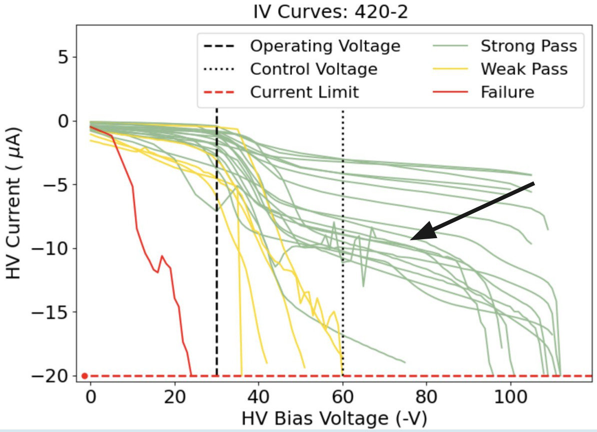

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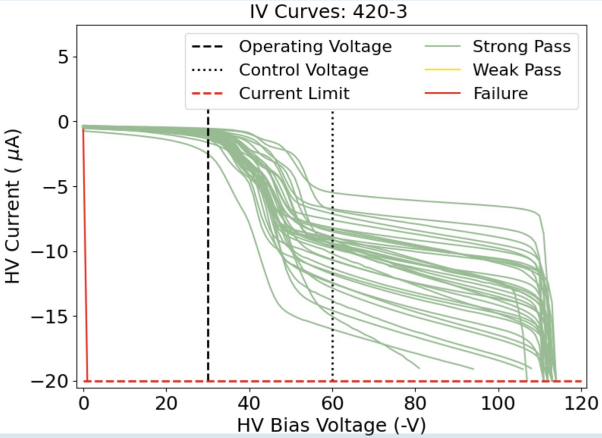

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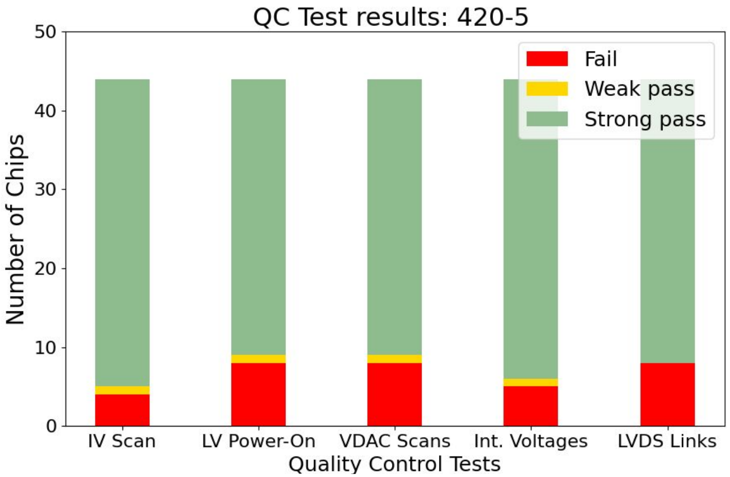

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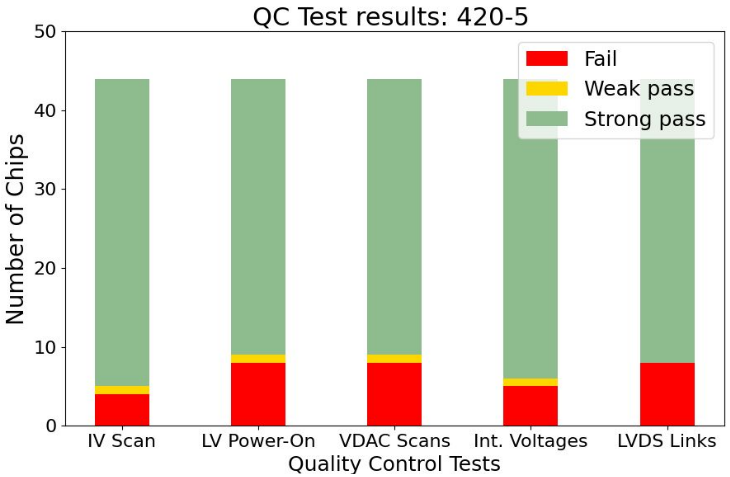

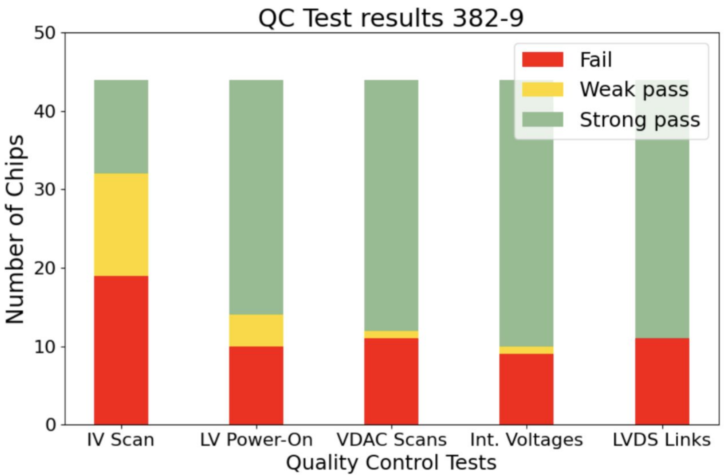

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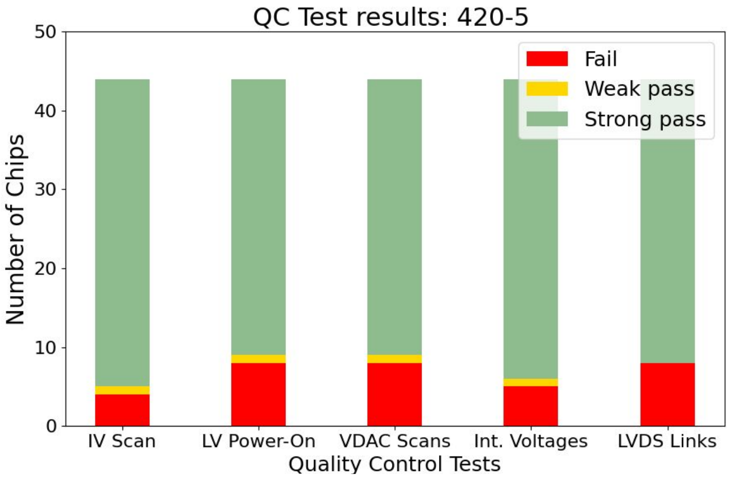
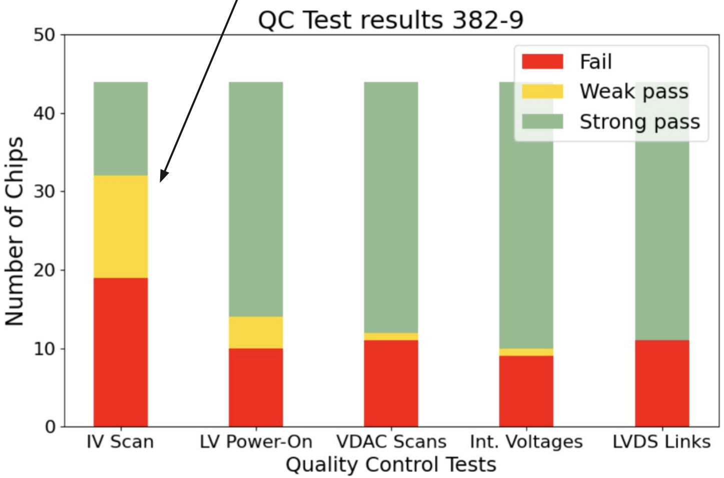
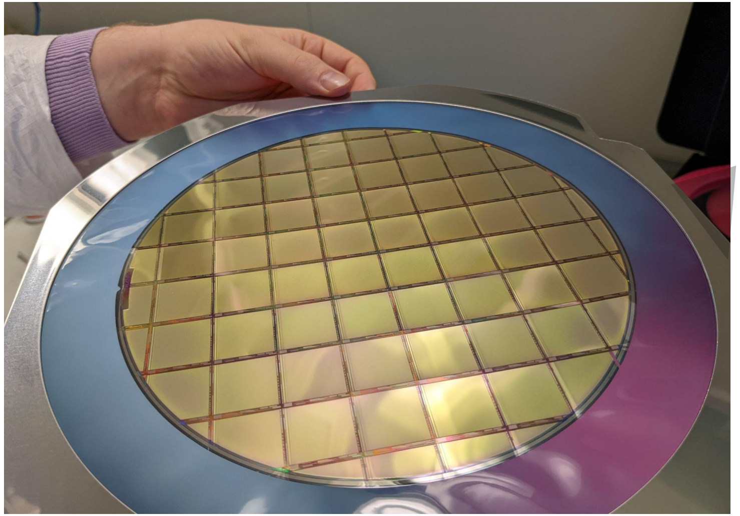




50 µm

Summary and Outlook



B. Weinläder

Summary and Outlook

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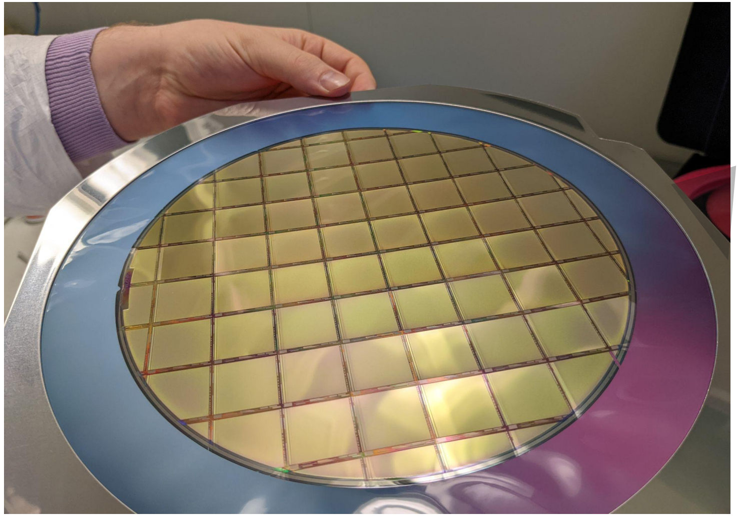

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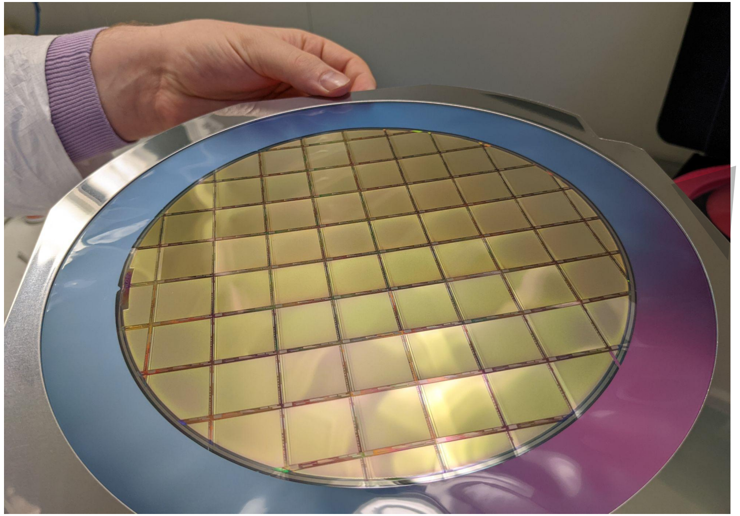

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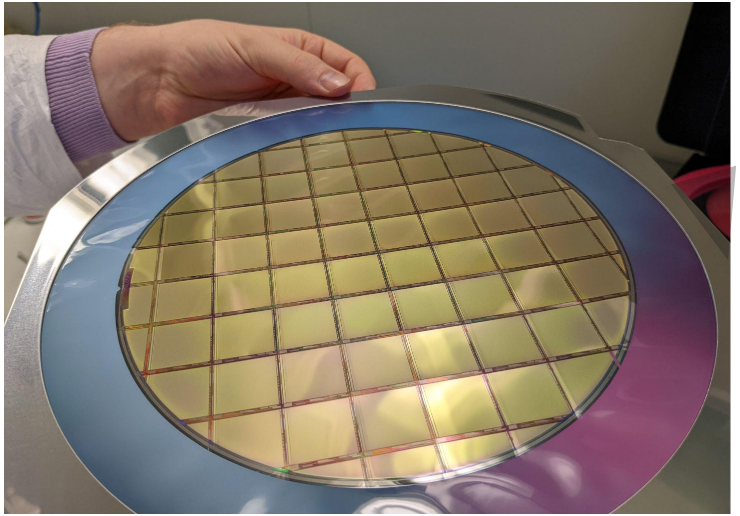

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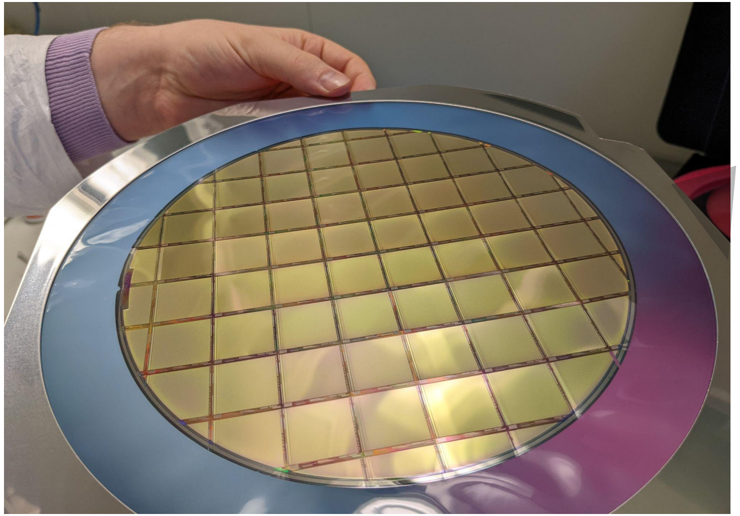

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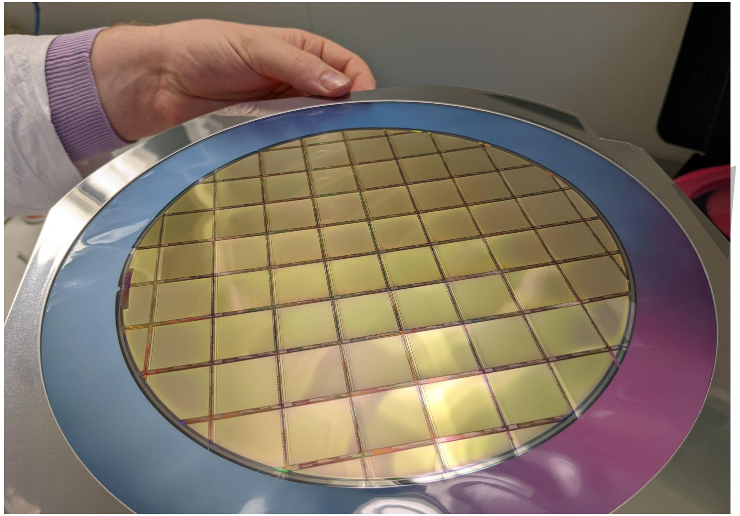

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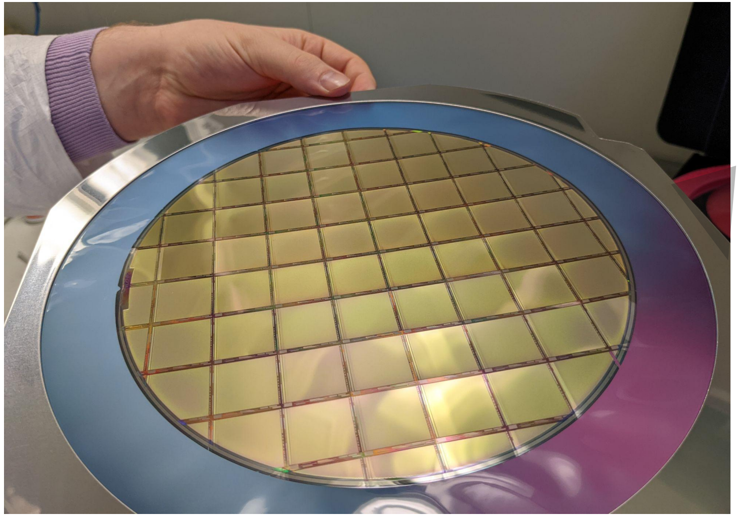

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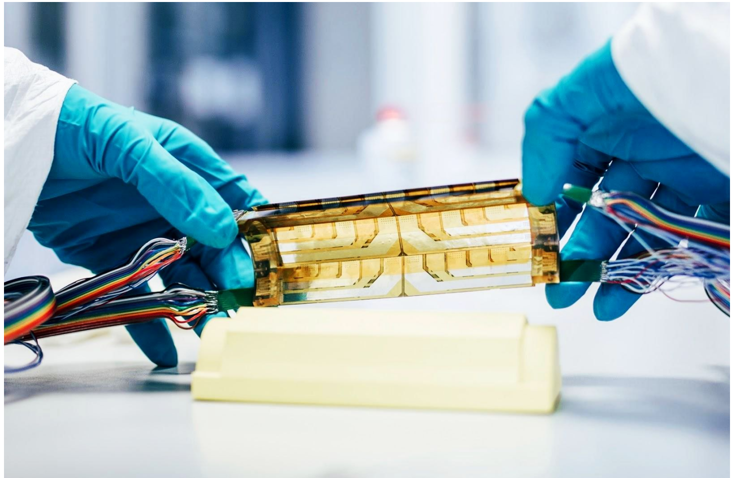

T. Rudzki

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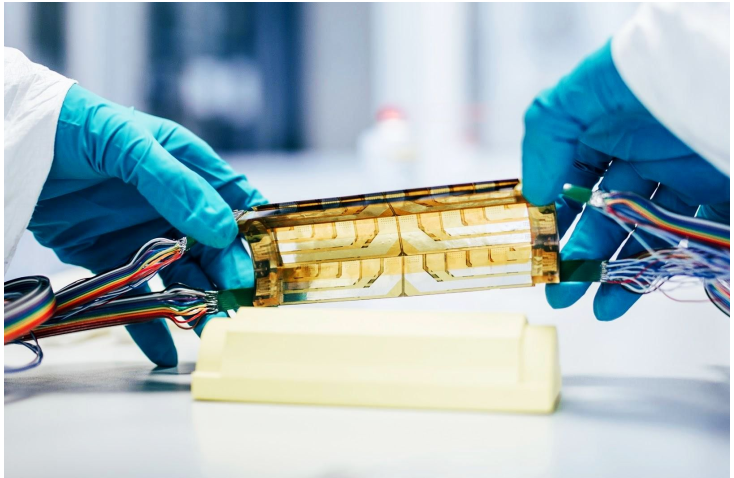

T. Rudzki

Questions?

Backup

Bibliography

Sources directly used in this presentation. For all contributing sources, see thesis bibliography.

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- A. Blondel et al. Research Proposal for an Experiment to Search for the Decay μ− > eee. 2013. arXiv: 1301.6113 [physics.ins-det].
- K. Arndt et al. “Technical design of the phase I Mu3e experiment”. doi: 10.1016/j.nima.2021.165679.
- I. Perić, “A novel monolithic pixelated particle detector implemented in high-voltage CMOS technology”, 2007.

The MuPix11 Quality Control Tests

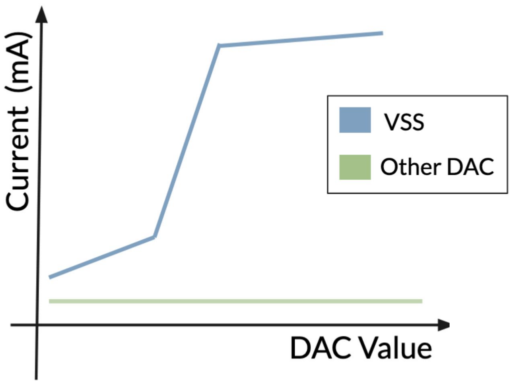
Each test evaluates a functions required for successful operation.

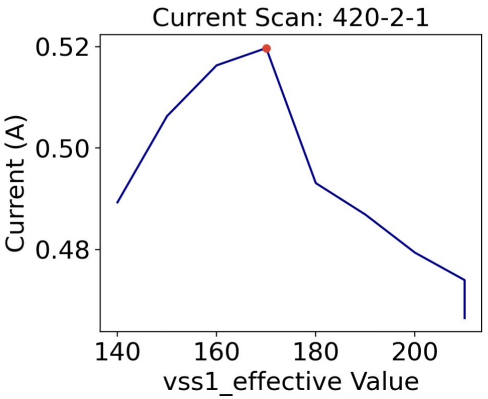
Test	Key Function	Fail Criteria
IV Scan	Pixel biasing for hit detection	High leakage current
LV Power- On	Powering of on-chip circuitry	Unsuitable LV current
Internal Voltages	Optimisation of the supply voltages	Incorrect voltages received
VDAC Scans	Setting of key voltages by Digital-to-Analogue Voltage Converters.	Unsuitable voltage or current response
LVDS Links	Data Transmission	Errors in transmitted data

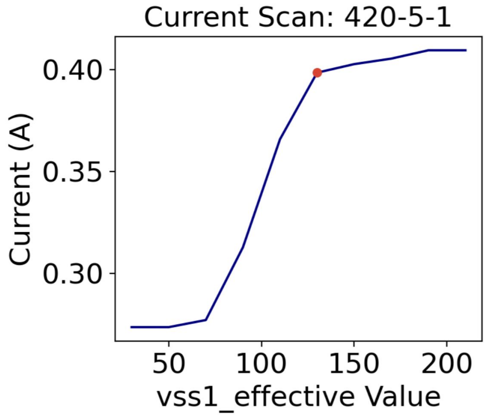
Improving for accuracy: the VDAC Scans

The VDAC scans investigate key components of the on-chip circuitry.

The VSS scan shows the current supplied to the amplifier against the VSS setting.







Expected VDAC scan

Initial VDAC scan

Improved VDAC scan

The VDAC Scan

The VDAC scan investigates key components of the on-chip circuitry.

<u>Observations:</u>

- Localised component failures.
- Most failures for analogue circuitry components.
- Higher failure rates for 50 µm.

<u>Context:</u>

- Significant short risk for the analogue domain.
- 50 µm sensors experience more thinning.
- Low sample size.

		Number of Failures	
VDAC	Location	70 µm	50 µm
VSS1	Pixel	4	10
VSS2	Pixel	4	10
BLPix	Pixel	6	10
Baseline	Periphery	3	7
ThHigh	Periphery	2	7
ThLow	Periphery	2	7
Total sensors:		44	44

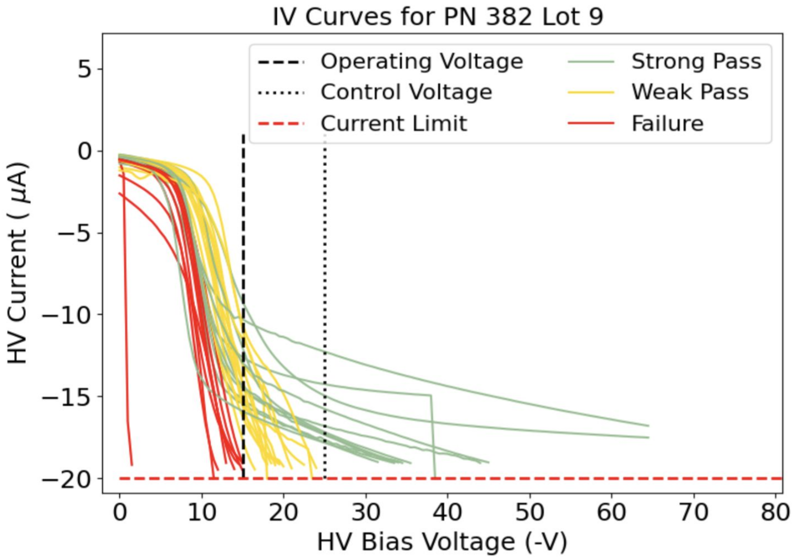
Failure profile: 50 µm sensors

The 50 µm yield is limited by the IV scan.

The low yield accurately describes the observed behaviour of the sensors.

Why do the sensors show high leakage currents?

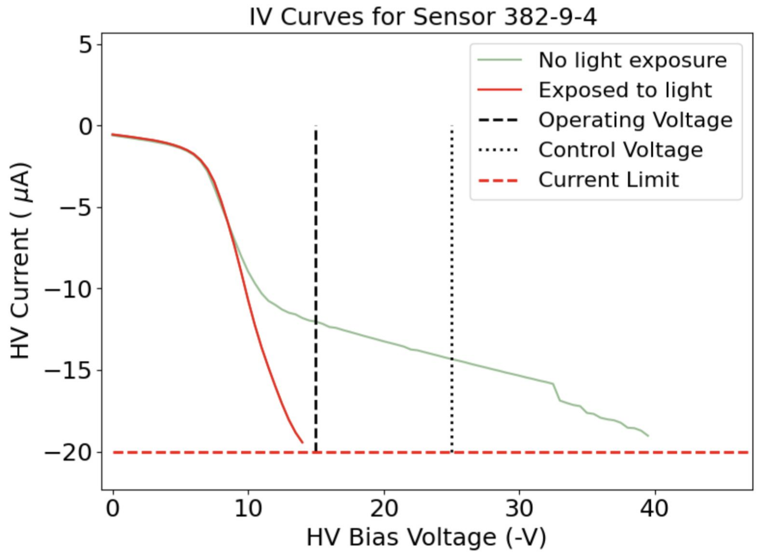
- Functionality?
- Systematic error?



Light dependency

Light dependency of the leakage current is inherent to silicon semiconductor pixels.

- ~2 mm diameter hole on the probe card lid.
- The 50 μm wafer was tested with the ceiling light switched on.
- The effect of light incident through the lid was investigated.



Light incident on the setup caused functional sensors to fail the IV scan.

The 50 μm yield can be improved

Yield estimate: Comparison with trends

Conservative estimate for improved IV yield: 75%

- Lowest yield 70 μm: 82%
- Total yield 70 μm: 66%

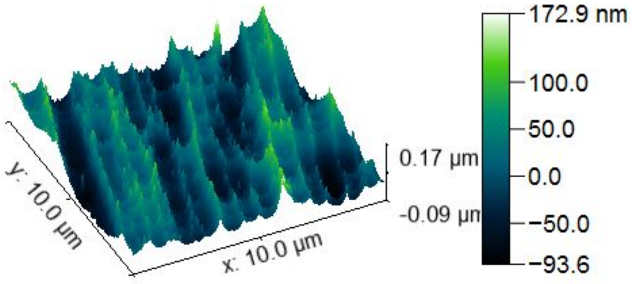
Estimate for overall 50 yield: 59%

Test	50 μm Yield (%)	
	Previous	Improved
IV Scan	53.2	54.5
LV Power-On	70.9	77.3
Internal Voltages	51.9	79.5
VDAC Scan	55.7	75.0
LVDS Links	74.7	75.0

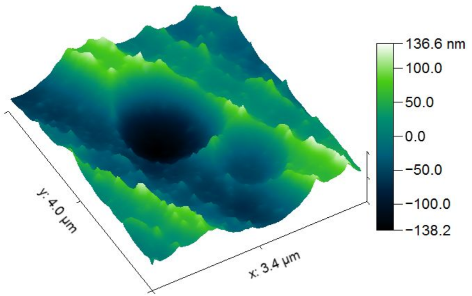
Test	70 μm Yield (%)	
	Previous	Improved
IV Scan	65.9	90.9
LV Power-On	65.5	81.8
Internal Voltages	70.1	88.6
VDAC Scan	65.5	81.8
LVDS Links	65.5	81.8

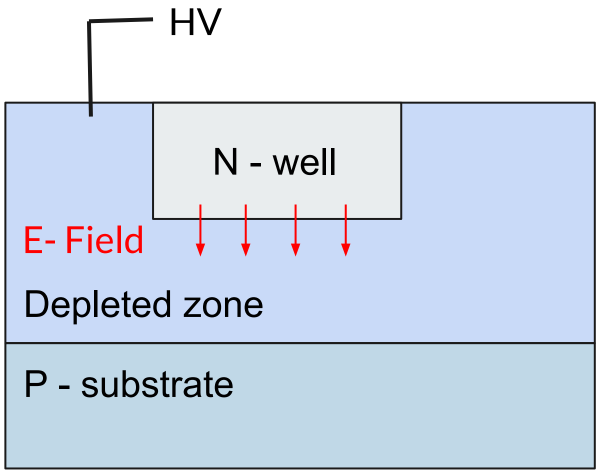
Thinning damage

- Grinding
    - Grooves
    - SSC
    - Warping



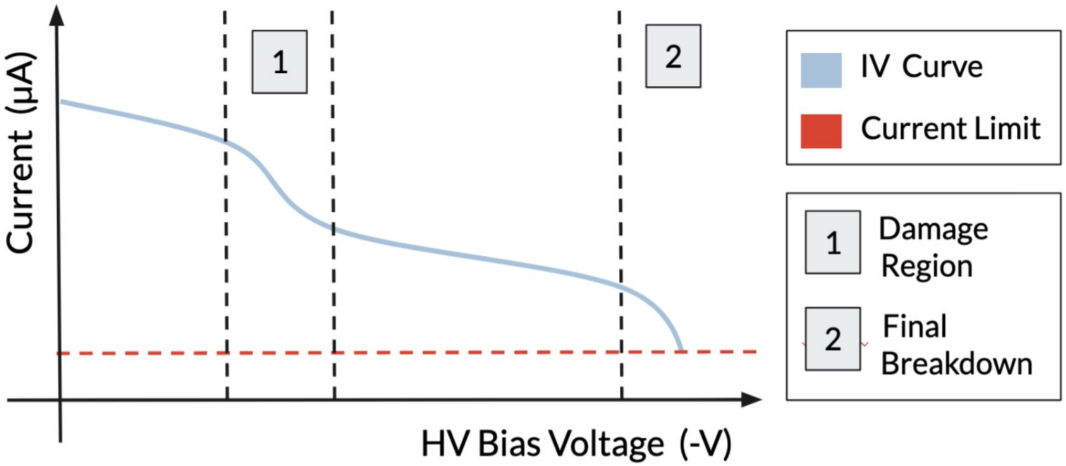
- Plasma- etching
    - Etching pits



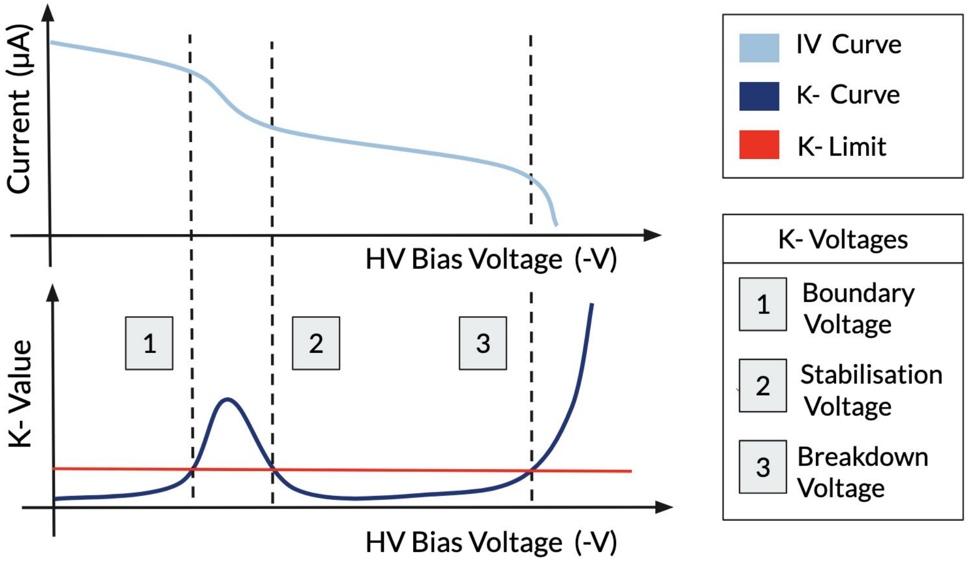


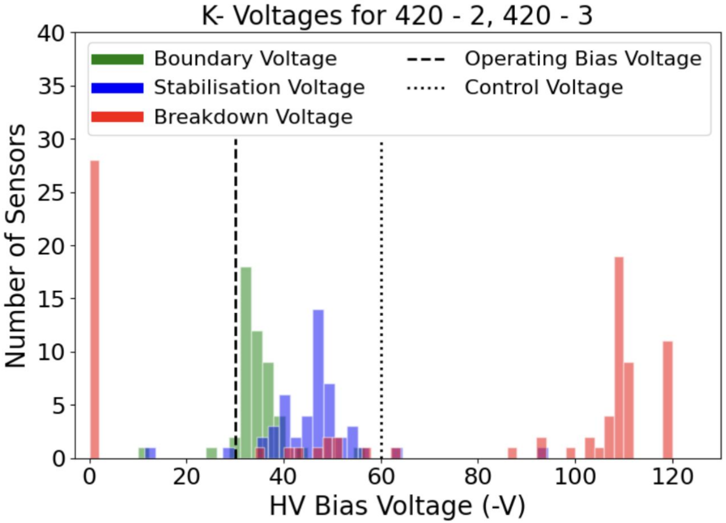
Contribution to leakage current

- Diffusion of minority charge carriers
- Volume leakage
  - ~ $\sqrt{(U_{bias})}$
  - ~T
  - Saturates at full depletion
- Surface contribution
  - Relevant after full depletion
  - Linear increase



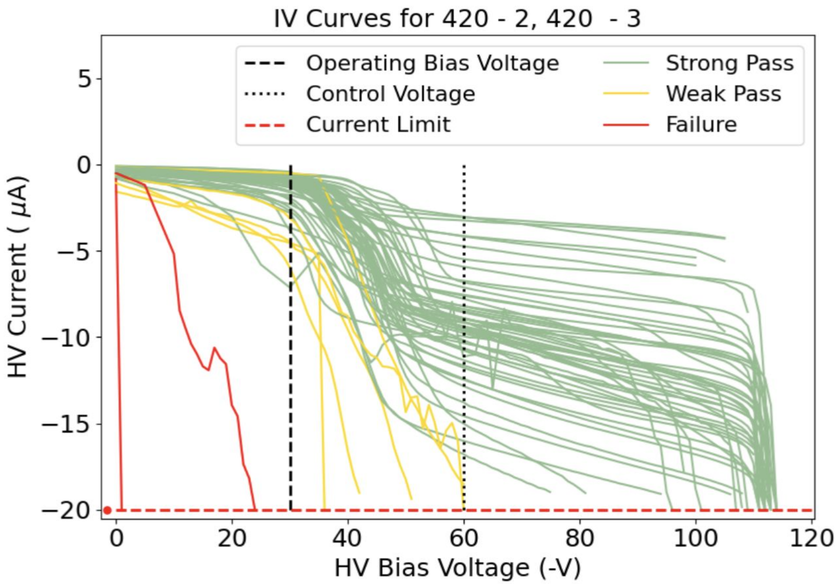
K-Value analysis of the IV Scan

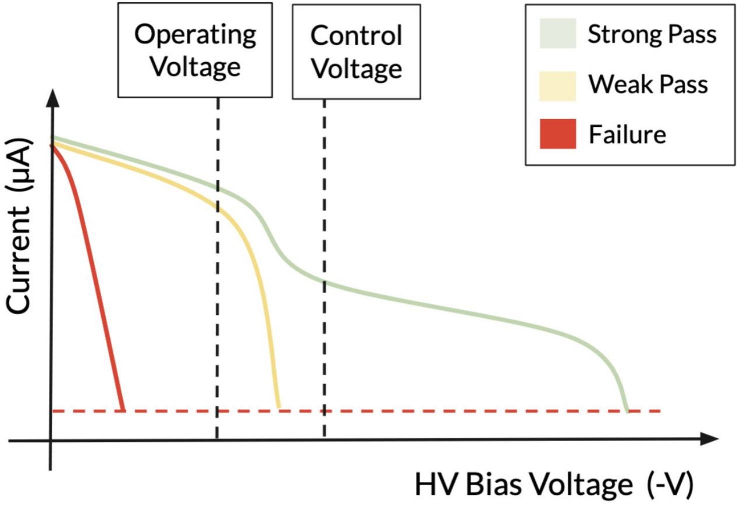




Chip Thickness	Operating Voltage (-V)	Control Voltage (-V)
70 µm	30	60
50 µm	15	25

Evaluation of the IV Scan





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70 µm	30	60
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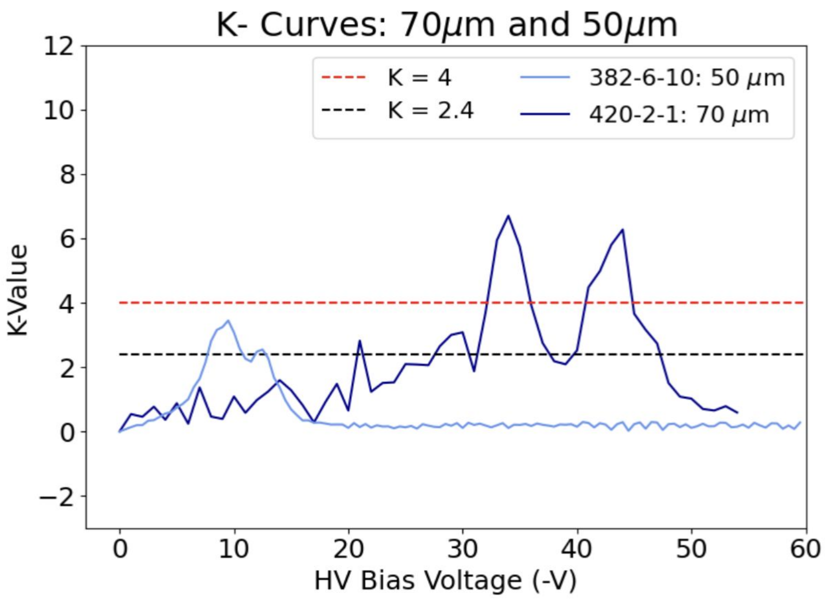
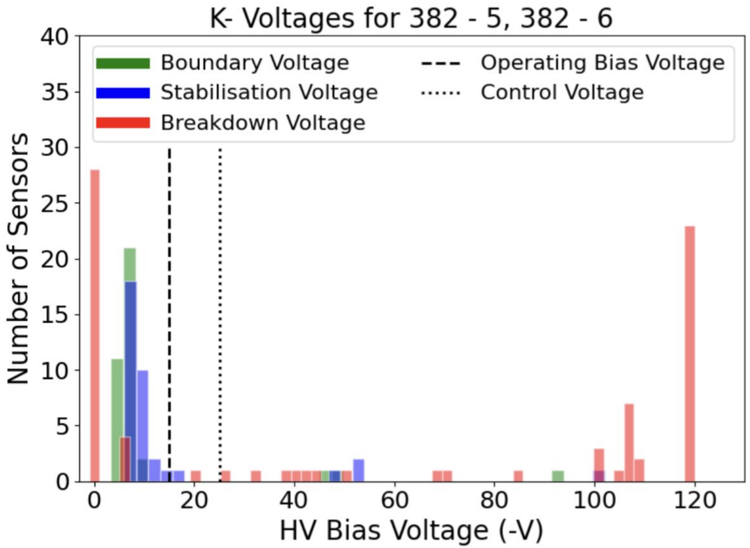
K-Value analysis of the IV Scan





Chip Thickness	Operating Voltage (-V)	Control Voltage (-V)
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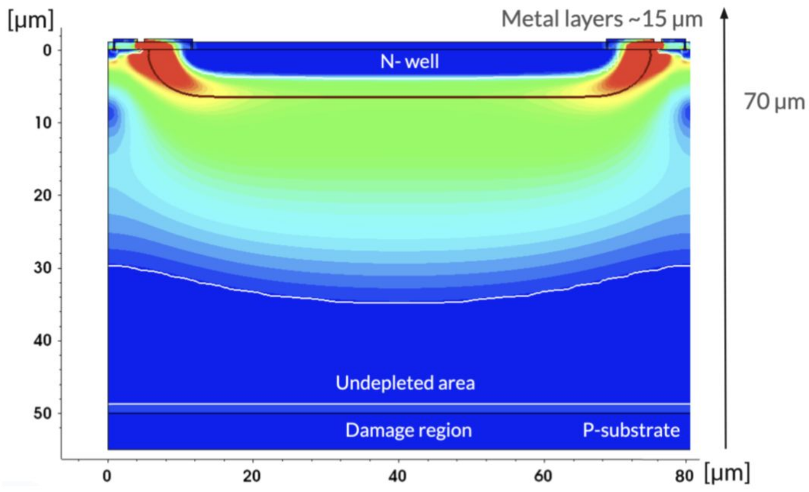
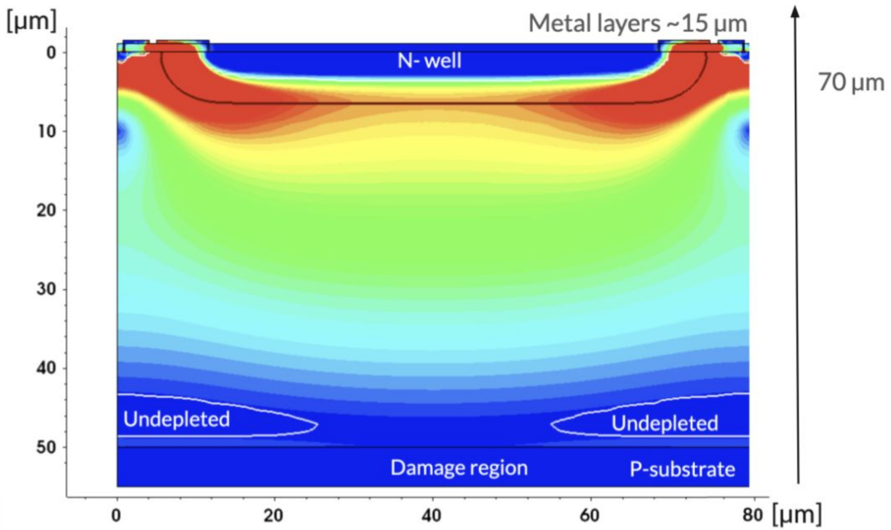
Depletion simulations





A. Meneses

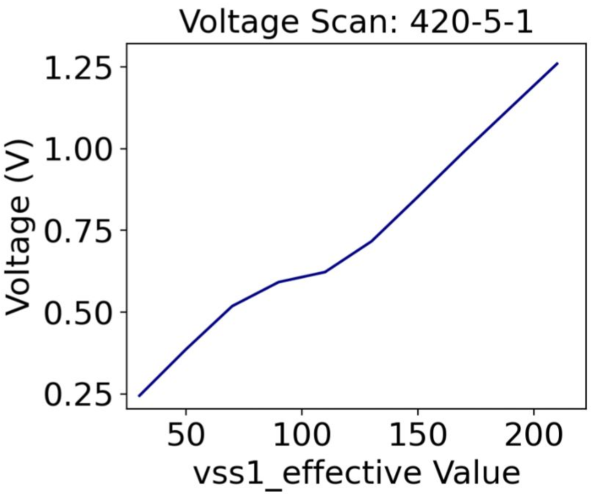
MuPix11 Detail

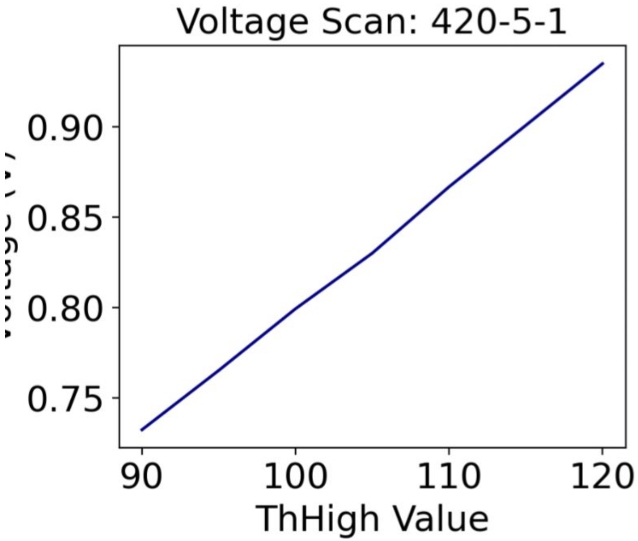
Pixel size ~ 80 x 80 microns

Feature	Target
Sensor dimensions [mm]	$\leq$ 21 x 23
Sensor size [mm]	$\approx$ 20 x 20
Thickness [μm]	≤ 50
Spatial resolution [μm]	≤ 30
Time resolution [ns]	≤ 20
Hit efficiency [%]	> 99
Number of LVDS links (inner layers)	1 (3)
Bandwidth per link [Gbit/s]	≥ 1.25
Power density [mW/cm^2]	≤ 350
Operation temperature range [°C]	0 - 70

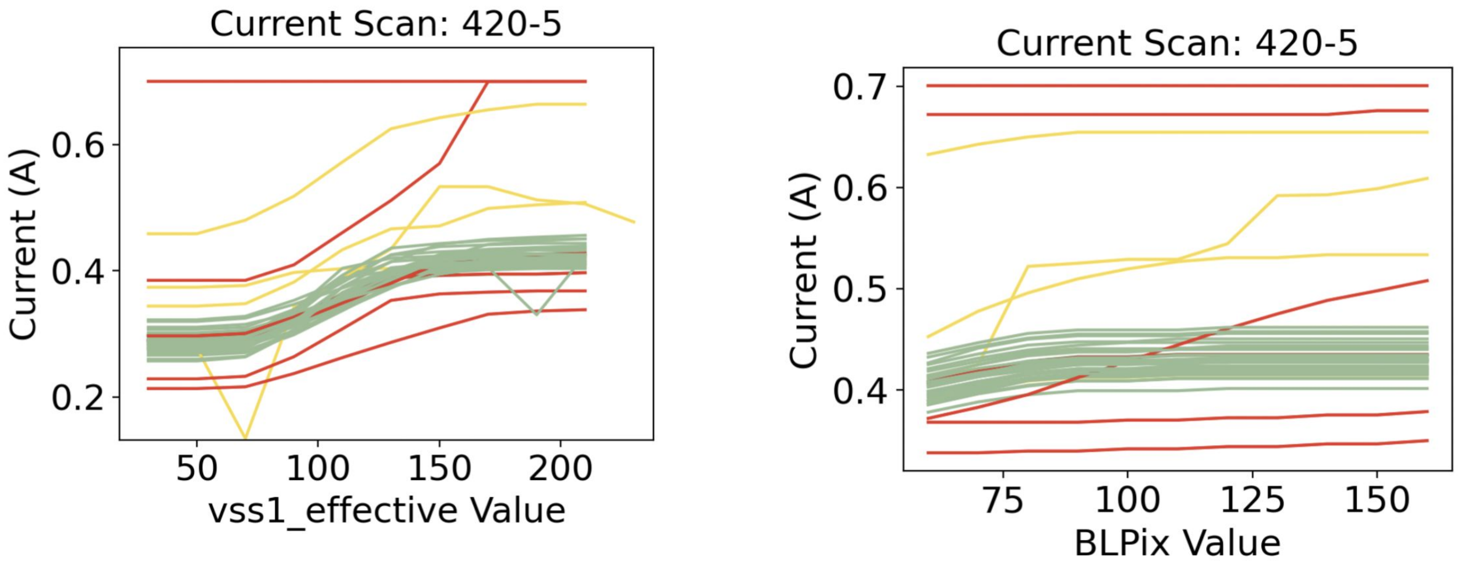
New evaluation strategy: VDAC

- Evaluation using current scan
    - VSS
    - BLPix
- Useful for future QCs
    - Ladder QC





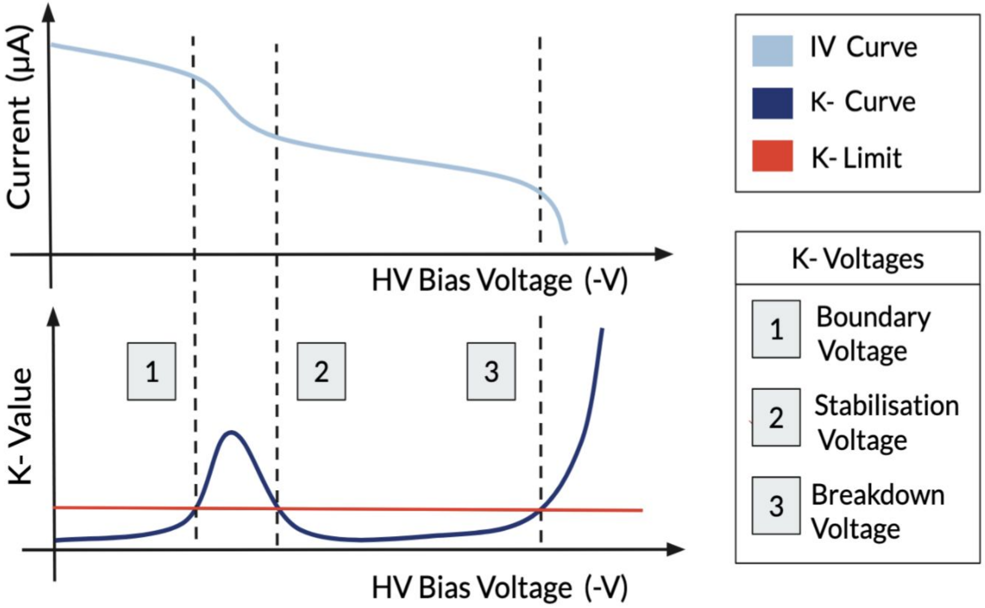
New evaluation strategy: VDAC



K-Value analysis of the IV Scan

Aim: to find the limits of the damage region to find a point of stable IV behaviour

$$K = \left(\frac{|\Delta I|}{|\Delta V|}\right) * \left|\frac{V}{I}\right|$$



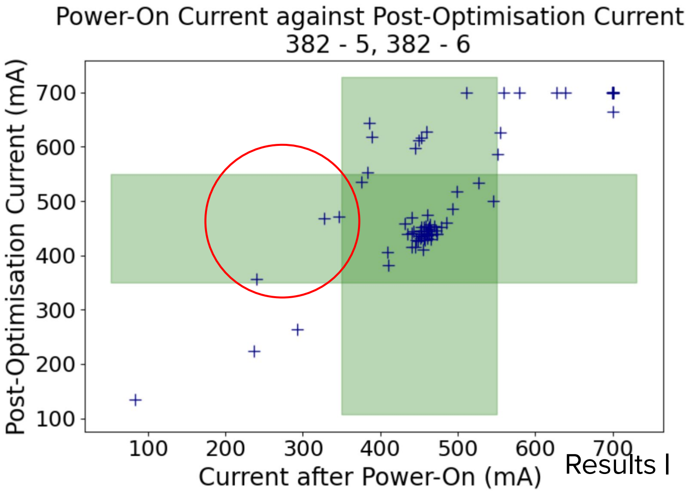
Failure profile: 70 µm sensors

Most common failures: the LV power-on test and the VDAC scan .

The LV power-on yield can be improved slightly:

- Some sensors recover the LV current after voltage optimisation.
- This shows functionality.
- A chip recovery strategy is suggested.
- Powering remains a key failure mode.

Test	70 µm Yield (%)	
	Strong	Weak
IV Scan	88.6	90.9
LV Power-On	79.5	81.8
Internal Voltages	86.4	88.6
VDAC Scan	79.5	81.8
LVDS Links	81.8	81.8



7-Step Power-On

- Powering of individual components unsuccessful
- Unoptimised supply voltage
- Can be repeated for evaluation
- Not necessary
- Already evaluated by other tests