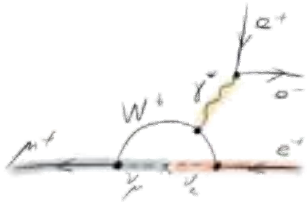
Firmware for the Mu3e Filter Farm

Marius Köppel on behalf of the Mu3e collaboration

Institute for Nuclear Physics, JGU Mainz

22.03.2023

Mu3e Motivation



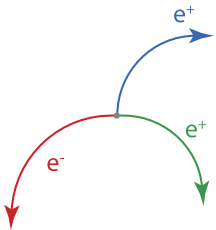
SM with ν oscillation Br: < 10^{-54}

- Search for Lepton Flavor Violation $\mu^+ \to e^+e^-e^+$
- Current limit (Br < 10^{-12}) set by SINDRUM (1988)

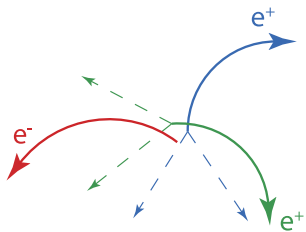
Paul Scherrer Institute (PSI)

- Muon beam of 10^8 μ/s
- One year of data taking
- Sensitivity up to one in 10^{15}

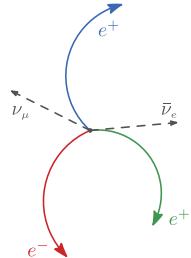
Mu3e Signal & Background



signal



random combinations of μ decays

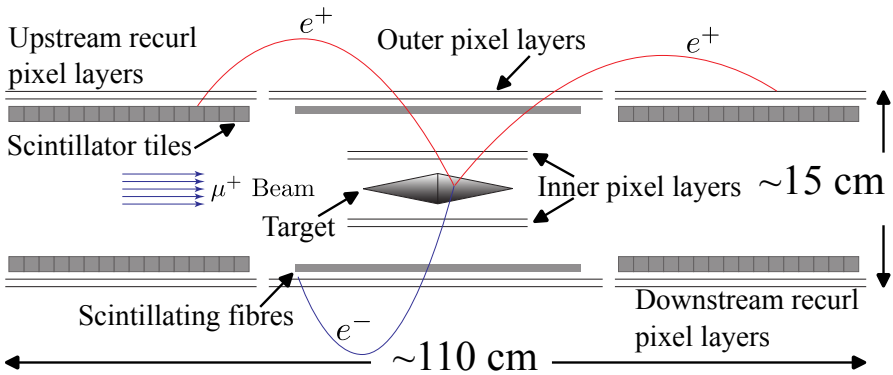


internal conversion

- $\sum p_e = 0$ and $\sum E_e = m_\mu$
- μ^+ decay at rest
- Good vertex and time resolution

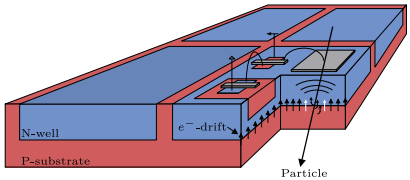
3 tracks $\rightarrow$ need of online reconstruction

Mu3e Detector Concept

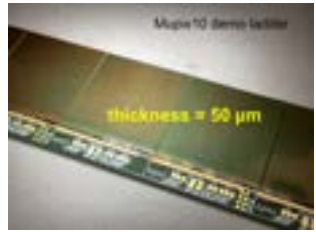


- Magnetic field of 1 T
- μ^+ stops at the target $\rightarrow$ decay at rest

High Voltage Monolithic Active Pixel Sensors



[1]



sensor: 20 x 20 mm^2 pixel 80 x 80 μm^2 [2]

- Thinned down to $50\,\mu m$
- Fast charge collection

- Time resoluton of a few ns
- Digitalization and zero suppression on the chip

$\rightarrow$ up to 3 links of continues 1.25 Gbit/s unsorted hit data

[1] Ivan Perić et al., NIM A582 (2007) 876-885
[2] HV-MAPS T 147.3

- Fibre < 500 ps time resolution
- Tiles < 70 ps time resolution

→ Readout via SiPM digitized via MuTRiG [3] chip, 1.25 Gbit/s unsorted hit data

[3] Huangshan Chen et al., JINST 12 (2017) C01043

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2 Data Acquisition of Mu3e

3 Mu3e Cosmic Run 2022

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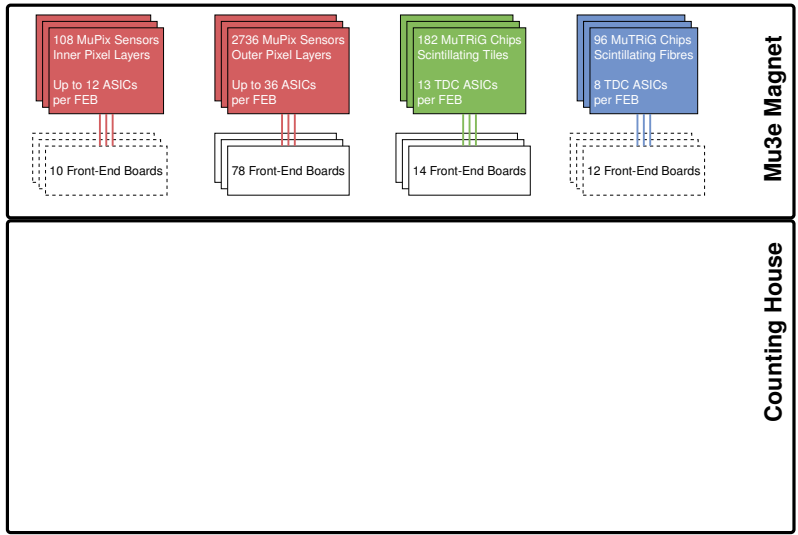
Mu3e DAQ

108 MuPix Sensors
Inner Pixel Layers
Up to 12 ASICs
per FEB
2736 MuPix Sensors
Outer Pixel Layers
Up to 36 ASICs
per FEB
182 MuTRiG Chips
Scintillating Tiles
13 TDC ASICs
per FEB
96 MuTRiG Chips
Scintillating Fibres
8 TDC ASICs
per FEB
Mu3e Magnet
Counting House

Mu3e DAQ

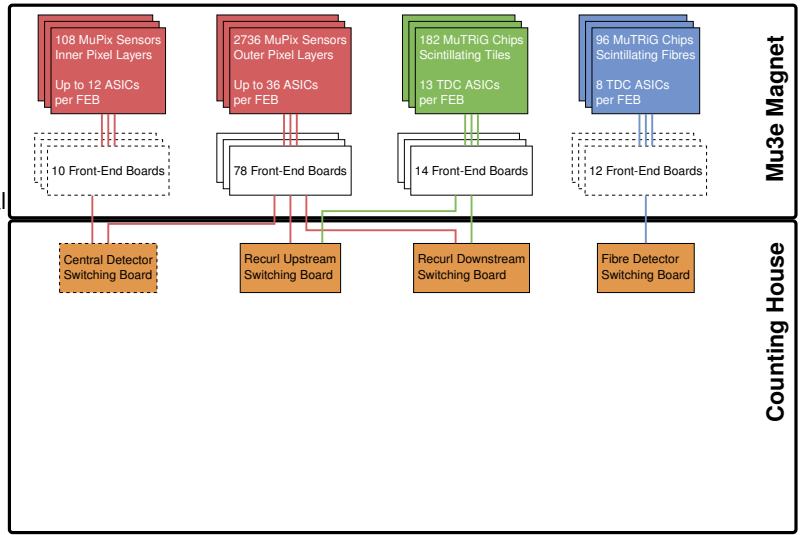
up to 3 x $1.25\,\mathrm{Gbit/s}$
LVDS links per ASIC



Mu3e DAQ

up to 3 x $1.25\,\mathrm{Gbit/s}$ LVDS links per ASIC

1-2 x $6.25\,\mathrm{Gbit/s}$ optical link per board



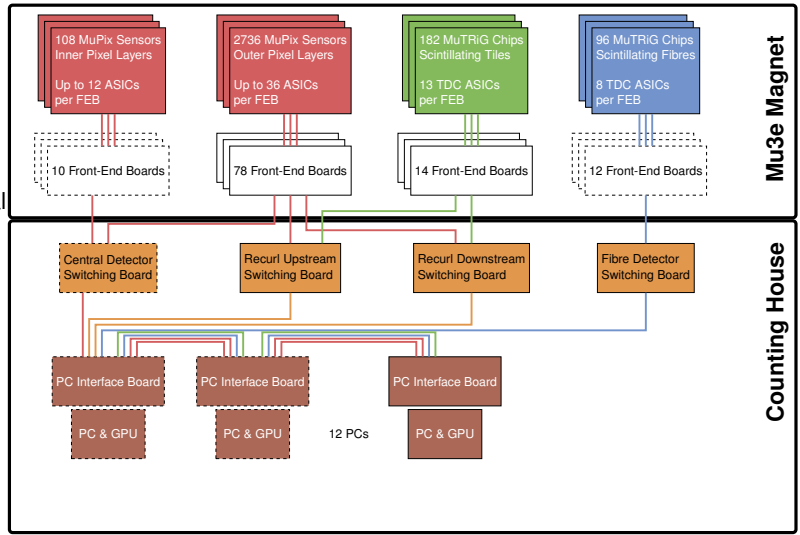
Mu3e DAQ

up to 3 x $1.25\,\mathrm{Gbit/s}$ LVDS links per ASIC

1-2 x $6.25\,\mathrm{Gbit/s}$ optical link per board

2-8 x $10\,\mathrm{Gbit/s}$ optical links per board

16 inputs per Farm FPGA



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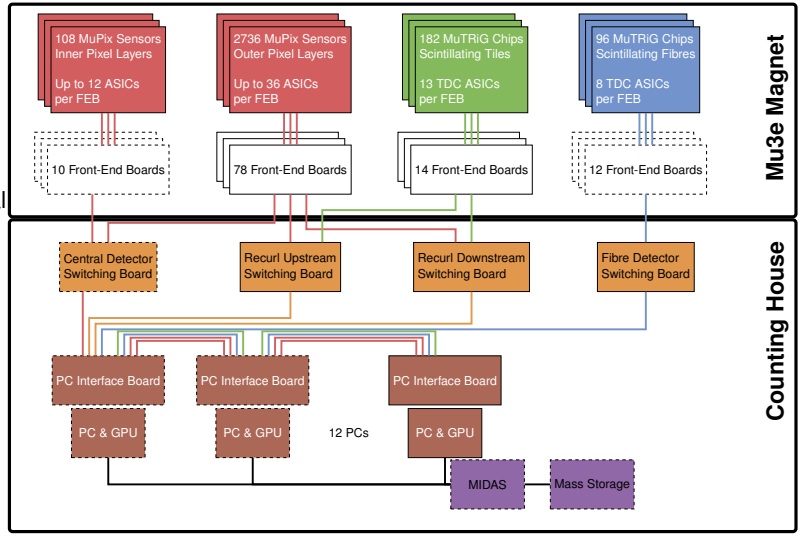
Gbit Ethernet



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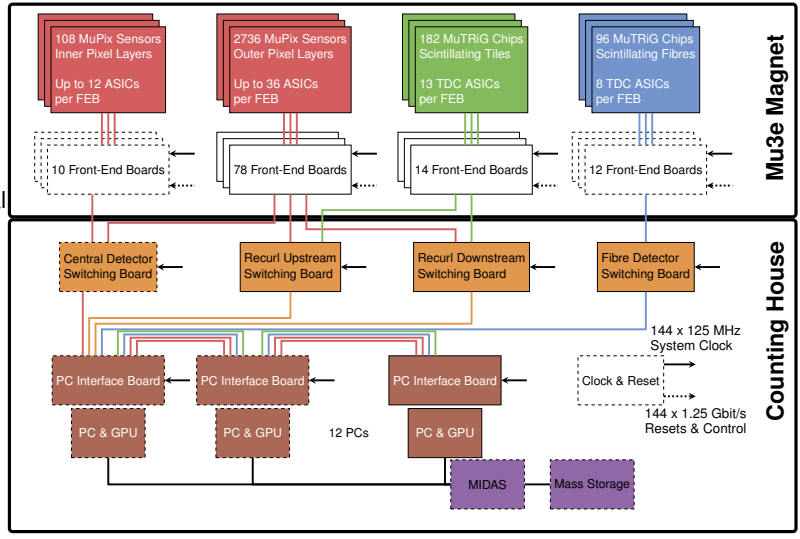
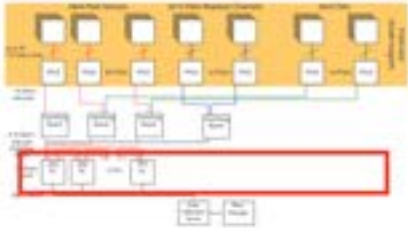
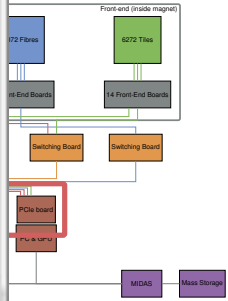


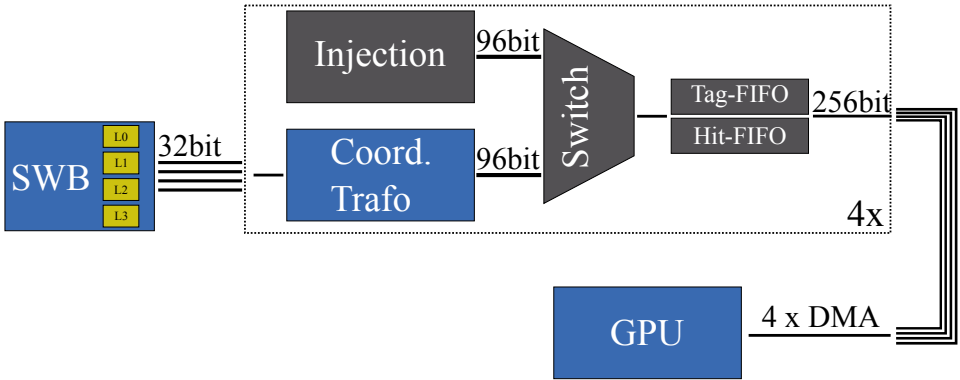
GPU PCs

- DE5aNET receiving boards from Terasic
- Enough boards available and tested
- Potential host box bought (including GTX 2080Ti GPU)
- Rack infrastructure needed (5 racks, 4 of which water-cooled, see infrastructure session)





PC Interface FPGA Board Firmware



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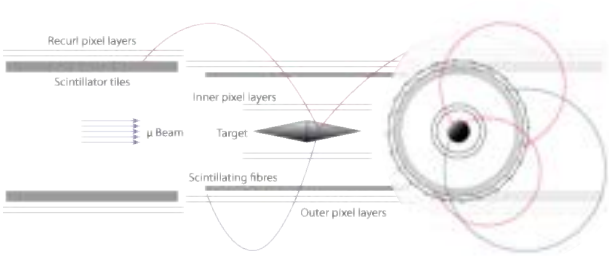

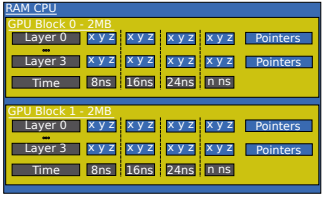

- Group hits from all layers into 0.5 MB
- All hits are sorted in 8 ns

- Time information by the pointers
- Collect 2 MB $\rightarrow$ send it off $\rightarrow$ streaming
- For GPU tracking $\rightarrow$ Do, 16:20 T 122.3

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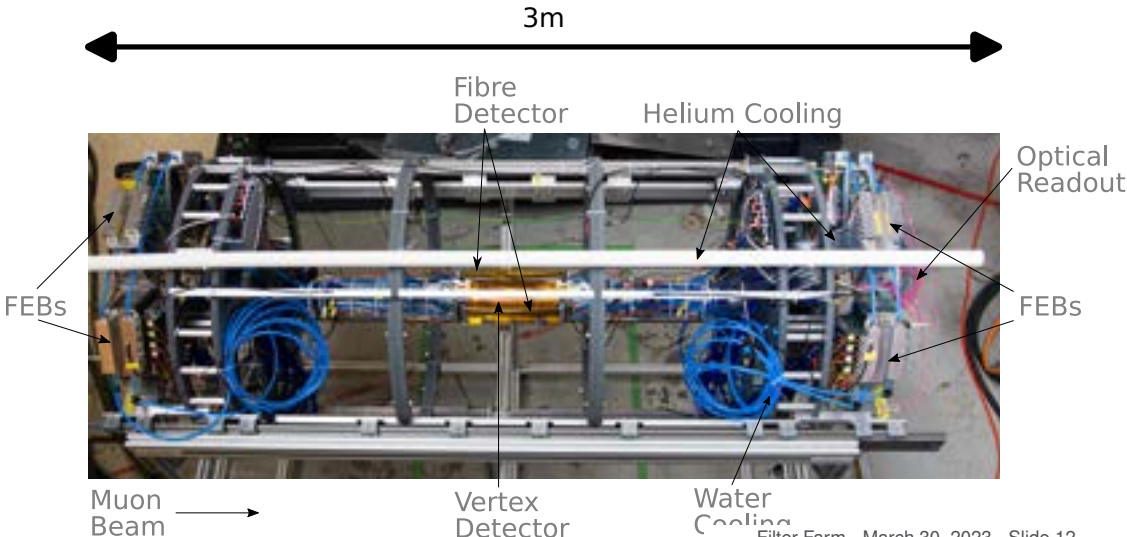
Mu3e Cosmic Run



Mu3e Cosmic Run DAQ

Scintillator panels

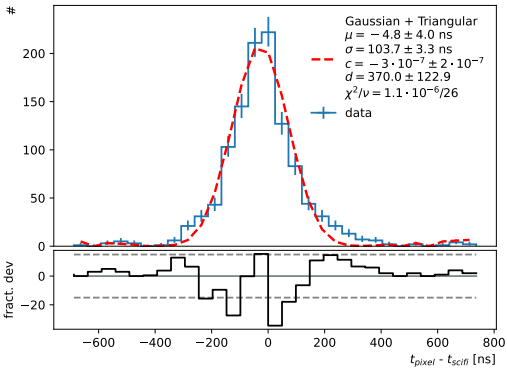
1 x Scintillating fibre ribbon

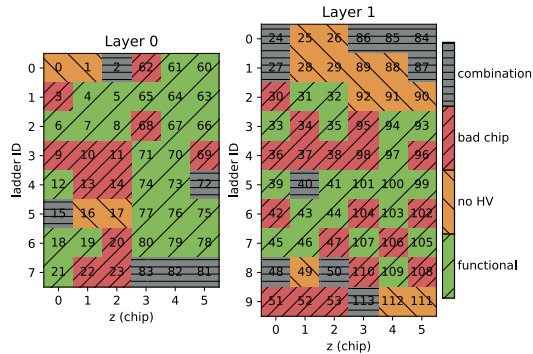
Inner pixel layers

Scintillator panels

Scintillator panels

Mu3e Cosmic Results





More on the Cosmic Run → Do, 16:05 T 112.2

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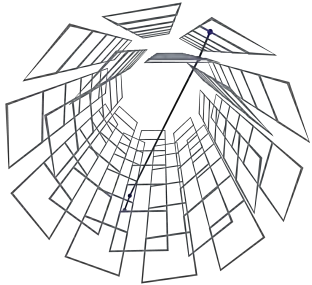

- Testing full DAQ with beam data in 2024
- Integration of the GPU selection
- Final commissioning of hit synchronisation