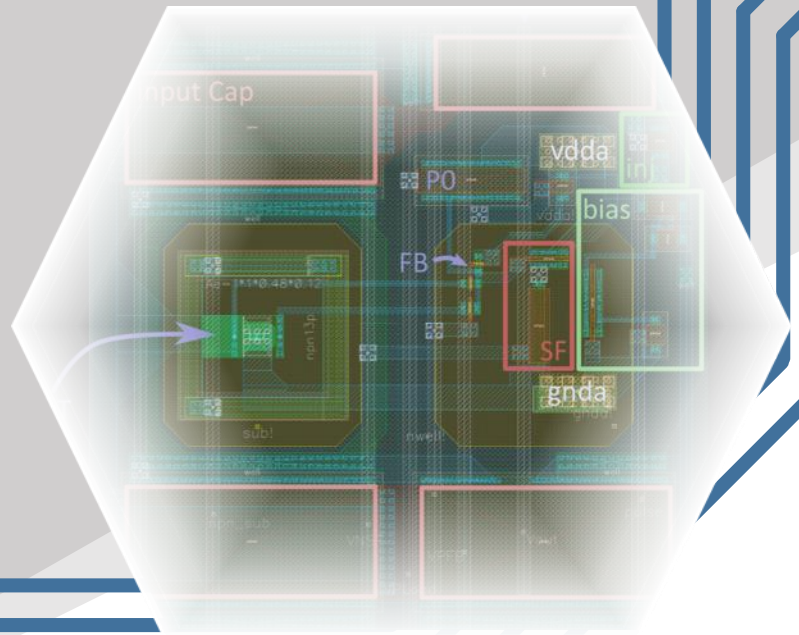

Development of a Pixel Sensor with sub-nanosecond Time Resolution in BiCMOS

Benjamin Weinläder
Physikalisches Institut, Uni Heidelberg

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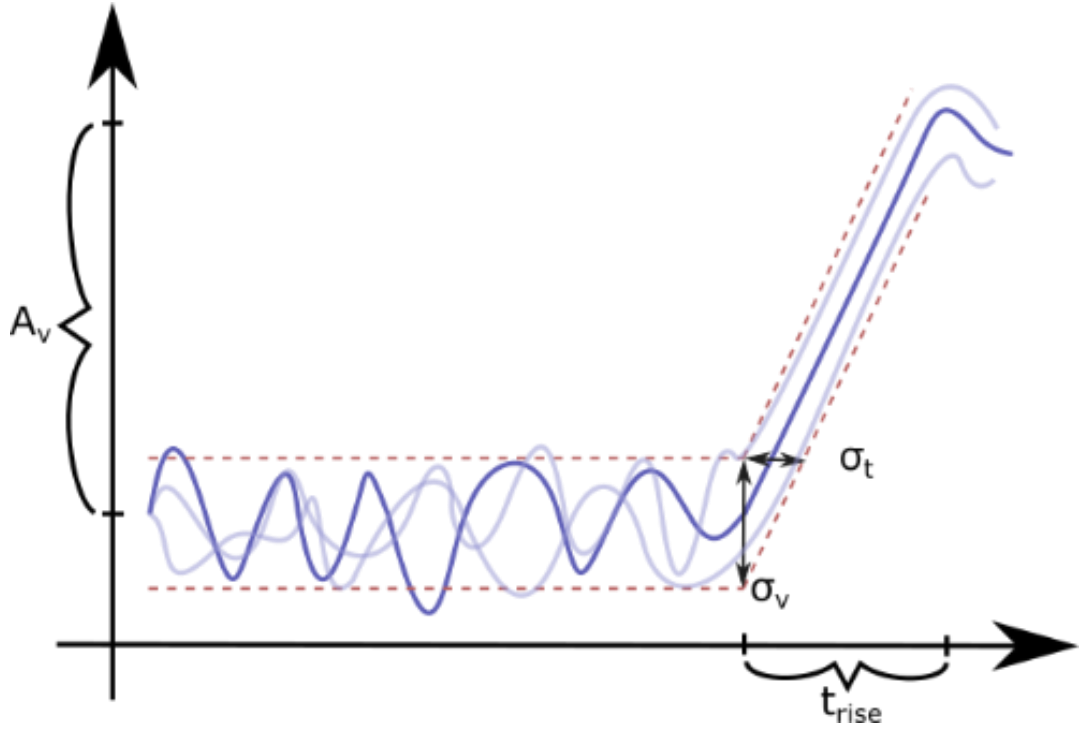
HighRR

UNIVERSITÄT HEIDELBERG
ZUKUNFT SEIT 1386

Challenge

- Optimal time resolution due to jitter
  - simplified model:
    $$\frac{\sigma_t}{\sigma_v} \approx \frac{t_{rise}}{A_v} \rightarrow \sigma_t \approx \frac{t_{rise}}{SNR}$$
  - Assuming effects like Time-Walk can be handled



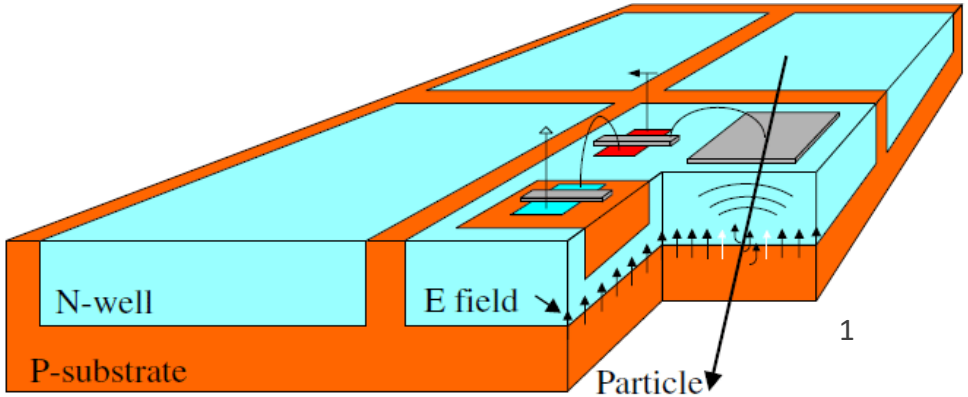
Required:

- Signal with fast rising edge and low noise

Defining the sensor

1.

- Sensor architecture: HV-MAPS
  - Part of the readout electronic directly implemented into active pixels



[1]

- As shown within the development of the MuPix/AtlasPix:
  - HV-MAPS achieve a precise time resolution in the order of $\sigma_t = 5\ ns$

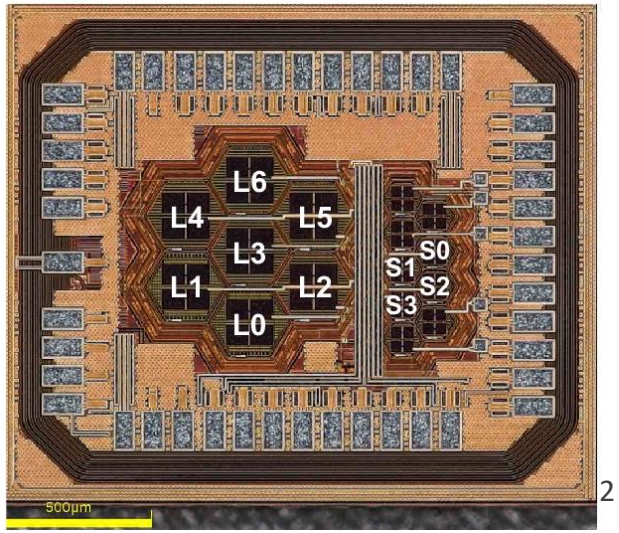
For more information refer to Dohun Kim (Session T64.9, 17.03.21)

[1] I. Peric, P. Fischer et al.: 'A novel monolithic pixelated particle detector implemented in high-voltage CMOS technology'

Defining the sensor

2.

- Combine HV-MAPS with BiCMOS technology
  - Benefit from advantages from bipolar (HBT) and MOS Transistors to improve the time resolution
- Proven by the TT-PET Project [2] :
  - $\sigma_t = 46 \pm 1\ ps$ for the hexagonal prototype



2

[2] G. Iacobucci et al.: 'A 50 ps resolution monolithic active pixel sensor without internal gain in SiGe BiCMOS technology'

Goal

- Development of an analogue pixel design using the BiCMOS Process SG13S[3] by IHP

HBT	DC-Gain β	900
	Transit Frequency f_t	$\sim 240\ GHz$

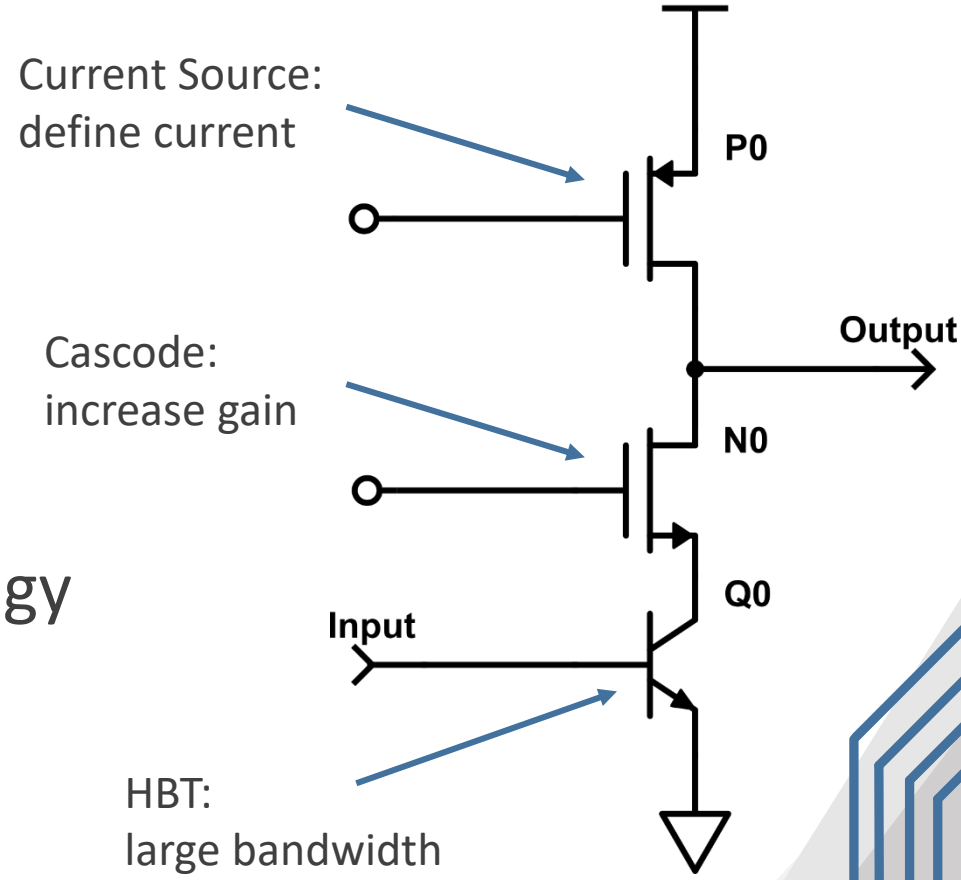
CMOS	Minimum length	$130\ nm$
	Transit Frequency f_t	$\sim 10\ GHz$

- Simulation and analysis of the timing response of the pixel and subsequent circuitries
  - Optimising the time resolution at feasible power consumption
  - Minimising pixel size to reduce pixel capacitance

[3] H. Rücker et al.: 'A 0.13m SiGe BiCMOS Technology Featuring fT/fmax of 240/330 GHz and Gate Delays Below 3 ps'

The Idea

- Amplifier defines crucial signal parameters
  - Use simple gain-stage to reduce electronic components and noise
  - Improve performance with HBT
- Remaining electronics uses CMOS technology in order to reduce power consumption



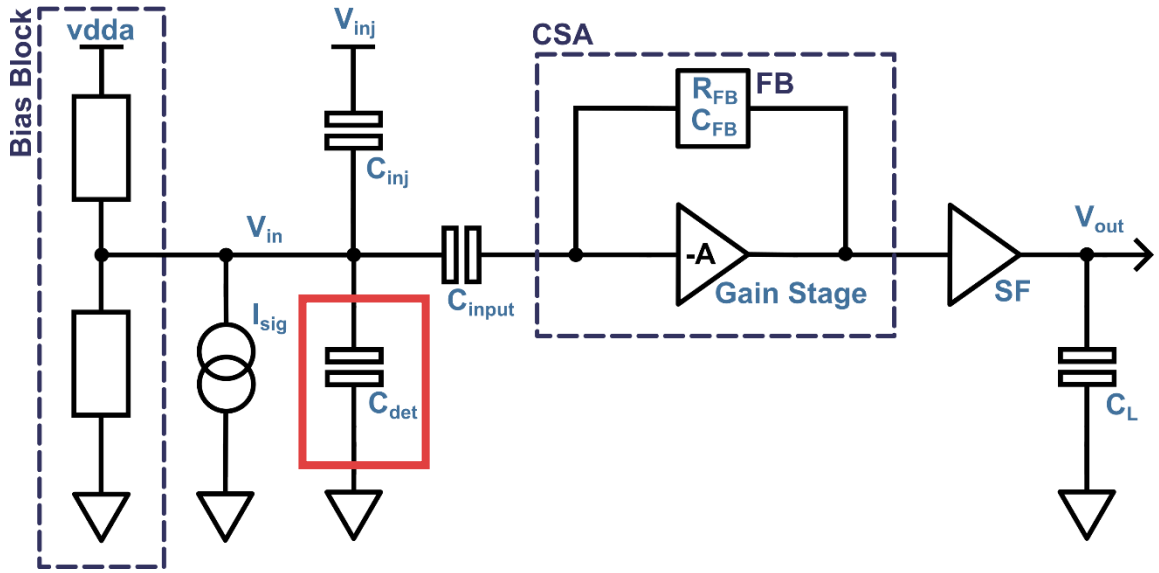
HBT	CMOS
Fast switching times	Low input capacitance
High current gain	Low power consumption

Pixel Circuitry

- Simplified pixel circuity
  - Circuity reduced to minimum for minimum pixel size

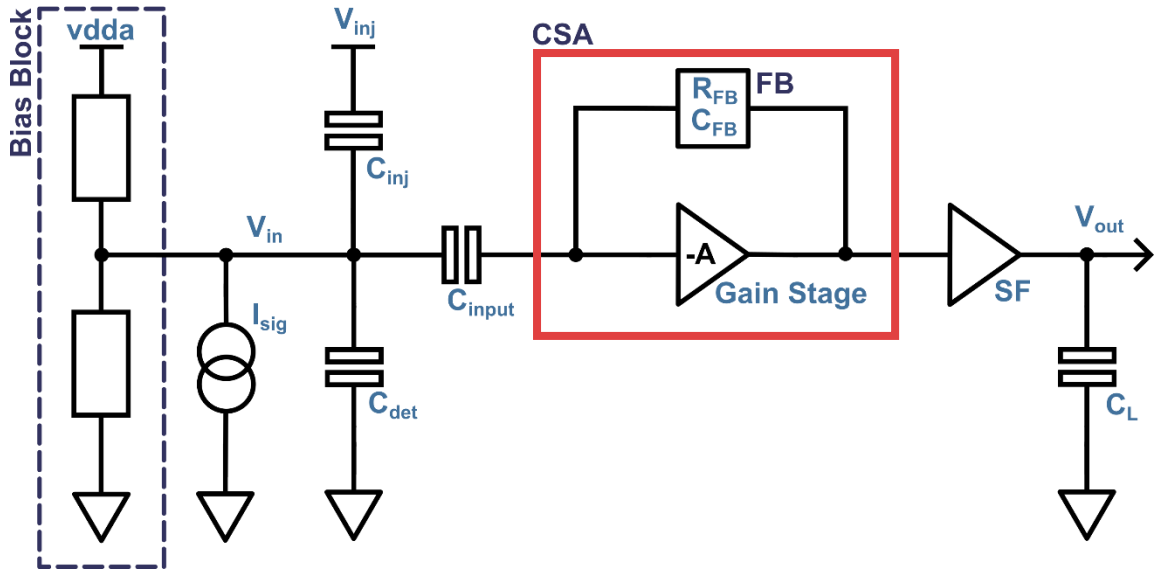
- Signal charge is distributed between all capacities but only processed on C_{input}

  Smaller C_{det} → larger amplitude
  Larger C_{input} → larger amplitude



Pixel Circuitry

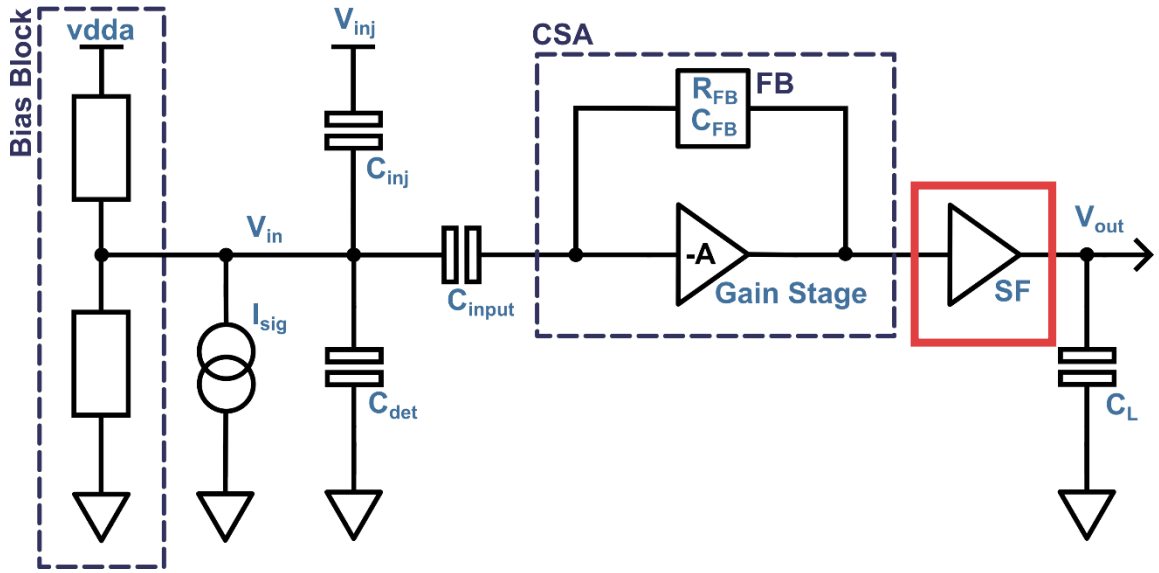
- Charge Sensitive Amplifier (CSA)
  - Rising edge defined by bandwidth of the gain stage
  - Falling edge defined by FB, $\tau \approx R_f C_f$
  - Gain of the CSA drops with decreasing R_f
  - C_f parasitic capacity



Amplifier with fast rising edge, low noise and low power consumption

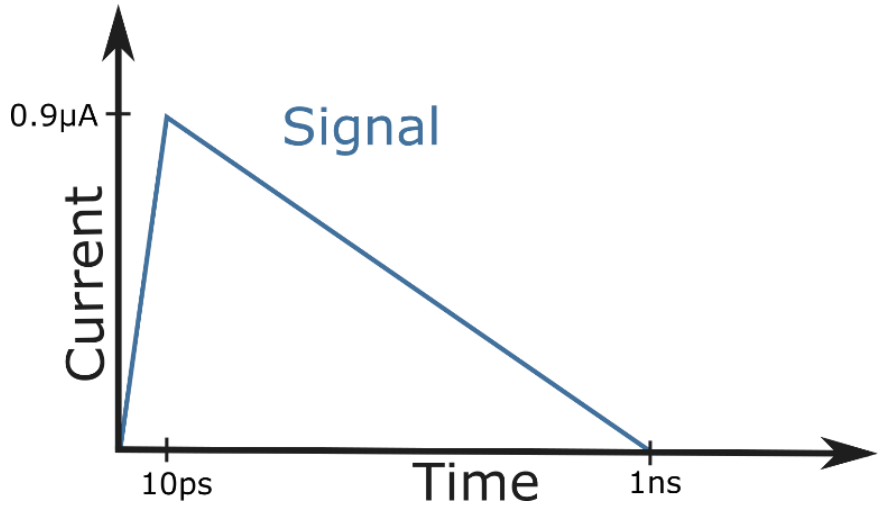
Pixel Circuitry

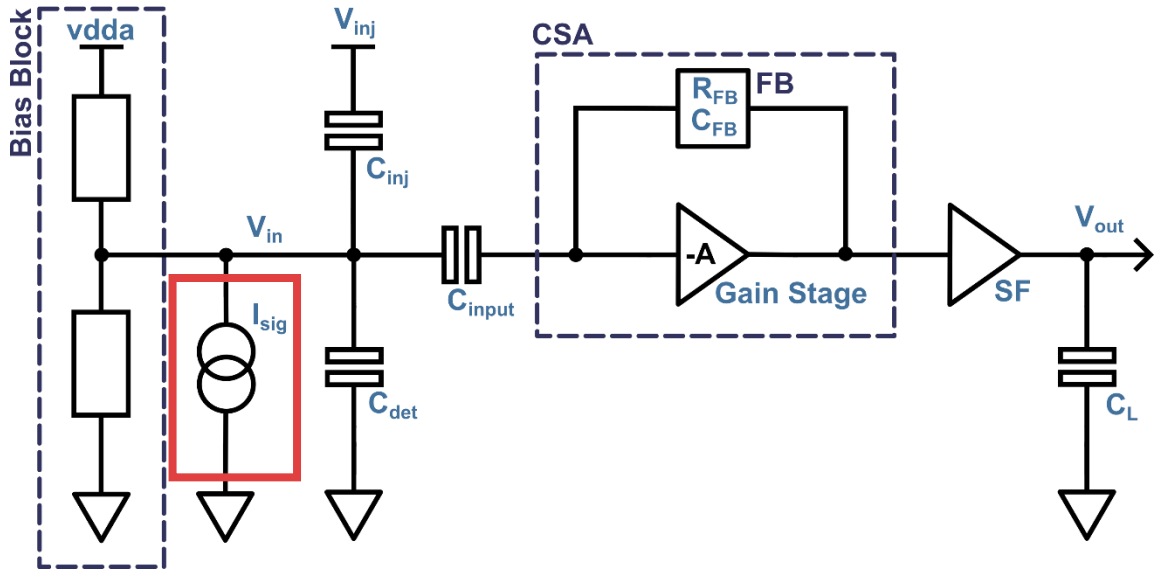
- Source Follower (SF)
  - Drives analogue signal to the periphery
- Alternative option: implement digitisation directly into the pixel



Pixel Circuitry

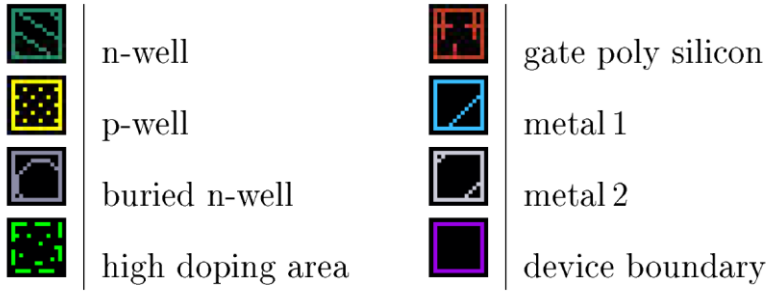
- Signal
  - Necessary for simulations
  - Induces a triangular signal with $Q_{sig} \approx 2800\ e^-$ (MIP)

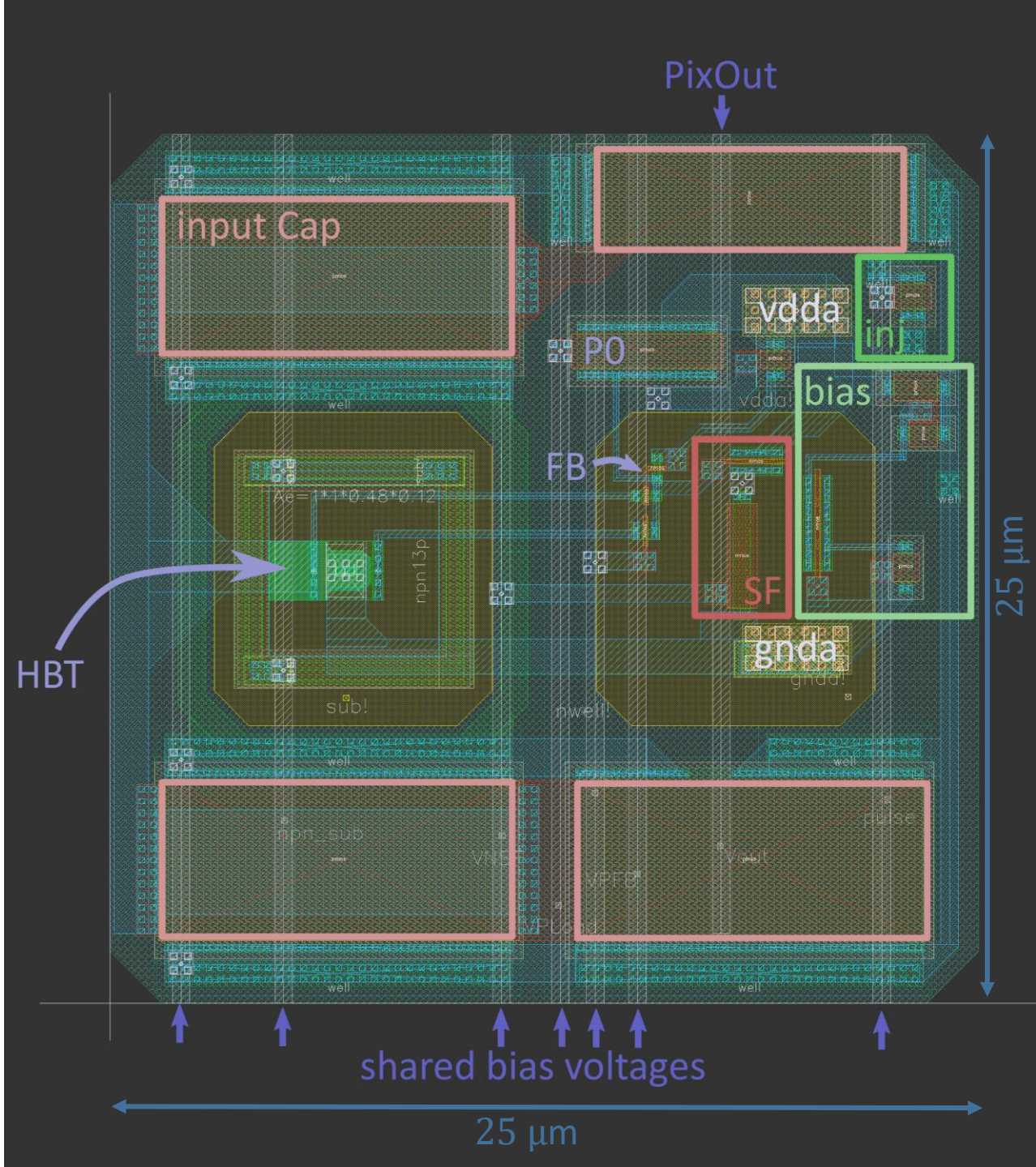




Pixel Layout

- Pixel w/ guard ring $40 \times 40\ \mu m^2$
  - Implant size $25 \times 25\ \mu m^2$
- HBT in separated p-well with guard ring
- Minimised parasitic capacities
  - avoid overlapping metal areas
- Shared bias voltages for all pixels



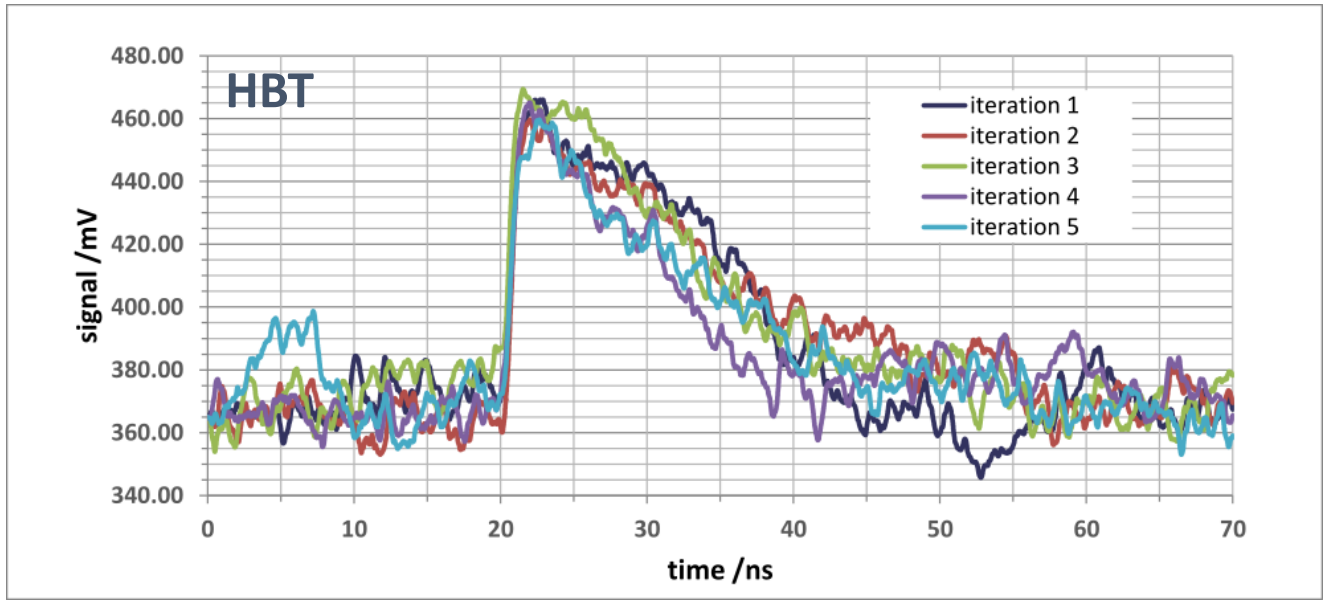


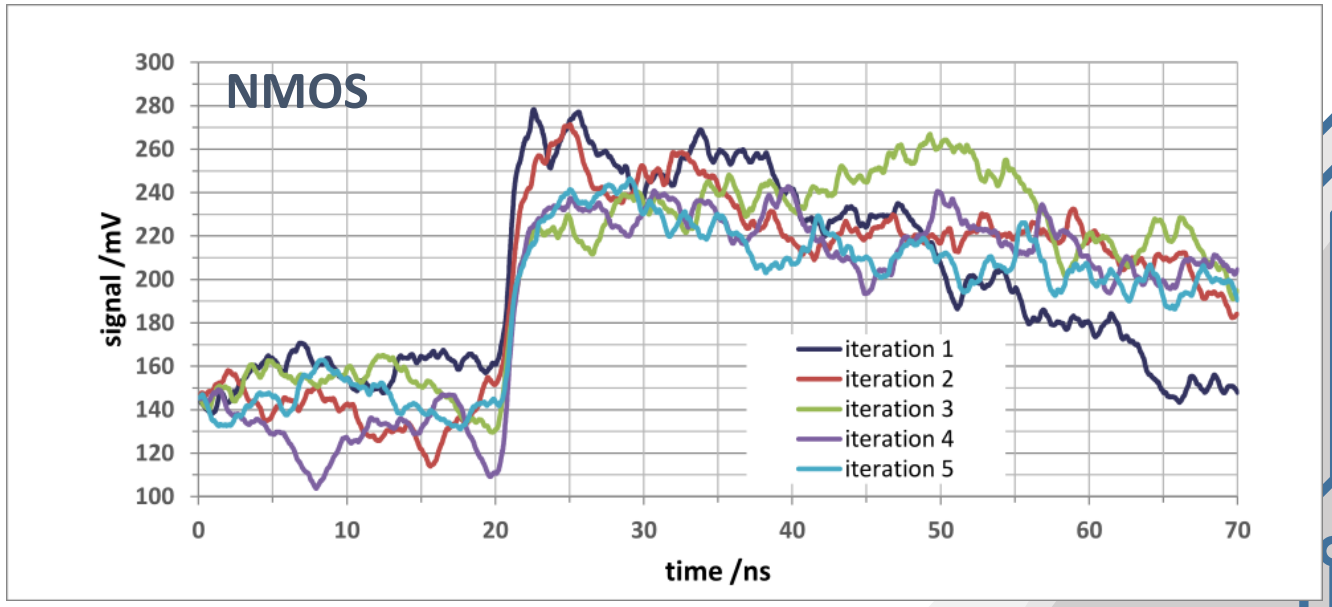
Transient Response

- Comparison HBT - NMOS

	$V_{amp}\ [mV]$	SNR	$\sigma_{ToA}\ [ps]$	ENC
HBT	115 ± 7	16.5 ± 3.3	62	$176\ e^-$
NMOS	114 ± 20	13.4 ± 4.5	301	$230\ e^-$

$f_{max} = 10\ GHz, \#Iterations = 100$





Summary

- Development of an analogue pixel design with a BiCMOS process and simulation of it:

	My Pixel	**TT-PET Project[2]**	
	(simulations)	(hexagonal Prototype)	(new Power Settings[4])
Pixel Size	$\sim 40 \times 40\ \mu m^2$	side 65 µm	
Power Consumption	$\sim 40\ \mu W/ch$	$\sim 375\ \mu W/ch$	$\sim 13\ \mu W/ch$
Min. Time Resolution	$62\ ps$	$46\ ps$	$140\ ps$

- To be done:
  - Study possibility to include comparator into the pixel
  - Implement the pixel in a large matrix

[2] G. Iacobucci et al.: 'A 50 ps resolution monolithic active pixel sensor without internal gain in SiGe BiCMOS technology'
[4] L. Paolozzi et al.: 'Time resolution and power consumption of a monolithic silicon pixel prototype in SiGe BiCMOS technology'