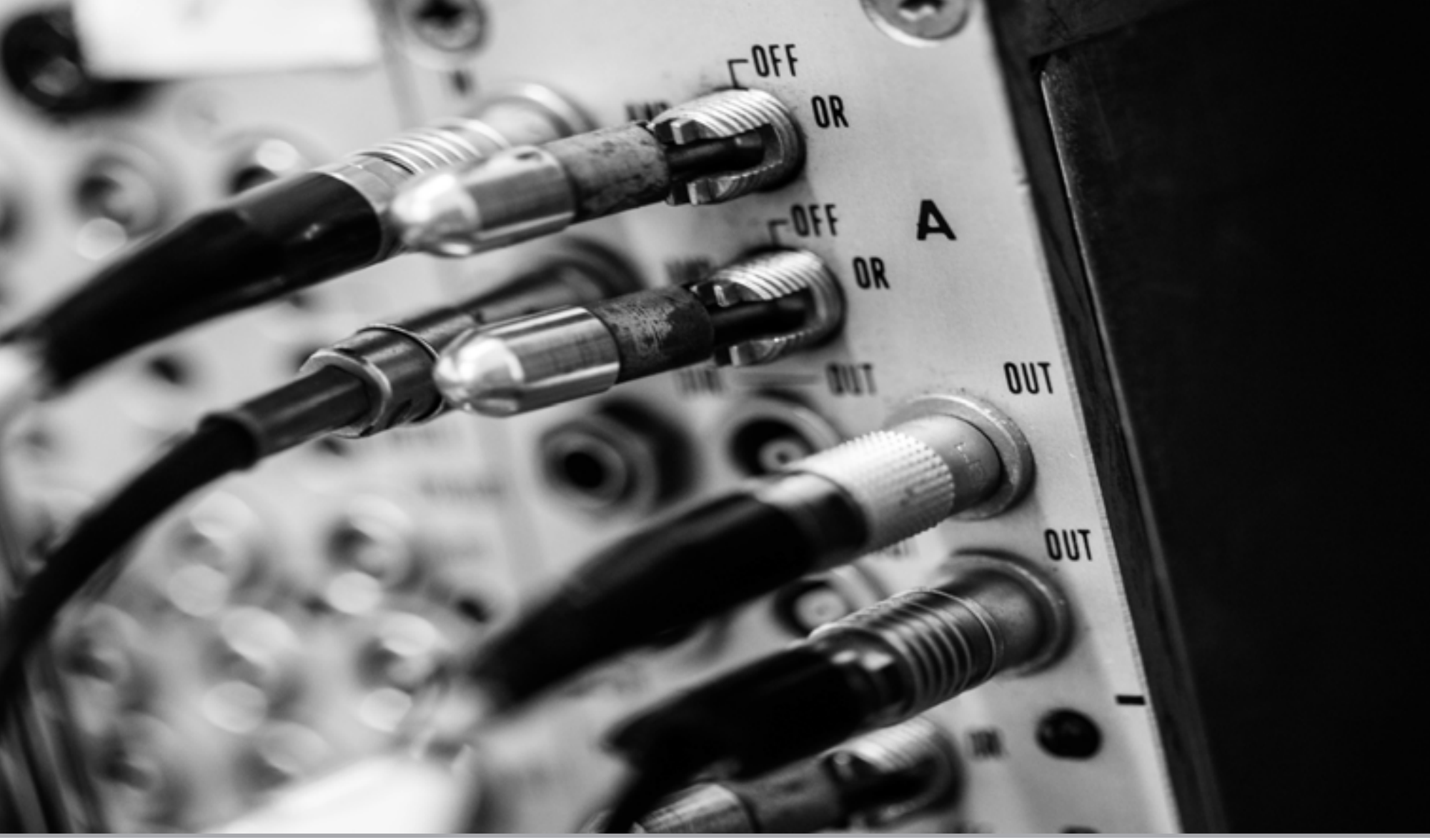

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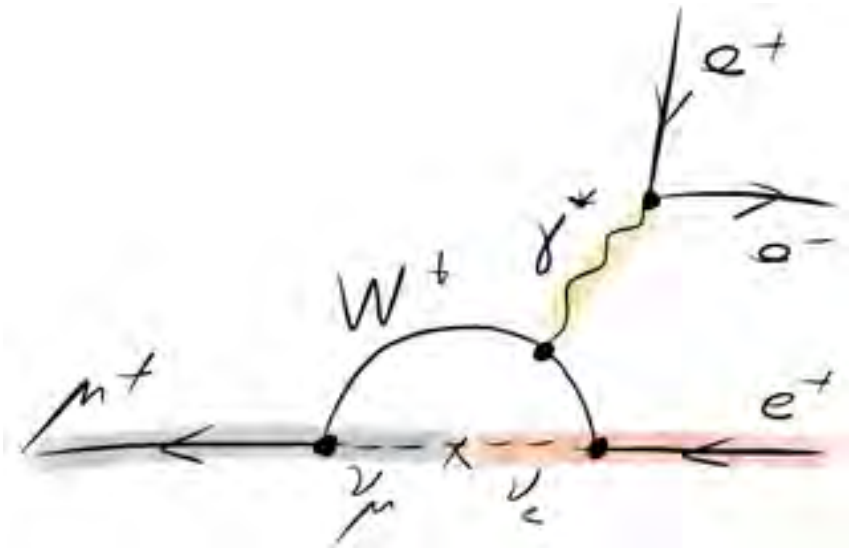
Firmware and Synchronisation of the First Layer in the Mu3e DAQ System

Martin Müller, DPG Spring Meeting 2021

Mu3e

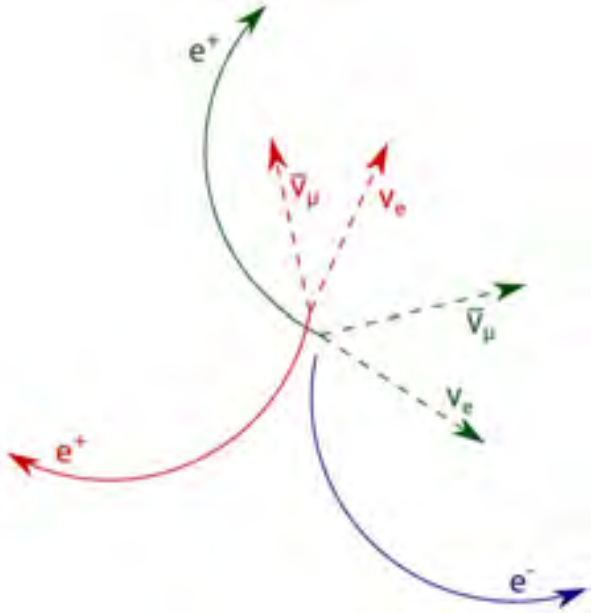
$\mu^+ \to e^+ e^- e^+$



Mu3e

- search for the lepton flavour violating decay $\mu^+ \to e^+ e^- e^+$
- predicted branching ratio of 10^{-54} (not observable)
- observation of $\mu^+ \to e^+ e^- e^+$ would be a clear sign for new Physics

Introduction
Background processes



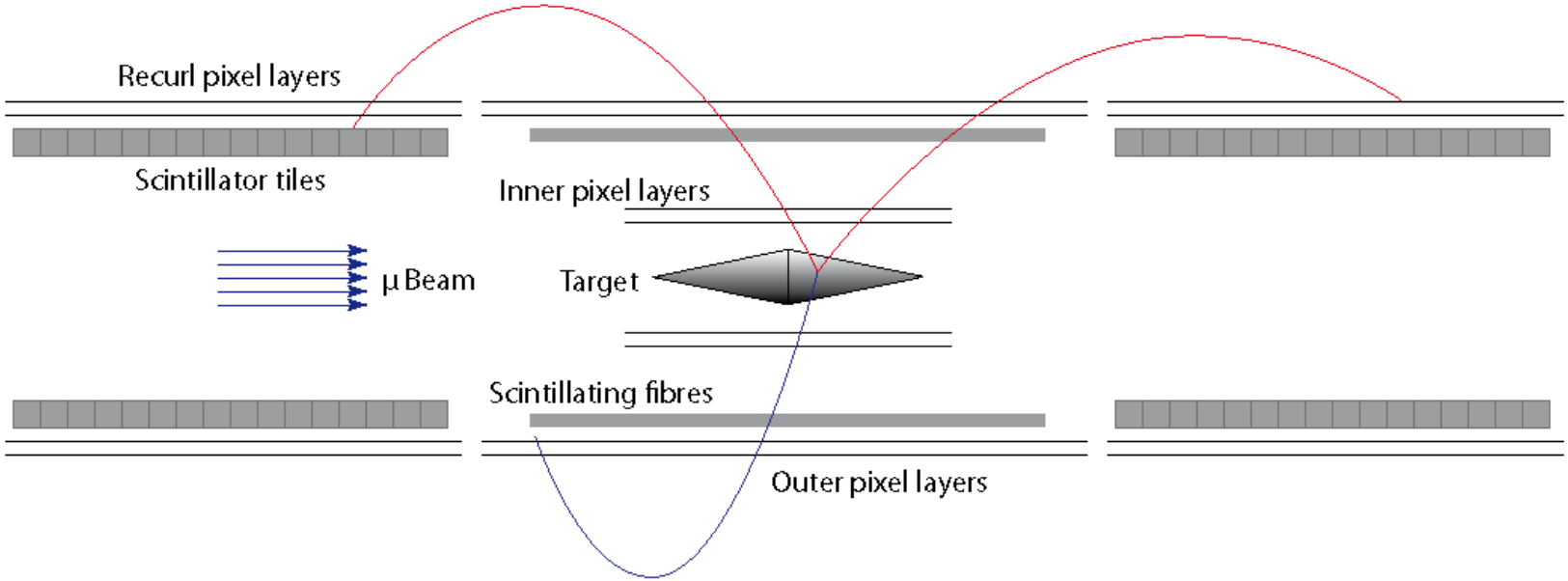
Background processes:

- $\mu^+ \rightarrow \mathrm{e}^+ \nu_\mathrm{e} \overline{\nu}_\mu \mathrm{e}^+ \mathrm{e}^-$
- combinatorial

For **signal** events: $\sum \vec{p} = 0$, $\sum E = m_\mu$, $\Delta t = 0$, same vertex

Low electron momenta $\rightarrow$ multiple scattering $\rightarrow$ material budget

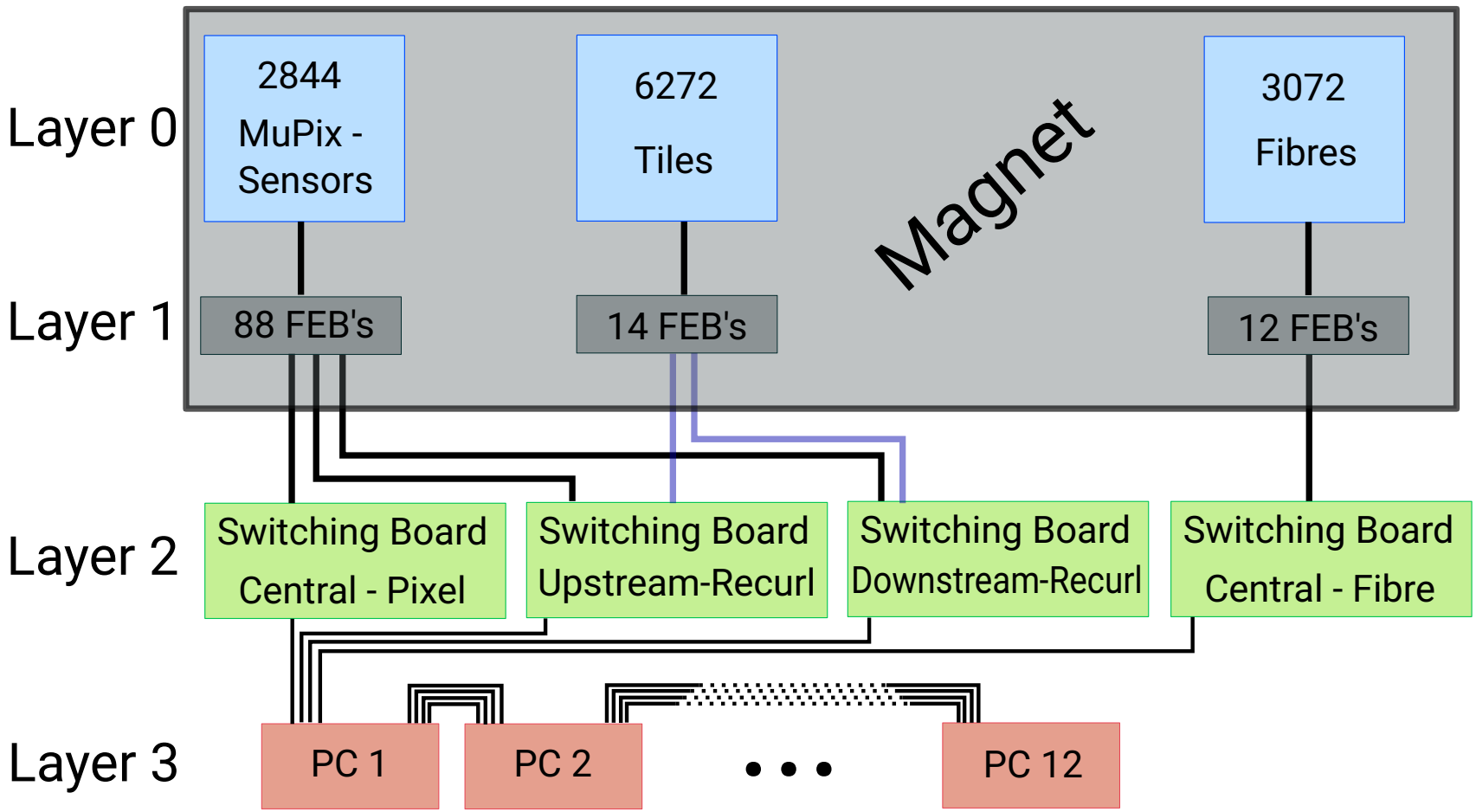
Introduction
The Mu3e Detector



- 4 layers of pixel sensors ($\sigma t = 10$ ns)
- scintillating fibres (σt =500 ps) & tiles (σt =70 ps) to increase timing precision
- $\rightarrow$ need time synchronization (clock and reset) to this precision
- expected data rate of up to 80 GBit/s

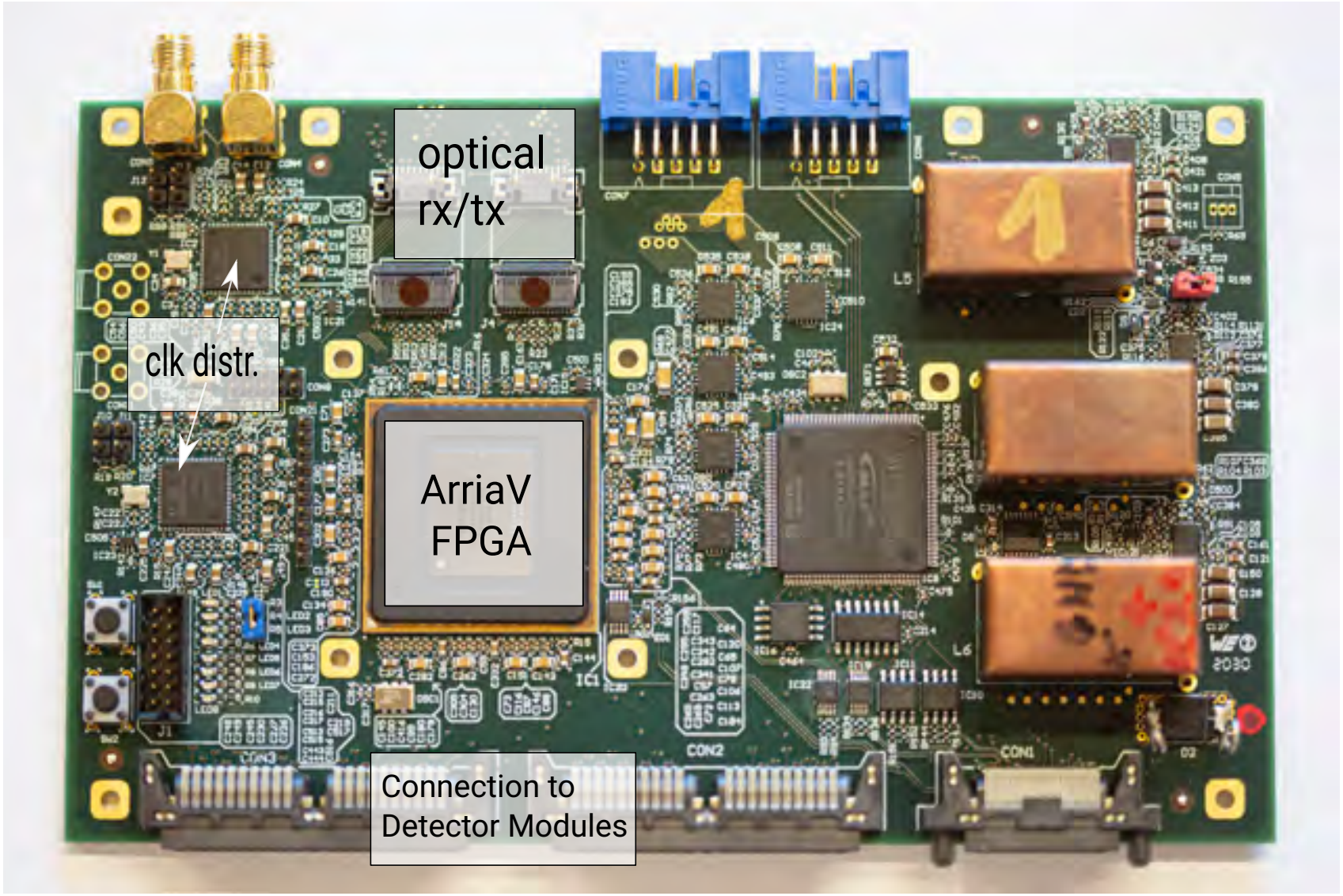
DAQ System

Overview



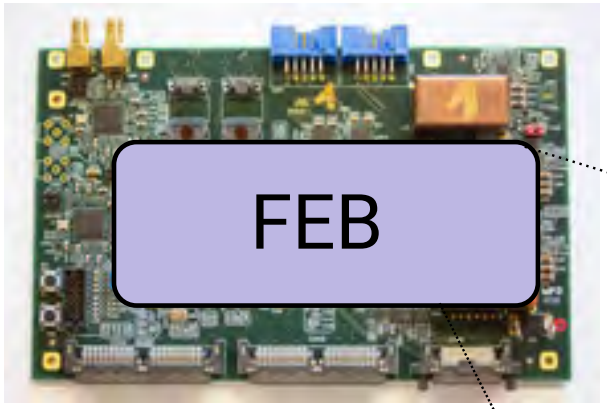
FE Board

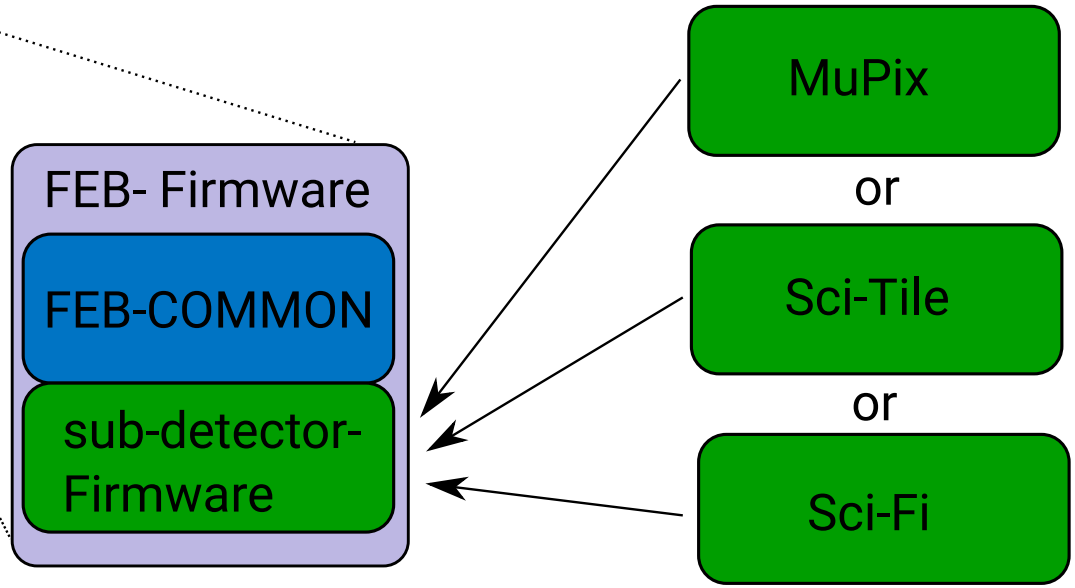
FE Board



FE Board

Firmware concept





Common ↔ sub-detector Interface

- Detector data
- access to slowcontrol system
- run state signals
- confirmation of run state changes

Synchronization

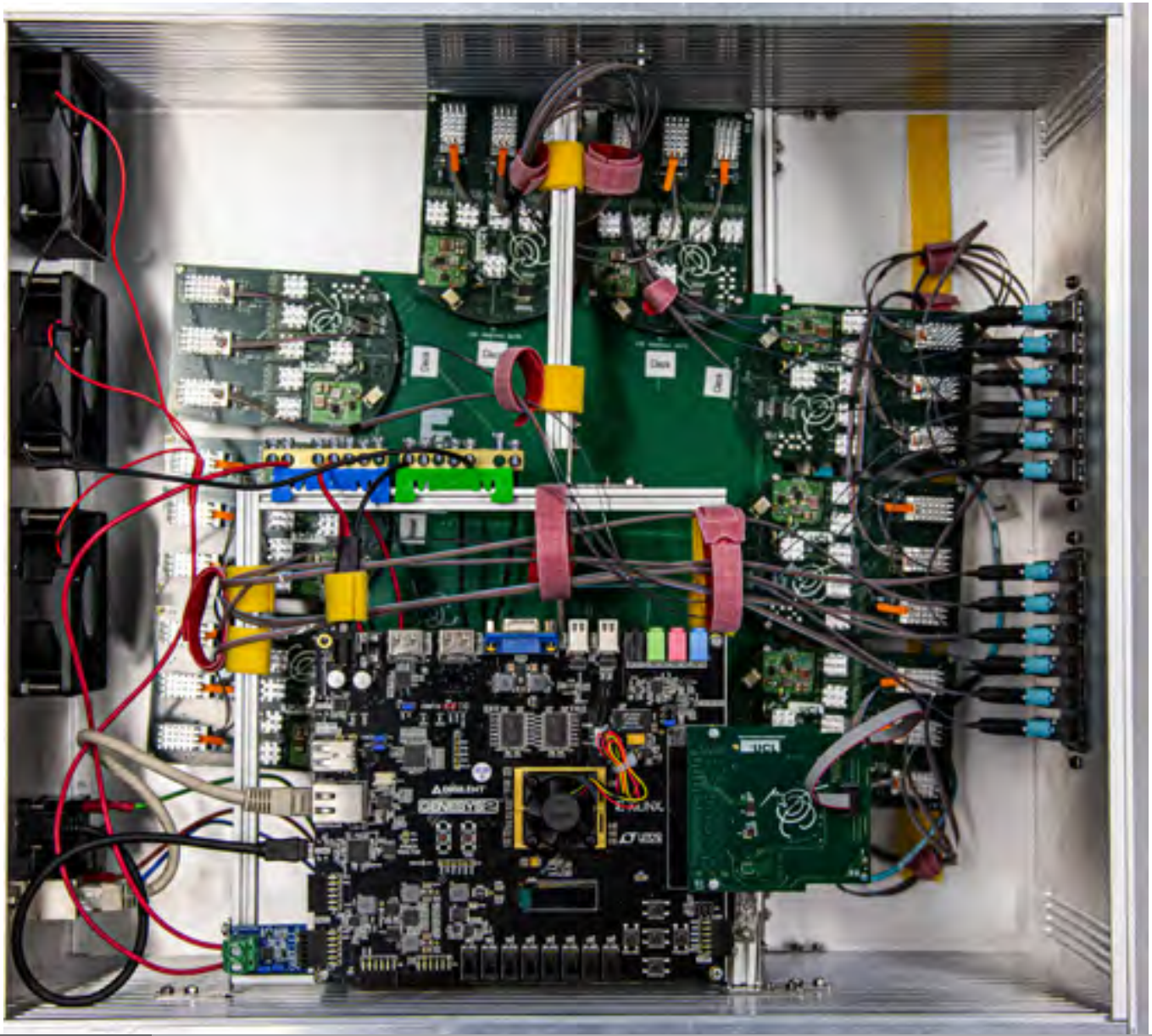
Reset idea

1. run starts need to happen in the same clock cycle for all components in the detector
2. $\rightarrow$ time window of 1 global clock cycle (125 MHz) where the reset has to arrive
3. $\rightarrow$ re-synchronise reset to global clock at detector-asic level
4. $\rightarrow$ reset with precision of clock distribution

$\rightarrow$ Additional optical Reset line.

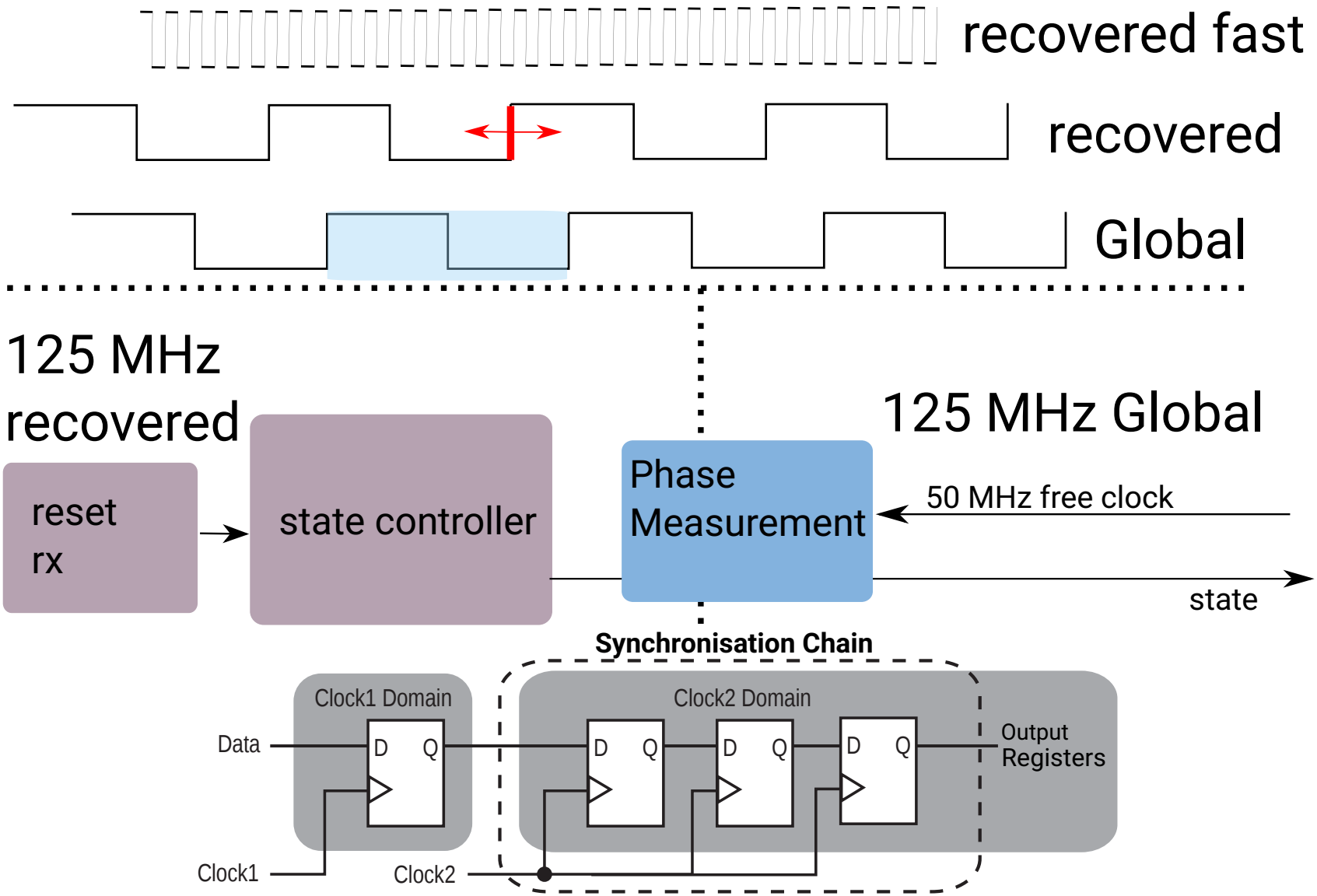
Synchronization

Clock and Reset Box



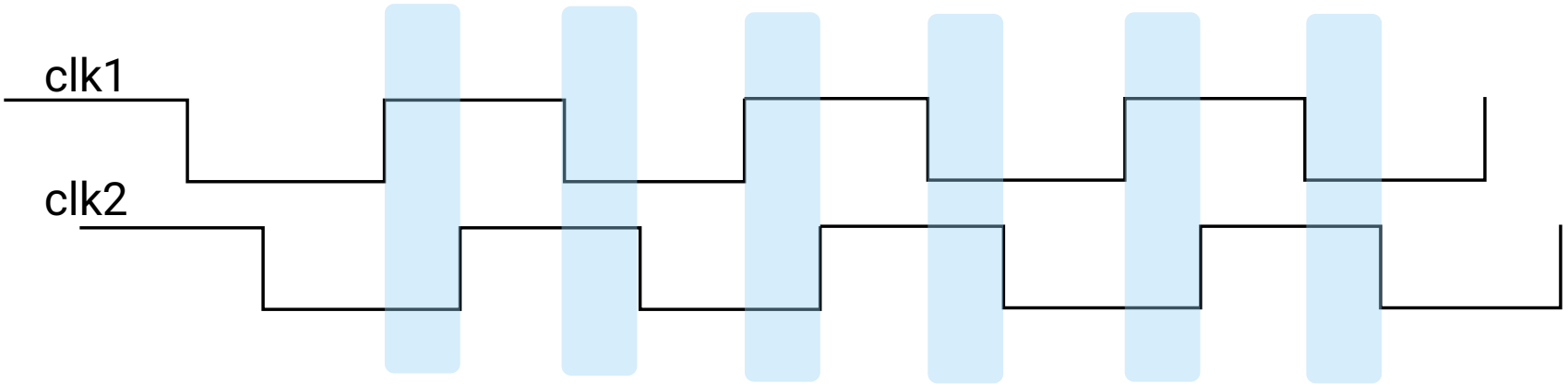
Synchronization

Clock Domains



Synchronization

Phase measurements



- using independent, free running clock with frequency f
- measurement time T
- count clk1 != clk2 events on rising edge of independent clock
- $\rightarrow$ phase difference $= \frac{counts}{T \cdot f} \cdot \pi$

We can use this measurement to check if the reset is synchronized even without physical access to the board

Conclusion and Outlook

- system was operated for the first time with all sub-detectors at DESY last Year.
- Preparation for the first test run with a pixel vertex detector and timing detectors inside the Mu3e Magnet at PSI is ongoing