Department of Physics and Astronomy
University of Heidelberg

Master Thesis in Physics
submitted by

Lars Olivier Sebastian Noehte

born in Heidelberg (Germany)

2019

Microstrip Impedance Control in High Density Interconnects for the Mu3e Electrical Readout Chain

This Master Thesis has been carried out by
Lars Olivier Sebastian Noehte
at the
Physikalisches Institut in Heidelberg
under the supervision of
Prof. André Schöning

Abstract

The Mu3e experiment is going to search for the charged lepton-flavor violating decay $\mu^+ \to e^+e^-e^+$ with a sensitivity of one in 10^{16} events in phase II. Since the muons decay at rest, the detector material thickness has to be minimized. The tracking layers of the detector deploy the HV-MAPS pixel sensor MuPix, which can be thinned down to 50 µm. Achieving a thickness of $X/X_0 = 0.115\%$ radiation lengths per layer requires an ultra-thin readout structure, capable of transmitting 1.25 Gb/s data streams reliably, in the form of a high density interconnect. Throughout this thesis, the impedance of two-layer aluminum polyimide high density interconnects has been studied. 2D simulations of 12 µm thin microstrips have been compared to an analytic model, to predict the proper trace parameters for impedance matching. Additionally, a first high density interconnect demonstrator has been operated at 1.25 Gb/s successfully in combination with the MuPix8 sensor prototype. The 24 cm long differential traces of this demonstrator have been characterized. An attenuation of 5.5 dB has estimated from eye diagram measurements, and a bit error rate of 2×10^{-15} (95 % CL) at 1.25 Gb/s has been achieved. To complete the readout chain between sensor and front-end board, 2 m long unshielded twisted pair cables have been characterized as well, giving an attenuation of 6.6 dB.

Zusammenfassung

Ziel des Mu3e experiments ist es, den $\mu^+ \to e^+e^-e^+$ Zerfall mit einer Sensitivität von einem aus 10^{16} Zerfällen zu messen. Da die Myonen in Ruhe zerfallen, muss das Material im Detektor minimal gehalten werden. Die Tracking-Lagen bestehen aus HV-MAPS Pixelsensoren, genannt MuPix, welche auf eine Dicke von 50 µm gedünnt werden können. Um eine Lagendicke von $X/X_0 = 0.115\%$ Strahlungslängen erreichen zu können, sind sehr dünne Auslesestrukturen in Form von "high density interconnects" (HDI) erforderlich, welche zuverlässig 1.25 Gb/s übertragen können. Im Rahmen dieser Abschlussarbeit wurden zweilagige Aluminium - Polyimid HDIs untersucht. Um die passenden Spurparameter zur Impedanzanpassung vorhersagen zu können, wurden 2D Simulationen von 12 µm dünnen Microstrips mit einem analytischen Modell verglichen. Zusätzlich wurde zum ersten Mal ein HDI in Kombination mit dem MuPix8 Sensor-Prototypen erfolgreich bei einer Datenübertragungsrate von 1.25 Gb/s in Betrieb genommen. Die 24 cm langen differenziellen Datenspuren wurden charakterisiert. Die Dämpfung der Spuren wurde mit Hilfe von Augendiagrammen auf 5.5 dB abgeschätzt. Außerdem konnte eine Bitfehlerrate von 2×10^{-15} (95 % CL) bei 1.25 Gb/s festgestellt werden. Um die Auslesekette zu vervollständigen, wurde ein 2 m langes "Unshielded Twisted Pair" Kabel ebenfalls charakterisiert. Die Dämpfung des Kabels wurde auf 6.6 dB geschätzt.

Contents

Chapter 1

Introduction

The ultimate goal of physics is to describe nature, to predict nature. From the largest scales of the universe to the tiniest elementary particle, physics pursuits a comprehensive mathematical expression of all phenomena – an equation that is as simple as possible from which all other theories can be derived from.
A promising candidate for this theory is the Standard Model. It is a confluence of the Dirac equation, Quantum Field Theories, the Gauge principle as well as the Higgs mechanism, supplemented with experimental data [Tho13]. The Standard Model possesses 25 free parameters (26 with strong CP violation). These parameters are the Yukawa couplings of the elementary fermions to the Higgs field, the coupling constants of the gauge interactions, the vacuum expectation value as well as the mixing angles of the PMNS and CKM matrices [Tho13]. Over the past decades, many parameters were measured with excellent precision. Nevertheless, some open questions remain. The Standard Model does not contain Gravity. Neither does it contain Dark Matter, nor does it explain the mass hierarchy of the elementary particles and many more questions.
The experimental physicists' task is to test the Standard Model for its credibility, especially in domains where little is know. One of many ways to test the Standard Model is high precision experiments of rare particle decay. Any significant deviation from the theory prediction would be a hint for new physics.

1.1 Mu3e experiment

The Mu3e experiment aims to measure the charged lepton flavor violating decay $\mu^+ \to e^+e^-e^+$ with a sensitivity of one in 10^{16} events in phase II [B$^+$]. The experiment will be situated at the πE5 muon beamline at the Paul-Scherrer Institut in Switzerland.[PSI19] The goal is to stop the muons in a target and measure the decay products. The latest experimental limit for the $\mu^+ \to e^+e^-e^+$ branching

ratio was set by the Sindrum experiment to be $B_{\mu^+\to e^+e^-e^+} < 1.0 \times 10^{-12}(90\,\%\text{CL})$ [UB88]. By doing cutting-edge detector development, Mu3e pushes this limit with a new generation of detector technology.

1.1.1 Signal vs. Background

To distinguish the rare decay $\mu^+ \to e^+e^-e^+$ from background events (sketched in figures 1.1), Mu3e requires to be able to reject two kinds of backgrounds. The accidental background is a combination of two or more different processes leading to a $\mu^+ \to e^+e^-e^+$ like signature in the detector. [B$^+$] A combination could be a Michel Decay $\mu^+ \to e^+\nu\bar{\nu}$ with Bhabha scattered electrons from the stopping target. The other background is internal conversion $\mu^+ \to e^+e^-e^+\nu\bar{\nu}$. The background looks similar to the signal except for a fraction of the momentum carried by neutrinos [B$^+$]. The products of the $\mu^+ \to e^+e^-e^+$ process are restricted by energy and momentum conservation:

$$\vec{p_\mu} = \sum_{i=1}^{3} \vec{p_i} = 0 \tag{1.1}$$

$$E_{tot} = \sum_{i=1}^{3} E_i = m_\mu c^2 \tag{1.2}$$

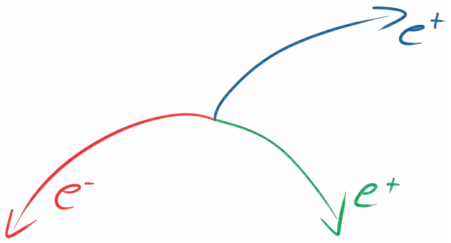
The muon decays at rest, which limits the maximal energy of each decay product to $\frac{m_\mu c^2}{2} \approx 53\,\text{MeV}$. In addition to the electron and positrons originating time coincident from the same vertex, these constraints are used to distinguish signal and background.

1.1.2 Multiple Coulomb scattering

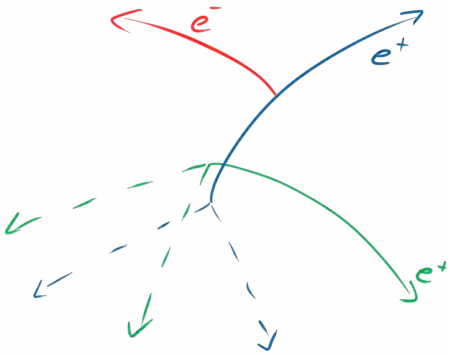
When reconstructing the low momentum of electrons and positrons, scattering is a limiting factor of the momentum resolution. The process of scattering on Coulomb fields of multiple nuclei in the detector material is called multiple Coulomb scattering. According to Molière, the central 98% of the resulting scattering angle is approximated to be Gaussian distributed. The Highland equation describes its root mean square [B$^+$12].

$$\theta_{RMS} = \frac{13{,}6\,\text{MeV}}{\beta cp} z \sqrt{\frac{x}{X_0}} \left[1 + 0.038 \ln\left(\frac{x}{X_0}\right)\right] \tag{1.3}$$

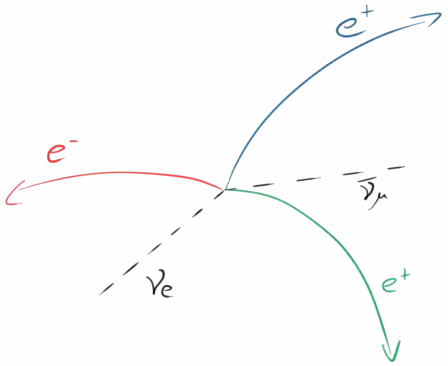
where $\beta = \frac{v}{c}$ is the relativistic velocity, z denotes the charge of the incident particle, and p its momentum. Only by reducing the thickness x, or increasing the radiation length X_0, of the material in the detector, the scattering distribution gets more



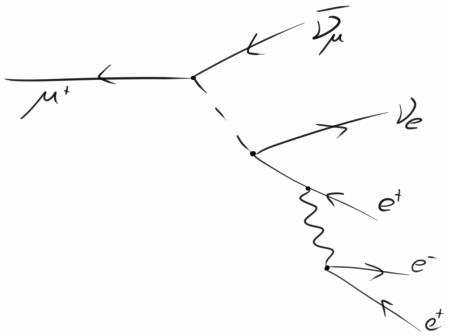
(a) $\mu^+ \to e^+e^-e^+$



(b) Possible accidental background with Bhabha scattering



(c) Background from radiative internal conversion



(d) Radiative internal conversion Feynman graph

Figure 1.1: Signal and background signature sketches

confined. Especially in the tracking region, keeping a minimal material budget is crucial.

1.2 Mu3e detector

The Mu3e detector [B+] is a barrel-shaped ultra-low material budget detector. To measure the momentum of the decay products, the trajectories are bend by a 1 T homogeneous solenoidal magnetic field. The magnet has a bore of 1 m and encloses the detector entirely. Figure 1.2 shows a rough sketch of the detector structure.

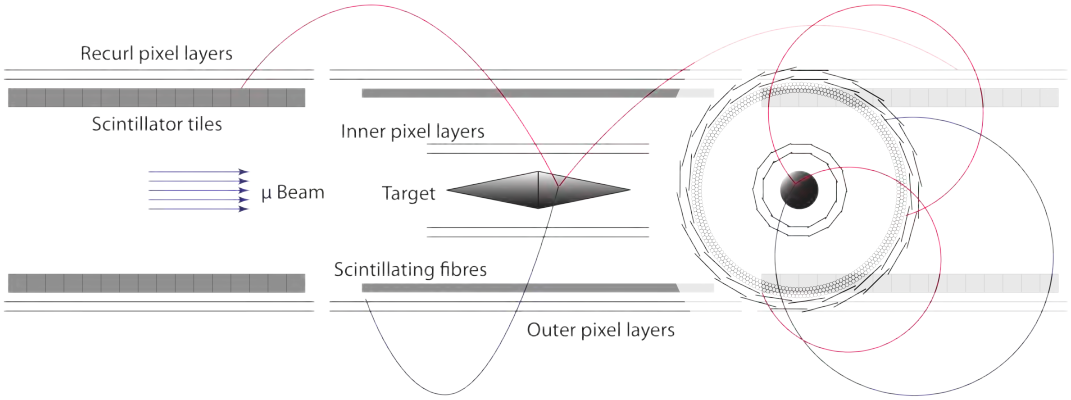


Figure 1.2: Mu3e detector sketch

The muon beam is stopped by the hollow double-cone target in the center of the sketch. The muon decay products are detected first by the two inner tracking layers and then by the two outer tracking layers. Higher energy electrons with suitable longitudinal momentum can reach the two recurl layers before being stopped in the scintillator tiles. The scintillator tile and fibre layers are used to increase the time information of the trajectories.

MuPix

The heart of the detector is the silicon pixel sensor called MuPix, deployed in the tracking layers. The MuPix is an about $2 \times 2\,\mathrm{cm}^2$ large High-Voltage Monolithic Active Pixel Sensor (HV-MAPS). The active pixel matrix is combined with the

entire readout electronic in a monolithic architecture. Compared to regular MAPS chips, a high-voltage is applied to the pixel diodes in reverse bias for fast charge collection in a large depletion zone. The MuPix has a triggerless readout system, which creates a continuous 1.25 Gb/s 8b/10b zero-suppressed serial data stream. The data is sent out with three differential links at the inner tracking layers and with one at the outer tracking layer.

Ladders and modules

The data is driven towards the support structure end-rings situated at the ends of the barrels. The barrel length is determined by the number of MuPix sensors in one ladder. The inner layers have a length of six sensors, while the outer layers contain 16 and 18 MuPix sensors. A inner layer ladder is shown in figure 1.3.

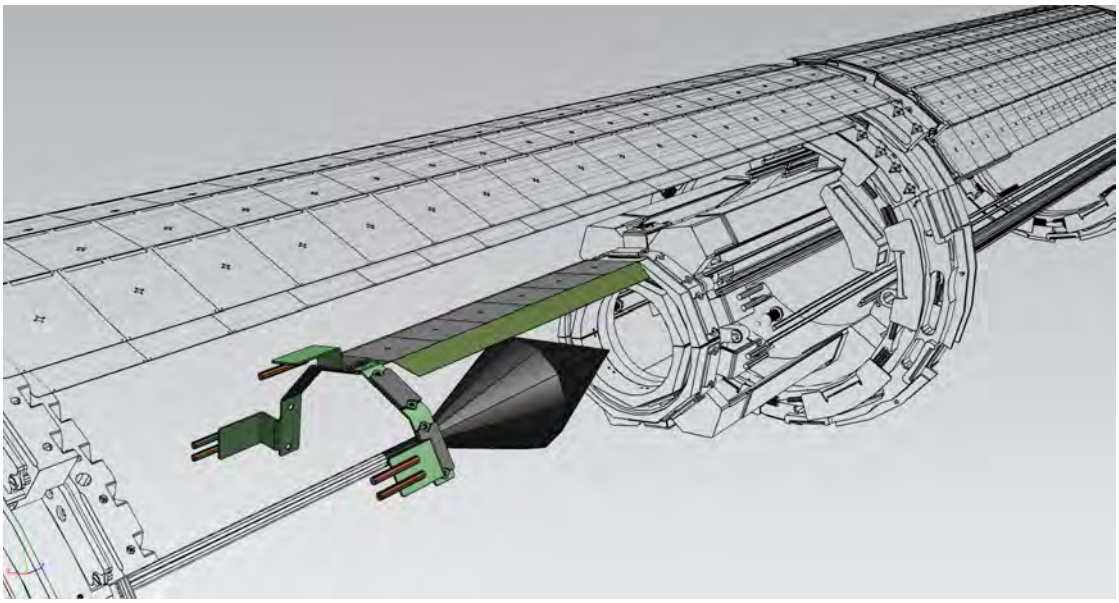


Figure 1.3: Mu3e Detector CAD; Colored parts show one inner-layer-ladder with six MuPix chips (gray) attached to an aluminum high density interconnect (warm-green), a flexible printed circuit board (light-green) shaped like a half-ring with mounting brackets (black), and short tubes resembling the unshielded twisted pair strands. The detector is cut open, and the scintillating fibres are removed, to show the inner-layer ladder.

Each layer has a total thickness of 0.115% radiation lengths. This also includes the transmission and power lines glued and bonded to the MuPix. The data and power lines are realized through high density interconnects (HDIs). The HDIs in

the detector are thin sheets of aluminum-polyimide laminate. They also serve as the support structure for the MuPix chips. The HDIs are electrically split in the middle and supply the chips from both ends of the ladder. At the end-rings, the HDIs are connected to a flexible printed circuit board (flexprint), which combines the ladders to a module. The signal traces of each module are routed on the flexprint, such that the data traces are conflated to strands of unshielded twisted pair (UTP) cables. The UTP cable strands are depicted in figure 1.3 as short tubes, when in fact, they are transmitting the signal to the field-programmable gate array (FPGA) front-end boards. The routing distance is estimated to be in the order of 2 m.

1.3 Electrical readout requirements for the tracking layers

The main focus of this thesis is the data transmission over the high density interconnects. The pixel sensors in the Mu3e experiment will be read out via 1.25 Gb/s links. In the confined space, no additional active components will be placed, whereby the material budget is reduced to a minimum. The data transmission is limited to two layers of aluminum. In the tracking region, the area of each layer must not exceed the area covered by the MuPix sensors in one ladder. The goal is to give a recommendation for a set of trace parameters for optimized signal transmission. Additionally, an HDI is studied in combination with a MuPix prototype as a proof of principle for this readout design.

Chapter 2

Signal transmission

The most crucial point in signal transmission is the prediction of the outgoing signal shape.
Mathematically every transmission line can be described as a linear, time-invariant mapping from the incidental signal $u(t)$ to the outgoing signal $v(t)$ [Sch16].

$$T: \ u(t) \ \rightarrow \ v(t) \tag{2.1}$$

Using the δ-Distribution , defined by $\int_{-\infty}^{\infty} x(t) \ \delta(t)dt = x(0)$[Sch16], as test function, the resulting signal is called pulse response.

$$T(\delta(t)) \ = \ h(t) \tag{2.2}$$

Expressing $u(t)$ as a convolution with $\delta(t)$ and using the linearity of T, any $y(t)$ can be calculated as the convolution of $u(t)$ and $h(t)$.

$$u(t) \ = \ \int_{-\infty}^{\infty} u(\tau) \ \delta(t-\tau)d\tau \tag{2.3}$$

$$\Rightarrow y(t) \ = \ T(u(t)) \ = \ \int_{-\infty}^{\infty} u(\tau) \ T(\delta(t-\tau))d\tau \tag{2.4}$$

$$= \int_{-\infty}^{\infty} u(\tau) \ h(t-\tau)d\tau = u(t) \ * \ h(t) \tag{2.5}$$

In this case the convolution theorem [Sch16] applies, which states that a Fourier transform $\mathcal{F}$ of a convolution of the signals $u(t)$ and $h(t)$ is the same as the product of the Fourier transform of these mappings $U(i\omega)$ and $H(i\omega)$.

$$Y(i\omega) \ = \ \mathcal{F}\{u(t) \ * \ h(t)\} \ = U(i\omega) \cdot H(i\omega) \tag{2.6}$$

The Fourier transform of $h(t)$ is called transfer function. Using the absolute value, one can derive the attenuation or gain of this system, quoted as the frequency

spectrum. [Sch16]

$$attenuation : a(\omega) = -20 \log_{10}(\|H(i\omega)\|) \quad \text{in dB} \tag{2.7}$$

$$gain : g(\omega) = 20 \log_{10}(\|H(i\omega)\|) \quad \text{in dB} \tag{2.8}$$

2.1 Transmission line

The transfer function of a transmission line can be determined either through measurements or estimated by a model. If the transmission line has many free parameters, relying on measurements often gets very costly and time-intensive. Since Maxwell published the equations of electromagnetism in the mid 19th century, nearly every model in electronics is based on these four equations.

$$\nabla \cdot \vec{E} = \frac{\rho}{\epsilon} \quad \text{Gauss's law} \tag{2.9}$$

$$\nabla \cdot \vec{B} = 0 \quad \text{Gauss's law for magnetism} \tag{2.10}$$

$$\nabla \times \vec{E} = -\frac{\partial \vec{B}}{\partial t} \quad \text{Faraday's law of induction} \tag{2.11}$$

$$\nabla \times \vec{B} = \mu \left(\vec{J} + \epsilon \frac{\partial \vec{E}}{\partial t} \right) \quad \text{Ampère's circuital law} \tag{2.12}$$

Not all conductor shapes have an analytical solution of the Maxwell's equations. For some problems, approximations derived from solved conductor shapes exist. Another way is to model the transmission line with ideal electronics components and support it with either measurement samples or numerical simulations.

2.1.1 Lumped element model

A common way to model a transmission line is to divide the length of the conductor into several lumped elements. In the case of digital signals, these lumped circuits shall be shorter than one-sixth of the length of the rising edge [JG11]. Rise-time and propagation speed define the length of the rising edge. As depicted in figure 2.1, each element is a four-port system composed of a series resistor and an inductor as well as a shunt capacitor and resistor [Zha15, JG03, Roh78].

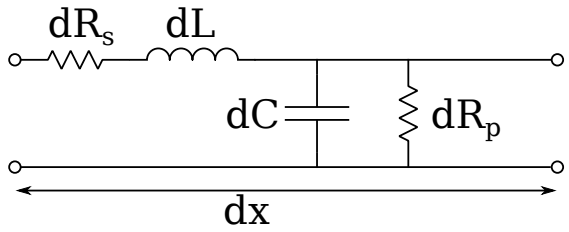


Figure 2.1: Schematic of a Lumped model element.

2.1.2 Telegrapher's equation

The Telegrapher's equations describe the current and voltage relations in the lumped element

$$dV(x,t) = -dL\ \frac{\partial I(x,t)}{\partial t} - dR\ I(x,t) \tag{2.13}$$

$$dI(x,t) = -dC\ \frac{\partial V(x,t)}{\partial t} - dG\ V(x,t) \tag{2.14}$$

where $G = 1/R_p$. They can be derived by adding the separate voltage drops dV (equation 2.15 and 2.16)and current losses dI (equation 2.17 and 2.18) according to Kirchhoff's circuit laws [JG11, Zha15, Roh78, Jac14].

$$dV_{R_s}(x,t) = dR_s\ I(x,t) \tag{2.15}$$

$$dV_L(x,t) = -dL\ \frac{\partial I(x,t)}{\partial t} \tag{2.16}$$

$$dI_C(x,t) = dC\ \frac{\partial V(x,t)}{\partial t} \tag{2.17}$$

$$dI_G(x,t) = \frac{1}{dR_p}\ V(x,t) = dG\ V(x,t) \tag{2.18}$$

d denotes the derivative $\frac{\partial}{\partial x}$.

2.1.3 Impedance

The lossless case $R_s = G = 0$ separates the time dependent components from the time-independent ones. In this case, only equation 2.16 and equation 2.17 needs to be solved:

$$dV(x,t) = -dL\ \frac{\partial I(x,t)}{\partial t} \tag{2.19}$$

$$dI(x,t) = -dC\ \frac{\partial V(x,t)}{\partial t} \tag{2.20}$$

In the sinusoidal steady-state the voltage and current can be treated as planar waves $\xi(x,t) = \xi(x) \cdot \exp(i\omega t)$ with known time derivatives [JG11, Zha15, Roh78, Jac14].

$$dV(x) = -i\omega L\ I(x) \tag{2.21}$$
$$dI(x) = -i\omega C\ V(x) \tag{2.22}$$

The second spacial derivative gives:

$$\frac{\partial^2}{\partial x^2}\ V(x) = -i\omega L\ \frac{\partial}{\partial x} I(x) \tag{2.23}$$
$$\frac{\partial^2}{\partial x^2}\ I(x) = -i\omega C\ \frac{\partial}{\partial x} V(x) \tag{2.24}$$

Inserting equation 2.21 and 2.22, this resolves into two quadratic differential equations.

$$\frac{\partial^2}{\partial x^2}\ V(x) = -\omega^2 LC\ \frac{\partial}{\partial x} I(x) \tag{2.25}$$
$$\frac{\partial^2}{\partial x^2}\ I(x) = -\omega^2 LC\ \frac{\partial}{\partial x} V(x) \tag{2.26}$$

The solutions can be expressed as complex wave function.

$$V(x) = V_1 e^{-ikx} + V_2 e^{+ikx} \tag{2.27}$$
$$I(x) = I_1 e^{-ikx} + I_2 e^{+ikx} \tag{2.28}$$
$$I(x) = \frac{V_1}{Z_0} e^{-ikx} - \frac{V_2}{Z_0}\ e^{+ikx} \tag{2.29}$$

V_1 and V_2 are constants, dependant on the boundary conditions. The wave number $k = \omega\sqrt{LC} = \frac{\omega}{u}$ connects the radial frequency ω with the propagation speed $u = \frac{1}{\sqrt{LC}}$. Z_0 is defined as the characteristic impedance of a transmission line [JG11, Zha15, Jac14].

2.1.4 Reflection

Impedance miss-match of two transmission lines or between a transmission line and termination usually causes reflections, which lead to interference distorting the waveform. The reflection coefficient Γ is defined as the fraction of the difference and the sum of the the two impedances [JG11].

$$\Gamma = \frac{Z_2 - Z_1}{Z_2 + Z_1} \tag{2.30}$$

Z_1 and Z_2 are the impedances of the two conductors. A system of a conductor with $Z_1 = 80\,\Omega$ being terminated with $Z_2 = 100\,\Omega$ has a reflection coefficient of $\Gamma \approx 11\%$. If the difference is negative, Γ is also negative. In this instance, the reflected wave has a phase-shift of π.

2.1.5 Ohmic resistance

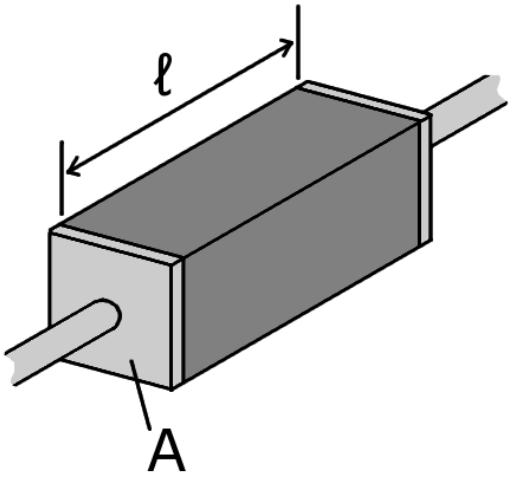


Figure 2.2: Geometry of a resistor

The ohmic resistance, is the basis of the series resistance of a transmission line. Applying a potential difference V to the ends of a conductor with a given cross-section A and length l creates an electric field $E = \frac{V}{l}$. The resulting force is connected to the electric field via the electron charge $F = eE$. In condensed matter, electrons in conductors are described as oscillations in reciprocal space. Electrons scattering in an ideal lattice leads to a vanishing average velocity. Only defects in the lattice cause a non zero drift velocity $v_D = \mu E$ of the charge, where μ denotes the mobility of the respective charge. Regarding the electrical current as number of charges transported per time, the current is proportional to the number of electrons per unit cell n.

$$I = \frac{\Delta Q}{\Delta t} = e\,\frac{\Delta N}{\Delta t} = enA\,\frac{\Delta s}{\Delta t} \tag{2.31}$$

With the volume $A\Delta s$ of charges transported over a distance being the same as

its thickness Δs. Per definition $\frac{\Delta s}{\Delta t}$ equals the drift velocity.

$$\frac{\Delta s}{\Delta t} = v_D = \mu \; E = \mu \; \frac{V}{l} \tag{2.32}$$

$$\Rightarrow I = enAv_D = enA\mu \; \frac{V}{l} \tag{2.33}$$

With Ohm's law the resistance can be defined.

$$R = \frac{1}{en\mu} \; \frac{l}{A} = \rho \; \frac{l}{A} \tag{2.34}$$

With the characteristic resistivity ρ of the conductor and $\frac{l}{A}$ being a geometry factor [Roh78, Hun14].

2.1.6 Skin effect

For the regular ohmic resistance a current running through the entire cross section was assumed. A uniformly distributed current is valid for DC currents. For AC currents, like a digital signal, the skin effect affects the current distribution. For simplicity, a circular cross-section is assumed. A uniformly distributed current creates a magnetic eddy current field. Because of the alternating current, this field is also changing and inducing an electric eddy current field. This electric field causes a secondary current, which interferes with the primary one sketched in figure 2.3. The resulting current density is exponentially distributed.

$$|I| \propto e^{-z/\sigma} \tag{2.35}$$

With the distance to the surface z and the skin depth σ where the current is $1/e$ of the current at the surface.

$$\sigma = \sqrt{\frac{2 \; \rho}{\omega \; \mu}} \tag{2.36}$$

Where ρ is defined in equation 2.34, $\omega = 2 \; \pi\nu$ being the frequency and $\mu = \mu_0\mu_r$ being the absolute permeability [Kar17].

2.2 Low Voltage Differential Signaling

Low Voltage Differential Signaling (LVDS) is a differential data transmission I/O standard, using two conductors. One conductor transmits the digital data stream, the other one carries the same data but inverted. Only the difference between the two signals is received. Thus, common-mode distortions are eliminated. In the far-field, the radiation of both conductors cancels. LVDS is current-driven with a maximal current of 4.5 mA. The signal is usually differentially terminated with 100 Ω to 120 Ω [TI-19].

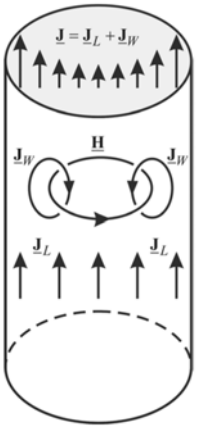


Figure 2.3: Three parted skech of the skin effect inside a cylindrical conductor. At the bottom is the DC like current density. In the center the eddy current is sketched and on top the combined current density is shown [Kar17]

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2.3 Analytic model of microstrips

Microstrips are planar conductors over a metal plane separated by a dielectric medium.The signal is transmitted by the planar conductor while the metal plane serves as a reference potential, which can be ground or also a low voltage DC power trace. A differential pair of microstrips is usually called edge- or parallel-coupled microstrips. The structure of an edge-coupled microstrip pair is shown in figure 3.1. The impedance for differential pairs has two modes. One is called even, in which both conductors transfer the identical signal. The second is the odd mode, in which one conductor carries the inverted signal of the other conductor. In the case of LVDS, the odd mode is the relevant one. Usually, the impedance is calculated for one conductor in this environment first and then doubled for the differential pair [Zha15].

$$Z_{diff} = 2 \cdot Z_{odd} \tag{2.37}$$

Deriving the impedance Z_{odd} requires to solve the Maxwell equations for a given geometry. The rectangular structure of microstrips is inapplicable to solve in polar coordinates. Elaborate models are based upon conformal mapping and perturbation. Typical parameters for these models are the trace width W, the gap between the two conductors s, and the dielectric height h between the two metal layers. The traces are mostly assumed to be thin, meaning the metal layer thickness t is much smaller than the width $t \ll W$. Thick traces have a more considerable electric fringe field. One very elaborate model is developed by E. Hammerstad and

Ø. Jensen, published in 1980 [HJ80]. The authors claim it to be 99.2% accurate in the range of $0.1 \leq u \leq 10$ and $g \geq 0.01$ with

$$u = \frac{W}{h} \tag{2.38}$$

$$g = \frac{s}{h} \tag{2.39}$$

where h is the dielectric height. The model (equation A.1) and its substitutions (equation A.2 - A.22) are presented in the appendix. Figure 2.4 shows the differential impedance Z_{diff} plotted over the height normalized trace width u and the height normalized gap g.

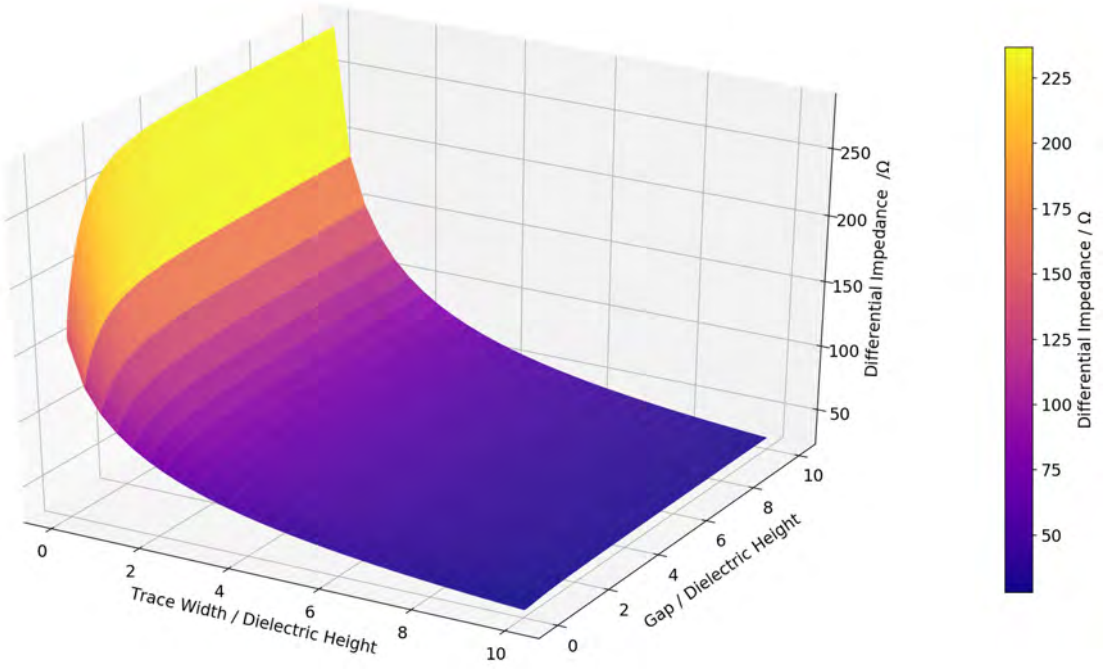
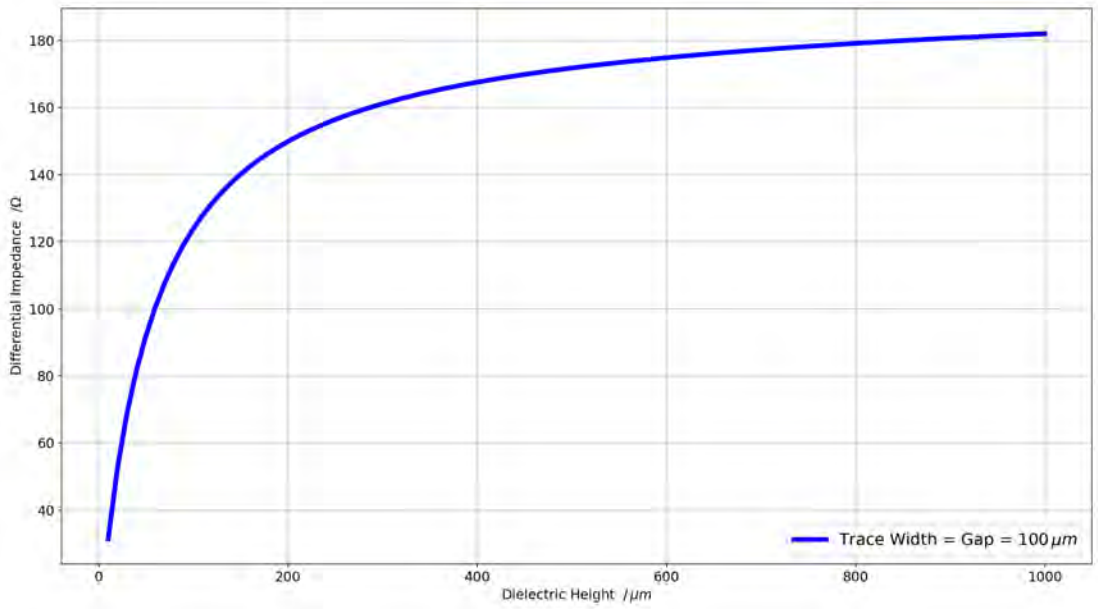
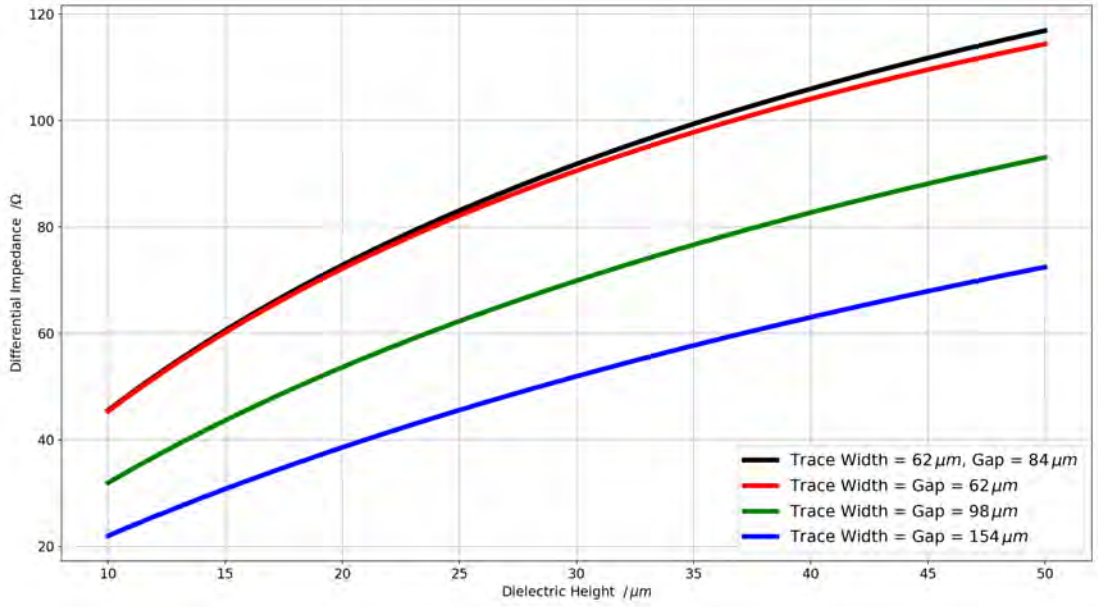


Figure 2.4: Differential impedance Z_{diff} after Hammerstad and Jensen plotted over the height normalized trace width u and the height normalized gap g for the range of $0.1 \leq u \leq 10$ and $0.01 \leq g \leq 10$.

The dominant contribution is the normalized trace width u, which causes the impedance to diverge towards infinity for small u. According to this model, the gap counteracts this behavior but is only in the domain of small width and narrow gap, an essential parameter according to this model. In figure 2.5(a) and figure 2.5(b) the differential impedance is shown as a function of the dielectric height



(a) Dielectric height at full range of model



(b) Dielectric height limited to application range

Figure 2.5: Differential impedance Z_{diff} after Hammerstad and Jensen plotted over the dielectric height for different combinations of gap and trace width.

h. Figure 2.5(a) shows the scope of the model for $W = s = 100\,\mu m$ and figure 2.5(b) shows the scope of the layer stack intended for the use in the Mu3e pixel detector(see section 3.1.1). Regarding the latter scope, the graph gets more linear for larger a trace width and gap. Additionally, for larger trace width and gap, the impedance is overall smaller. The graph suggests that the dielectric height should be higher than 35 µm to reach LVDS standards. It should be noted that this model does not take the thickness and signal frequency into account. Fortunately, the differential impedance is nearly frequency-independent in the frequency domain for the Mu3e readout [Get73a, Get73b]. A summary and comparison of several models by Stefan Jahn [Jah19] is highly recommended for further reading.

Chapter 3

Materials and tools

3.1 High Density Interconnect

This chapter describes the structure and layout used for the High Density Interconnects (HDI). The HDI needs to serve all power and data connections to fully operate, configure, and read out the MuPix8 sensor. This thesis is focused on data transmission. For a discussion on powering schemes, see [Noe16].

3.1.1 Layer stack

The final tracking modules will consist of a simple layer stack of two electrical layers. Each layer consists of a layer of 12.5 µm thick aluminum laminated to 10 µm polyimide. Aluminum has a radiation length of 8.897 cm [PDG19a] and resistivity of $2.65 \times 10^{-8}\,\Omega\,\mathrm{m}$ [Win19], while copper has a radiation length of 1.436 cm [PDG19b] and resistivity of $1.68 \times 10^{-8}\,\Omega\,\mathrm{m}$ [Win19]. Aluminum was chosen for its longer radiation length, even if it has a higher resistivity compared to copper. The complete layer stack is shown in figure 3.1. Optionally, a spacer of 25 µm polyimide is added to adjust the distance to the reference plane, and thus to adjust the impedance. Sheets of polyimide usually come in multiple of 1 mil = 25.4 µm thicknesses. Hence, the dielectric height can only be changed in steps of 25 µm, plus an additional layer of glue. The trace structures are etched in the aluminum before assembling the stack. Therefore data traces are not restricted to one layer.

3.1.2 Single point Tape Automated Bonding

To transition between the two electrical layers, a particular type of via is used. The technique used for these HDIs is called Single point Tape Automated Bonding (SpTAB). For the via a cut-out in every dielectric layer, above the aluminum layer,

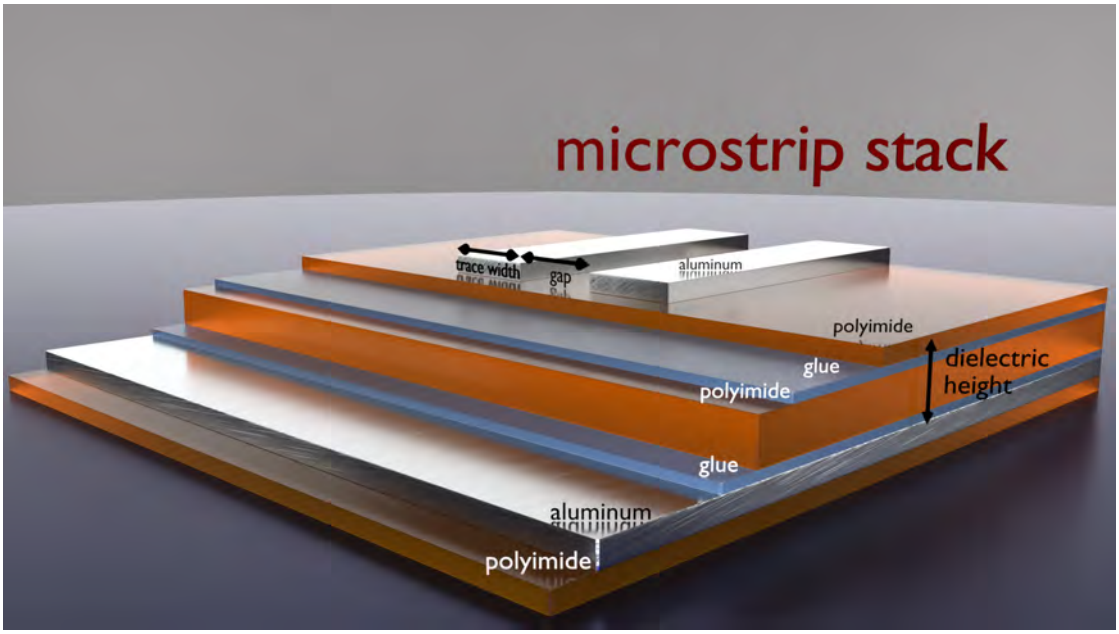


Figure 3.1: Layer stack from bottom to top: 10 µm polyimide, 12.5 µm aluminum, 5 µm glue, 25 µm polyimide, 5 µm glue, 10 µm polyimide, 12.5 µm aluminum

is required. The trace on top is pushed down through the cut-out, using a wedge tool, which is not much wider at its tip than the trace. The dimension of the cut-out must be chosen to ensure that the trace does not rip off when pushed down. At the point at which the trace is touching the bottom layer, the wedge tool needs to apply some force to press the two layers together while vibrating at ultrasonic frequencies produced by a transducer. As a result, the two metal layers fuse to a single lattice. If the force through the vibration and pressure is controlled precisely, the resulting bond gets robust and reliable. This technique can also be used to connect the bottom layer electrically to a sensor chip or a printed circuit board (PCB). PCBs are usually gold-coated to prevent corrosion. Since the bond does not heat up significantly during the process, the SpTAB prevents the production of gold - aluminum intermetallics [Jon97]. Hence, the bond does not get brittle or isolating. Besides reliability, using the trace itself for the connection is a significant advantage. Compared to traditional bonding techniques, SpTAB does not add additional material. SpTAB vias are also more versatile than traditional vias because a broader cut-out across two or more adjacent bond-spots is possible. A mutual cut-out for multiple layer transitions, allows for a parallel layer transition within a differential pair, preserving the impedance. Regular PCB vias do not preserve the impedance.

3.1.3 LTU constraints

Producing aluminum HDIs requires specialized machines for all required steps. One specialized company LTU [LTU13], based in Ukraine, produces such aluminum HDIs. They are capable of producing HDIs large enough for the outer tracking layers in the Mu3e detector. LTU does most of the alignment steps and gluing by hand. With hand alignment, the tolerances usually grow with the size of the assemblies, making smaller pieces preferable. Concerning structure size, the etching process is limited by the photomask defining the contour of the traces. LTU allows for a minimal structure size of 63 µm with a grid of 7 µm.

3.1.4 Single MuPix8 HDI

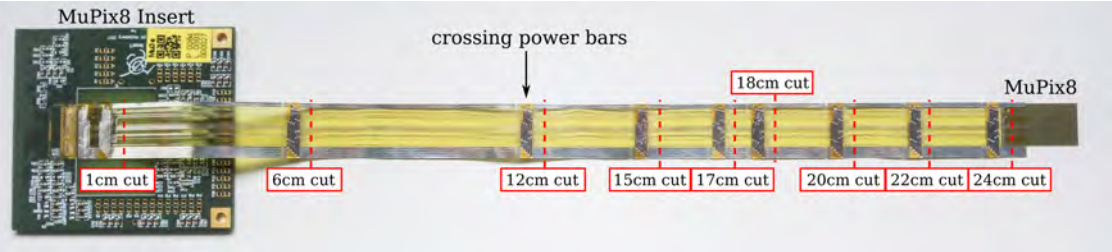


Figure 3.2: Single MuPix8 HDI shown with cutting points, bonded to the MuPix8 and the MuPix8 Insert

Before building an entire ladder with up to nine chips electrically connected in a row, it is essential to clarify that the MuPix sensor can be operated. The Single MuPix8 HDI is approximately 2 cm wide and 24 cm long and can be cut to various lengths (compare with figure 3.2). The region of interest is at 18 cm according to the longest traces in the outer tracking layers of the detector. It bonds via SpTAB to the Insert and on the other end to one MuPix8. The HDI provides all mandatory power and data connections. These include separate traces for VDD, VDDA, VSSA, GND, and GNDA, as well as four differential trace pairs for input and output links. All differential trace have the same trace width $W = 63$ µm and the same gap $s = 84$ µm. Except for crossing power bars for power distribution, the top layer is blank. The differential trace parameters are chosen to fit the impedance calculations for a microstrip cross-section (section 2.3). A reference plane is required to make the microstrip stack complete. This can be achieved by gluing a layer of aluminum underneath the HDI. The advantage is that the dielectric height and the gluing pattern can be chosen in the lab.

3.2 Unshielded Twisted Pairs

In the Mu3e detector, unshielded micro twisted pair (UTP) cables transmit the digital signals over the distance between end-rings and front-end boards. Shielding is not an option since it adds extra cross-section, and routing space is limited. The self-bonding wire W240 B200 from Heermann GmbH [Hee19] is a conceivable option, as well used by the CMS pixel detector at data rates up to 160 Mbit/s [PSI16].The wires have a solid copper core with a diameter of 127 µm. The isolation is 25 µm thick polyimide. The two strands stick together by a self-bonding enamel of 10 µm polyamide. Figure 3.3 visualizes the cross-section. For measurement purposes, the ends are separated and striped using a scalpel. Each wire-end is soldered to the signal pin of an SMA connector.

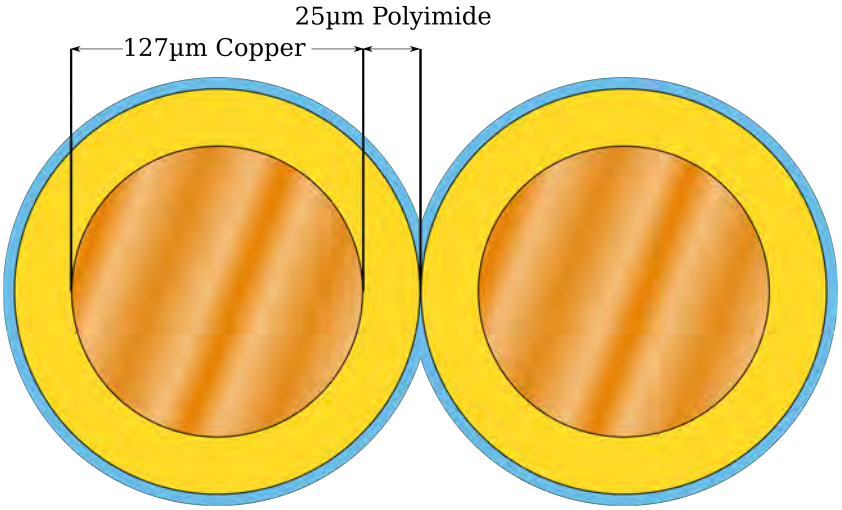
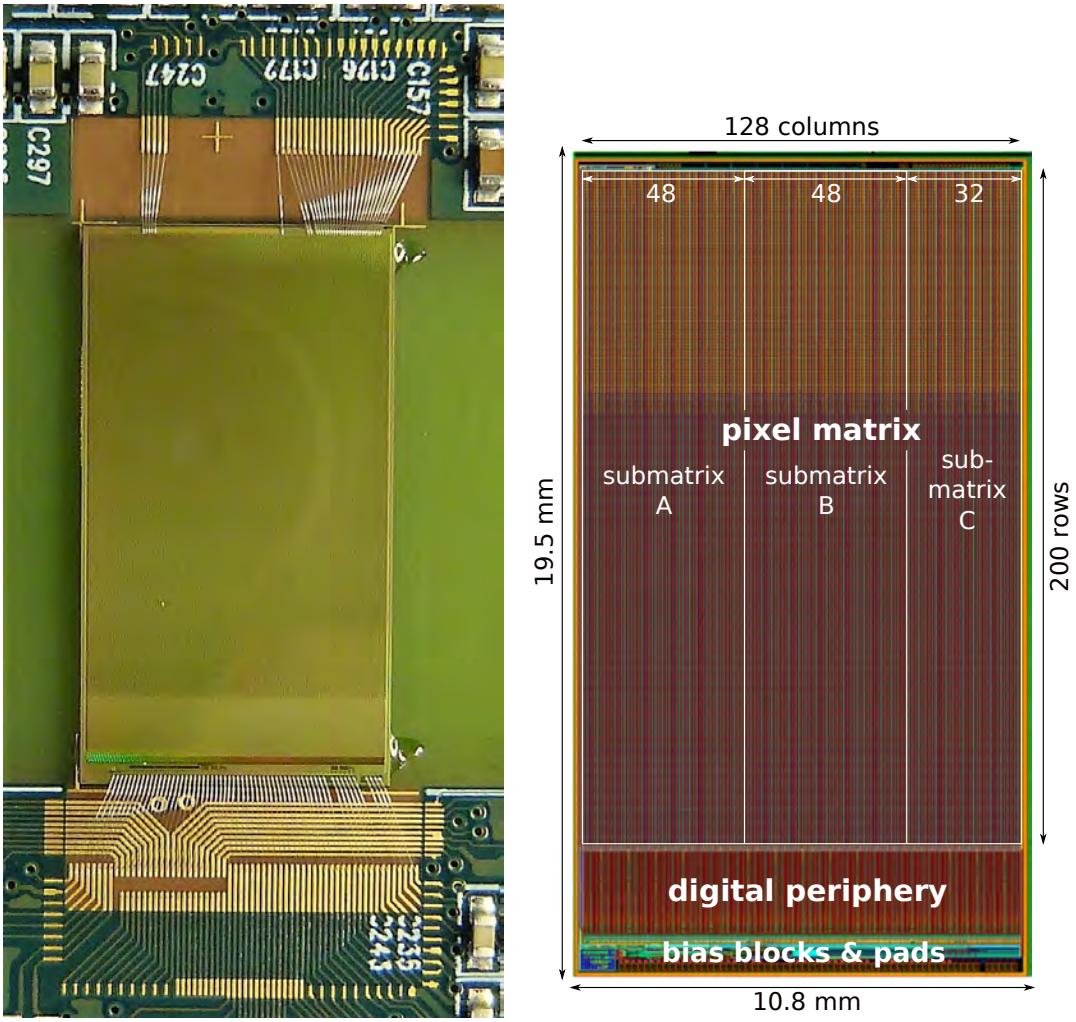


Figure 3.3: UTP cross-section

3.3 Measurement tools

3.3.1 MuPix8

The MuPix8 is the first MuPix prototype that is compatible with SpTAB. Figure 3.3.1 shows a photo of the sensor. All mandatory bond pads are in a single row along the bottom edge of the chip. All obligatory pads have a size of $124 \times 184\,\mu m^2$ with a pitch of 150 µm. Some additional pads are smaller, only suitable for wire-bonding. The MuPix8 sensor needs VDD, VDDA supplied in a range of 1.8 V to 2.0 V, and VSSA at around 1 V. The sensor also needs a differential clock at 125 MHz as well as single-ended configuration signals. MuPix8 provides four differential data outputs. The first three connect to the pixel submatrices A, B,



(a) Picture of a wire-bonded MuPix8

(b) Coarse MuPix8 layout structure

Figure 3.4: MuPix8 HV-MAPS chip

and C, whereas the fourth output is multiplexed, which shows each submatrix. The active area is a 128×200 pixel matrix segmented vertically into the three submatrices. The individual pixels have a size of 81×80 µm^2. Comprehensive descriptions and characterizations of the MuPix8 can be found in [Dit18, Hut18, Ham18].

3.3.2 MuPix8 Insert

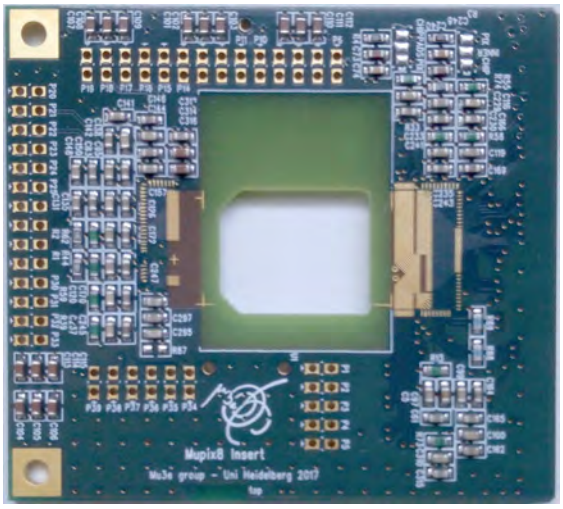


Figure 3.5: MuPix8 Insert PCB

The MuPix8 Insert was designed to connect to the MuPix8 via wire-bonds [Krö17]. The pads for wire bonding are 100 µm wide and 200 µm long with a pitch of 200 µm. The bond pad surface is chemical Ni/Au. The Insert also provides solder pads for SMD filter capacities and resistors for powering being the closest component to the MuPix8 chip. Most signal traces run uninterrupted from the bond pads to an edge connector. Two differential pairs, serving as an external clock and a synchronous reset signal, have termination resistors in parallel. These terminations are left on the board for the commissioning part in section 5.2 but are removed for the characterization part in section 5.1. Notable are the pull-up resistors to VDD for the differential data outputs, which are not present in the MuPix8. Since the wire-bond pad layout does not violate the constraints for an LTU HDI, the Insert can be used to connect an HDI via SpTAB.

3.3.3 MuPix8 Motherboard

Another essential part of the MuPix8 readout is the MuPix8 motherboard [DW18]. It is the counterpart to the Insert. Near the center of the Motherboard, one can slide the Insert into an edge connector socket. The MuPix8 motherboard provides several filter capacities and resistors as well as voltage converters for "internal" powering. "Internal" means, in this case, that converters create the VDD, VDDA, and VSSA voltages on this board from a 5 V source. The converters can also be bypassed for "external" powering, and then, the three voltages need to be set separately and directly from the power supply. Besides several test points, the MuPix8 motherboard also provides SMA connectors for all data outputs. The SMA connectors are usually bypassed using solder-jumpers. When bypassed, the data outputs are sent through a repeater alongside all other data connections over a SCSI cable to a mezzanine board to an FPGA. The combination of Motherboard and Insert helps to reduce systematic effects by having a consistent base. Switching only Inserts reduces systematic variations when changing MuPix sensors.

3.3.4 Backup PCB

As the name implies, the Backup PCB is a backup solution for the Single MuPix8 HDI. In case the MuPix8 is malfunctioning, this PCB can be bonded next to the crossing bars described in section 3.1.4. The layout is straightforward. It connects all three supply voltages with SMA ports separately. The two grounds are also separated. On the back, it provides SMD pads for pull-up resistors for the data outputs, as well as additional high-pass filters for the on-chip voltage controlled oscillator. The high-pass filters redirect the high frequencies away from control voltage for the on-chip clock generator. With solder jumpers, one can choose if the SMD parts are connected to voltage levels at the chip or the ones provided by the SMA connectors. The Backup PCB also provides two differential pairs. The differential reset signal, as well as the clock signal, can be read out this way at the chip-sided end of the HDI via SMA terminals.

3.3.5 Assembly

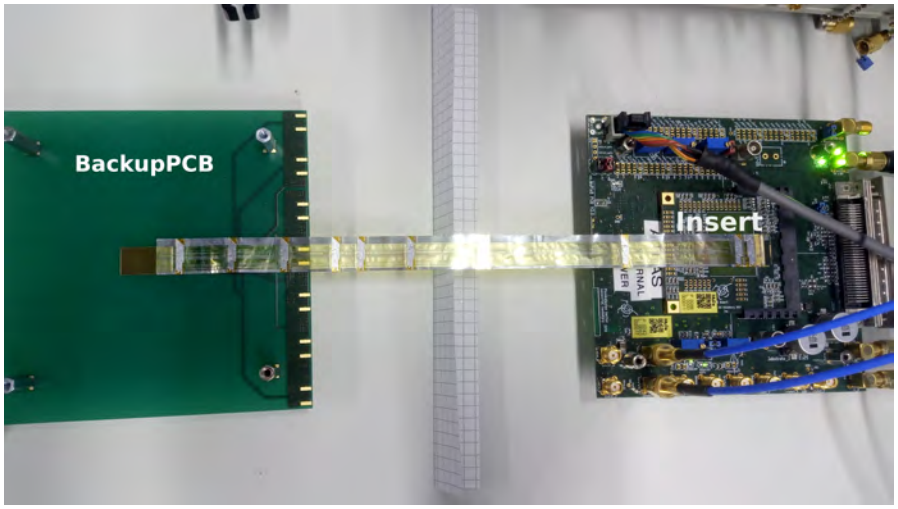


Figure 3.6: Assembly: Backup PCB and MuPix8 are bonded to the left end of the Single MuPix8 HDI. The Insert is bonded to the right end and slid into the Edge-Connector on the MuPix8 Motherboard.

Attaching the Insert to the MuPix8 motherboard via the Edge-Connector is straightforward. The challenging part is bonding the HDI to the Insert and the sensor. At first, the HDI is glued to the MuPix8 to make bonding more manageable. Only the tiniest amount of glue is applied to keep the two surfaces as close together as possible. The application and the subsequent alignment was done by hand under a microscope. Araldite® 2012 epoxy glue [Kra07] was used, which cures within ten minutes. For bonding, a Delvotec 6400 was used with an 1183 04510B TiC Double Cross Groove bonding tool. Only one bond was done at the time to ensure that the tool always hits the center of the trace. The process is for the Insert is analog as for the MuPix8. The results can be seen in figure 3.8

Insert inventory number	MuPix8 number from Wafer 12 80 Ω cm
84-3-11	26
84-3-27	27
84-3-28	28
84-4-23	32
84-4-24	25

Table 3.1: Insert - MuPix8 assignment

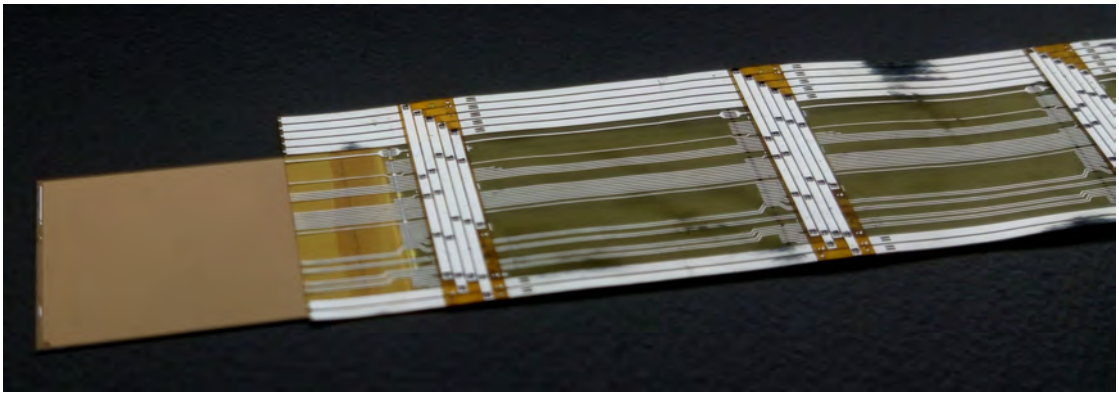
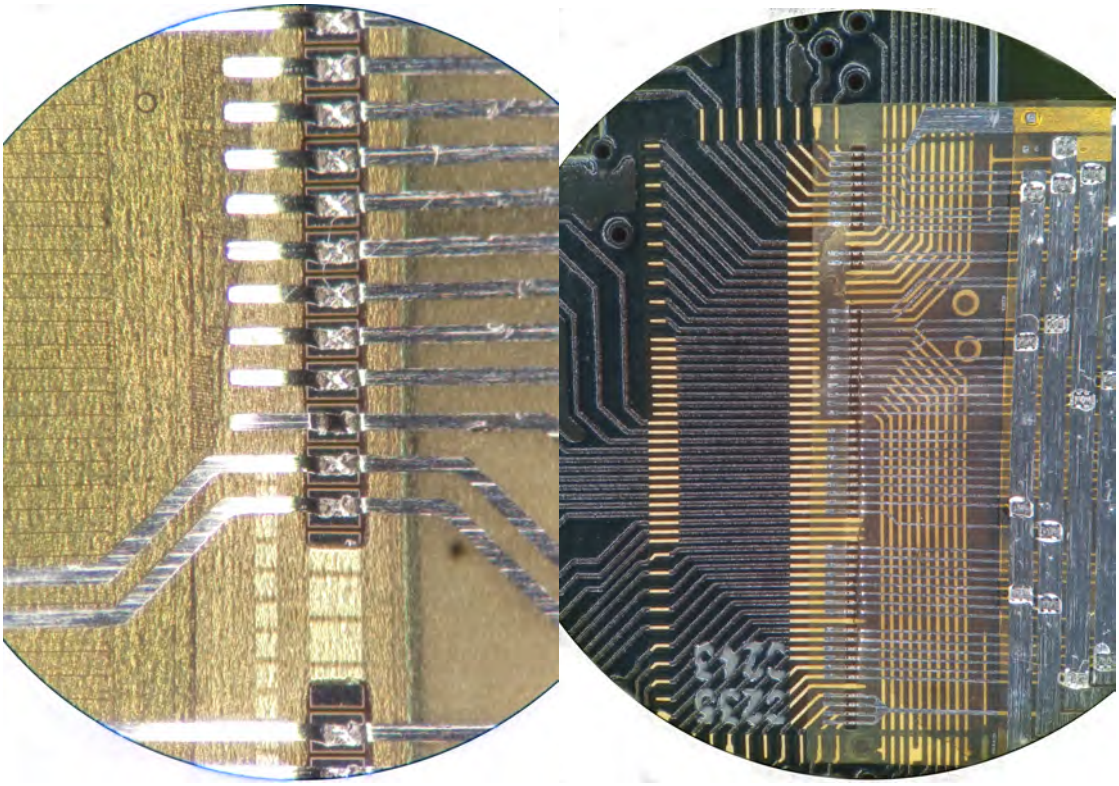


Figure 3.7: HDI glued and bonded to MuPix8



(a) HDI bonded to the MuPix8 chip.

(b) HDI bonded to the Insert.

Figure 3.8: Single MuPix8 HDI bonded via SpTAB

3.3.6 Edge-Connector to SMA breadboard

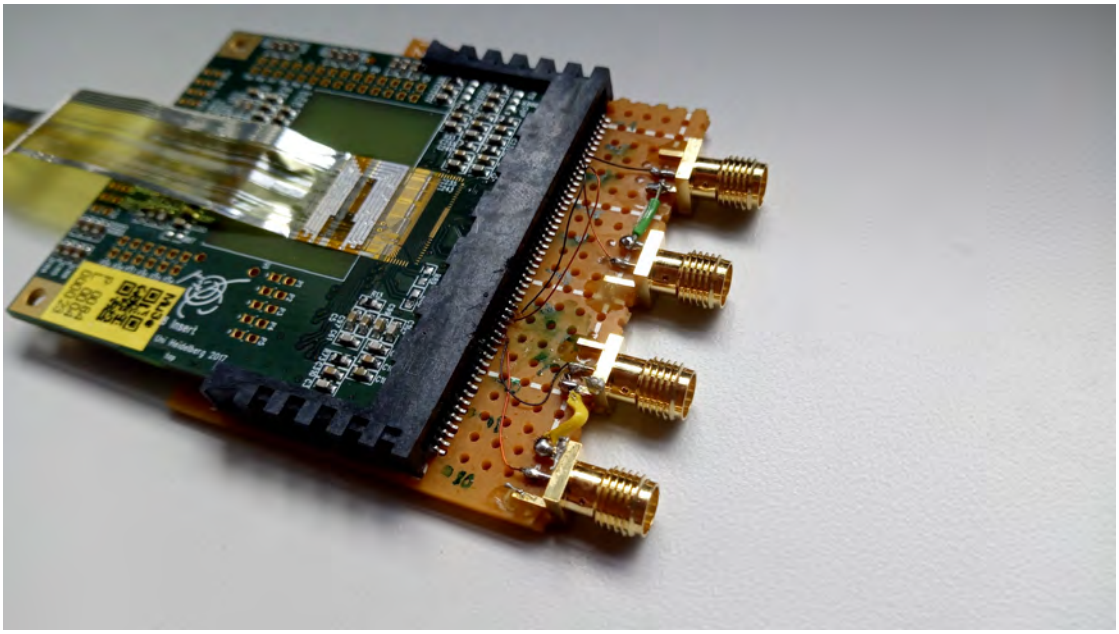


Figure 3.9: MuPix8 Insert connected to the Edge-Connector to SMA breadboard

For characterization purposes, a connector at each end of the differential pairs is required. The Single MuPix8 HDI has four differential pairs. The two differential data outputs can only be terminated to an SMA or SCSI port on the MuPix8 Motherboard. The two differential inputs can only be accessed via the Backup PCB's SMA ports. For this reason, a dummy edge connector and four SMA ports were secured on a breadboard. The SMA signal pins were placed as close as possible to input pins of the edge connector. The gap was bridged with twisted-pair cables described in section 3.2.

Chapter 4

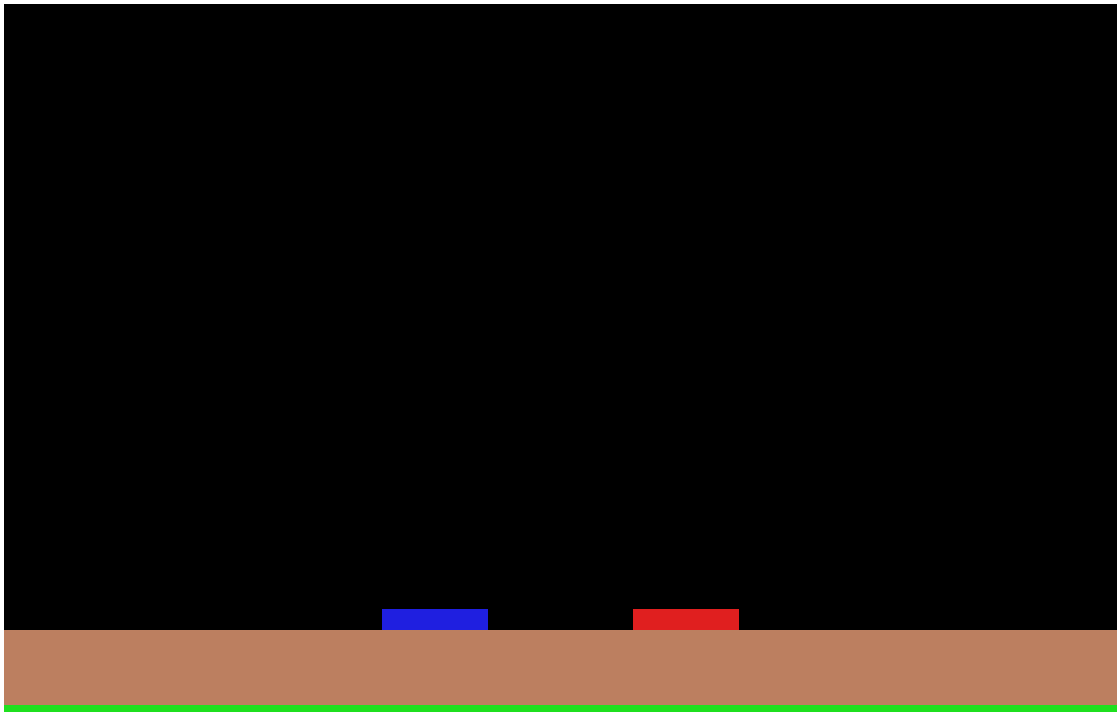
Impedance Simulations

4.1 Simulation software atlc2

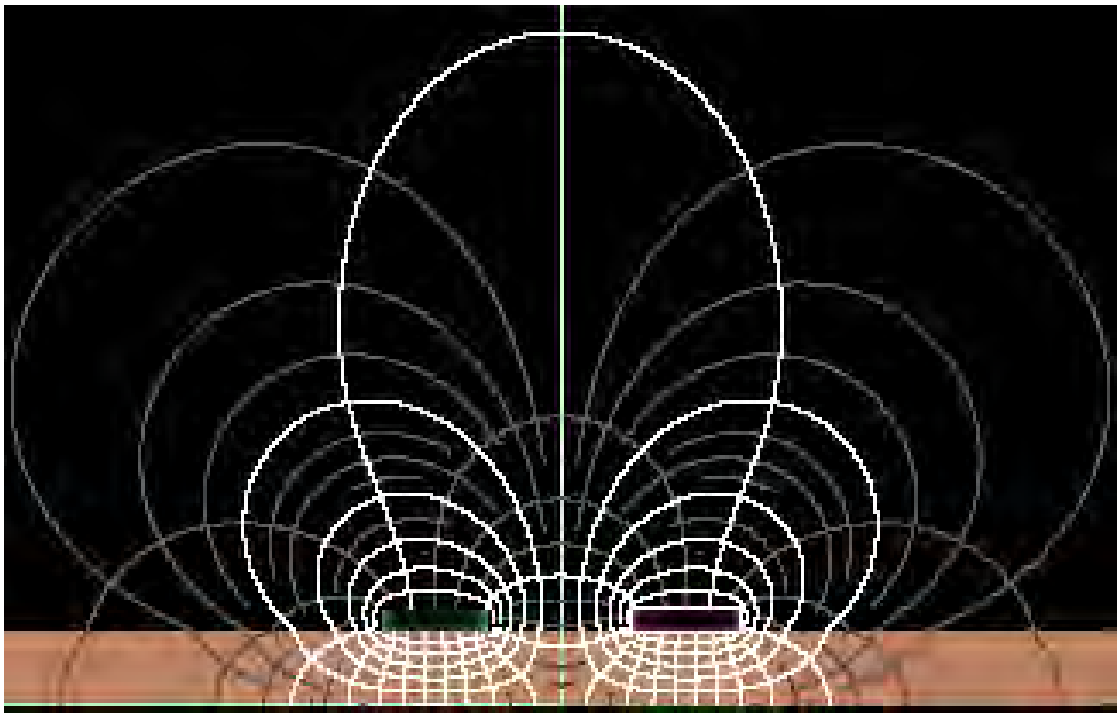
Atlc2 is a free-ware 2D impedance simulation tool and is the successor to the "arbitrary transmission line calculator" (atlc)[DDK19a, DDK19b]. Atlc2 uses a finite element method on Faraday's law to determine the current distributions in the conductors. It handles every possible cross-section that can be drawn or approximated in a bitmap pixel grid picture. Based on the distribution of conductive and dielectric material, atlc2 calculates the electric and magnetic fields. It is possible to create a cross-section with up to three different signals, $\pm \sin \omega\, t$ denoted as ± 1 and 0 as ground. Atlc2 comes with a pre-defined color mapping, containing various metals and dielectrics. The software's author claims an accuracy of $99 - 95\%$, dependant on the complexity of the cross-section [DDK19b]. The statement of a 2D simulation is not as significant as the statement of a 3D simulation, but it gives a clue about the behavior of a cross-section. Besides, many 3D tools only allow calculation for parametrized cross-sections, but not for arbitrary cross-sections.

4.2 Simulation results

Since atlc2 takes bitmap pictures as cross-section information, several cross-sections with variations in the trace width, the gap, and the dielectric height were drawn. Each bitmap is only 800×400 pixels large to reduce simulation time. One pixel resembles the scale of $2\,\mu m$. An example of a bitmap is shown in figure 4.1(a). The metal areas are filled with shades of red ($+\sin \omega\, t$), blue ($-\sin \omega\, t$), and green (ground) for aluminum, according to atlc2's color pallet. The brown coloring indicates a dielectric layer, resembling epoxy, being the closest in the atlc2 color pallet to polyimide and Araldite. Despite the description in the atlc2 manual[DDK19b], a 2-pixel thick ground box is drawn around the differential pair to solve unphysical



(a) Simulation input bitmap with red and blue as the differential pair. Green is ground, brown is the dielectric, and black vacuum.



(b) Simulation output bitmap with current density as well as E- and B-field lines

Figure 4.1: Atlc2 simulation example bitmaps; These are cropped, the full size pictures are in the appendix B.1(a)

asymmetries in the field lines. The simulated field lines are shown in figure 4.1(b). Besides, it shows the current distribution in the microstrip lines, which is most dominant close to the surface. Except for the outermost 2 pixels in the microstrips, there is no current flow due to the skin effect 2.1.6. Hence, the microstrips in figure 4.1(b) appear hollow. Atlc2 also provides a result for the differential impedance. The entire sample of simulated data is shown in the 3D scatter plot in figure 4.2. For all simulations, the frequency was set to 625 MHz, which is the minimal frequency required to produce a 1.25 Gb/s data stream. The trace width and gap step sizes, as well as their ranges, were chosen according to the LTU constraints and the application. This gives a first idea of the achievable impedance range. In figure 4.3 subset is compared to the analytic model from section 2.3. Both

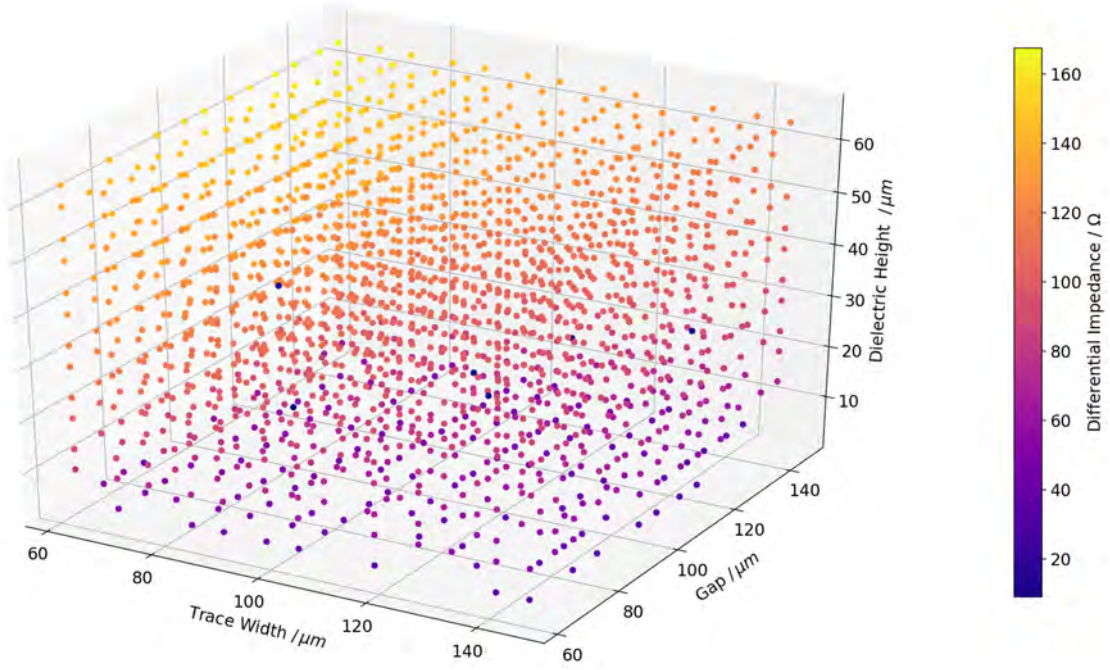


Figure 4.2: Complete simulation sample

approaches show a similar dependence on the dielectric height. For larger gaps and widths, the behavior is more linear than for smaller ones. In comparison, the simulation results in a higher impedance than the analytic model for the same set of parameters. The systematic discrepancy is in the order of 30 Ω, which is significant regarding the accuracy given by the authors of the model and simulation. When plotting the differential impedance against the trace width and the gap, this difference is also prominent. In figure 4.4(a) and figure 4.4(b) this difference is compared to three measured data points (in pink), which were taken in 2016

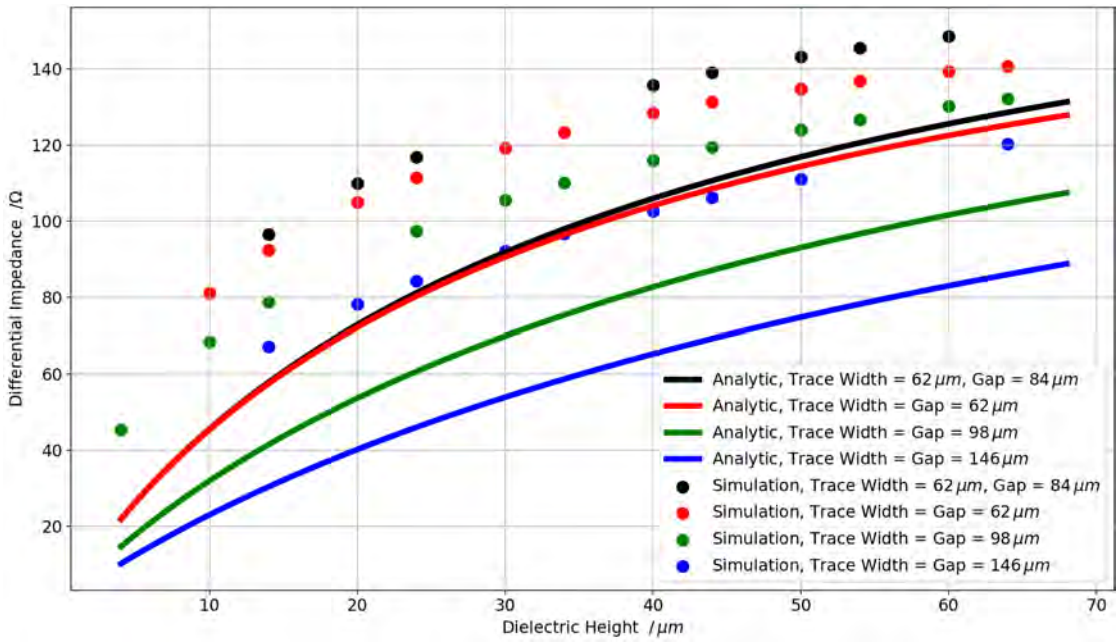
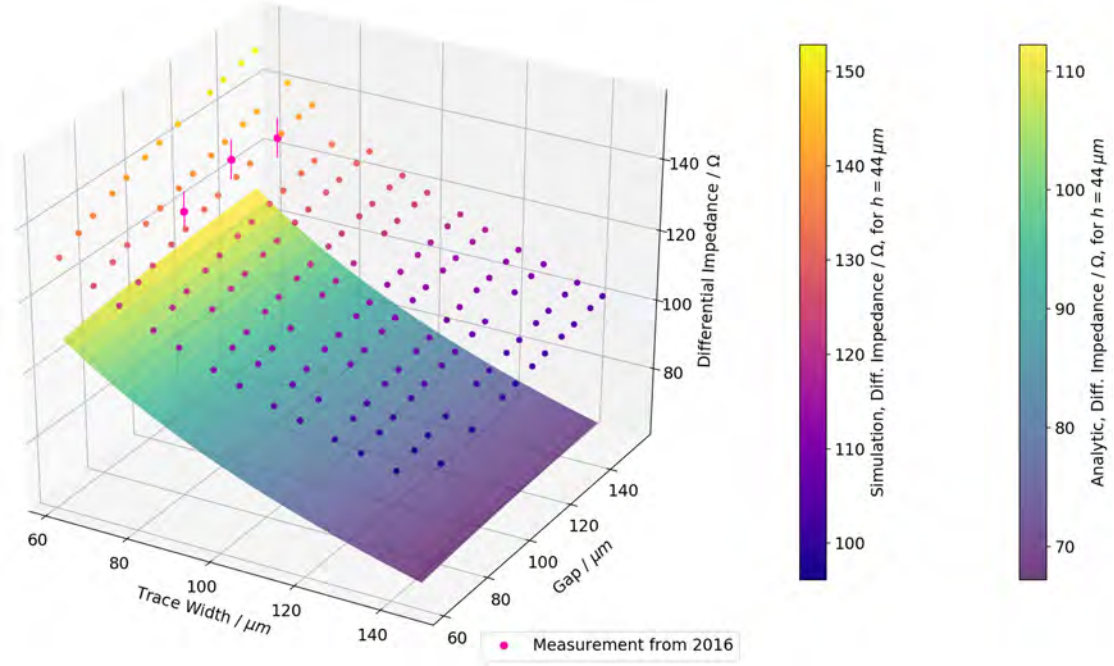
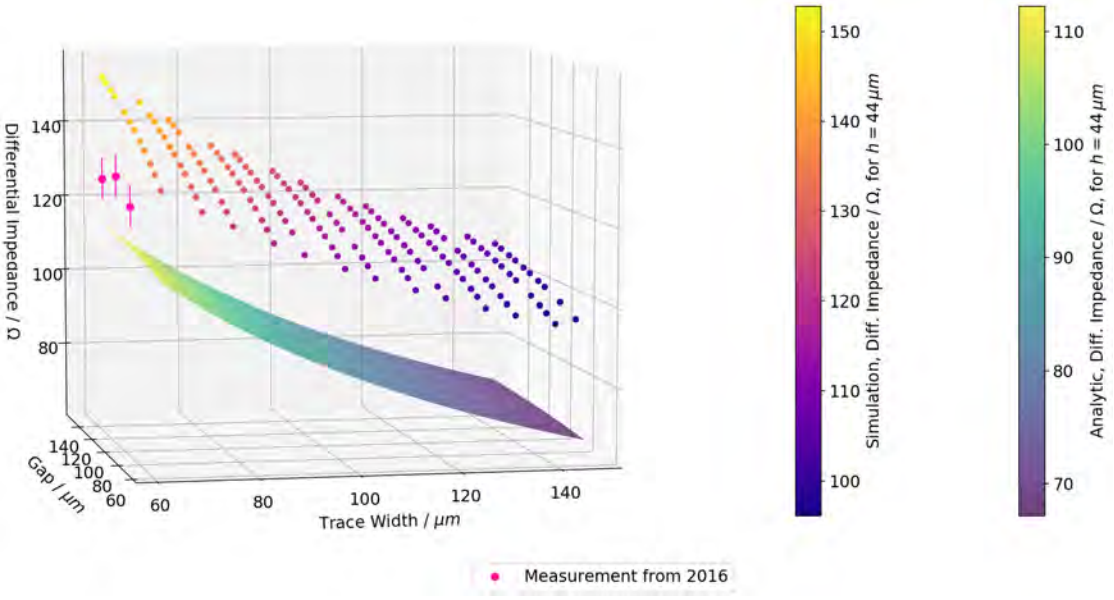


Figure 4.3: atlc2 simulation compared to analytic model as functions of the dielectric height

from a similar HDI with the same layer stack [Noe16]. The measurements suggest that the simulation might overestimate, and the analytic model might underestimate the impedance. A test series of differential pairs with different trace widths would clarify this. The tolerances of the manufacturing process is also unknown and need to be determined for this test.



(a)



(b)

Figure 4.4: Atlc2 simulation compared to the analytic model (section 2.3) and measurements from 2016 [Noe16] at a dielectric height of 44 µm

Chapter 5

Measurements

5.1 Electrical characterization

5.1.1 Microstrips

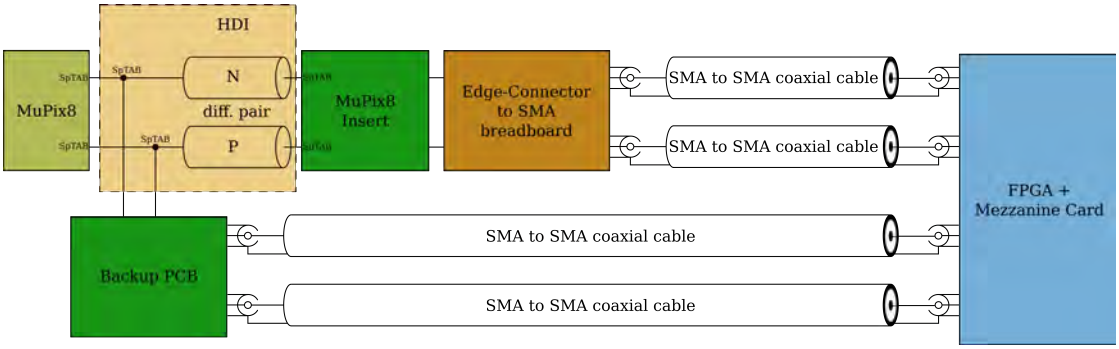


Figure 5.1: Microstrip BERT setup sketch

For the characterization of the differential pairs on the HDI, the assembly of MuPix8, HDI, and Insert (inventory number 84-4-23) is used. To access the traces via SMA ports, the breadboard (section 3.3.6) is utilized, and the Backup PCB (section 3.3.4) is bonded to the HDI. The default termination resistors for the differential input signals are removed from the Insert, realizing a point connection between the HDI and the Edge-Connector board.
For some industry standards, it is sufficient to transfer random data and count the bits recognized by the receiver, which is called the Bit Error Rate Test (BERT). For this purpose, a 1.25 Gb/s pseudo-random binary sequence (PBRS7) was produced by a StratixV field-programmable gate array (FPGA) development board. The

FPGA has differential receivers and was programmed to compare the incoming with the outgoing bits. An HSMC to SMA break-out-board [ter19] is connected to the FPGA development board to connect to the FPGA. The output terminals are connected via SMA coaxial cables to the SMA connectors on the Backup PCB, and the input terminals are connected to the Edge-Connector to SMA breadboard. A sketch of the entire signal chain is shown in figure 5.1. The MuPix8 is still bonded to the HDI but is not powered, making it a high-impedance barrier. The short distance, between the Backup PCB bonds and the sensor, is expected to cause no significant reflections.
The result of the BERT shows that out of $N = 1.509 \times 10^{15}$ bit, not a single error occurred. Assuming a Poisson distribution, the BER upper limit given a confidence level CL is calculated by:

$$BER < \frac{-\ln(1 - CL)}{N} \tag{5.1}$$

$$BER < 1.985 \times 10^{-15} \ @ \ 95\,\% \ CL \tag{5.2}$$

Eye diagrams

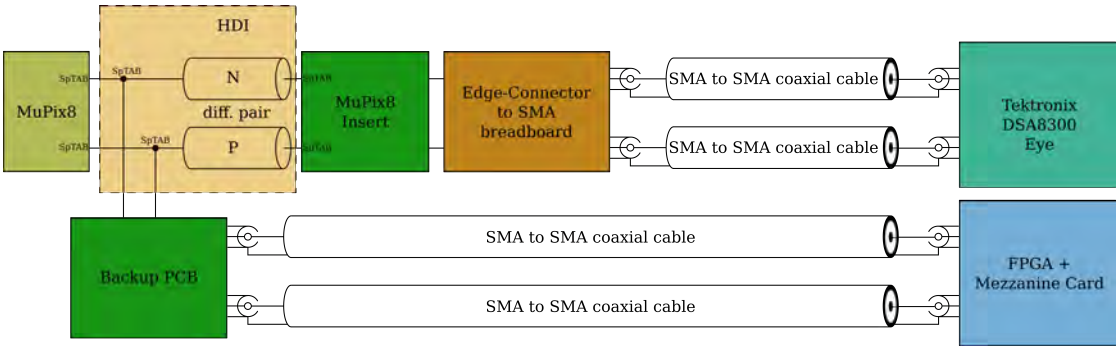


Figure 5.2: Microstrip eye diagram setup sketch

Using eye diagrams, the quality of digital data streams in the time domain is determined. Eye diagrams are a superimposition of all bit patterns occurring in the data stream aligned to a rising or falling edge. The connotation to the eye comes from the shape of the diagram. An excellent digital signal has a wide-open eye. That means that the eye height, which is the height of the void space in the center of the eye, is close to the signal amplitude, and the eye width, which is the width of the void space, is nearly the bit length. The eye height can be degraded by noise, whereas the eye width can be degraded by jitter.
The measurement setup (figure 5.2) is the same as for the BERT, but instead of

going with the coaxial SMA cables back to the FPGA, the signal is fed into the Tektronix DSA8300 Digital Sampling Oscilloscope [Tek16]. The measurement can be seen in figure 5.3.

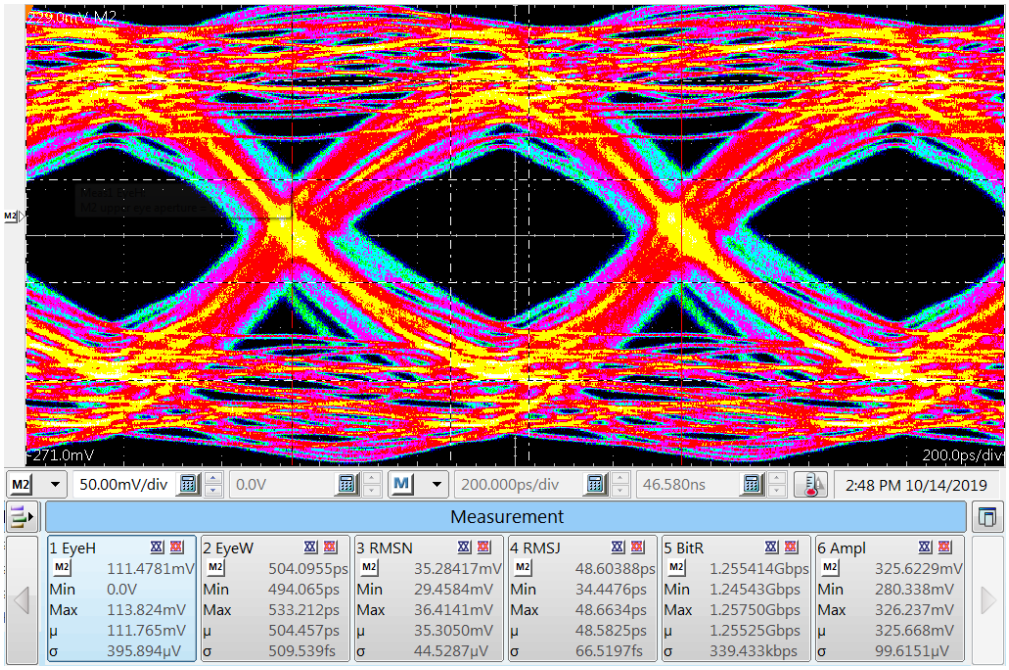


Figure 5.3: 84-4-23 eye diagram; EyeH = eye height, EyeW = eye width, RMSN = noise standard deviation, RMSJ = jitter standard deviation, BitR = measured bit rate, Ampl = amplitude.

As a reference, the SMA coaxial cables were directly connected with an SMA female to SMA female connector. The reference eye diagram is shown in figure 5.4. Compared to the reference the measured eye height shrinks from 211 mV to 112 mV. According to equation 2.7 the attenuation is

$$a_{HDI} = -20 \log_{10} \left(\frac{112\,\mathrm{mV}}{211\,\mathrm{mV}} \right) = 5.5\,\mathrm{dB}. \tag{5.3}$$

The cause for this reduction does not originate from increased noise but from a decreased slew rate. On the one hand, the signal is not fast enough to switch within one bit between the two digital voltage levels. On the other hand, for bit sequences with, for example, five equal bits in a row, the signal has enough time to reach the intended level. This creates a range of amplitudes in the outgoing signal, which forms bands below and above the eyes in the eye diagram of figure 5.3. Besides, the jitter on a single bit pattern is not large. However, Fthe combination of different amplitudes and a low slew rate degrades the jitter as well.

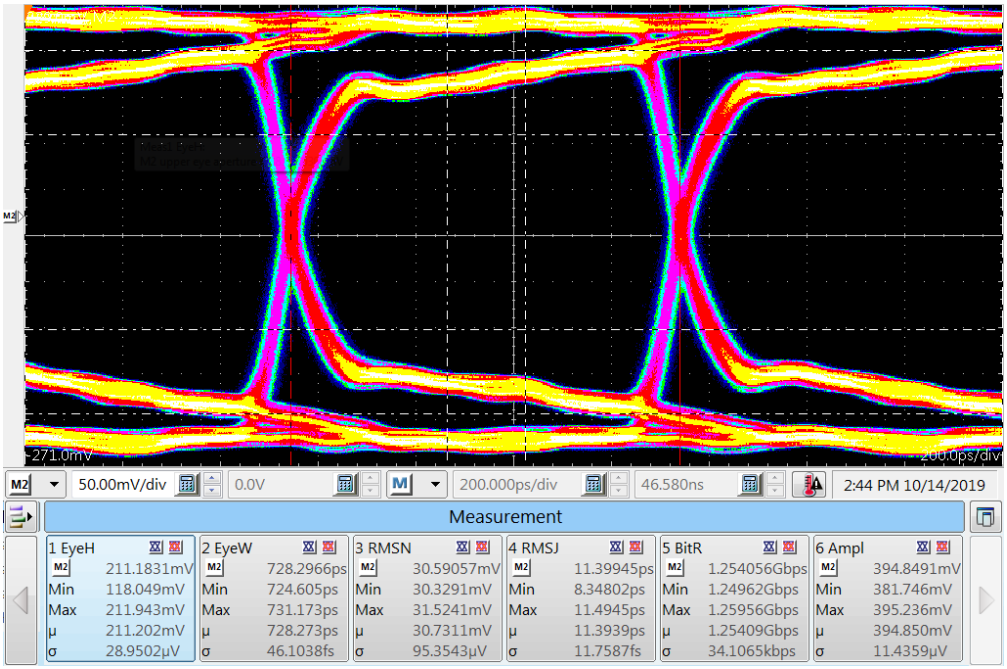


Figure 5.4: StratixV reference eye diagram; EyeH = eye height, EyeW = eye width, RMSN = noise standard deviation, RMSJ = jitter standard deviation, BitR = measured bit rate, Ampl = amplitude.

Time Domain Reflectometry

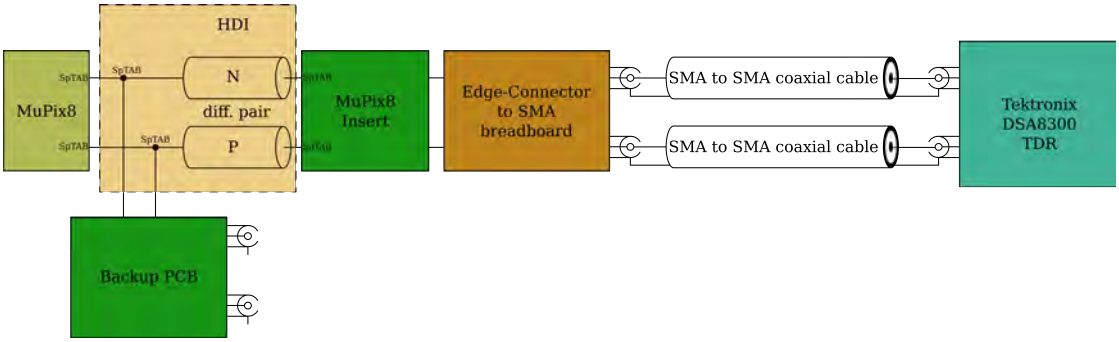


Figure 5.5: Microstrip TDR setup sketch

The Time Domain Reflectometry (TDR) is a method to measure the impedance of a trace nearly independent from the other transmission lines and connectors between the trace and the measurement oscilloscope. For the measurement, the TDR

module of the Tektronix DSA8300 Digital Sampling Oscilloscope was used. The module connects to only one end of the whole transmission system, while the other end is left unterminated (shown in figure 5.5). In this case, it was connected to the Edge-Connector to SMA breadboard. The module sends a short pulse through the transmission system. According to equation 2.30, each point of impedance change is a point of reflection. The module measures the reflection amplitudes at the same port and compares it to the initial amplitude, which gives the reflection coefficient. Knowing the termination impedance of its module, the Oscilloscope can solve the equation 2.30 for the impedance. In the end, the Oscilloscope plots the impedance against the propagation time of the reflection, which is twice the time the signal needs to reach the point of reflection. Figure 5.6 shows the resulting plot for the differential pair.

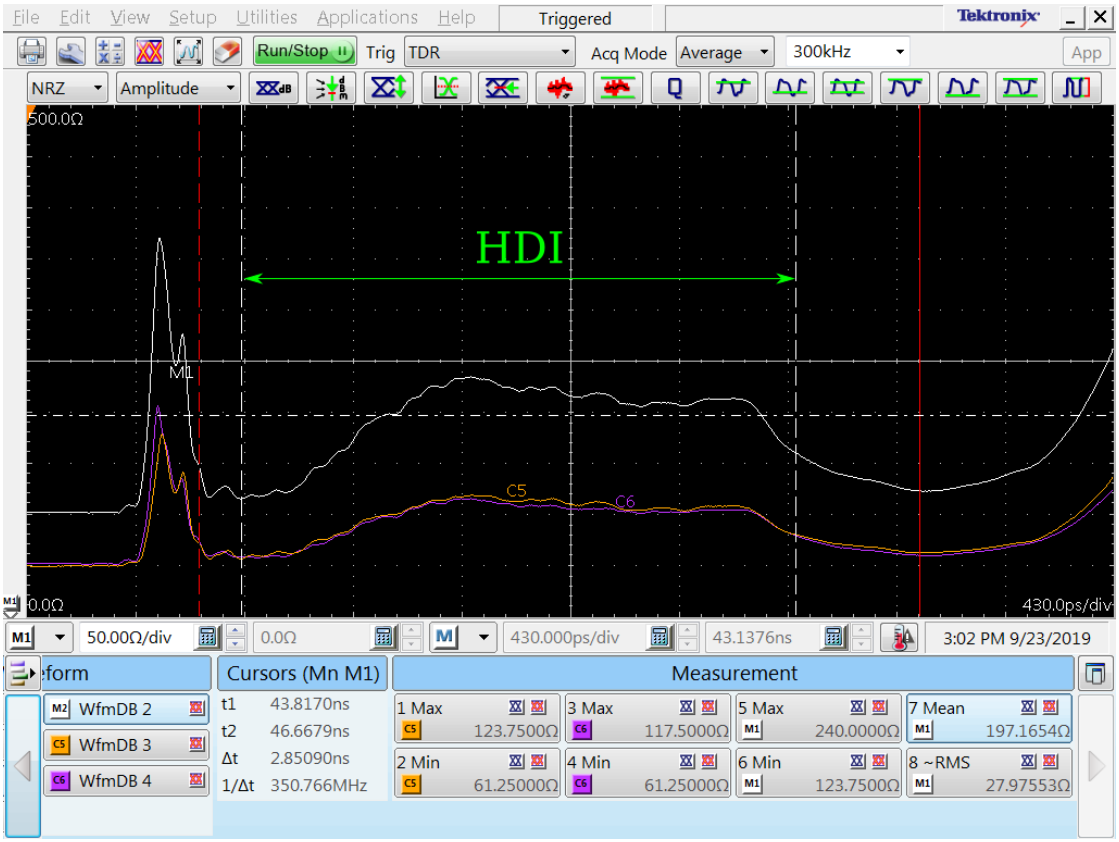


Figure 5.6: 84-4-23 TDR measurement from Insert to BackupPCB

The plot shows three graphs. The purple and the orange ones are the single trace impedances of the two traces, and the white graph is the differential

impedance of the pair. The abscissa can be divided into three time-domains. The first includes the components between the TDR module and the HDI, the second is the impedance curve of the HDI, and the last is just the Backup PCB, and the open trace ends. Dominant in the first section is an impedance spike, which is typical for an SMA connector being connected to a non-coaxial transmission line. The third domain shows the traces being just above 100 Ω differentially on the Backup PCB and the tail diverging towards infinity for the impedance of the open end. The central domain shows a rising edge and a plateau. The rising part is stretched in time by the fact that the HDI is glued to the Insert. Hence, the trace is in a different dielectric environment, compared to the not glued part. The signal propagates slower in the glued part and thus takes more time to pass it. The measurements provided by the Oscilloscope in figure 5.6 show a maximum differential impedance of 240 Ω. It should be noted that the measurements are taken from only the HDI domain. The mean value, including the ramp at the beginning of the HDI, is at 197 Ω. This impedance is well above the LVDS standard. As explained in section 3.1.4, the reference layer underneath the microstrips is missing intentionally. An atlc2 simulation without reference layer gives a result of 218 Ω. Therefore, such a high impedance is expected if the ground plane is missing. This impedance mismatch causes reflections in the signal as well as AC resistance, leading to the low slew rate in the eye diagram of figure 5.3.

5.1.2 Unshielded Twisted Pair

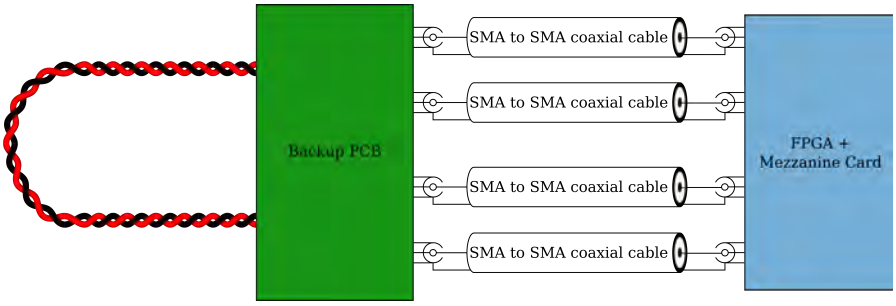


Figure 5.7: Unshielded twisted pair BERT setup sketch

The measurements done for the characterization of the HDI are repeated for the unshielded twisted pairs. Initially, the measurements were started with the copper core of the SMA connector soldered directly to the signal pins of SMA ports, shown in figure 5.8. The BERT was not able to detect any bits. The eyes are

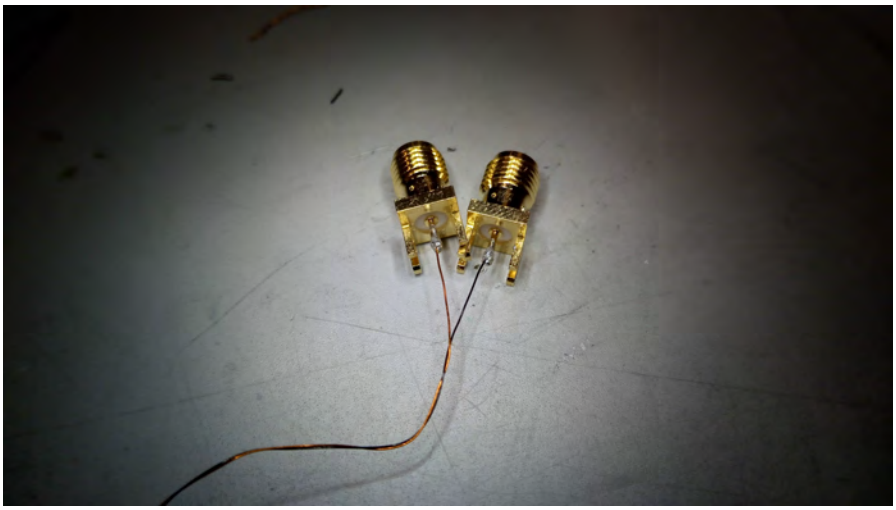


Figure 5.8: UTP soldered to SMA pins

completely closed, which explains the failed BERT. It was assumed that the large splice at the end of the cables causes signal degradation. As a workaround, the twisted pair cables were surface-mounted to the differential traces of the Backup PCB. The solder mask above the traces was scraped away to expose the copper traces for soldering. The remaining parts between the bond pad and the solder point were cut off, to prevent reflections. The surface-mount can be seen in figure 5.9. Performing the BERT with this setup resulted in $BE = 9$ faulty out of

$N = 8.324 \times 10^{14}$ tested bits.

$$BE = 9 \tag{5.4}$$

$$N = 8.324 \times 10^{14} \tag{5.5}$$

$$BER = \frac{BE}{N} = 1.081 \times 10^{-14} \tag{5.6}$$

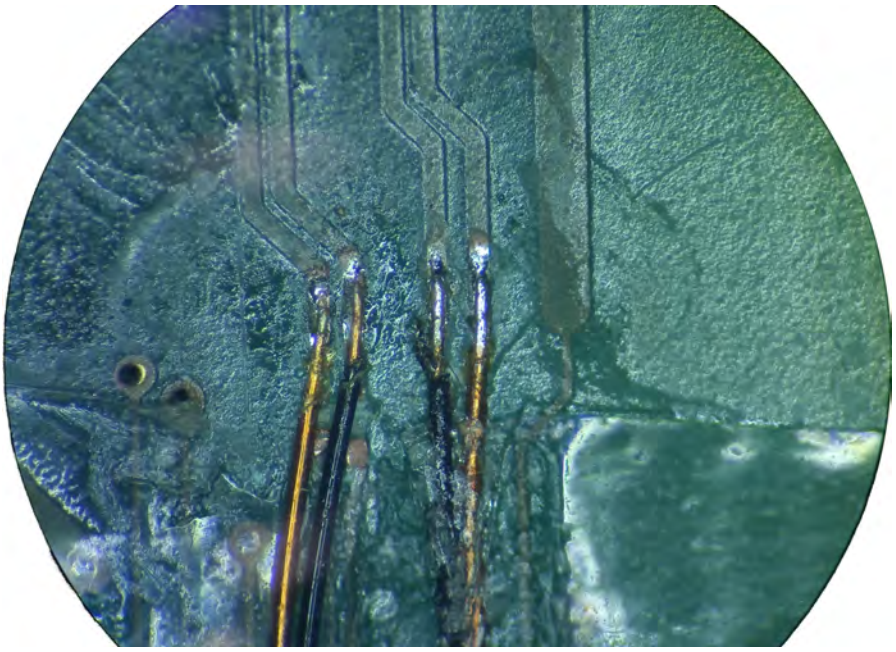


Figure 5.9: UTP soldered to the Backup PCB

Eye diagrams

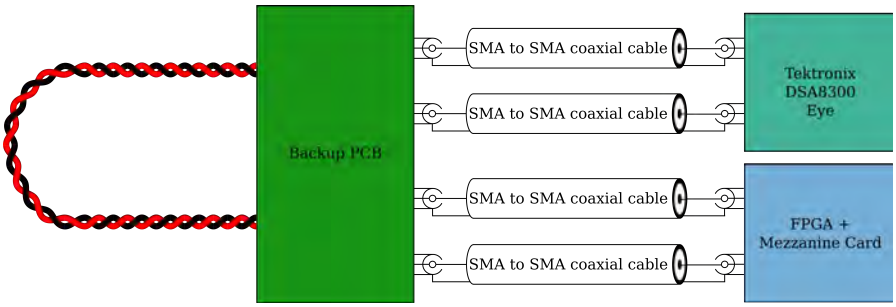
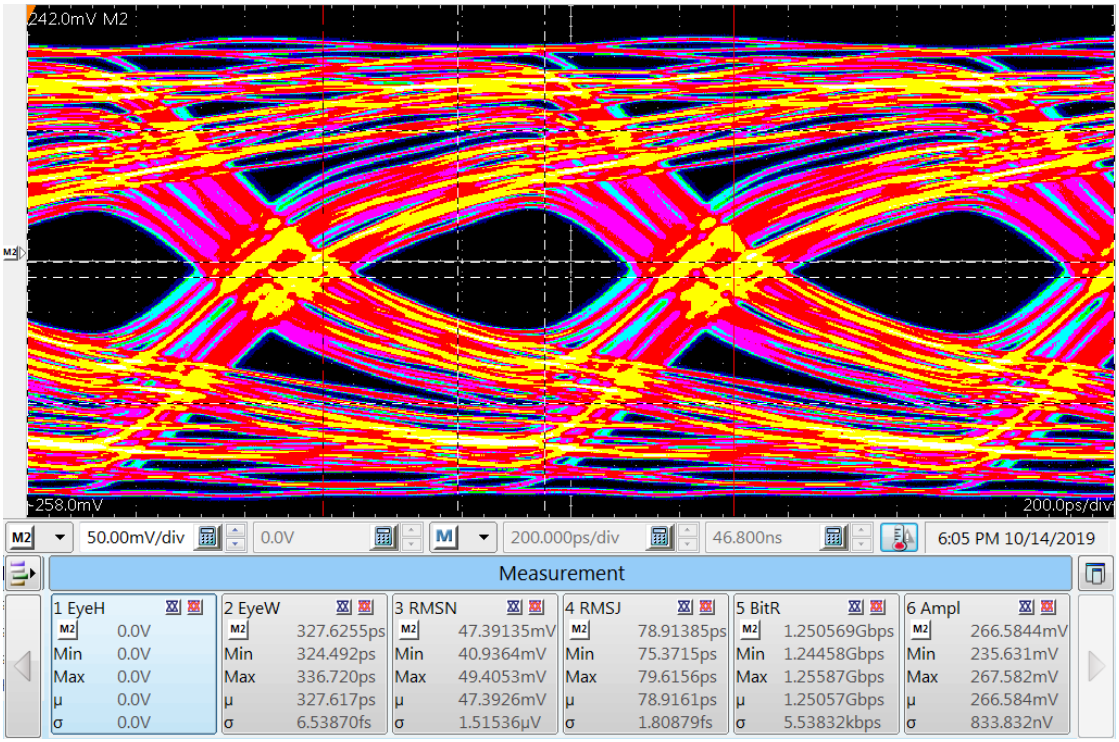


Figure 5.10: Unshielded twisted pair eye diagram setup sketch

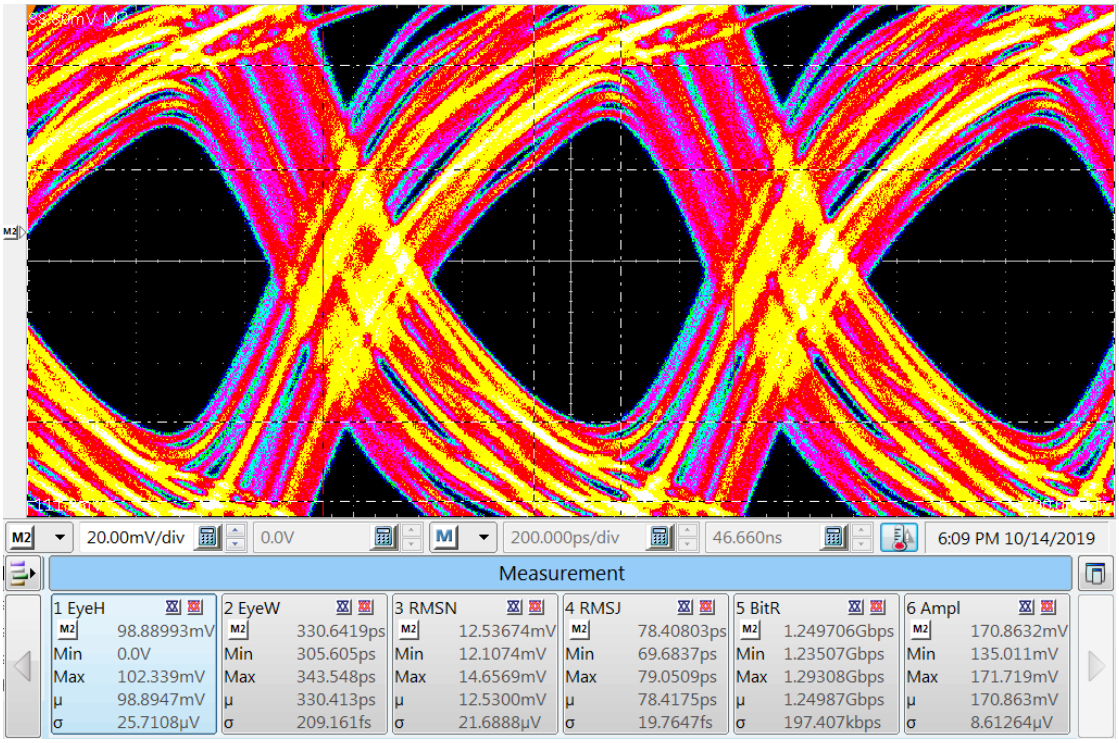
Repeating the eye diagram measurement with the UTP bonded to the Backup PCB results in the diagram shown in figure 5.11. Due to the even lower slew rate compared to the HDI, the wave-forms created by the different bit patterns are clearly separated, leading to more jitter and a smaller eye height of 99 mV. According to equation 2.7 the attenuation is

$$a_{UTP} = -20 \log_{10} \left(\frac{99\,\mathrm{mV}}{211\,\mathrm{mV}} \right) = 6.6\,\mathrm{dB}. \tag{5.7}$$

It is hard to judge the performance of the cables with this clearly improvised setup. The more elaborate CMS characterization [PSI16] of this UTP shows that 160 Mb/s can be transmitted, and also eye diagram measurements were performed. Their eye diagrams are much more open than the ones in figure 5.11, but this is at an eighth of the bit rate. Focusing on only the first eighth of the CMS eye diagram, it suggests that their eye diagram would look similar to figure 5.11 if they would have tested the cable at 1.25 Gb/s. However, it is not clear how much the signal driver influences the CMS eye diagram at high frequencies.



(a) UTP eye diagram



(b) UTP eye with zoomed ordinate for eye height measurement.

Figure 5.11: UTP eye diagram; EyeH = eye height, EyeW = eye width, RMSN = noise standard deviation, RMSJ = jitter standard deviation, BitR = measured bit rate, Ampl = amplitude.

Time Domain Reflectometry

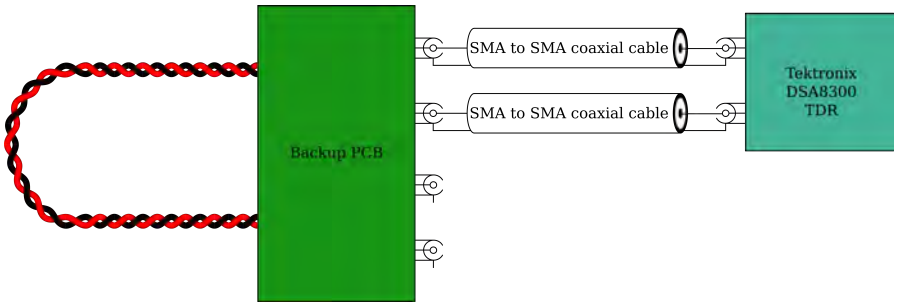


Figure 5.12: Unshielded twisted pair TDR setup sketch

In contrast to the eye diagram, the TDR measurement shown in figure 5.13 looks much more promising. The time-domain that can be assigned to the UTP shows an impedance between 90 Ω and 113 Ω with a mean of 96 Ω, which is close to the LVDS standard. The spikes causing the impedance maximum are defects in the cable. At the points where the impedance spikes occur, the cables are separated for one twist, causing an air-gap. The TDR graph in figure 5.14, of another UTP cable soldered directly to SMA sense pins, does not show these defects. Both TDR measurements show a rise in the impedance over the length of the cable. This is expected to be an effect of the measurement module, not taking the ohmic resistance into account. Due to ohmic resistance, the reflected signal loses strength on its way back to the module. It is peculiar that the impedance is lower than the 100 Ω termination, and the eye diagram still has such a flat slope. A lower impedance on the transmission line compared to the termination usually causes a phase shift in the reflected signal of π (section 2.1.4). The interference with these reflections usually causes ringing at the beginning of the bit. Probably the slew rate is dominated at this point by a lack of high frequencies shaping the edges.

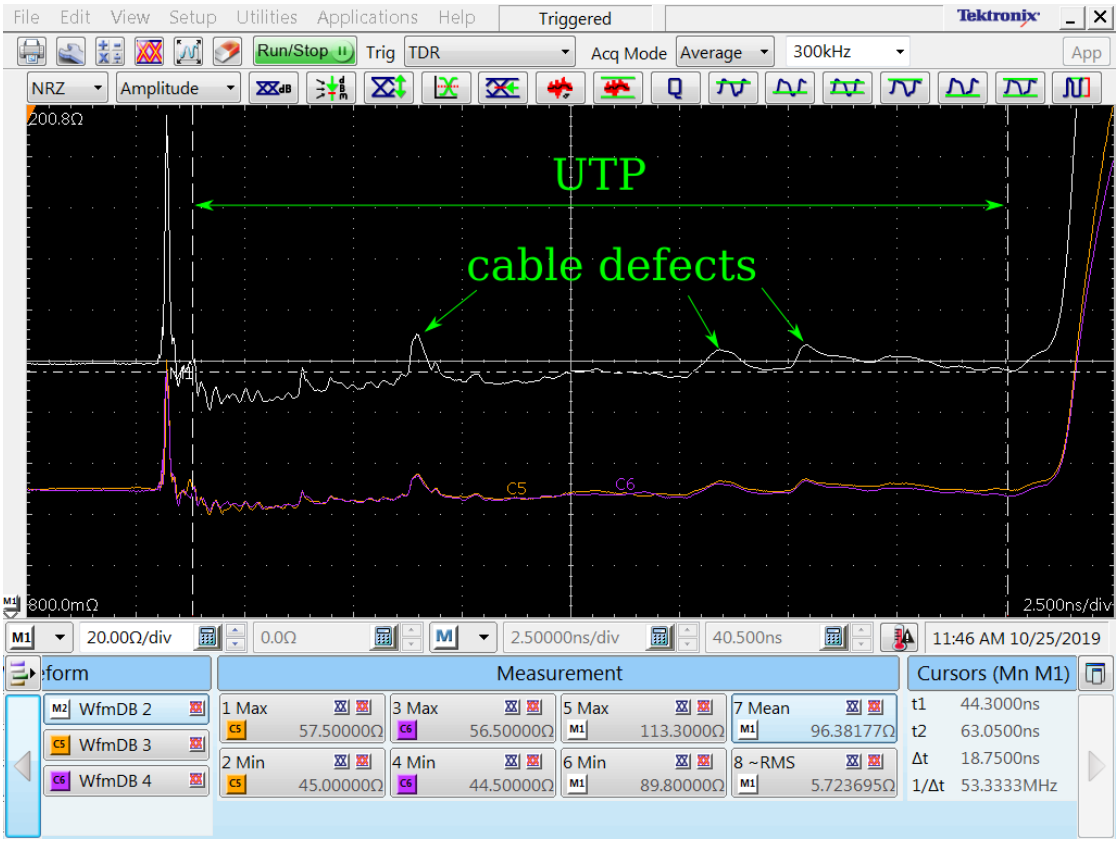


Figure 5.13: TDR of 2 m UTP soldered to the Backup PCB

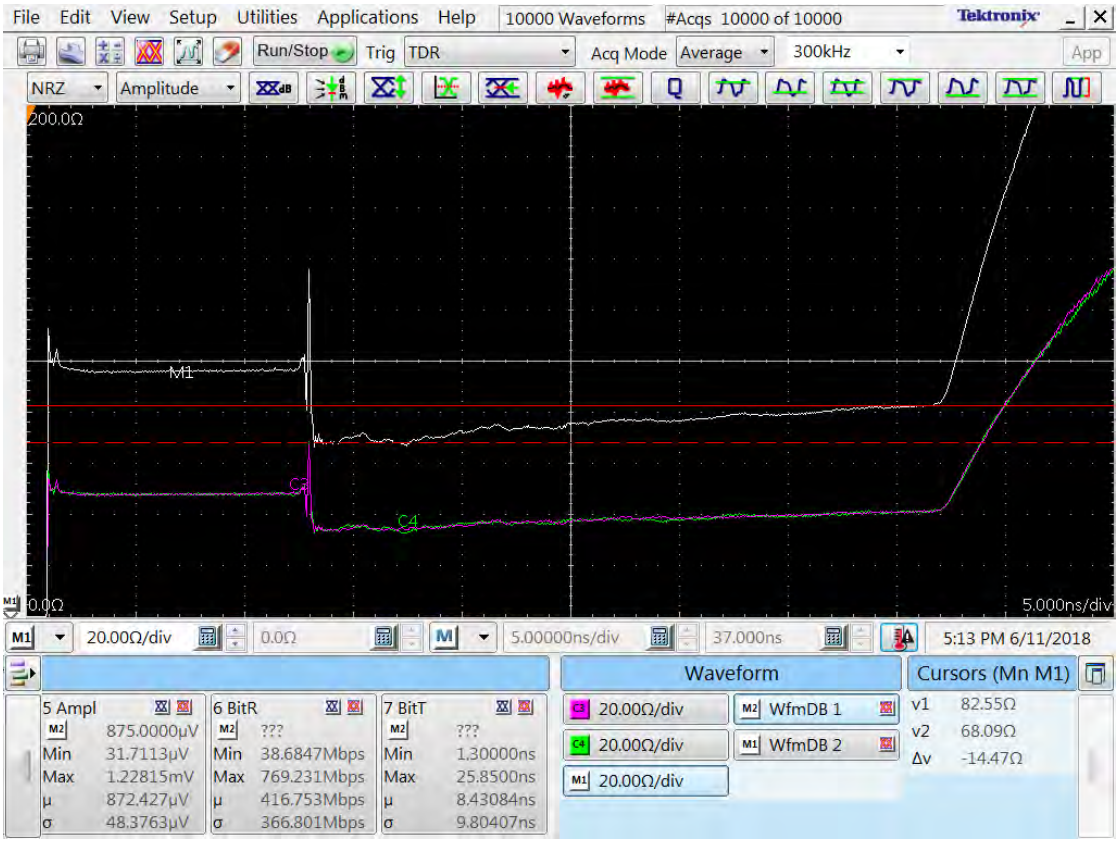


Figure 5.14: TDR of 3 m UTP soldered directly to SMA sense pins

5.2 Commissioning MuPix8 with HDI

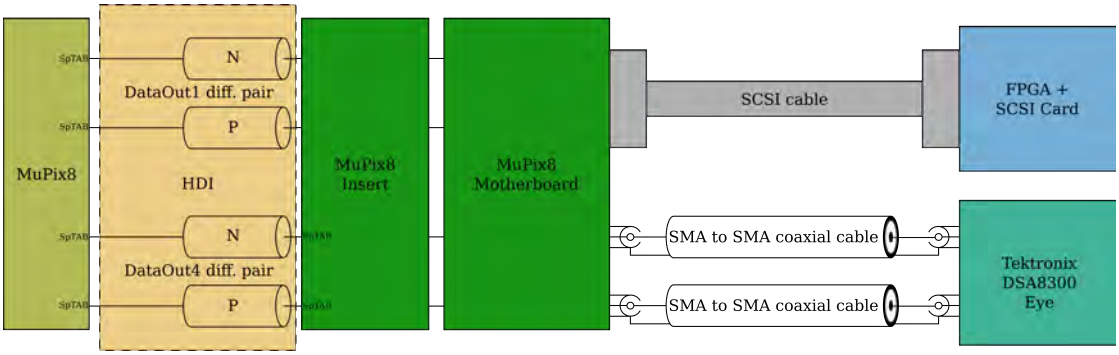


Figure 5.15: MuPix8 + HDI + Insert commissioning setup sketch

The ultimate test for the HDI is the operation in combination with the MuPix8 sensor. For this setup, the assembly with the 84-3-11 Insert was used. At first, the MuPix8 was operated without the Backup PCB. After tuning the Digital Analog Converter (DAC) values to configure the MuPix8, it was possible to run at 625 Mb/s readout speed. Since the readout links behave similar to DAC value changes [Dit18], the first data output was routed to the SCSI cable while the fourth link was bypassed to use the SMA ports. The SMA port was connected with coaxial cables to the Tektronix DSA8300 Digital Sampling Oscilloscope, to acquire the eye diagrams at the same time. The strategy for DAC tuning is to alter the values systematically, trying to improve the quality of the eye diagram. After that, the DAC values are fine-tuned to minimize the bit error rate detected by the FPGA on the other end of the SCSI cable. An attempt was made to bond the power traces to the Backup PCB to get a better handle on the power input. Unfortunately, only the contact with VDD and ground was successful. The high pass filters were also connected to stabilize the voltage controlled oscillator in the chip. With this setup, it was possible to measure the voltage drop over the HDI. The input voltages were raised by 100 mV to compensate for it. With the high pass filters to ground, the voltage controlled oscillator was stabilized, and it was possible to set the DAC values for the VCO back to default. Again, the DAC values were optimized for this setup. As a result, the chip worked at full speed with 1.25 Gb/s. The most decisive change in DAC values was the tuning of the output amplitude and the pre-emphasis. The amplitude was raised to drive the signal as strong as possible. The pre-emphasis, on the other hand, was used to limit the maximum amplitude. It is implemented as a delayed and inverted signal added to the output. By increasing the magnitude of the pre-emphasis, the

signal was tuned to have two distinct voltage levels for zeros and ones. Previously the signal was not fast enough to make the transition within one bit length As a consequence, intermediate voltage levels occurred. An attempt was made to reduce the pre-emphasis and the amplitude, to achieve the same output, but this only led to bit errors at the FPGA receiver. The eye diagram of the fourth data output for an optimized and stable DAC configuration can be seen in figure 5.16. The eye with an height of only about 31 mV is very small, due to the limitation

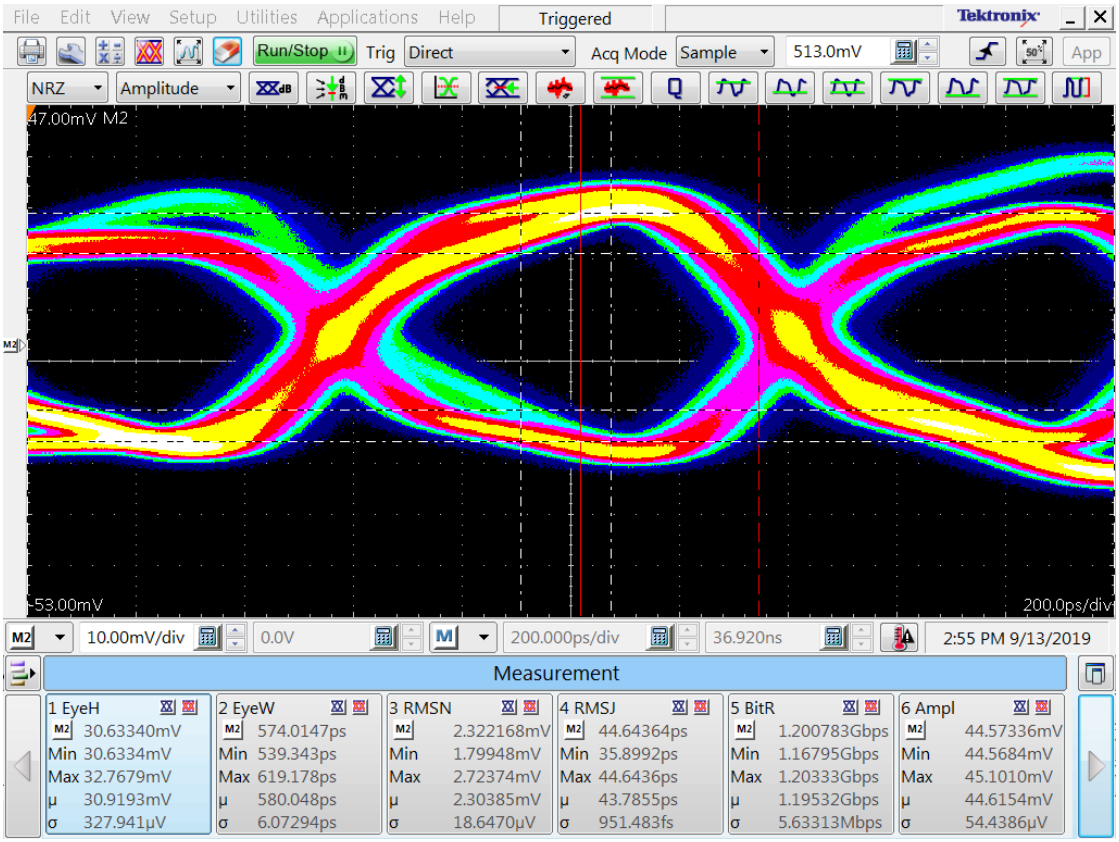


Figure 5.16: 1.25 Gb/s MuPix8 DataOut4 signal transmitted over a 24 cm long HDI. The high-pass filters is attached via the Backup PCB. EyeH = eye height, EyeW = eye width, RMSN = noise standard deviation, RMSJ = jitter standard deviation, BitR = measured bit rate, Ampl = amplitude

through the pre-emphasis. The noise and jitter are in the same range as results from a wire-bonded MuPix8 [Dit18]. With the "external" powering modification on the MuPix8 motherboard, the input voltages were directly applied with a HAMEG power supply [HI09]. In previous measurements with wire-bonded MuPix8 sensors, a decrease of noise and jitter has been observed when the supply voltages were

raised slightly. The voltages were also raised with this setup but with a contrary result. The jitter and noise grew with higher voltages and got slightly better with lower voltages compared to the defaults. Due to the floating ground over the long HDI, it was suspected that the change of input voltages has an influence in the form of a ground shift. This was not possible to confirm with this setup since only the ground and one supply voltage was bonded successfully to the Backup PCB, as described at the beginning of this section. More tests and measurements are planned to be conducted with another HDI. As a feasibility test, the assembly with the Insert inventory number 84-3-27 has been configured with the same tuned DAC values as the previous assembly, and it worked out of the box. It should be noted that this assembly does not have a Backup PCB attached yet. This setup has a jitter of $73\,\mathrm{ps} \pm 1\,\mathrm{ps}$, which is due to the lack of the filters for the voltage controlled oscillator.

Chapter 6

Conclusion and outlook

As part of this thesis, an analytic model for edge coupled microstrips has been compared with 2D simulations. Both approaches have shown that the LVDS standard can be met with the proper set of parameters. The intended dielectric height for the HDIs in the Mu3e experiment is 45 µm, which resembles a spacer thickness of 25 µm. At this dielectric height, the trace width should be in the range of 63 µm to 84 µm according to the analytic model, whereas the simulation recommends a range of 98 µm to 140 µm. There is no hesitation in choosing the smallest feature size for the gap between the microstrips, offered by the manufacturer, which is 63 µm. This comes with the advantage of rejecting the most common mode distortions. It is advantageous to remove the layer spacer and to set the trace width likewise to the smallest feature size. According to the simulation, one should consider removing the spacer and setting the trace width to 63 µm. However, it is inevitable to conduct a measurement series checking the final choice under real-world conditions, covering the determination of manufacturing variations.
To further explore the transmission line quality, bit error rates were measured for both the high density interconnect (HDI) prototype as well as for the unshielded twisted pair (UTP). The HDI showed excellent behavior, giving an upper limit of 2×10^{-15} ($95\,\%$ CL) at 1.25 Gb/s. Over the course of measurements, the UTP transmitted nine erroneous bits, leading to a rate of 1.081×10^{-14} at 1.25 Gb/s. For both transmission lines, the eye diagrams show that the slew rate degraded its height and width. For a 1.25 Gb/s pseudo random bit pattern, the attenuation for the 24 cm long HDI traces was estimated from the eye heights to be 5.5 dB whereas the attenuation of the UTP is 6.6 dB. The differential impedance on the HDI has been measured to be above 200 Ω, well-matching expectations of this setup without a reference layer. This causes losses when terminated differentially to 100 Ω. Matching the impedance correctly is expected to improve the signal quality. With only five produced HDIs, the permanent modification of gluing the reference layer to the HDI, giving the proper impedance, was saved for the point

when all non-destructive measurements are finished.
Exceeding the required length of 18 cm, the 24 cm long HDI can be operated in combination with a MuPix8 sensor at 1.25 Gb/s readout speed. Except for the longest traces in the tracking layers of the Mu3e detector, the other traces are even shorter, making this a promising solution for the MuPix sensor readout. Besides, the additional 6 cm gives extra headroom for routing and the transition to the UTP cables.
The setup for this feasibility study possesses useful features worth exploiting in the future. For example, the extremely low material budget, as well as the length of this Single MuPix8 HDI, makes it possible to use the MuPix8 sensor in detector like setups or even as an active target. Furthermore, three edges of the MuPix8 are accessible, making it a potential setup for edge *transient current technique (TCT)* measurements.

Appendix A

Hammerstad and Jensen model of coupled microstrips

$$Z_{L,odd}\left(u,g\right)=\frac{Z_L(u)}{1-Z_L(u)\cdot\Phi_o\left(u,g\right)/Z_{F0}} \tag{A.1}$$

$$u=\frac{W}{h}\quad,\quad g=\frac{s}{h}\quad,\quad Z_{F0}=377\,\Omega \tag{A.2}$$

$$\Phi_o\left(u,g\right)=\Phi_e\left(u,g\right)-\frac{\theta(g)}{\Psi(g)}\cdot\exp\left(\beta(g)\cdot u^{-n(g)}\cdot\ln u\right) \tag{A.3}$$

$$\theta(g)=1.729+1.175\cdot\ln\left(1+\frac{0.627}{g+0.327\cdot g^{2.17}}\right) \tag{A.4}$$

$$\Psi(g)=1+\frac{g}{1.45}+\frac{g^{2.09}}{3.95} \tag{A.5}$$

$$\beta(g)=0.2306+\frac{1}{301.8}\cdot\ln\left(\frac{g^{10}}{1+(g/3.73)^{10}}\right)+\frac{1}{5.3}\cdot\ln\left(1+0.646\cdot g^{1.175}\right) \tag{A.6}$$

$$n(g)=\left(\frac{1}{17.7}+\exp\left(-6.424-0.76\cdot\ln g-(g/0.23)^5\right)\right)\cdot\ln\left(\frac{10+68.3\cdot g^2}{1+32.5\cdot g^{3.093}}\right) \tag{A.7}$$

$$\Phi_e\left(u,g\right)=\frac{\varphi(u)}{\Psi(g)\cdot\left(\alpha(g)\cdot u^{m(g)}+(1-\alpha(g))\cdot u^{-m(g)}\right)} \tag{A.8}$$

$$\varphi(u)=0.8645\cdot u^{0.172} \tag{A.9}$$

$$\alpha(g)=0.5\cdot e^{-g} \tag{A.10}$$

$$m(g)=0.2175+\left(4.113+(20.36/g)^6\right)^{-0.251}+\frac{1}{323}\cdot\ln\left(\frac{g^{10}}{1+(g/13.8)^{10}}\right) \tag{A.11}$$

$$Z_L\left(W,h,\varepsilon_r\right)=\frac{Z_{F0}}{2\pi\cdot\sqrt{\varepsilon_r}}\cdot\ln\left(f_u\frac{h}{W}+\sqrt{1+\left(\frac{2h}{W}\right)^2}\right) \tag{A.12}$$

$$f_u=6+(2\pi-6)\cdot\exp\left(-\left(30.666\cdot\frac{h}{W}\right)^{0.7528}\right) \tag{A.13}$$

$$\varepsilon_{eff,e,o}\left(u,g,\varepsilon_r\right)=\frac{\varepsilon_r+1}{2}+\frac{\varepsilon_r-1}{2}\cdot F_o\left(u,g,\varepsilon_r\right) \tag{A.14}$$

$$F_o\left(u,g,\varepsilon_r\right)=f_o\left(u,g,\varepsilon_r\right)\cdot\left(1+\frac{10}{u}\right)^{-a(u)\cdot b(\varepsilon_r)} \tag{A.15}$$

$$a\left(u\right)=1+\frac{1}{49}\cdot\ln\left(\frac{u^4+\left(u/52\right)^2}{u^4+0.432}\right)+\frac{1}{18.7}\cdot\ln\left(1+\left(\frac{u}{18.1}\right)^3\right) \tag{A.16}$$

$$b\left(\varepsilon_r\right)=0.564\cdot\left(\frac{\varepsilon_r-0.9}{\varepsilon_r+3}\right)^{0.053} \tag{A.17}$$

$$f_o\left(u,g,\varepsilon_r\right)=f_{o1}\left(g,\varepsilon_r\right)\cdot\exp\left(p(g)\cdot\ln u+q(g)\cdot\sin\left(\pi\cdot\log u\right)\right) \tag{A.18}$$

$$p(g)=\frac{\exp\left(-0.745\cdot g^{0.295}\right)}{\cosh\left(g^{0.68}\right)} \tag{A.19}$$

$$q(g)=\exp\left(-1.366-g\right) \tag{A.20}$$

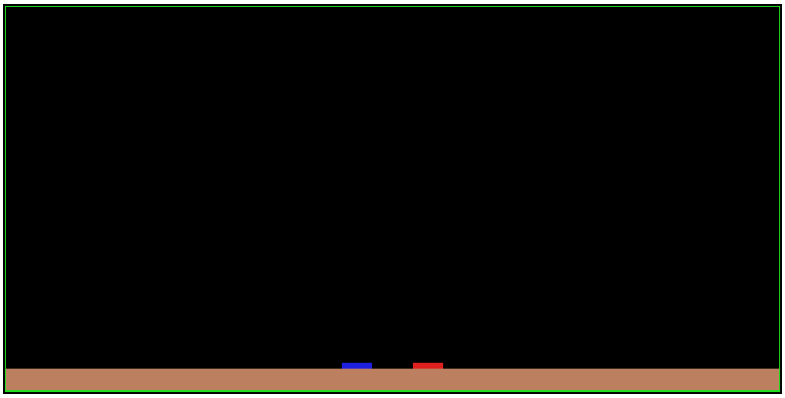
$$f_{o1}\left(g,\varepsilon_r\right)=1-\exp\left(-0.179\cdot g^{0.15}-\frac{0.328\cdot g^{r(g,\varepsilon_r)}}{\ln\left(e+\left(g/7\right)^{2.8}\right)}\right) \tag{A.21}$$

$$r\left(g,\varepsilon_r\right)=1+0.15\cdot\left(1-\frac{\exp\left(1-\left(\varepsilon_r-1\right)^2/8.2\right)}{1+g^{-6}}\right) \tag{A.22}$$

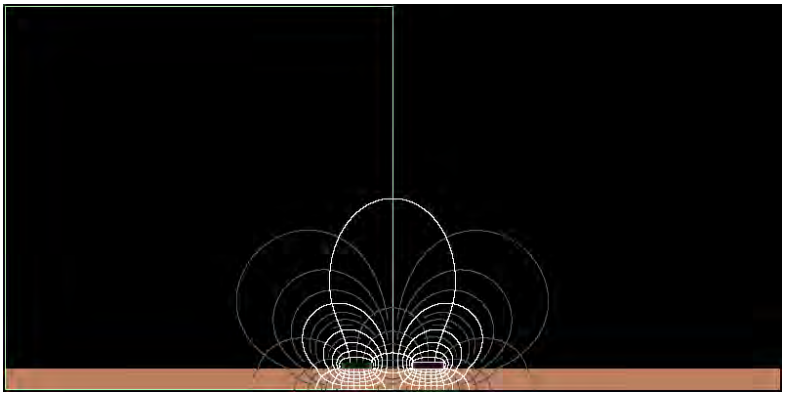
[HJ80, Jah19]

Appendix B

Simulation bitmaps



(a) Simulation input bitmap with red and blue as the differential pair. Green is ground, brown is the dielectric, and black vacuum.



(b) Simulation output bitmap with current density as well as E- and B-field lines

Figure B.1: Atlc2 simulation example bitmaps

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Acknowledgments

The last words apply to thank Prof. Schöning for allowing me to work on such an exciting topic for my master thesis. Therefore, and for numerous inspiring and engaging discussions, guiding me throughout my thesis, I would like to express my gratitude.

Moreover, I would like to thank Prof. Masciocchi to be my second examiner and for taking the time and effort to deal with my master thesis.

I am grateful to Adrian, Benjamin, David, Heiko, Jan, Sebastian, and Thomas for offering their help whenever I needed it. Without a great team, such a project would not have been possible.

My highest esteem goes to Dr. Frank Meier Aeschbacher for his great guidance and for being an even more excellent mentor.

Last but not least, I would like to thank from the bottom of my heard my friends and family, who supported me even in the darkest moments of my life. Without them, I would have never got this far.

Erklärung

Ich versichere, dass ich diese Arbeit selbstständig verfasst und keine anderen als die angegebenen Quellen und Hilfsmittel benutzt habe.
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