Calibration and commissioning of the Mu3e Vertex Detector

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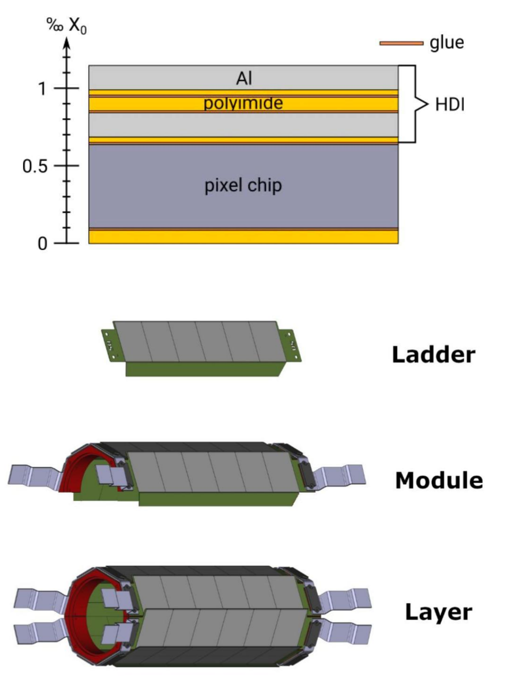
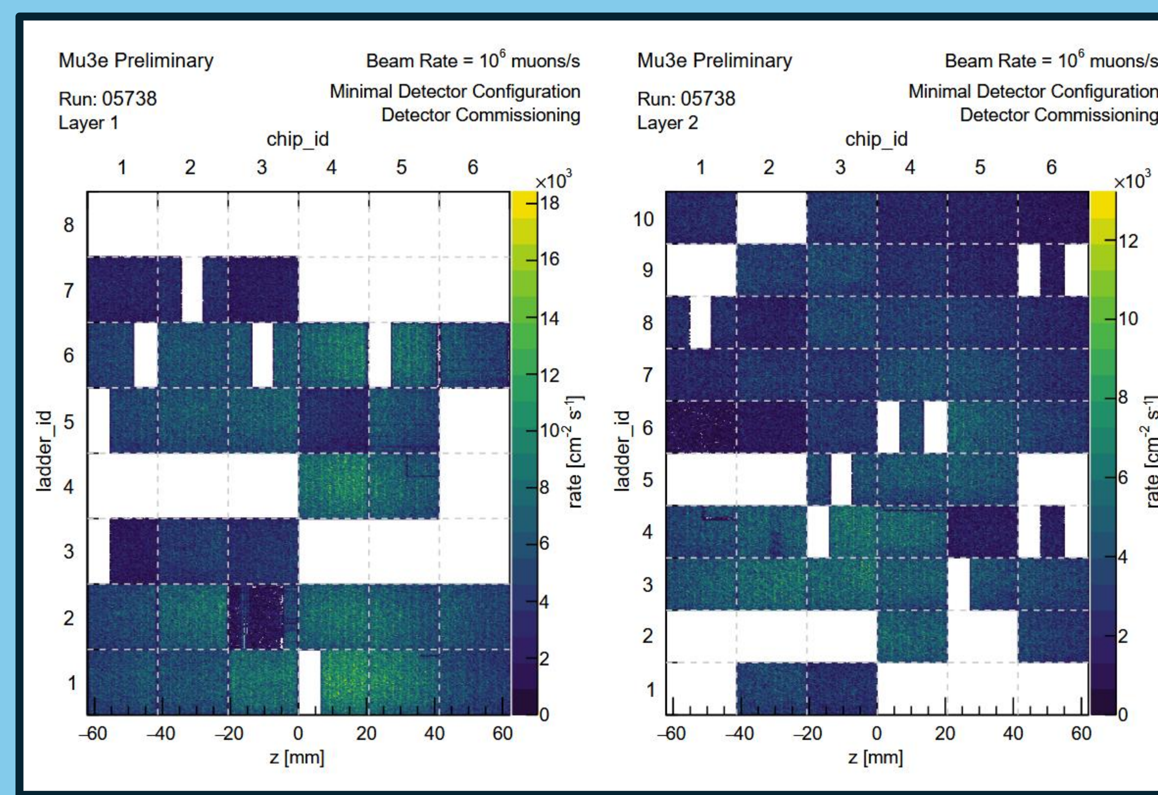
Abstract: The Mu3e experiment aims to search for the charged lepton flavour violating decay $\mu^+ \rightarrow e^+e^-e^+$ with an ultimate sensitivity of 10^{-16}. Its Vertex Detector employs ultra-thin MuPix11 sensors to provide precise tracking with minimal material. During our beam time at PSI this year, we successfully commissioned the detector.
Through Time over Threshold calibration, signal transmission tuning, and in-pixel threshold adjustment, we achieved efficient operation and recorded the first positron tracks from muon decays. This milestone marks a major step toward physics data taking in 2026.

Vertex Detector

- Two layers of **50µm** thin Mupix 11 pixel sensors
- Chips glued and bonded on High Density Interconnects (HDIs)
- Connection via interposers (pressed against Readout flexes)
- **Thinnest** (0.12% X_0/ layer) **pixel-vertex-detector currently operational**
- All 108 chips installed with 75 % of the submatrices operational

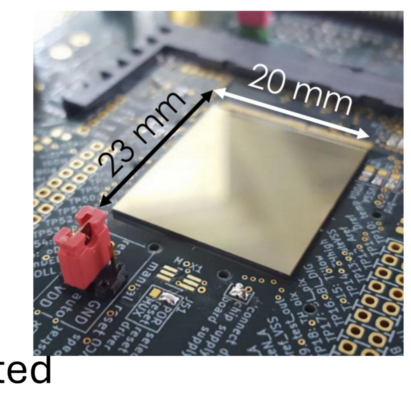


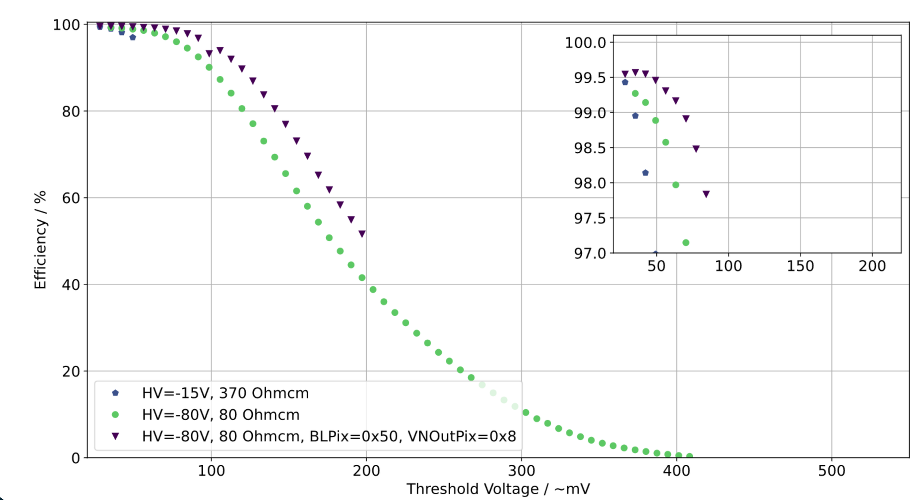
Hit rate map of the Vertex Detector (Layer 1 & 2)

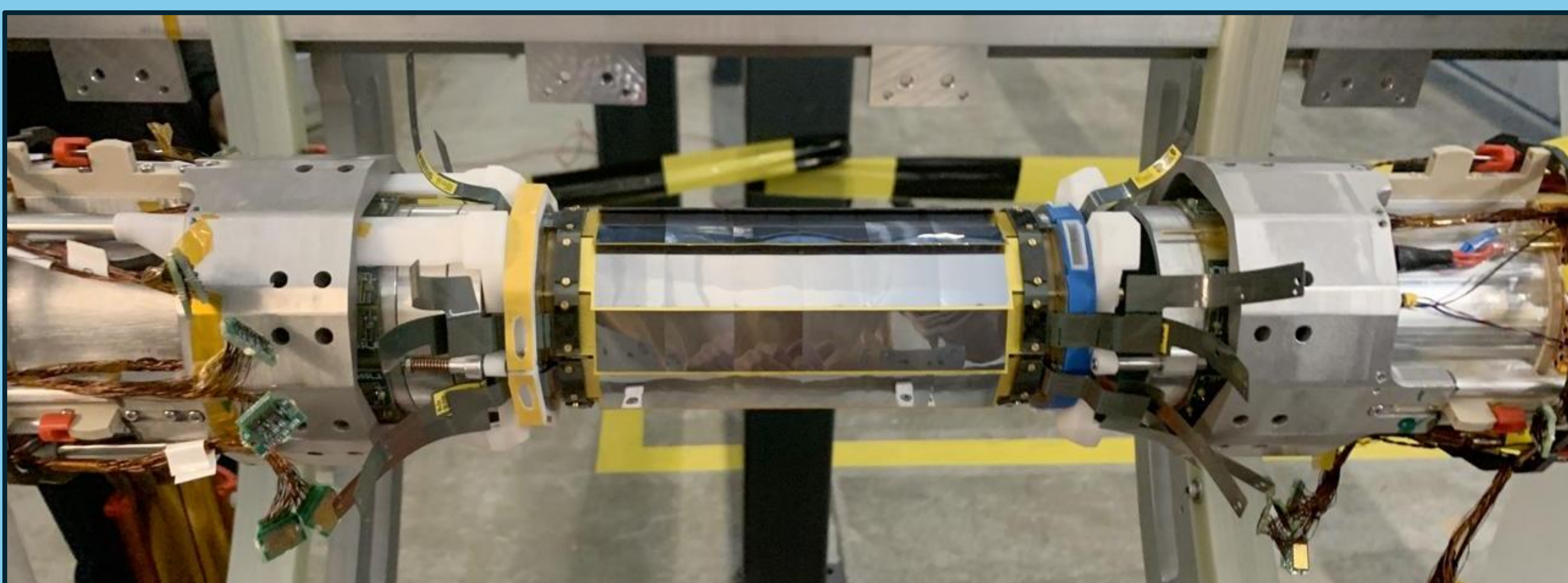


MuPix 11

- **H**igh-**V**oltage **M**onolithic **A**ctive **P**ixel **S**ensor (HV-MAPS)
  - Integrated readout electronics implemented in deep n-well structures
- 20 × 20 mm² active area
- Fully digital **1.25 Gbit/s LVDS** output
- **99% efficiency** with **<20 ns** time resolution
- Low-ohmic substrates (10–400 Ω cm)
- High-voltage operation up to 100 V

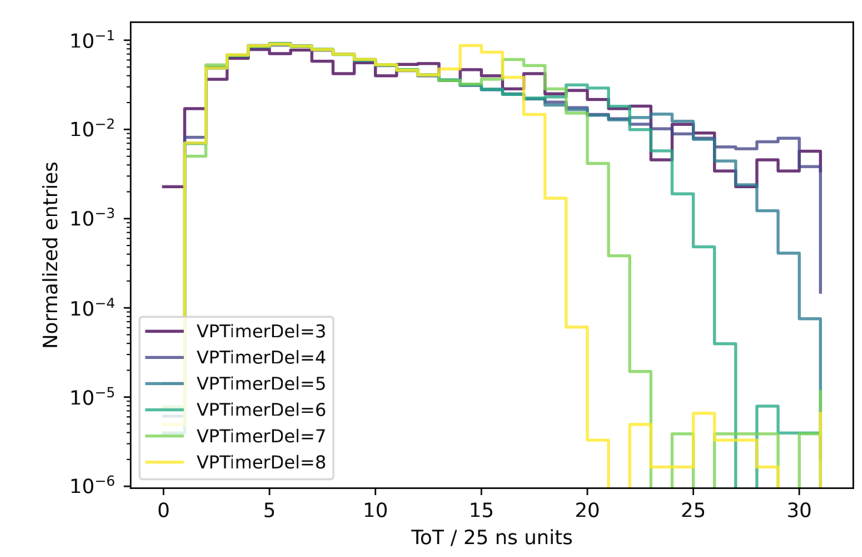






Time over Threshold (ToT) sampling

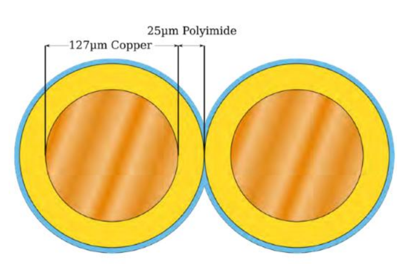
- **VPTimerDel** is set by a 6-bit DAC
- Controls the current of the analogue delay circuit
- Capacitor charging defines a programmable delay time
- Delay sets the **maximum measurable ToT**
- Small/medium pulses → ToT ∝ amplitude
  - Can be used for **timewalk correction**
- Long pulses → clipped at the delay and collected in the **end-peak**
- At Lower VPTimerDel a broader ToT spectrum is visible
- Calibration maximizes the usable ToT range



Example **ToT** spectra for different **VPTimerDel** values.

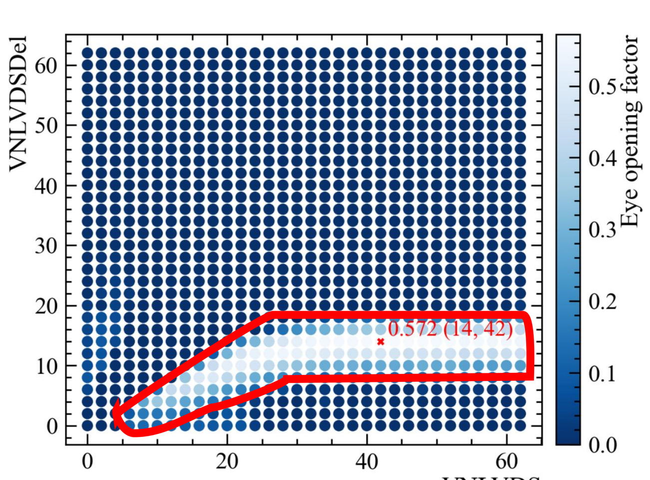
Signal transmission

- Up to **70%** amplitude loss at 1.25 Gbit/s due to Micro Twisted Pair (µTP) cables
- Signal integrity can be recovered through on-chip preemphasis (**VNLVDSDel**) and signal amplification (**VNLVDS**)
- LVDS transmission over µTP cables is a challenge for **error-free** operation
- Eye-diagram scans of single chips shows the error-free region in the LVDS parameter space
- Region **coincides** with the error-free window of the full vertex

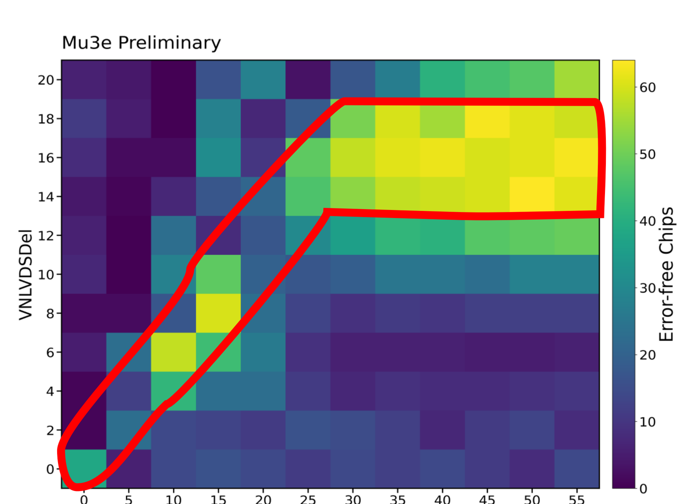


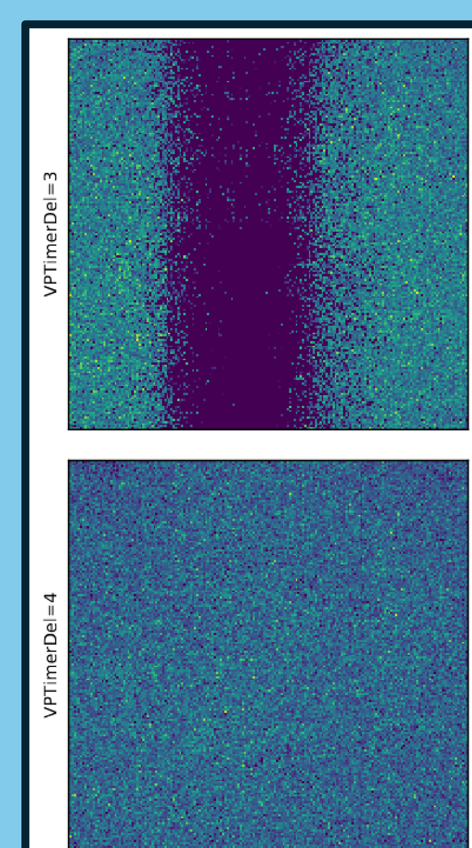
Cross section of a µTP cable

Map of the **Eye opening factor** of a sensor for different values of **VNLVDS** and **VNLVDSDel**



Data transmission results of the Vertex Detector for different values of **VNLVDS** and **VNLVDSDel**



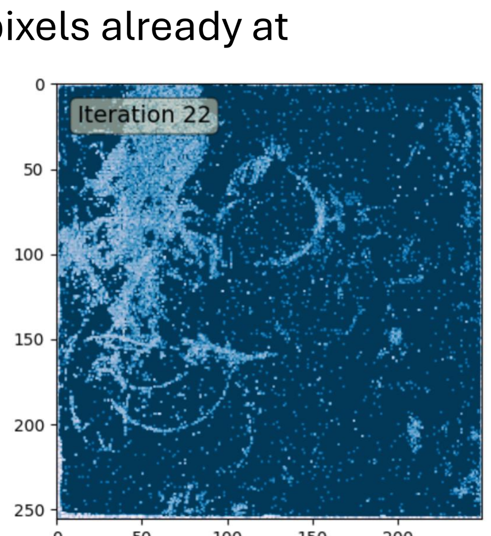


Example Hitmaps of a sensor for **low VPTimerDel's**. For **too long** delays, hits are **missing** in the sensor centre

Threshold Challenge

- Global threshold per chip, set as low as possible to detect small signals
- Only a narrow plateau region with >99% efficiency
- 50 µm ultra-thin sensors show noisy pixels already at higher thresholds
  - Possible causes: thinning process, mechanical stress, enhanced noise at sensor edges
- High noise occupancy can cause buffer saturation and data corruption and prevent other pixels from being read out
- Masking of noisy pixels is required but each masked pixel lowers the total efficiency

→ **In-pixel tuning** is essential for 50 µm ultra-thin pixel sensors



Noise map of a 50µm sensor showing characteristic **patterns** from **mechanical stress** and enhanced noise at **sensor edges**

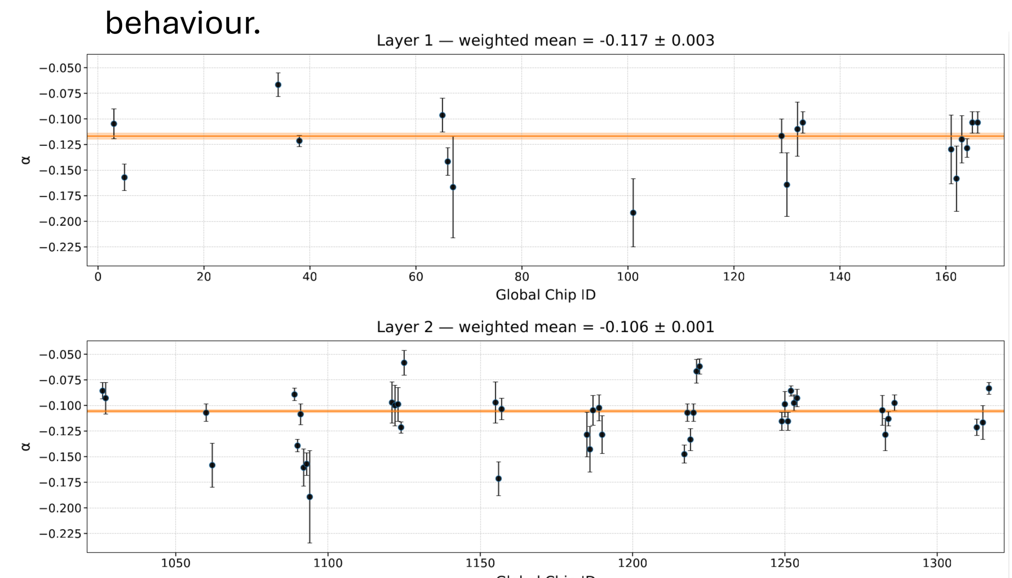
Tuning + Masking

- Each pixel has an individual TDAC(3 bits) to fine-tune its effective threshold
- **VPDAC** is set globally per chip and defines the tuning range
- **α** is a chip dependent constant, gives threshold shift per TDAC step.

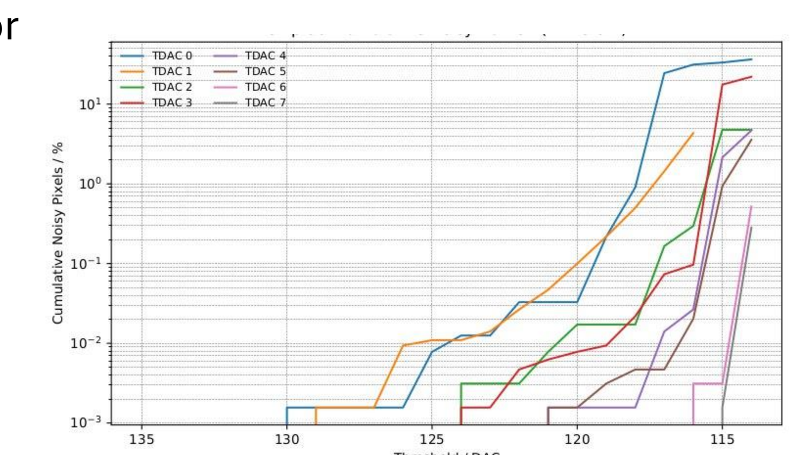
$$\mathrm{ThHigh_{eff}} = \mathrm{ThHigh} + \alpha \cdot \mathrm{VPDAC} \cdot \mathrm{TDAC}$$

- Pixels above certain threshold are masked, pixels below are tunes until the target working point is reached
  - Trade-off between dynamic tuning range and granularity
- Current algorithm takes approximately 10h to tune the full vertex detector

Tuning slope α per chip
Consistent α values across all chips validate uniform tuning behaviour.



Noise occupancy vs. threshold
Different TDAC values shift the noise curves; the separation defines the tuning slope α



Final TDAC map
Noisy pixels are tuned up instead of being masked, preserving partial efficiency. Edge pixels require the highest TDAC values, while the chip centre remains largely untuned.